S-8264A/B/C Series

BATTERY PROTECTION IC FOR 2-SERIAL TO 4-SERIAL-CELL PACK (SECONDARY PROTECTION)

www.ablic.com

Rev.4.4_00

The S-8264A/B/C Series is used for secondary protection of lithium-ion rechargeable batteries, and incorporates a high-accuracy voltage detection circuit and a delay circuit.
Short-circuiting between cells makes it possible for serial connection of two cells to four cells.

■ Features

(1) High-accuracy voltage detection circuit for each cell
- Overcharge detection voltage n (n = 1 to 4)
  4.200 V to 4.800 V (in 50 mV steps) Accuracy : ±25 mV (+25°C), Accuracy : ±30 mV (–5°C to +55°C)
- Overcharge hysteresis voltage n (n = 1 to 4)
  –0.520 ±0.210 V, –0.390 ±0.160 V, –0.260 ±0.110 V, –0.130 ±0.06 V, None

(2) Delay times for overcharge detection can be set by an internal circuit only (external capacitors are unnecessary)
(3) Output control function via CTL pin (CTL pin is pulled down internally) (S-8264A Series)
Output control function via CTL pin (CTL pin is pulled up internally) (S-8264C Series)
(4) Output latch function after overcharge detection (S-8264B Series)
(5) Output form and logic CMOS output active “H”
(6) High withstand voltage Absolute maximum rating 26 V
(7) Wide operation voltage range 3.6 V to 24 V
(8) Wide operation temperature range –40°C to +85°C
(9) Low current consumption
- At 3.5 V for each cell 5.0 μA max. (+25°C)
- At 2.3 V for each cell 4.0 μA max. (+25°C)

(10) Lead-free, Sn 100%, halogen-free*1

***1.** Refer to “■ **Product Name Structure**” for details.

■ Application

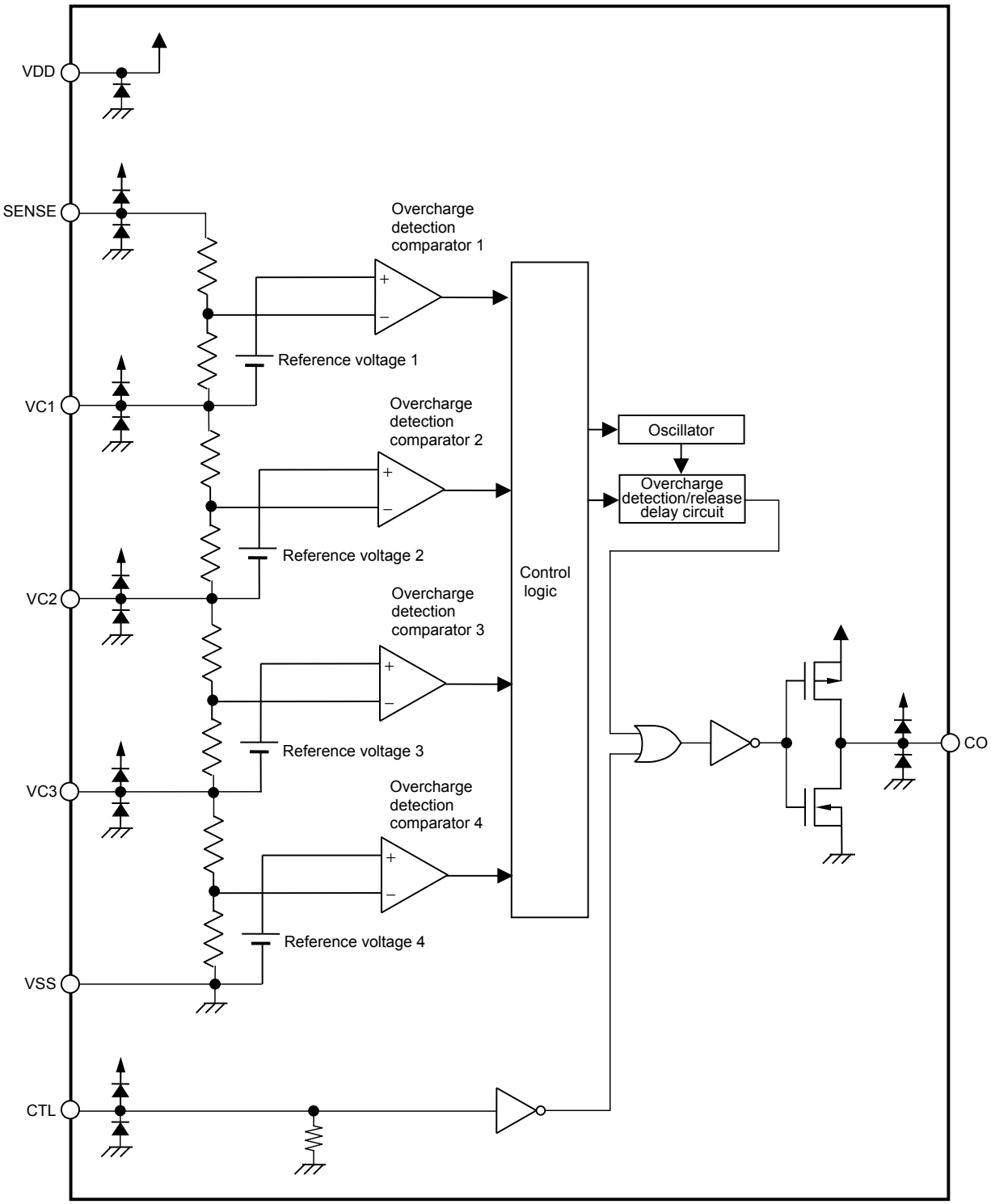
- Lithium-ion rechargeable battery packs (for secondary protection)

■ Packages

- SNT-8A
- 8-Pin TSSOP

■ Block Diagrams

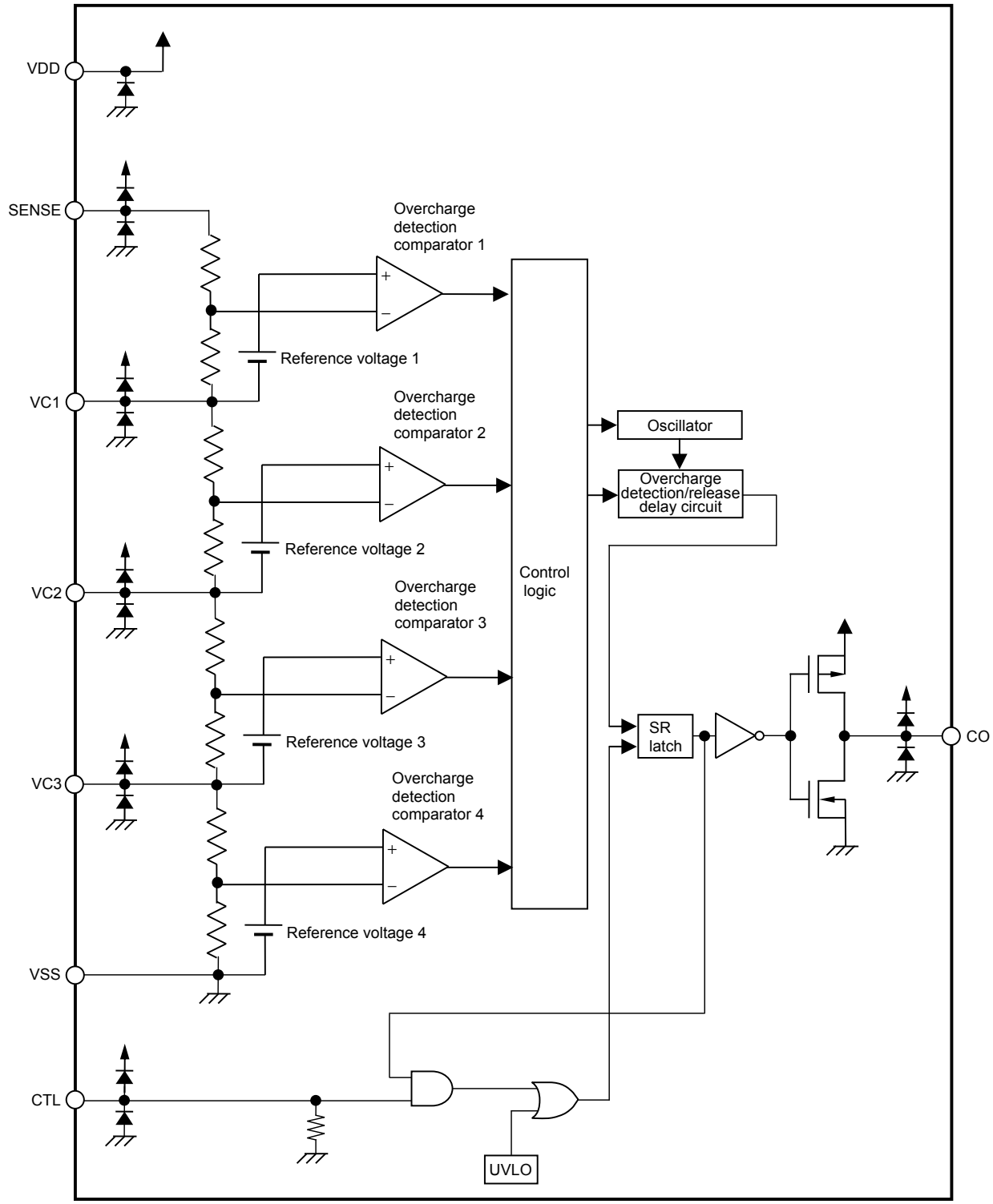
(1) S-8264A Series



Remark The diodes in the figure are parasitic diodes.

Figure 1

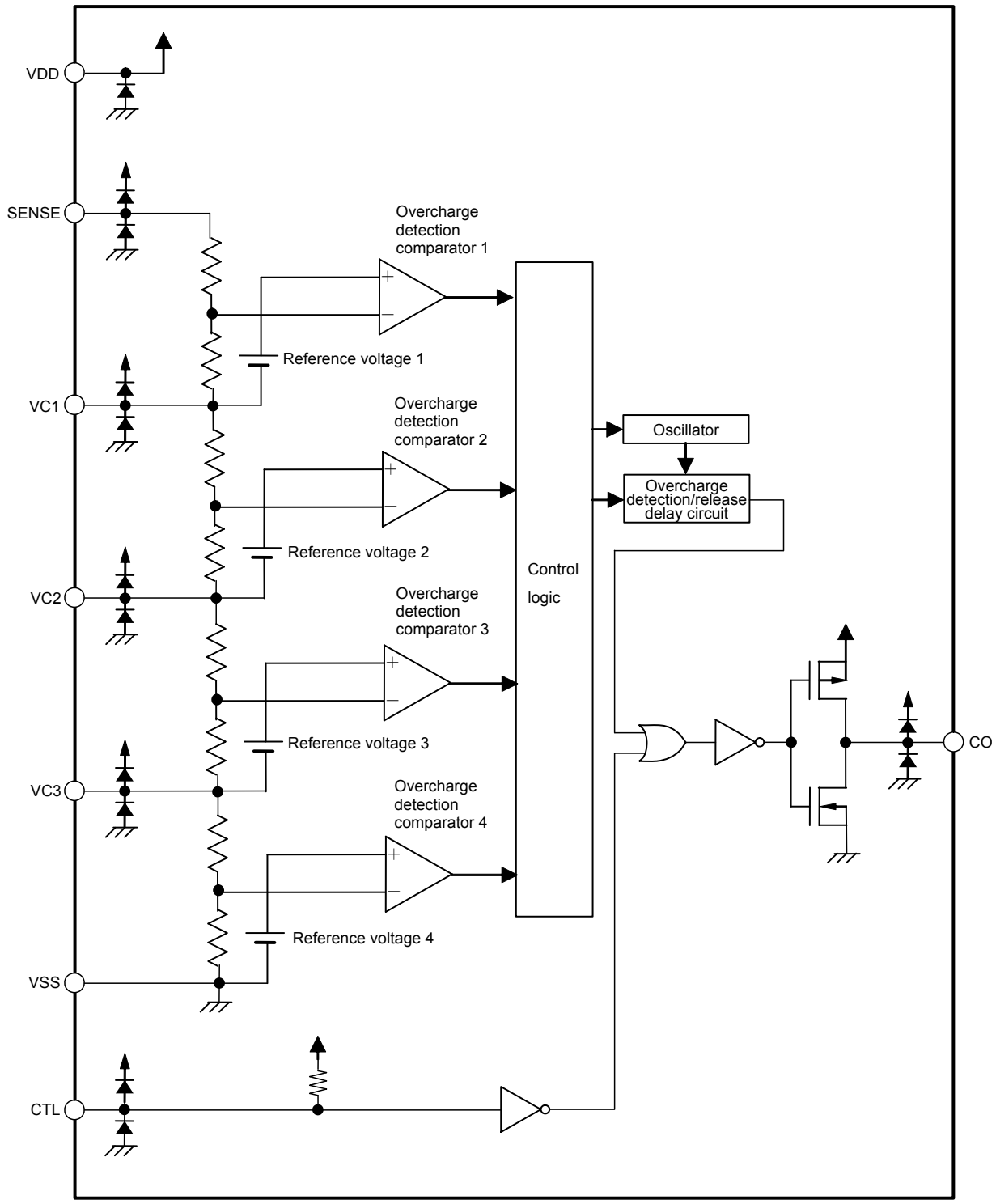
(2) S-8264B Series



Remark The diodes in the figure are parasitic diodes.

Figure 2

(3) S-8264C Series



Remark The diodes in the figure are parasitic diodes.

Figure 3

■ Product Name Structure

1. Product Name

(1) SNT-8A

S-8264 x xx - I8T1 U

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specification*1
  - I8T1: SNT-8A, Tape
- Serial code*2
  - Sequentially set from AA to AZ
- Product type
  - A: Without CO pin output latch function (CTL pin is pulled down internally)
  - B: With CO pin output latch function
  - C: Without CO pin output latch function (CTL pin is pulled up internally)

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product Name List**".

(2) 8-Pin TSSOP

S-8264 x xx - T8T1 x

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
  - G: Lead-free (for details, please contact our sales office)
- Package abbreviation and IC packing specification*1
  - T8T1: 8-Pin TSSOP, Tape
- Serial code*2
  - Sequentially set from AA to AZ
- Product type
  - A: Without CO pin output latch function (CTL pin is pulled down internally)
  - B: With CO pin output latch function
  - C: Without CO pin output latch function (CTL pin is pulled up internally)

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product Name List**".

2. Packages

Package Name		Drawing Code			
		Package	Tape	Reel	Land
SNT-8A		PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD
8-Pin TSSOP	Environmental code = G	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD	—
	Environmental code = U	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-S1	

3. Product Name List

(1) S-8264A Series

Table 1 SNT-8A

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Hysteresis Voltage [V_{HC}]	Overcharge Detection Delay Time [t_{CU}]	Output Form
S-8264AAA-I8T1U	4.450 ±0.025 V	−0.390 ±0.160 V	4.0 ±0.8 s	CMOS output active “H”
S-8264AAB-I8T1U	4.350 ±0.025 V	−0.390 ±0.160 V	4.0 ±0.8 s	CMOS output active “H”
S-8264AAC-I8T1U	4.500 ±0.025 V	−0.390 ±0.160 V	4.0 ±0.8 s	CMOS output active “H”
S-8264AAD-I8T1U	4.350 ±0.025 V	−0.390 ±0.160 V	2.0 ±0.4 s	CMOS output active “H”
S-8264AAE-I8T1U	4.300 ±0.025 V	−0.390 ±0.160 V	4.0 ±0.8 s	CMOS output active “H”
S-8264AAF-I8T1U	4.450 ±0.025 V	−0.390 ±0.160 V	2.0 ±0.4 s	CMOS output active “H”
S-8264AAG-I8T1U	4.300 ±0.025 V	−0.390 ±0.160 V	2.0 ±0.4 s	CMOS output active “H”
S-8264AAH-I8T1U	4.400 ±0.025 V	−0.390 ±0.160 V	4.0 ±0.8 s	CMOS output active “H”
S-8264AAI-I8T1U	4.400 ±0.025 V	−0.390 ±0.160 V	2.0 ±0.4 s	CMOS output active “H”
S-8264AAJ-I8T1U	4.450 ±0.025 V	−0.390 ±0.160 V	5.65 ±1.15 s	CMOS output active “H”
S-8264AAK-I8T1U	4.350 ±0.025 V	−0.390 ±0.160 V	5.65 ±1.15 s	CMOS output active “H”
S-8264AAO-I8T1U	4.400 ±0.025 V	−0.390 ±0.160 V	5.65 ±1.15 s	CMOS output active “H”
S-8264AAS-I8T1U	4.500 ±0.025 V	−0.390 ±0.160 V	5.65 ±1.15 s	CMOS output active “H”
S-8264AAT-I8T1U	4.550 ±0.025 V	−0.390 ±0.160 V	5.65 ±1.15 s	CMOS output active “H”
S-8264AAV-I8T1U	4.600 ±0.025 V	−0.390 ±0.160 V	5.65 ±1.15 s	CMOS output active “H”
S-8264AAW-I8T1U	4.220 ±0.025 V	−0.390 ±0.160 V	2.0 ±0.4 s	CMOS output active “H”

Table 2 8-Pin TSSOP

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Hysteresis Voltage [V_{HC}]	Overcharge Detection Delay Time [t_{CU}]	Output Form
S-8264AAA-T8T1x	4.450 ±0.025 V	−0.390 ±0.160 V	4.0 ±0.8 s	CMOS output active “H”
S-8264AAB-T8T1x	4.350 ±0.025 V	−0.390 ±0.160 V	4.0 ±0.8 s	CMOS output active “H”
S-8264AAK-T8T1U	4.350 ±0.025 V	−0.390 ±0.160 V	5.65 ±1.15 s	CMOS output active “H”

(2) S-8264B Series

Table 3 SNT-8A

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Hysteresis Voltage [V_{HC}]	Overcharge Detection Delay Time [t_{CU}]	Output Form
S-8264BAA-I8T1U	4.450 ±0.025 V	−0.390 ±0.160 V	4.0 ±0.8 s	CMOS output active “H”
S-8264BAB-I8T1U	4.350 ±0.025 V	−0.390 ±0.160 V	4.0 ±0.8 s	CMOS output active “H”
S-8264BAC-I8T1U	4.550 ±0.025 V	−0.390 ±0.160 V	4.0 ±0.8 s	CMOS output active “H”

Table 4 8-Pin TSSOP

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Hysteresis Voltage [V_{HC}]	Overcharge Detection Delay Time [t_{CU}]	Output Form
S-8264BAB-T8T1x	4.350 ±0.025 V	−0.390 ±0.160 V	4.0 ±0.8 s	CMOS output active “H”

(3) S-8264C Series

Table 5 SNT-8A

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Hysteresis Voltage [V_{HC}]	Overcharge Detection Delay Time [t_{CU}]	Output Form
S-8264CAA-I8T1U	4.450 ±0.025 V	−0.390 ±0.160 V	2.0 ±0.4 s	CMOS output active “H”
S-8264CAB-I8T1U	4.220 ±0.025 V	−0.260 ±0.110 V	2.0 ±0.4 s	CMOS output active “H”

Remark 1. Please contact our sales department for the products with detection voltage value other than those specified above.
2. x: G or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Pin Configurations

SNT-8A
Top view

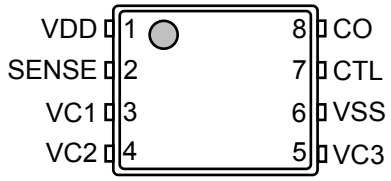


Figure 4

Table 6

Pin No.	Symbol	Description
1	VDD	Positive power input pin
2	SENSE	Positive voltage connection pin of battery 1
3	VC1	Negative voltage connection pin of battery 1 Positive voltage connection pin of battery 2
4	VC2	Negative voltage connection pin of battery 2 Positive voltage connection pin of battery 3
5	VC3	Negative voltage connection pin of battery 3 Positive voltage connection pin of battery 4
6	VSS	Negative power input pin Negative voltage connection pin of battery 4
7	CTL	CO output control pin (S-8264A/C Series) Overcharge detection latch reset pin (S-8264B Series)
8	CO	FET gate connection pin for charge control

8-Pin TSSOP
Top view

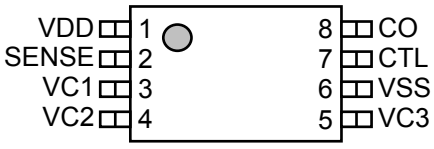


Figure 5

Table 7

Pin No.	Symbol	Description
1	VDD	Positive power input pin
2	SENSE	Positive voltage connection pin of battery 1
3	VC1	Negative voltage connection pin of battery 1 Positive voltage connection pin of battery 2
4	VC2	Negative voltage connection pin of battery 2 Positive voltage connection pin of battery 3
5	VC3	Negative voltage connection pin of battery 3 Positive voltage connection pin of battery 4
6	VSS	Negative power input pin Negative voltage connection pin of battery 4
7	CTL	CO output control pin (S-8264A/C Series) Overcharge detection latch reset pin (S-8264B Series)
8	CO	FET gate connection pin for charge control

■ Absolute Maximum Ratings

Table 8

(Ta = 25°C unless otherwise specified)

Item		Symbol	Applied Pin	Rating	Unit
Input voltage between VDD and VSS		V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 26	V
Input pin voltage		V_{IN}	SENSE, VC1, VC2, VC3, CTL	V_{SS} – 0.3 to V_{DD} + 0.3	V
CO output pin voltage		V_{CO}	CO	V_{SS} – 0.3 to V_{DD} + 0.3	V
Power dissipation	SNT-8A	P_D	—	450*1	mW
	8-Pin TSSOP			700*1	mW
Operation ambient temperature		T_{opr}	—	–40 to +85	°C
Storage temperature		T_{stg}	—	–40 to +125	°C

***1.** When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

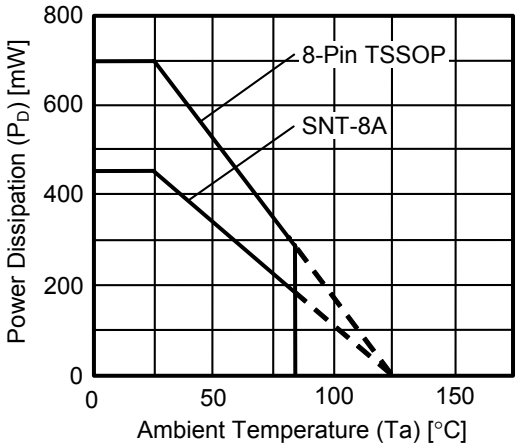


Figure 6 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. Except Detection Delay Time

Table 9

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE								
Overcharge detection voltage n (n = 1, 2, 3, 4)	V_{CUn}	4.200 V to 4.800 V, adjustable, Ta = 25°C	V_{CUn}–0.025	V_{CUn}	V_{CUn}+0.025	V	1	1
		4.200 V to 4.800 V, adjustable, Ta = –5°C to +55°C*1	V_{CUn}–0.030	V_{CUn}	V_{CUn}+0.030	V	1	1
Overcharge hysteresis voltage n*2 (n = 1, 2, 3, 4)	V_{HCn}	—	V_{HCn}–0.210	–0.520	V_{HCn}+0.210	V	1	1
INPUT VOLTAGE								
Operation voltage between VDD and VSS	V_{DSOP}	—	3.6	—	24	V	—	—
CTL input “H” voltage	V_{CTLH}	—	V_{DD}×0.95	—	—	V	6	2
CTL input “L” voltage	V_{CTLL}	—	—	—	V_{DD}×0.4	V	6	2
INPUT CURRENT								
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V4 = 3.5 V	—	2.5	5.0	µA	7	4
Current consumption during overdischarge	I_{OPED}	V1 = V2 = V3 = V4 = 2.3 V	—	2.0	4.0	µA	7	4
SENSE pin current	I_{SENSE}	V1 = V2 = V3 = V4 = 3.5 V	—	1.5	3.2	µA	8	5
VC1 pin current	I_{VC1}	V1 = V2 = V3 = V4 = 3.5 V	–0.3	0	0.3	µA	8	5
VC2 pin current	I_{VC2}	V1 = V2 = V3 = V4 = 3.5 V	–0.3	0	0.3	µA	8	5
VC3 pin current	I_{VC3}	V1 = V2 = V3 = V4 = 3.5 V	–0.3	0	0.3	µA	8	5
CTL pin “H” current	I_{CTLH}	A/B Series V1 = V2 = V3 = V4 = 3.5 V, V_{CTL} = V_{DD}	1.1	1.5	1.8	µA	8	5
		C Series V1 = V2 = V3 = V4 = 3.5 V V_{CTL} = V_{DD}	—	—	0.15	µA	8	5
CTL pin “L” current	I_{CTLL}	A/B Series V1 = V2 = V3 = V4 = 3.5 V, V_{CTL} = 0 V	–0.15	—	—	µA	8	5
		C Series V1 = V2 = V3 = V4 = 3.5 V V_{CTL} = 0 V	–150	–50	–10	µA	8	5
OUTPUT CURRENT								
CO pin sink current	I_{COL}	V_{COP} = V_{SS}+0.5 V	0.4	—	—	mA	9	6
CO pin source current	I_{COH}	V_{COP} = V_{DD}–0.5 V	20	—	—	µA	9	6

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

***2.** –0.390 ±0.160 V, –0.260 ±0.110 V, –0.130 ±0.060 V, or none, except for –0.520 V hysteresis product circuits. The overcharge release voltage is the total of the overcharge detection voltage (V_{CUn}) and the overcharge hysteresis voltage (V_{HCn}).

2. Detection Delay Time

(1) S-8264AAA, S-8264AAB, S-8264AAC, S-8264AAE, S-8264AAH, S-8264BAA, S-8264BAB, S-8264BAC

Table 10

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME								
Overcharge detection delay time	t_{CU}	—	3.2	4.0	4.8	s	2	1
Overcharge timer reset delay time	t_{TR}	—	6	12	20	ms	3	1
Overcharge release delay time	t_{CL}	—	51	64	77	ms	2	1
CTL pin response time	t_{CTL}	—	—	—	2.5	ms	4	2
Transition time to Test mode	t_{TST}	V1 = V2 = V3 = V4 = 3.5 V, $V_{DD} \geq V_{SENSE} + 8.5$ V	—	—	80	ms	5	3

(2) S-8264AAD, S-8264AAF, S-8264AAG, S-8264AAI, S-8264CAA, S-8264CAB

Table 11

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME								
Overcharge detection delay time	t_{CU}	—	1.6	2.0	2.4	s	2	1
Overcharge timer reset delay time	t_{TR}	—	6	12	20	ms	3	1
Overcharge release delay time	t_{CL}	—	1.6	2.0	3.0	ms	2	1
CTL pin response time	t_{CTL}	—	—	—	2.5	ms	4	2
Transition time to Test mode	t_{TST}	V1 = V2 = V3 = V4 = 3.5 V, $V_{DD} \geq V_{SENSE} + 8.5$ V	—	—	80	ms	5	3

(3) S-8264AAJ, S-8264AAK, S-8264AAO, S-8264AAS, S-8264AAT, S-8264AAV

Table 12

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME								
Overcharge detection delay time	t_{CU}	—	4.5	5.65	6.8	s	2	1
Overcharge timer reset delay time	t_{TR}	—	8	17	28	ms	3	1
Overcharge release delay time	t_{CL}	—	70	88	110	ms	2	1
CTL pin response time	t_{CTL}	—	—	—	2.5	ms	4	2
Transition time to Test mode	t_{TST}	V1 = V2 = V3 = V4 = 3.5 V, $V_{DD} \geq V_{SENSE} + 8.5$ V	—	—	80	ms	5	3

(4) S-8264AAW

Table 13

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME								
Overcharge detection delay time	t_{CU}	—	1.6	2.0	2.4	s	2	1
Overcharge timer reset delay time	t_{TR}	—	6	12	20	ms	3	1
Overcharge release delay time	t_{CL}	—	51	64	77	ms	2	1
CTL pin response time	t_{CTL}	—	—	—	2.5	ms	4	2
Transition time to Test mode	t_{TST}	V1 = V2 = V3 = V4 = 3.5 V, $V_{DD} \geq V_{SENSE} + 8.5$ V	—	—	80	ms	5	3

■ Test Circuits

(1) Test Condition 1, Test Circuit 1

Set V1, V2, V3, and V4 to 3.5 V. Overcharge detection voltage 1 (V_{CU1}) is the V1 voltage when CO is "H" after the voltage of V1 has been gradually increased. The overcharge hysteresis voltage (V_{HC1}) is the difference between V1 and V_{CU1} when CO is "L" after the voltage of V1 has been gradually decreased.

Overcharge detection voltage V_{CUn} (n = 2 to 4) and overcharge hysteresis V_{HCn} (n = 2 to 4) can be determined in the same way as when n = 1.

(2) Test Condition 2, Test Circuit 1

Set V1, V2, V3, and V4 to 3.5 V and in a moment of time (within 10 μs) increase V1 up to 5.0 V. The overcharge detection delay time (t_{CU}) is the period from when V1 reached 5.0 V to when CO becomes "H". After that, in a moment of time (within 10 μs) decrease V1 down to 3.5 V. The overcharge release delay time (t_{CL}) is the period from when V1 has reached 3.5 V to when CO becomes "L".

(3) Test Condition 3, Test Circuit 1

Set V1, V2, V3, and V4 to 3.5 V and in a moment of time (within 10 μs) increase V1 up to 5.0 V. This is defined as the first rise. Within t_{CU} – 20 ms after the first rise, in a moment of time (within 10 μs) decrease V1 down to 3.5 V and then in a moment of time (within 10 μs) restore up to 5.0 V. This is defined as the second rise. When the period from when V1 was fallen to the second rise is short, CO becomes "H" after t_{CU} has elapsed since the first rise. If the period from when V1 falls to the second rise is gradually made longer, CO becomes "H" when t_{CU} has elapsed since the second rise. The overcharge timer reset delay time (t_{TR}) is the period from V1 fall till the second rise at that time.

(4) Test Condition 4, Test Circuit 2

In the S-8264A/C Series, set V1, V2, V3, and V4 to 3.5 V and V5 to 14 V. The CTL pin response time (t_{CTL}) is the period from when V5 reaches 0 V after V5 is in a moment of time (within 10 μs) decreased down to 0 V to when CO becomes "H".

In the S-8264B Series, set V1, V2, V3, and V4 to 3.5 V and V5 to 14 V after an overvoltage is detected and CO becomes "H". In a moment of time (within 10 μs) raise V5 from 0 V to 14 V. The CTL pin response time (t_{CTL}) is the period from when V5 becomes 14 V to when CO becomes "L".

(5) Test Condition 5, Test Circuit 3

After setting V1, V2, V3, and V4 to 3.5 V and V5 to 0 V, in a moment of time (within 10 μs) increase V5 up to 8.5 V and decrease V5 again down to 0 V. When the period from when V5 was raised to when it has fallen is short, if an overcharge detection operation is performed subsequently, the overcharge detection time is t_{CU}. However, when the period from when V5 is raised to when it is fallen is gradually made longer, the overcharge detection time during the subsequent overcharge detection operation is shorter than t_{CU}. The transition time to test mode (t_{TST}) is the period from when V5 was raised to when it has fallen at that time.

(6) Test Condition 6, Test Circuit 2

Set V1, V2, V3, and V4 to 3.5 V and V5 to 0 V. The CTL input "H" voltage (V_{CTLH}) is the maximum voltage of V5 when CO is "L" after V5 has been gradually increased. Next, set V5 to 14 V. The CTL input "L" voltage (V_{CTLL}) is the minimum voltage of V5 when CO is "H" after V5 has been gradually decreased.

(7) Test Condition 7, Test Circuit 4

The current consumption during operation (I_{OPE}) is the total of the currents that flow in the VDD pin and SENSE pin when V1, V2, V3, and V4 are set to 3.5 V.

The current consumption during overdischarge (I_{OPED}) is the total of the currents that flow in the VDD pin and SENSE pin when V1, V2, V3, and V4 are set to 2.3 V.

(8) Test Condition 8, Test Circuit 5

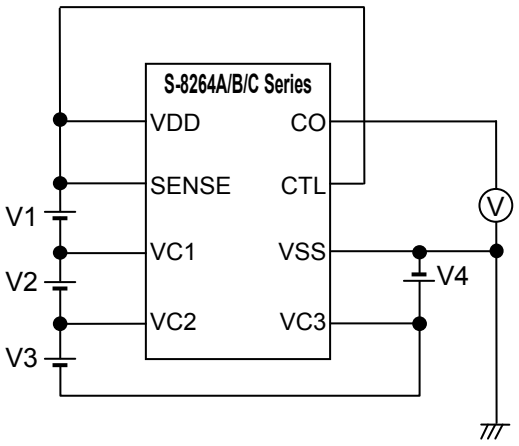
The SENSE pin current (I_{SENSE}) is I1, the VC1 pin current (I_{VC1}) is I2, the VC2 pin current (I_{VC2}) is I3, the VC3 pin current (I_{VC3}) is I4, and the CTL pin "H" current (I_{CTLH}) is I5 when V1, V2, V3, and V4 are set to 3.5 V, and V5 to 14 V.

The CTL pin "L" current (I_{CTLL}) is I5 when V1, V2, V3, and V4 are set to 3.5 V and V5 to 0 V.

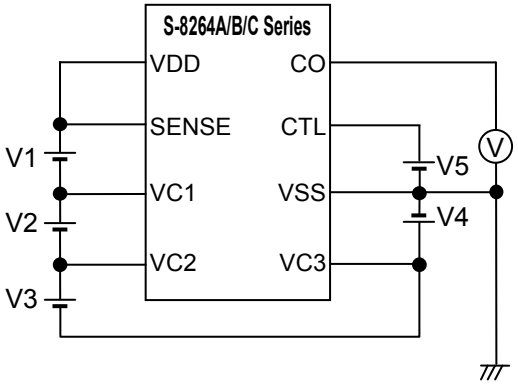
(9) Test Condition 9, Test Circuit 6

Set SW1 to OFF and SW2 to ON. The CO pin sink current (I_{COL}) is I2 when V1, V2, V3, and V4 are set to 3.5 V and V6 to 0.5 V.

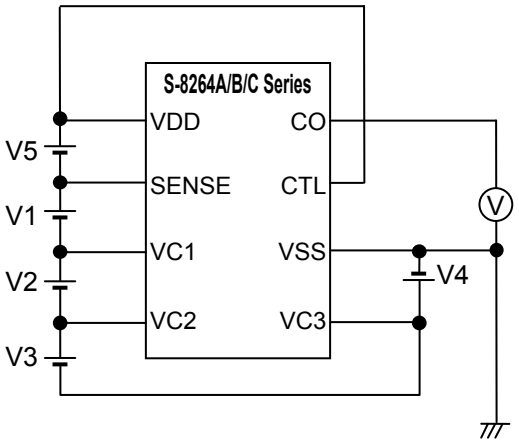
Set SW1 and SW2 to OFF. Set V1 to V5, set V2, V3, and V4 to 3.0 V, and set V5 to 0.5 V. After t_{CU} has elapsed, set SW1 to ON and SW2 to OFF. I1 is the CO pin source current (I_{COH}).



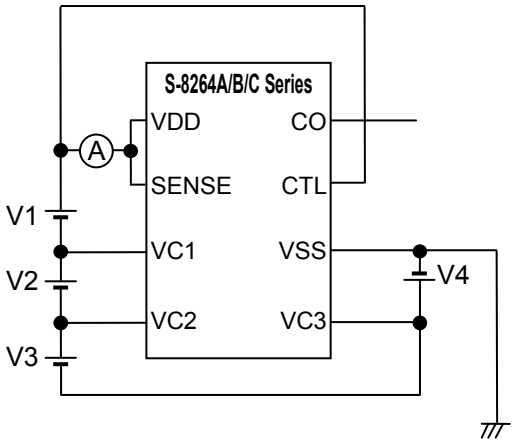
Test Circuit 1



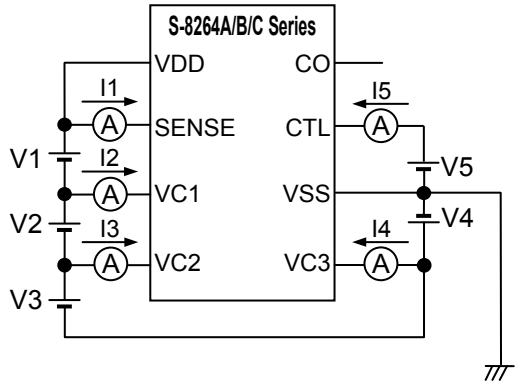
Test Circuit 2



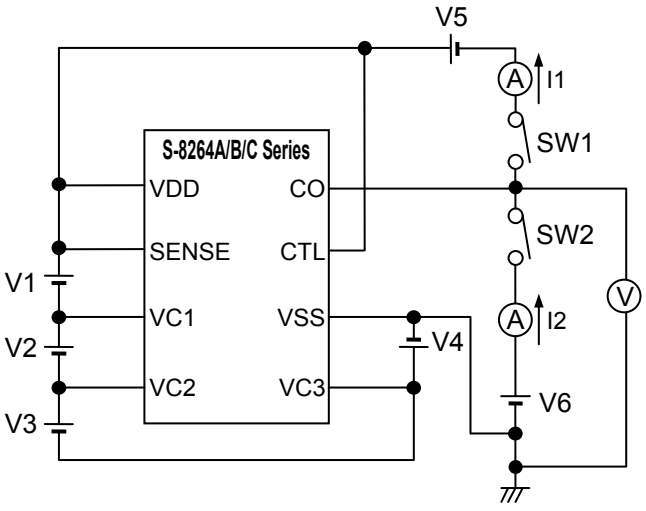
Test Circuit 3



Test Circuit 4



Test Circuit 5



Test Circuit 6

Figure 7

■ Operation

Remark Refer to **"■ Battery Protection IC Connection Example".**

1. Overcharge Detection

When the voltage of one of the batteries exceeds the overcharge detection voltage (V_{CU}) during charging under normal conditions and the state is retained for the overcharge detection delay time (t_{CU}) or longer, CO becomes "H". This state is called overcharge. Connecting FET to the CO pin provides charge control and a second protection.

In the S-8264A/C Series, if the voltage of each of the batteries is lower than V_{CU} + the overcharge hysteresis voltage (V_{HC}) and the state is retained for the overcharge release delay time (t_{CL}) or longer, CO becomes "L".

In the S-8264B Series, if the voltage of each of the batteries is lower than V_{CU} + V_{HC} and the state is retained for t_{CL} or longer, the overcharge state is released; however, CO stays at "H". When the CTL pin is switched from "L" to "H", CO becomes "L".

2. Overcharge Timer Reset Operation

When an overcharge release noise that forces the voltage of one of the batteries temporarily below V_{CU} is input during t_{CU} from when V_{CU} is exceeded to when charging is stopped, t_{CU} is continuously counted if the time the overcharge release noise persists is shorter than the overcharge timer reset delay time (t_{TR}). Under the same conditions, if the time the overcharge release noise persists is t_{TR} or longer, counting of t_{CU} is reset once. After that, when V_{CU} has been exceeded, counting t_{CU} resumes.

3. CTL Pin

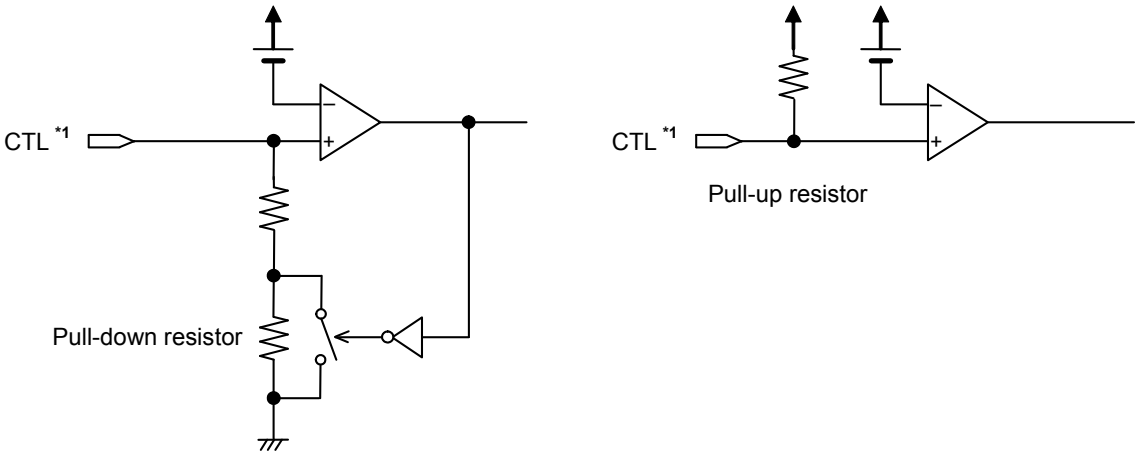
The S-8264A/B/C Series has a control pin. The CTL pin is used to control the output voltage of the CO pin.
In the S-8264A/C Series, the CTL pin takes precedence over the overcharge detection circuit.
In the S-8264B Series, when the CTL pin is switched from "L" to "H", a reset signal is output to the overcharge detection latch and CO becomes "L".

Table 14 Control via CTL Pin

CTL Pin	CO Pin		
	S-8264A Series	S-8264B Series	S-8264C Series
"H"	Normal state*1	Without latch	Normal state*1
Open	"H"	Normal state*1	Normal state*1
"L"	"H"	Normal state*1	"H"
"L" → "H"	–	Latch reset*2	–
"H" → "L"	–	–	–

***1.** The state is controlled by the overcharge detection circuit.

***2.** Latch reset becomes effective when the voltage of each of the batteries is lower than the overcharge detection voltage (V_{CU}) + the overcharge hysteresis voltage (V_{HC}) and the overcharge release delay time (t_{CL}) has elapsed.



S-8264A/B Series S-8264C Series

***1.** The reverse voltage "H" to "L" or "L" to "H" of CTL pin is VDD pin voltage – 2.8 V (Typ.), does not have the hysteresis.

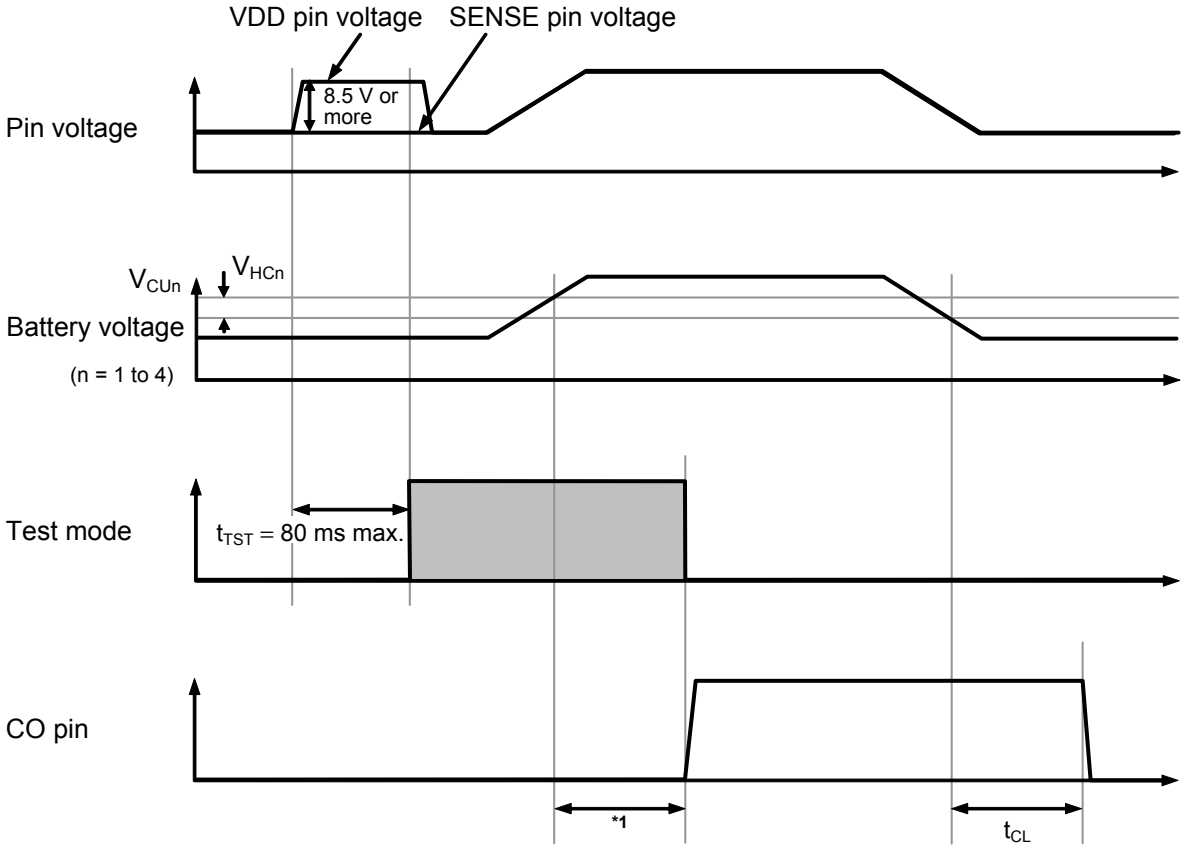
Figure 8 Internal Equivalent Circuit of CTL Pin

Caution 1. In the S-8264A/B Series, since the CTL pin implements high resistance of 8 MΩ to 12 MΩ for pull down, be careful of external noise application. If an external noise is applied, CO may become "H". Perform thorough evaluation using the actual application.

2. In the S-8264B Series, when the CTL pin is open or "L", CO latches "H". When the VDD pin voltage is decreased to the UVLO voltage of 2 V (Typ.) or lower, the latch is reset.

4. Test Mode

In the S-8264A/B/C Series, the overcharge detection delay time (t_{CU}) can be shortened by entering the test mode.
The test mode can be set by retaining the VDD pin voltage 8.5 V or more higher than the SENSE pin voltage for at least 80 ms (V1 = V2 = V3 = V4 = 3.5 V, Ta = 25°C). The status is retained by the internal latch and the test mode is retained even if the VDD pin voltage is decreased to the same voltage as that of the SENSE pin.
When CO becomes "H" when the delay time has elapsed after overcharge detection, the latch for retaining the test mode is reset and the S-8264A/B Series exits from the test mode.



***1.** In the product t_{CU} = 4 s Typ. during normal mode, t_{CU} = 64 ms Typ.
In the product t_{CU} = 2 s Typ. during normal mode, t_{CU} = 32 ms Typ.
In the product t_{CU} = 5.65 s Typ. during normal mode, t_{CU} = 88 ms Typ.

Figure 9

Caution
1. **When the VDD pin voltage is decreased to lower than the UVLO voltage of 2 V (Typ.), the S-8264A/B/C Series returns to the normal mode.**
2. **Set the test mode when no batteries are overcharged.**
3. **The overcharge release delay time (t_{CL}) is not shortened in the test mode.**
4. **The overcharge timer reset delay time (t_{TR}) is not shortened in the test mode.**

■ Timing Charts

1. Overcharge Detection Operation

(1) S-8264A/C Series

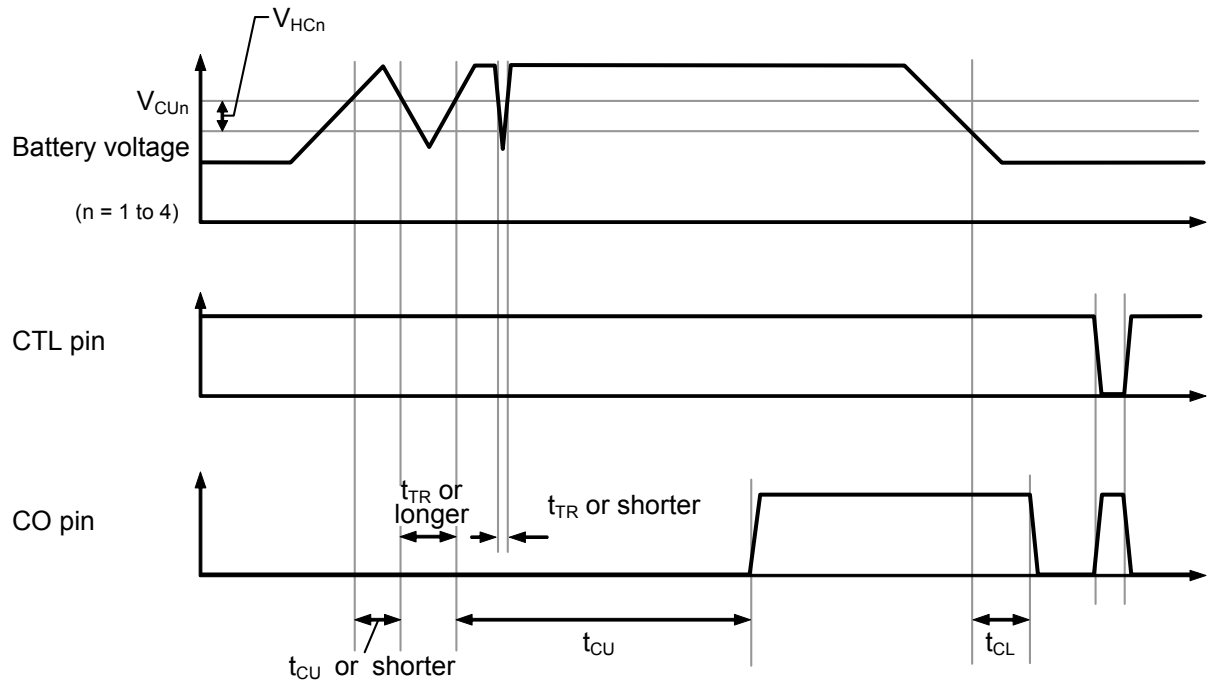


Figure 10

(2) S-8264B Series

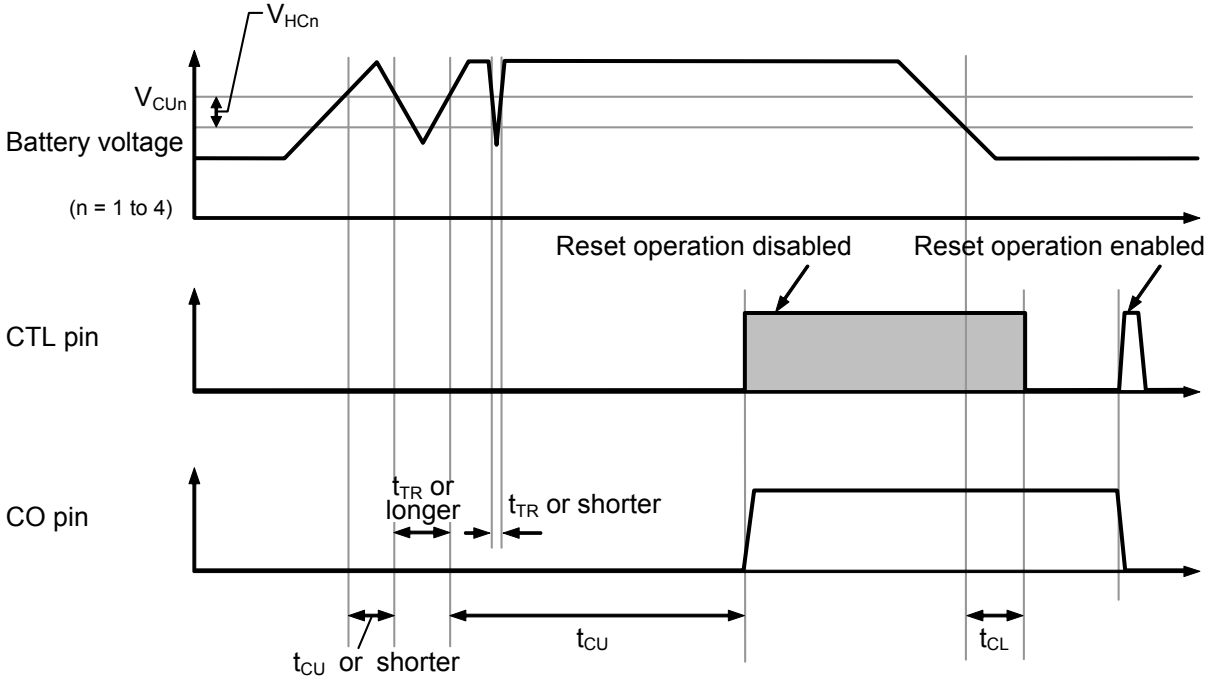


Figure 11

2. Overcharge Timer Reset Operation

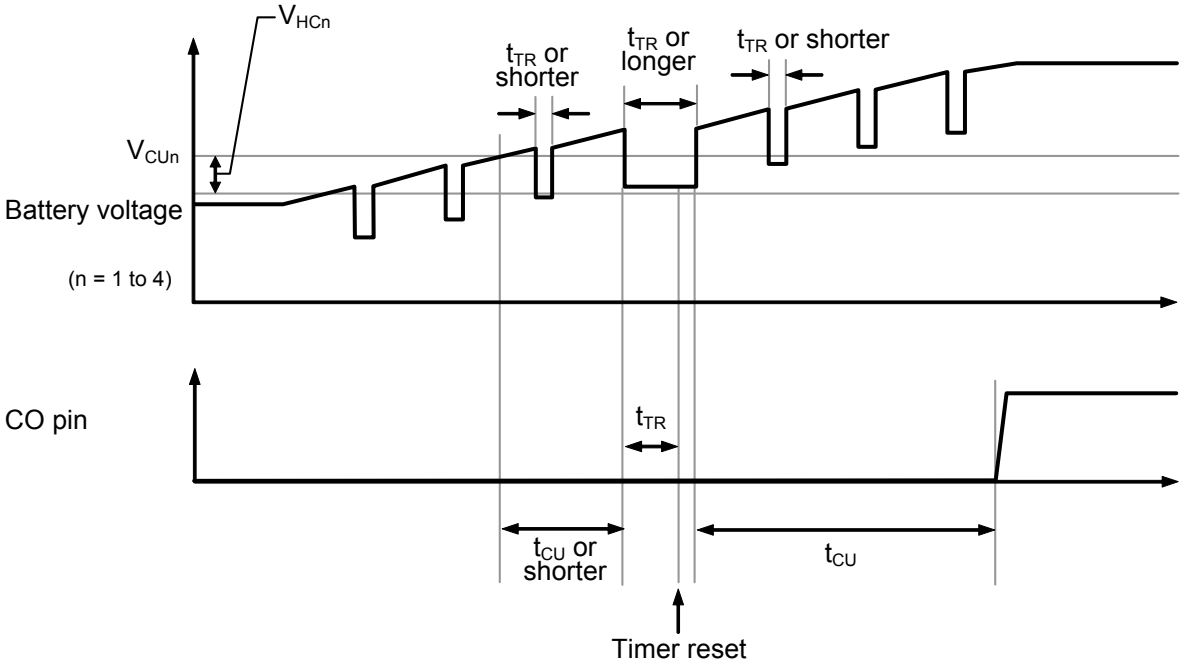


Figure 12

■ Battery Protection IC Connection Example

(1) 4-serial cell

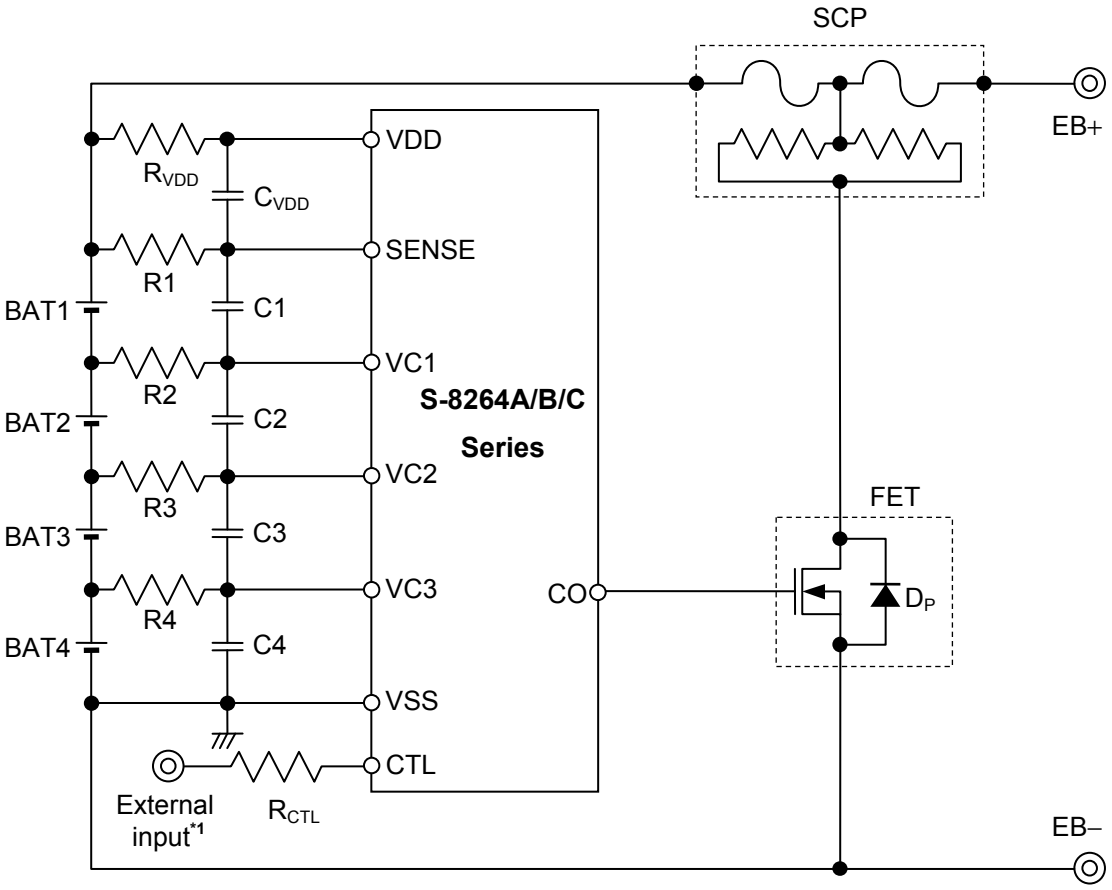


Figure 13

*1. Refer to **Table 14** for setting on external input.

Table 15 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R4	0.1	1	10	kΩ
2	C1 to C4, C_{VDD}	0.01	0.1	1	μF
3	R_{VDD}	50	100	500	Ω
4	R_{CTL}	0	100	500	Ω

Caution
1. **The above constants are subject to change without prior notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**
3. **Set the same constants to R1 to R4 and to C1 to C4 and C_{VDD}.**
4. **Set R_{VDD}, C1 to C4, and C_{VDD} so that the condition (R_{VDD}) × (C1 to C4, C_{VDD}) ≥ 5×10^{-6} is satisfied.**
5. **Set R1 to R4, C1 to C4, and C_{VDD} so that the condition (R1 to R4) × (C1 to C4, C_{VDD}) ≥ 1×10^{-4} is satisfied.**
6. **Since "H" may be output at CO transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.**

(2) 3-serial cell

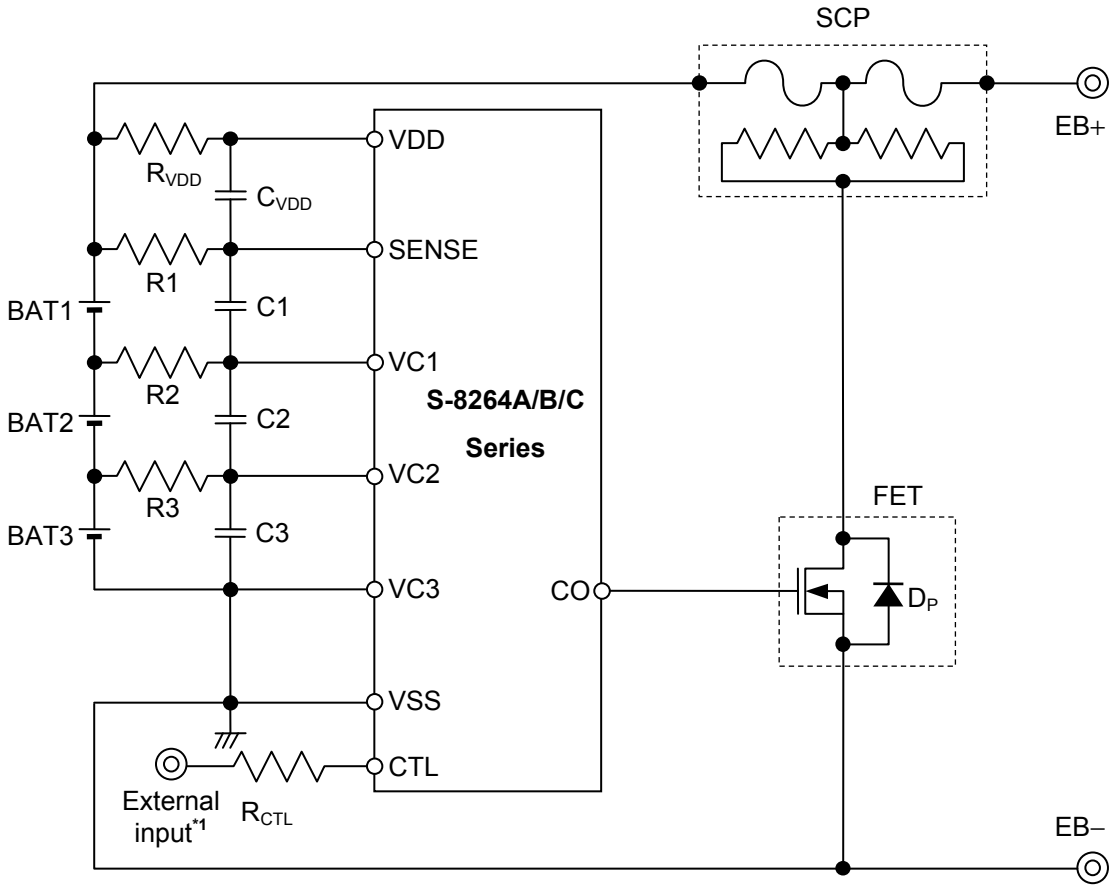


Figure 14

***1.** Refer to **Table 14** for setting on external input.

Table 16 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R3	0.1	1	10	kΩ
2	C1 to C3, C_{VDD}	0.01	0.1	1	μF
3	R_{VDD}	50	100	500	Ω
4	R_{CTL}	0	100	500	Ω

Caution
1. **The above constants are subject to change without prior notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**
3. **Set the same constants to R1 to R3 and to C1 to C3 and C_{VDD}.**
4. **Set R_{VDD}, C1 to C3, and C_{VDD} so that the condition (R_{VDD}) × (C1 to C3, C_{VDD}) ≥ 5×10^{-6} is satisfied.**
5. **Set R1 to R3, C1 to C3, and C_{VDD} so that the condition (R1 to R3) × (C1 to C3, C_{VDD}) ≥ 1×10^{-4} is satisfied.**
6. **Since "H" may be output at CO transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.**

(3) 2-serial cell

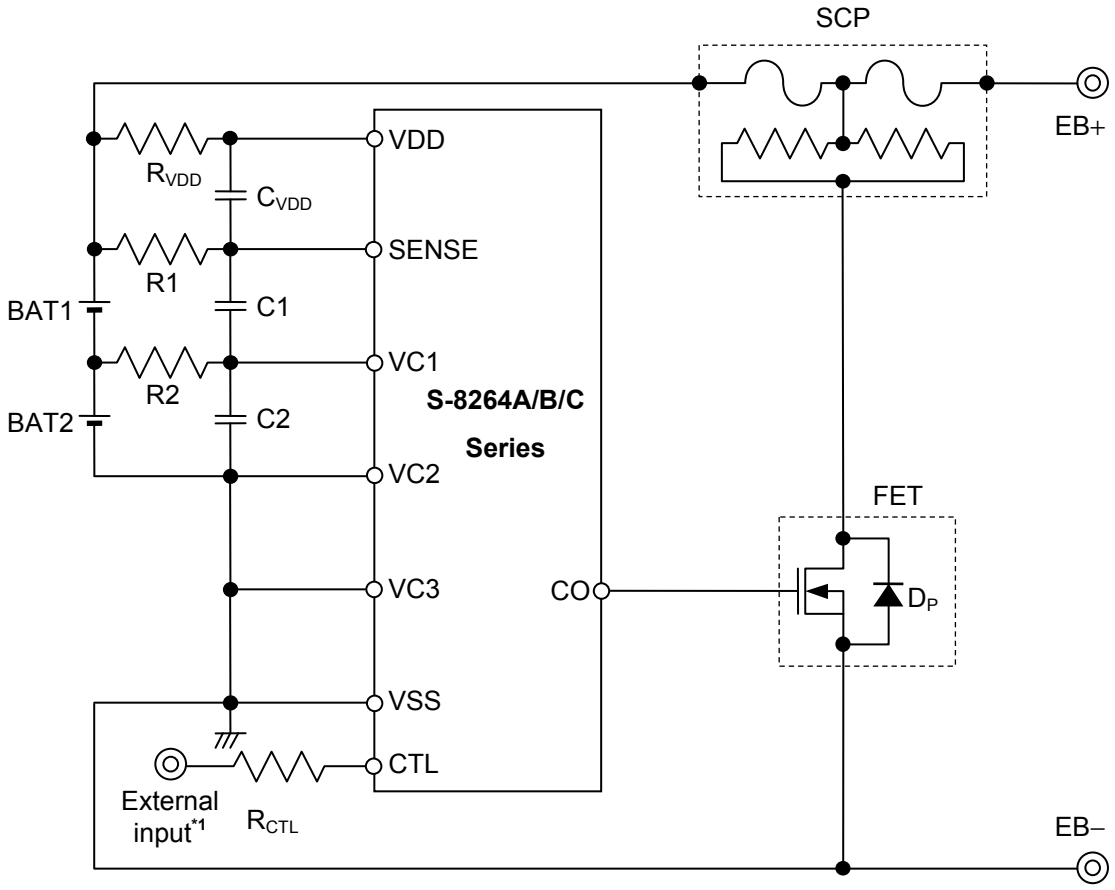


Figure 15

*1. Refer to **Table 14** for setting on external input.

Table 17 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 and R2	0.1	1	10	kΩ
2	C1 and C2, C_{VDD}	0.01	0.1	1	μF
3	R_{VDD}	50	100	500	Ω
4	R_{CTL}	0	100	500	Ω

Caution
1. **The above constants are subject to change without prior notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**
3. **Set the same constants to R1 to R3 and to C1 to C3 and C_{VDD}.**
4. **Set R_{VDD}, C1 to C3, and C_{VDD} so that the condition (R_{VDD}) × (C1 to C3, C_{VDD}) ≥ 5×10^{-6} is satisfied.**
5. **Set R1 to R3, C1 to C3, and C_{VDD} so that the condition (R1 to R3) × (C1 to C3, C_{VDD}) ≥ 1×10^{-4} is satisfied.**
6. **Since "H" may be output at CO transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.**

■ Precautions

- Do not connect batteries charged with V_{CU} + V_{HC} or higher. If the connected batteries include a battery charged with V_{CU} + V_{HC} or higher, "H" may be output at CO after all pins are connected.
- In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of CO detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.
- In the S-8264B Series, "H" may be output at CO after all the pins are connected. In this case, set the CTL pin from "L" to "H".
- Before the battery connection, short-circuit the battery side pins R_{VDD} and R1, shown in the figure in "**■ Battery Protection IC Connection Example**".
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

■ Example of Application Circuit

1. Overheat Protection via PTC (S-8264A Series)

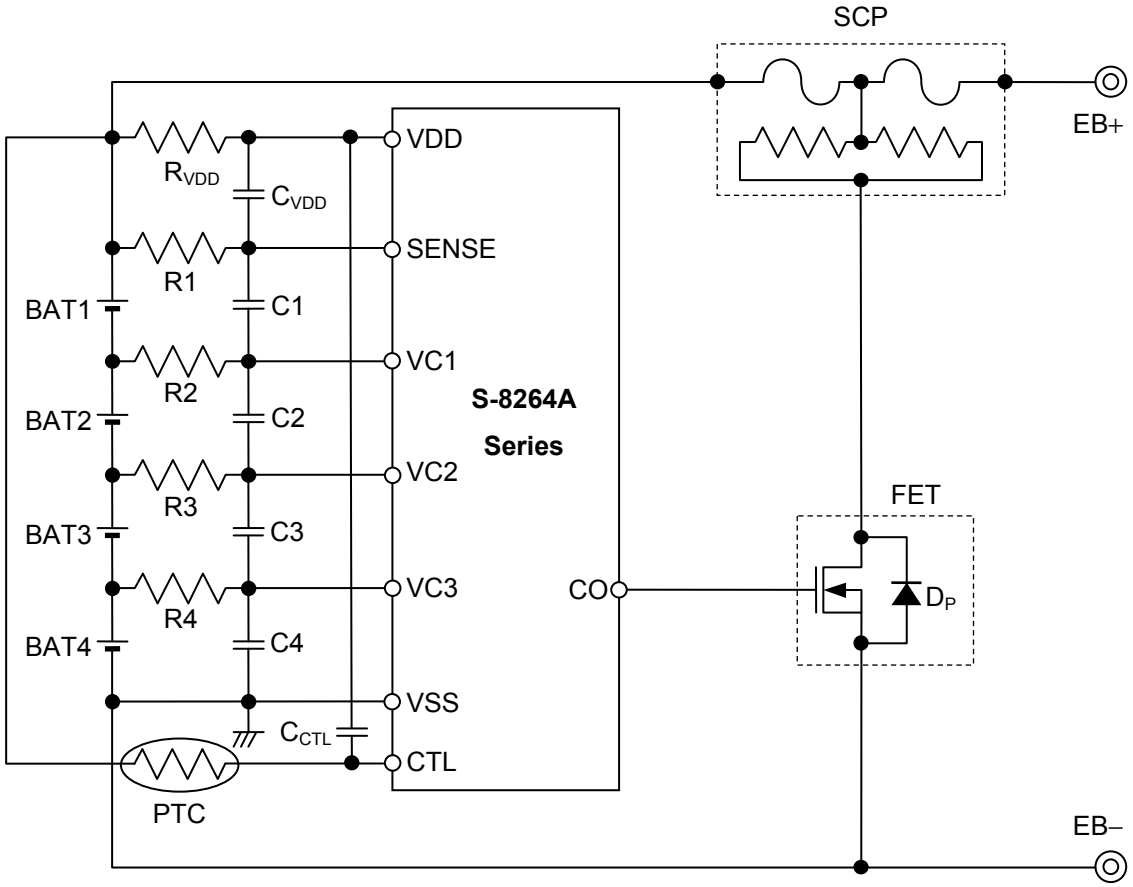


Figure 16

Cautions
1. **The above connection example will not guarantee successful operation. Perform thorough evaluation using the actual application.**
2. **A pull-down resistor is included in the CTL pin. To perform overheat protection via the PTC in the S-8264A Series, connect the PTC before connecting batteries.**
3. **When the power fluctuation is large, connect the power supply of the PTC to the VDD pin of the S-8264A Series.**
4. **Since "H" may be output at CO transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.**

[For SCP, contact]

Global Sales & Marketing Division, Dexerials Corporation
Gate City Osaki East Tower 8F, 1-11-2
Osaki, Shinagawa-ku, Tokyo, 141-0032, Japan
TEL +81-3-5435-3946
Contact Us: http://www.dexerials.jp/en/

[For PTC, contact]

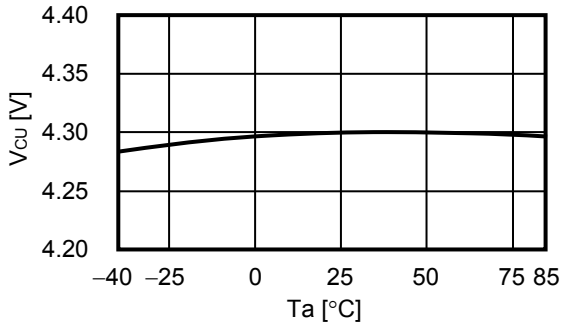
Murata Manufacturing Co., Ltd.
Thermistor Products Department
Nagaokakyo-shi, Kyoto, 617-8555, Japan
TEL +81-75-955-6863
Contact Us: http://www.murata.com/contact/index.html

■ Characteristics (Typical Data)

1. Detection Voltage vs. Temperature

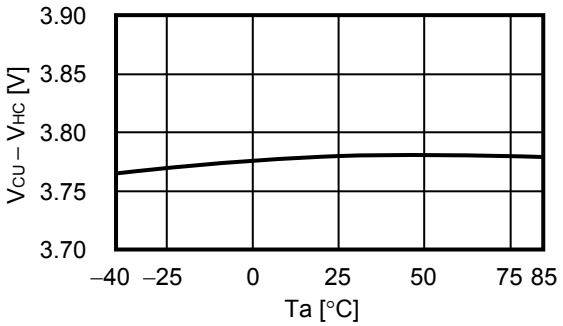
(1) Overcharge Detection Voltage vs. Temperature

V_{CU} = 4.3 V



(2) Overcharge Release Voltage vs. Temperature

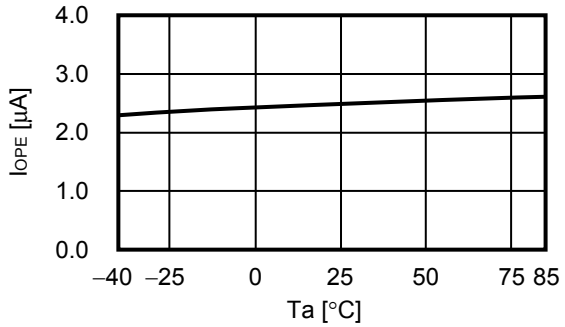
V_{HC} = 0.52 V



2. Current Consumption vs. Temperature

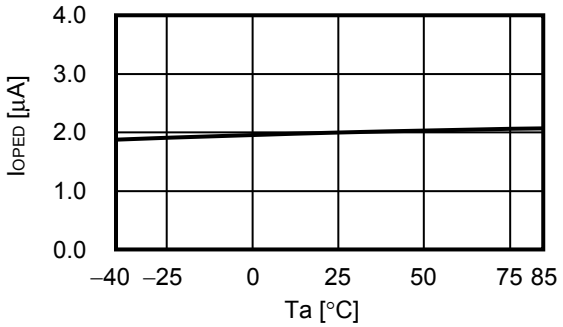
(1) Current Consumption during Normal Operation vs. Temperature

V_{DD} = 14 V



(2) Current Consumption during Overdischarge vs. Temperature

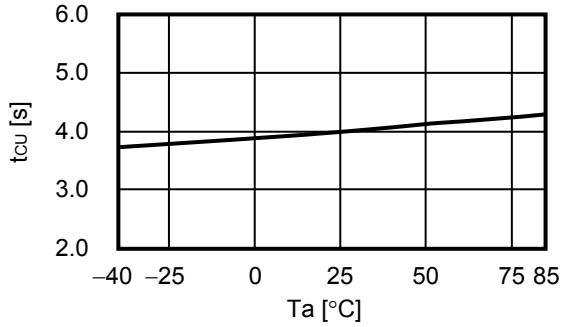
V_{DD} = 9.2 V



3. Delay Time vs. Temperature

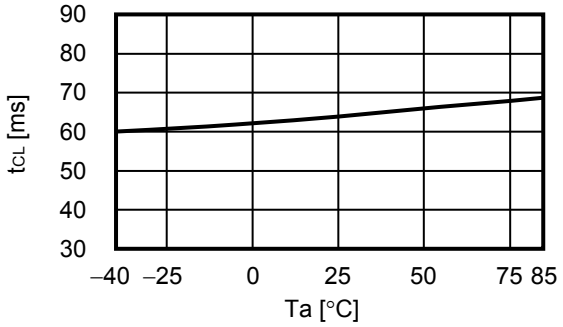
(1) Overcharge Detection Delay Time vs. Temperature

V_{DD} = 20 V



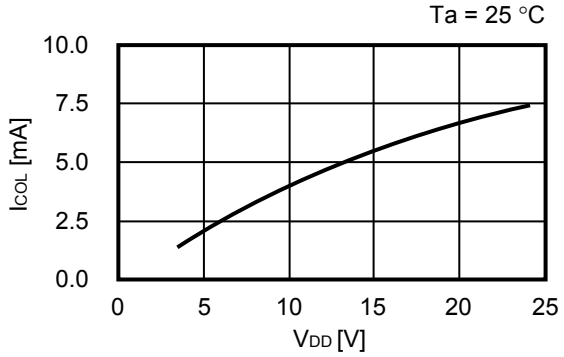
(2) Overcharge Release Delay Time vs. Temperature

V_{DD} = 14 V

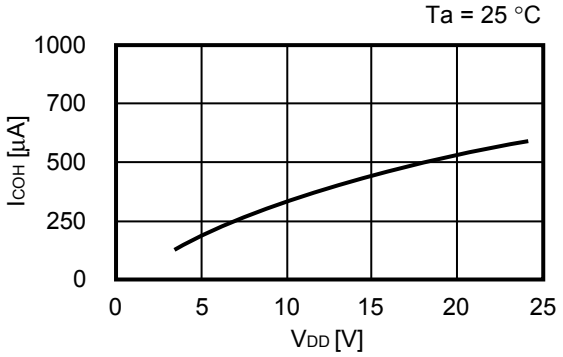


4. Output Current vs. Temperature

(1) CO Pin Sink Current vs. V_{DD}

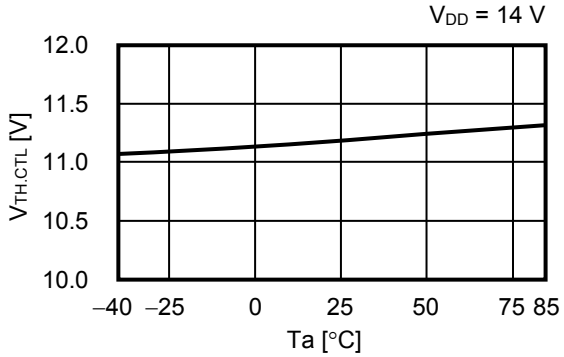


(2) CO Pin Source Current vs. V_{DD}

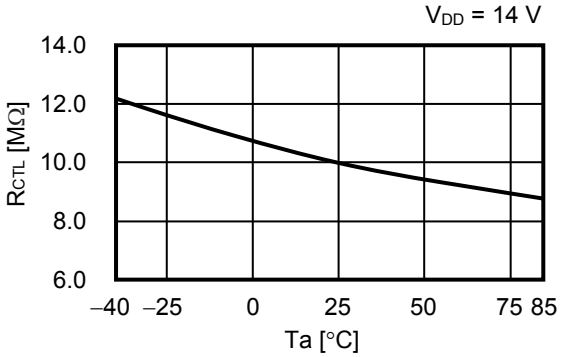


5. CTL Pin vs. Temperature

(1) CTL Pin Threshold Voltage vs. Temperature

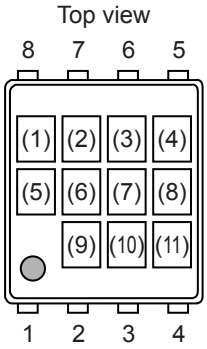


(2) CTL Pin Input Resistance vs. Temperature



■ Marking Specifications

(1) SNT-8A



(1)	Blank
(2) to (4)	Product code (Refer to **Product name vs. Product code**)
(5), (6)	Blank
(7) to (11)	Lot number

Product name vs. Product code

(a) S-8264A Series

Product Name	Product Code		
	(2)	(3)	(4)
S-8264AAA-I8T1U	Q	5	A
S-8264AAB-I8T1U	Q	5	B
S-8264AAC-I8T1U	Q	5	C
S-8264AAD-I8T1U	Q	5	D
S-8264AAE-I8T1U	Q	5	E
S-8264AAF-I8T1U	Q	5	F
S-8264AAG-I8T1U	Q	5	G
S-8264AAH-I8T1U	Q	5	H
S-8264AAI-I8T1U	Q	5	I
S-8264AAJ-I8T1U	Q	5	J
S-8264AAK-I8T1U	Q	5	K
S-8264AAO-I8T1U	Q	5	O
S-8264AAS-I8T1U	Q	5	S
S-8264AAT-I8T1U	Q	5	T
S-8264AAV-I8T1U	Q	5	V
S-8264AAW-I8T1U	Q	5	W

(b) S-8264B Series

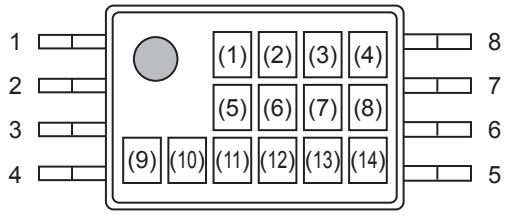
Product Name	Product Code		
	(2)	(3)	(4)
S-8264BAA-I8T1U	Q	6	A
S-8264BAB-I8T1U	Q	6	B
S-8264BAC-I8T1U	Q	6	C

(c) S-8264C Series

Product Name	Product Code		
	(2)	(3)	(4)
S-8264CAA-I8T1U	Q	7	A
S-8264CAB-I8T1U	Q	7	B

(2) 8-Pin TSSOP

Top view



(1) to (5)	Product name: S8264 (Fixed)
(6) to (8)	Function code
(9) to (14)	Lot number

Product name vs. Product code

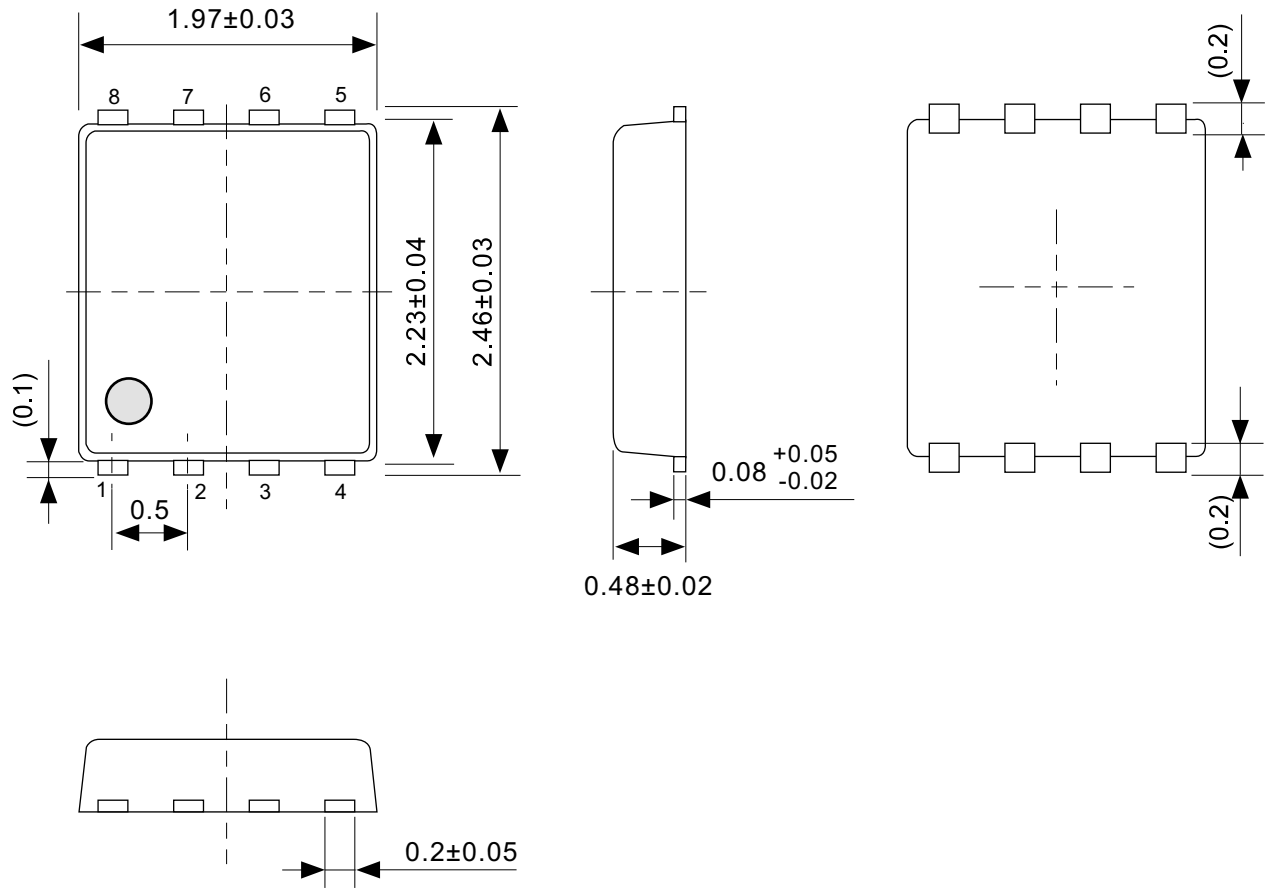
(a) S-8264A Series

Product Name	Product Code		
	(1)	(2)	(3)
S-8264AAA-T8T1x	A	A	A
S-8264AAB-T8T1x	A	A	B
S-8264AAK-T8T1U	A	A	K

(b) S-8264B Series

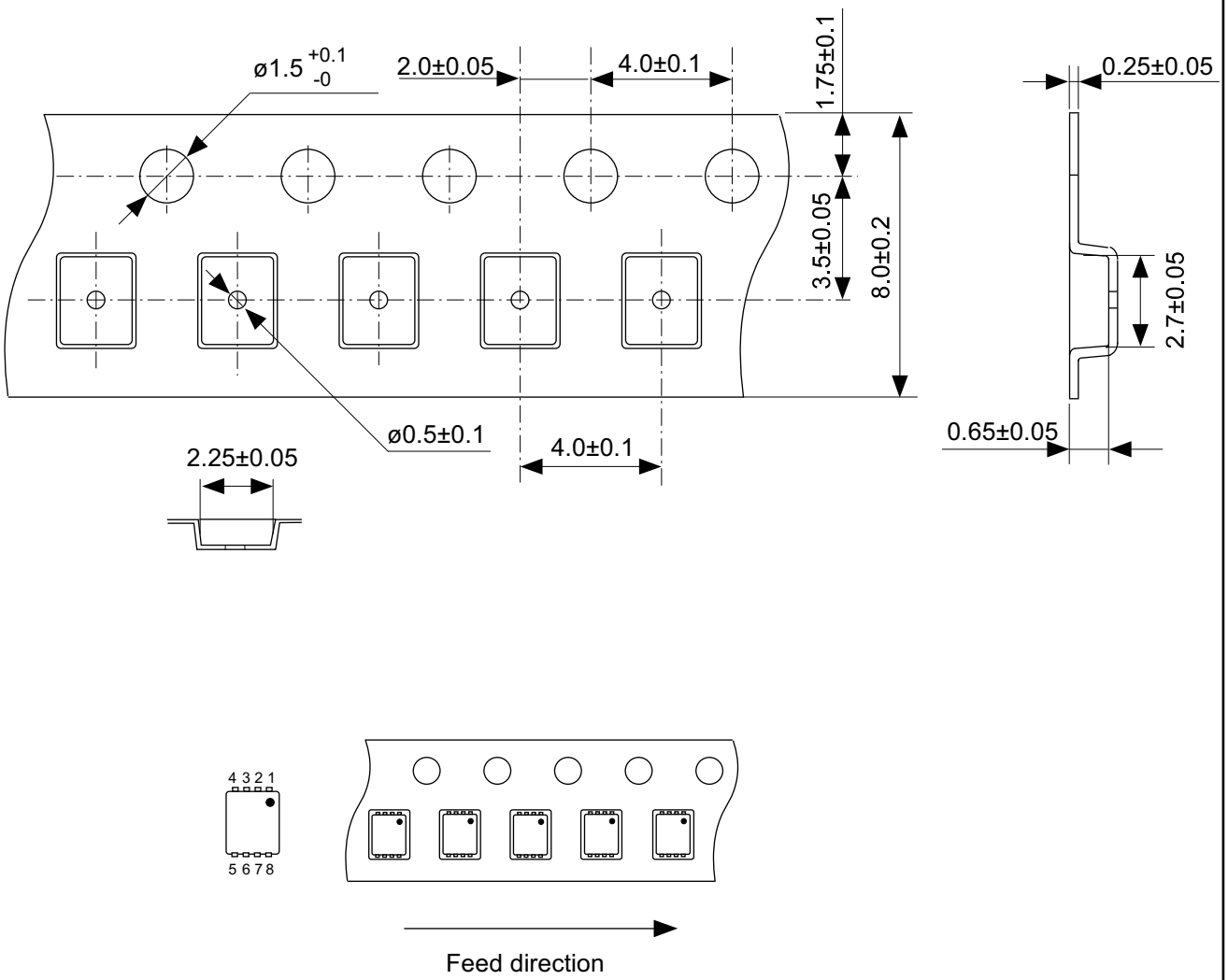
Product Name	Product Code		
	(1)	(2)	(3)
S-8264BAB-T8T1x	B	A	B

Remark **1.** x: G or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.



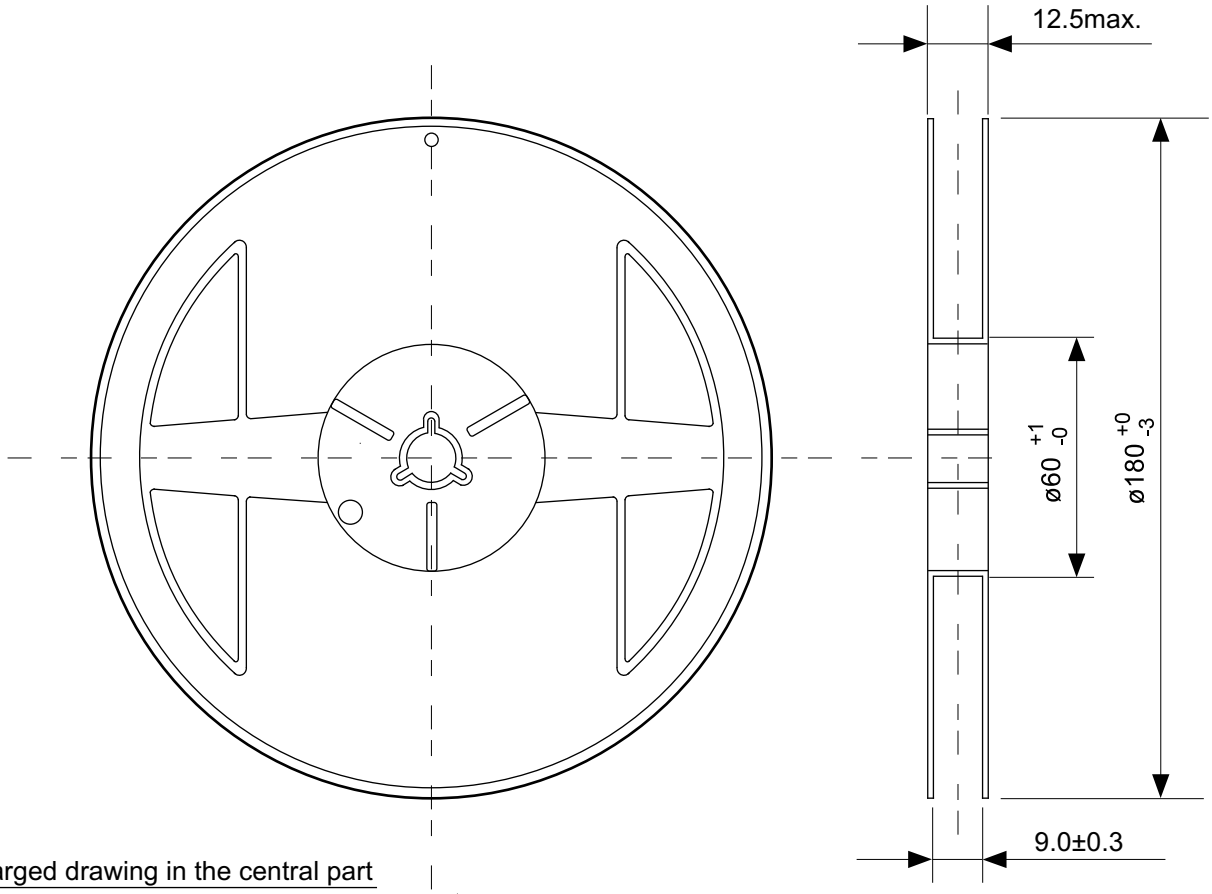
No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

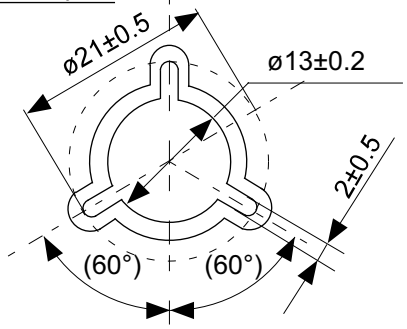


No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

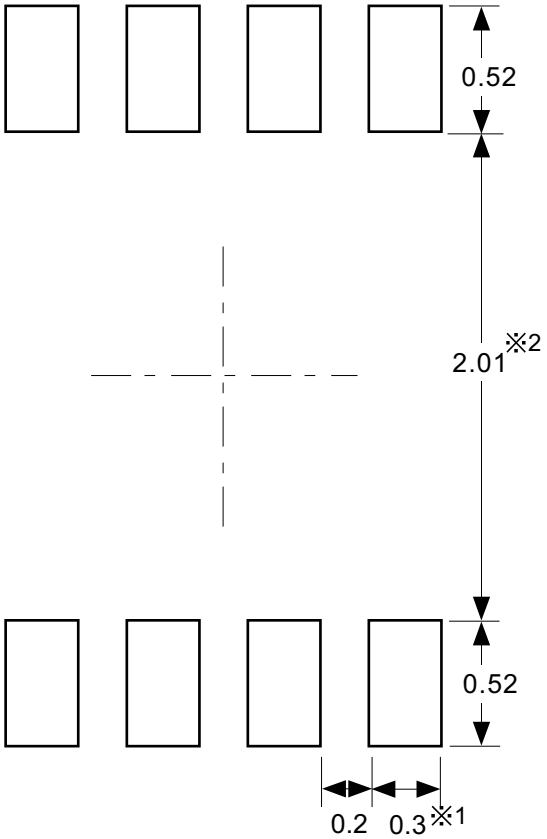


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

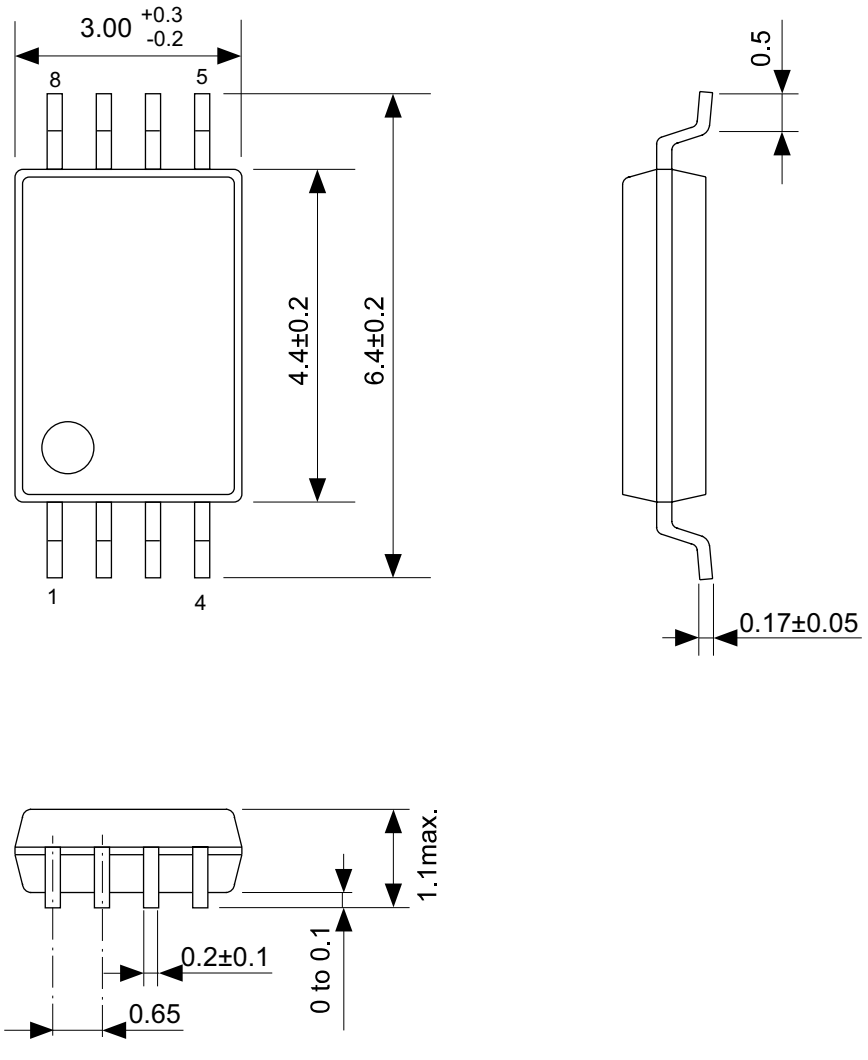
Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

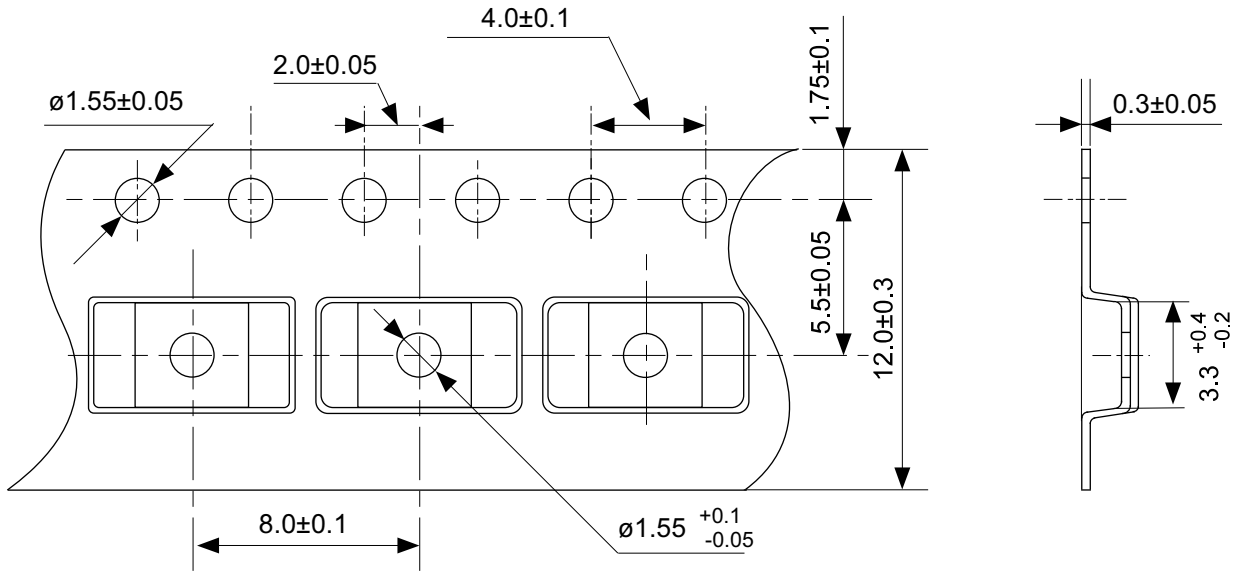
TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

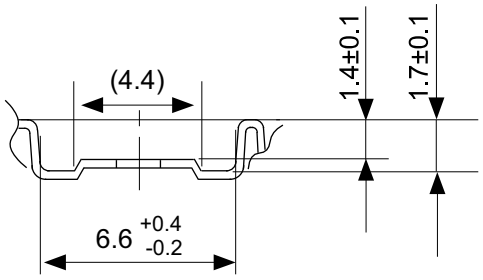


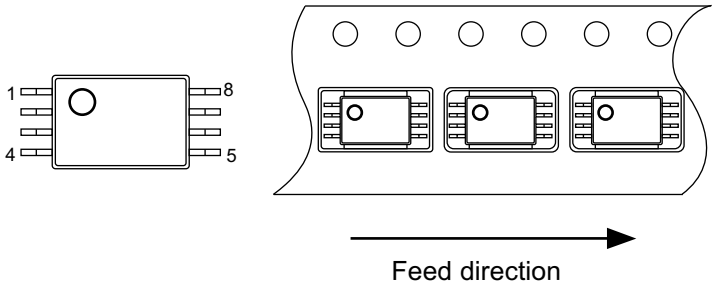
No. FT008-A-P-SD-1.2

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.2
ANGLE	
UNIT	mm

ABLIC Inc.

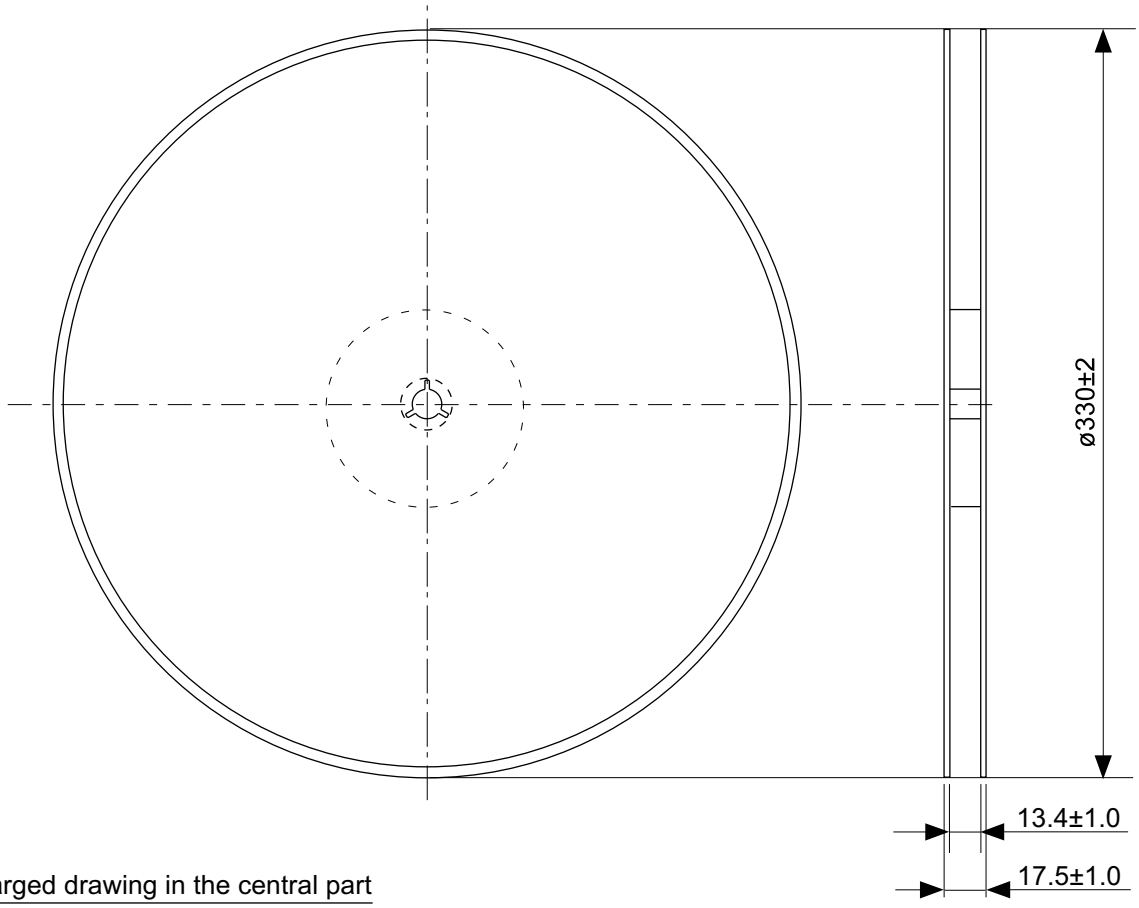




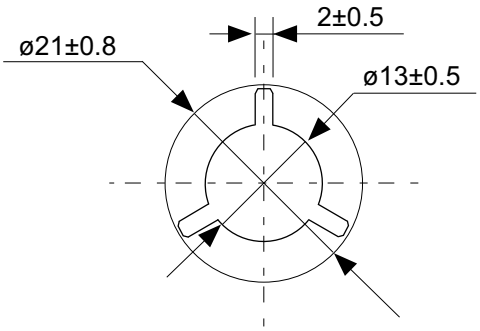


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

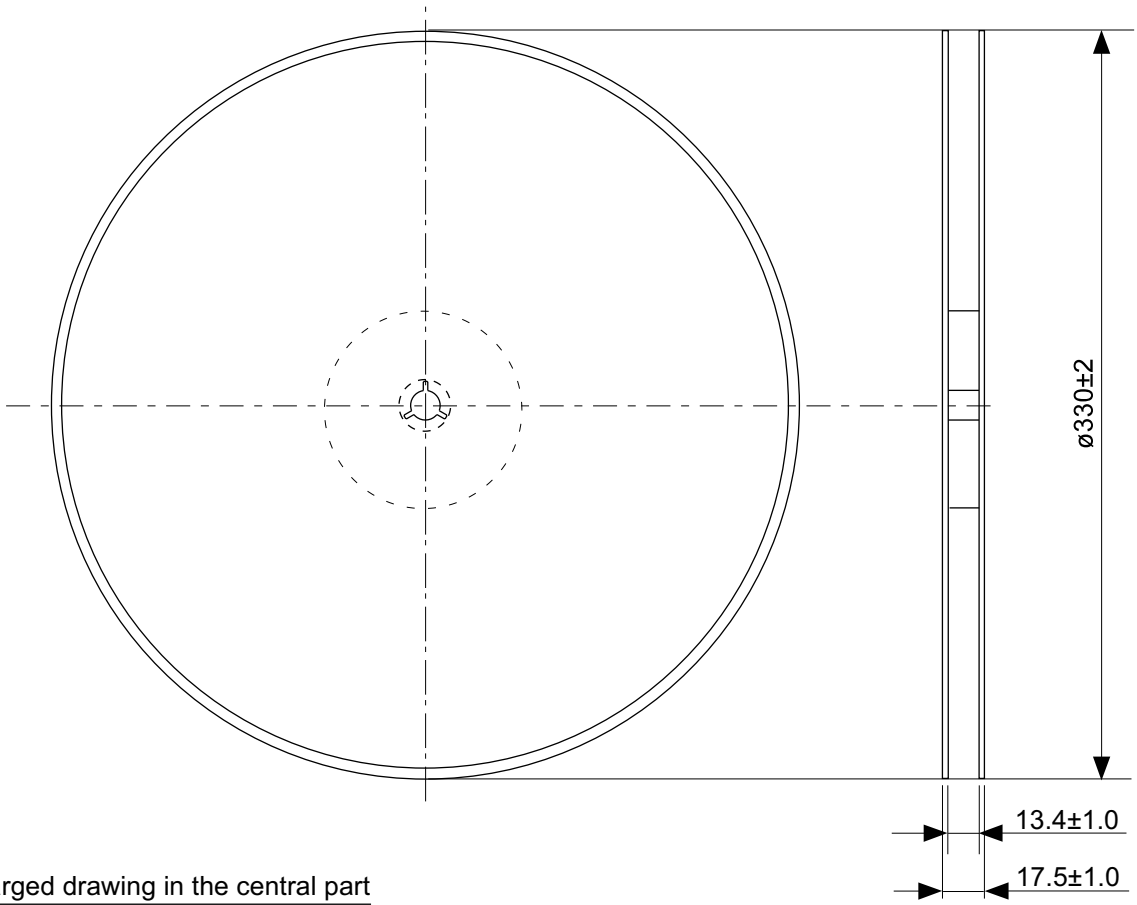


Enlarged drawing in the central part

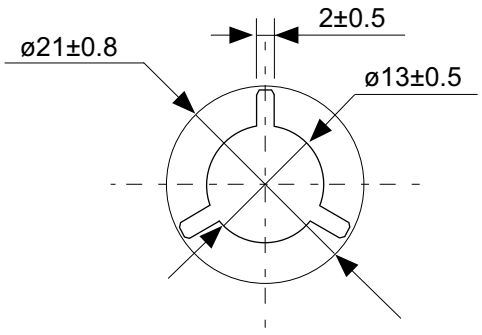


No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



Enlarged drawing in the central part



No. FT008-E-R-S1-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-S1-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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2.4-2019.07