DS90UB964-Q1 Quad FPD-Link III Deserializer Hub

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 2: –40℃ to +105℃ Ambient Operating Temperature Range
  - Device HBM ESD Classification Level ±4 kV
  - Device CDM ESD Classification Level C6
- Aggregates Data From up to 4 Cameras Over FPD-Link III Interface
- Supports 1-Megapixel Sensors With HD 720p/800p/960p Resolution at 30-Hz or 60-Hz Frame Rate
- Multi-Camera Synchronization
- MIPI DPHY Version 1.2 / CSI-2 Version 1.3 Compliant
  - 2× CSI-2 Output Ports
  - Supports 1, 2, 3, 4 Data Lanes per CSI-2 port
  - CSI-2 Data Rate Scalable for 400 Mbps / 800 Mbps / 1.5 Gbps / 1.6 Gbps each Data Lane
  - Programmable Data Types
  - Four Virtual Channels
  - ECC and CRC Generation
- Supports Single-Ended Coaxial or Shielded Twisted-Pair (STP) Cable
- Adaptive Receive Equalization
- I2C With Fast-Mode Plus up to 1 Mbps
- Flexible GPIOs for Camera Sync and Functional Safety
- Compatible With DS90UB913AQ/913Q/933Q Serializers
- CRC protection on the internal Data Path
- ISO 10605 and IEC 61000-4-2 ESD Compliant

2 Applications

- Automotive ADAS
  - Surround View Systems
  - Camera Monitoring Systems
  - Sensor Fusion
- Security and Surveillance

3 Description

The DS90UB964-Q1 is a versatile camera hub capable of connecting serialized camera data received from 4 independent video datastreams via an FPD-Link III interface. When coupled with DS90UB913AQ/913Q/933Q serializers, the DS90UB964-Q1 receives data from 1-Megapixel image sensors supporting 720p/800p/960p resolution at 30-Hz or 60-Hz frame rates. Data is received and aggregated into a MIPI CSI-2 compliant output for interconnect to a downstream processor. A second MIPI CSI-2 output port is available to provide additional bandwidth, or offers a second replicated output.

The DS90UB964-Q1 includes 4 FPD-Link III deserializers, each enabling a connection via cost-effective 50-Ω single-ended coaxial or 100-Ω differential STP cables. The receive equalizer automatically adapts to compensate for cable loss characteristics, including degradation over time.

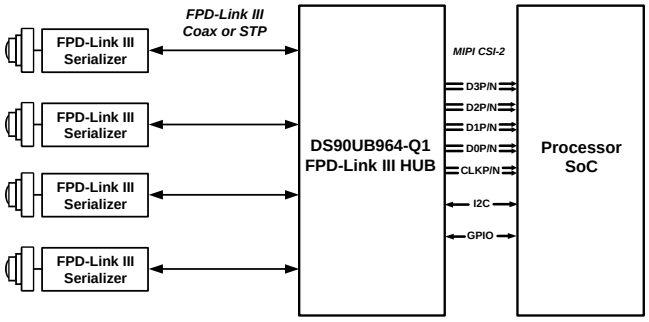
Each of the FPD-Link III interfaces also includes a separate low latency bi-directional control channel that conveys control information from an I2C port and is independent of video blanking period. General purpose I/O signals such as those required for camera synchronization and functional safety features also make use of this bi-directional control channel.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UB964-Q1	VQFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

DATE	REVISION	NOTES
July 2016	*	Initial release.

5 Pin Configuration and Functions

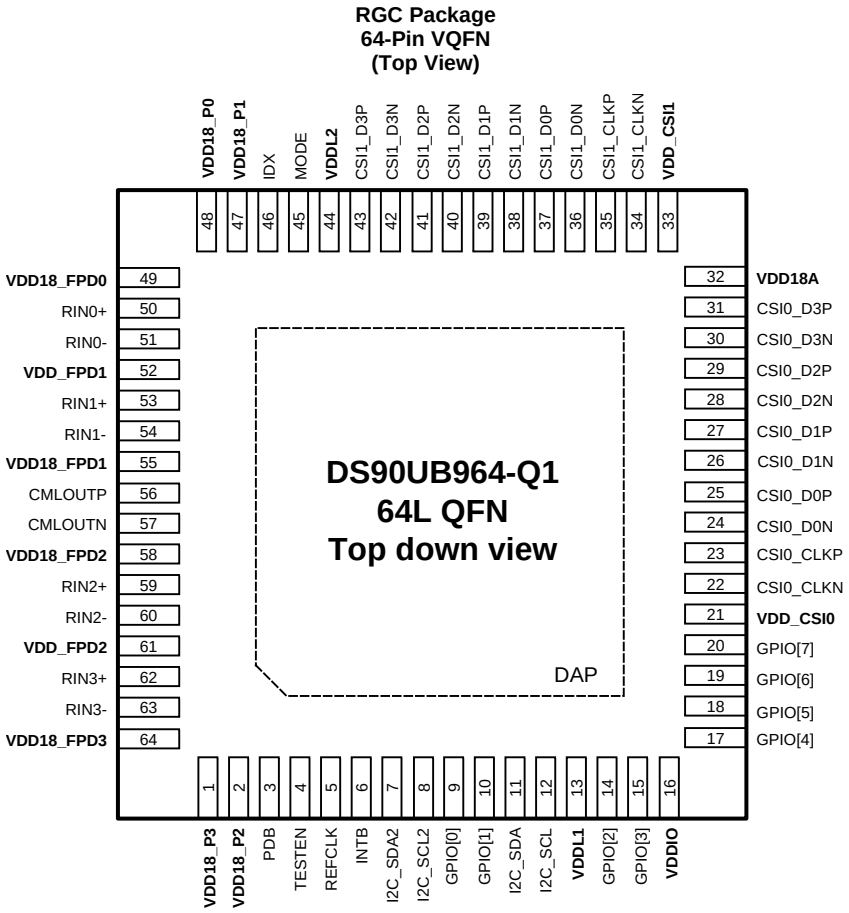


Table 1. Pin Functions

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
MIPI DPHY/CSI-2			
CSI0_CLKN/P	22, 23	O, DPHY	CSI0 Differential clock If unused, leave this pin unconnected.
CSI0_D0N/P	24, 25	O, DPHY	CSI0 Differential data pair 0 If unused, leave this pin unconnected.
CSI0_D1N/P	26, 27	O, DPHY	CSI0 Differential data pair 1 If unused, leave this pin unconnected.
CSI0_D2N/P	28, 29	O, DPHY	CSI0 Differential data pair 2 If unused, leave this pin unconnected.
CSI0_D3N/P	30, 31	O, DPHY	CSI0 Differential data pair 3 If unused, leave this pin unconnected.
CSI1_CLKN/P	34, 35	O, DPHY	CSI1 Differential clock If unused, leave this pin unconnected.
CSI1_D0N/P	36, 37	O, DPHY	CSI1 Differential data pair 0 If unused, leave this pin unconnected.
CSI1_D1N/P	38, 39	O, DPHY	CSI1 Differential data pair 1 If unused, leave this pin unconnected.
CSI1_D2N/P	40, 41	O, DPHY	CSI1 Differential data pair 2 If unused, leave this pin unconnected.

Table 1. Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
CSI1_D3N/P	42, 43	O, DPHY	CSI1 Differential data pair 3 If unused, leave this pin unconnected.
FPD-LINK III INTERFACE			
RIN0-/+	51, 50	I/O, CML	FPD-Link III Input/Output. The pin must be AC-coupled with a capacitor. If port is unused, set RX_PORT_CTL register bit N to 0 to disable.
RIN1-/+	54, 53	I/O, CML	FPD-Link III Input/Output. The pin must be AC-coupled with a capacitor. If port is unused, set RX_PORT_CTL register bit N to 0 to disable.
RIN2-/+	60, 59	I/O, CML	FPD-Link III Input/Output. The pin must be AC-coupled with a capacitor. If port is unused, set RX_PORT_CTL register bit N to 0 to disable.
RIN3-/+	63, 62	I/O, CML	FPD-Link III Input/Output. The pin must be AC-coupled with a capacitor. If port is unused, set RX_PORT_CTL register bit N to 0 to disable.
GPIO PINS (GENERAL PURPOSE INPUT OUTPUT)			
GPIO[0]	9	I/O, LVCMOS, PD	General Purpose Input/Output 0 See *GPIO Support*.
GPIO[1]	10	I/O, LVCMOS, PD	General Purpose Input/Output 1 See *GPIO Support*.
GPIO[2]	14	I/O, LVCMOS, PD	General Purpose Input/Output 2 See *GPIO Support*.
GPIO[3]	15	I/O, LVCMOS, PD	General Purpose Input/Output 3 See *GPIO Support*.
GPIO[4]	17	I/O, LVCMOS, PD	General Purpose Input/Output 4 See *GPIO Support*.
GPIO[5]	18	I/O, LVCMOS, PD	General Purpose Input/Output 5 See *GPIO Support*.
GPIO[6]	19	I/O, LVCMOS, PD	General Purpose Input/Output 6 See *GPIO Support*.
GPIO[7]	20	I/O, LVCMOS, PD	General Purpose Input/Output 7 See *GPIO Support*.
I2C PINS			
I2C_SCL	12	I/O, LVCMOS, Open Drain	I2C Clock Input / Output Interface Recommended Pull-up(1) to 4.7 kΩ to VDDIO.
I2C_SDA	11	I/O, LVCMOS, Open Drain	I2C Data Input / Output Interface Recommended Pull-up(1) to 4.7 kΩ to VDDIO.
I2C_SCL2	8	I/O, LVCMOS, Open Drain	I2C Clock Input / Output Interface Recommended Pull-up(1) to 4.7 kΩ to VDDIO.
I2C_SDA2	7	I/O, LVCMOS, Open Drain	I2C Data Input / Output Interface Recommended Pull-up(1) to 4.7 kΩ to VDDIO.
IDx	46	S	I2C Serial Control Bus Device ID Address Connect to external pull-up to VDD18 and pull-down to GND to create a voltage divider. See Table 10.
CONTROL PINS			
MODE	45	S	Mode selection Connect to external pull-up to VDD18 and pull-down to GND to create a voltage divider. See Table 2.
PDB	3	I, 1.8V LVCMOS, PD	Power-down mode **INPUT IS 3.3V TOLERANT** PDB = 1.8 V, device is enabled (normal operation) PDB = 0, device is powered down.
STATUS PINS			
INTB	6	O, LVCMOS, Open Drain	Interrupt Output INTB is an active-low open drain and controlled by the status registers. Recommended Pull-up with 4.7 kΩ to VDDIO.
POWER AND GROUND			

(1) Optimum Pull-up Resistor (RPU) value depends on the I2C mode of operation, refer to *SLVA689*

Table 1. Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
VDDIO	16	P	1.8 V (±5%) OR 3.3V (±10%) LVCMOS I/O Power Requires 1 μF, 0.1 μF, and 0.01 μF capacitors to GND
VDD_CSI0 VDD_CSI1	21 33	P	1.1 V (±5%) Power Supplies Requires 0.1 μF or 0.01 μF capacitors to GND at each VDD pin.
VDDL1 VDDL2	13 44	P	1.1 V (±5%) Power Supplies Requires 0.1 μF or 0.01 μF capacitors to GND at each VDD pin.
VDD_FPD1 VDD_FPD2	52 61	P	1.1 V (±5%) Power Supplies Requires 0.1 μF or 0.01 μF capacitors to GND at each VDD pin.
VDD18_P2 VDD18_P3 VDD18_P1 VDD18_P0	2 1 47 48	P	1.8 V (±5%) Power Supplies Requires 0.1 μF or 0.01 μF capacitors to GND at each VDD pin.
VDD18A	32	P	1.8 V (±5%) Power Supplies Requires 0.1 μF or 0.01 μF capacitors to GND at each VDD pin.
VDD18_FPD0 VDD18_FPD1 VDD18_FPD2 VDD18_FPD3	49 55 58 64	P	1.8 V (±5%) Power Supplies Requires 0.1 μF or 0.01 μF capacitors to GND at each VDD pin.
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the VQFN package. Connect to the ground plane (GND).
OTHERS			
REFCLK	5	I, LVCMOS	Reference clock oscillator input. 25 MHz or 23 MHz LVCMOS-level oscillator input (100 ppm). For 400/800 Mbps / 1.6 Gbps a 25 MHz input is used, and for < 1.5 Gbps operation use 23 MHz (1.47 Gbps) See *REFCLK*.
TESTEN	4	I, LVCMOS, PD	This pin should be tied Low.
CMLOUTP/N	56, 57	O	Channel Monitor Loop-through Output Driver Route to test point or pad with 100 Ω termination resistor between pins for channel monitoring (recommended). See *Channel Monitor Loop-Through Output Driver*.

The definitions below define the functionality of the I/O cells for each pin.

TYPE:

- P = Power Supply
- G = Ground
- CML = CML Interface
- DPHY = MIPI DPHY Interface
- LVCMOS = LVCMOS pin
- I = Input
- O = Output
- I/O = Input/Output
- S = Strap Input
- PD, PU = Internal Pull-Down/Pull-Up (All strap pins have weak internal pull-ups or pull-downs determined by IOZ specification. If the default strap value is needed to be changed then an external 1 kΩ resistor should be used.)

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage	VDD11	–0.3	1.8	V
	VDD18	–0.3	2.5	V
	VDDIO	–0.3	4	V
LVCMOS IO voltage		–0.3	VDDIO + 0.3	V
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office or Distributors for availability and specifications.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings – JEDEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	RIN[3:0]+, RIN[3:0]-	±8000	V
			Other pins	±4000	
		Charged device model (CDM), per AEC Q100-011		±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings – IEC and ISO

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ESD Rating (IEC 61000-4-2) R_D= 330 Ω, C_S = 150 pF	Contact Discharge (RIN[3:0]+, RIN[3:0]-)	±8000	V
			Air Discharge (RIN[3:0]+, RIN[3:0]-)	±18000	
		ESD Rating (ISO 10605) R_D= 330 Ω, C_S = 150 pF and 330 pF R_D= 2 kΩ, C_S = 150 pF and 330 pF	Contact Discharge (RIN[3:0]+, RIN[3:0]-)	±8000	V
			Air Discharge (RIN[3:0]+, RIN[3:0]-)	±18000	

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage	VDD11		1.045	1.1	1.155	V
	VDD18		1.71	1.8	1.89	V
LVCMOS supply voltage	VDDIO	1.8V Option	1.71	1.8	1.89	V
		3.3V Option	3.0	3.3	3.6	V
Operating free-air temperature, T_A			–40	25	105	°C
MIPI data rate (per CSI-2 lane)			400	800	1600	Mbps
MIPI CSI-2 HS clock frequency			200	400	800	MHz
Local I^2C frequency, f_{I2C}					1	MHz

Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply Noise(1)	VDD11				25	mV_{P-P}
	VDD18				50	mV_{P-P}
	VDDIO	1.8V Option			50	mV_{P-P}
		3.3V Option			100	mV_{P-P}

(1) Supply noise testing was performed with minimum capacitors (as shown Figure 38 on the PCB). A sinusoidal signal is AC coupled from DC to 10 MHz to the VDD11, VDD18, and VDDIO (1.8V / 3.3V) supply pins with amplitude of 25 mVp-p, 50 mVp-p, and 50 mVp-p / 100 mVp-p respectively measured at the device VDD pins.

6.5 Thermal Information

THERMAL METRIC(1)		DS90UB964-Q1 RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
1.8 V LVCMOS I/O (VDDIO = 1.8 V ± 5%)							
V_{IH}	High Level Input Voltage		GPIO[7:0], PDB, REFCLK	0.65 × VDDIO		VDDIO	V
V_{IL}	Low Level Input Voltage			GND		0.35 × VDDIO	V
I_{IN}	Input Current	VIN = 0 V or VDDIO	GPIO[7:0](1), PDB	–20		20	µA
V_{OH}	High Level Output Voltage	I_{OH} = –2 mA	GPIO[7:0]	VDDIO – 0.45		VDDIO	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA	GPIO[7:0], INTB	GND		0.45	V
I_{OS}	Output Short Circuit Current	VOUT = 0 V	GPIO[7:0]		–35		mA
I_{OZ}	TRI-STATE Output Current	VOUT = 0 V or VDDIO, PDB = LOW	GPIO[7:0]	–20		20	µA
3.3 V LVCMOS I/O (VDDIO = 3.3 V ± 10%)							
V_{IH}	High Level Input Voltage		GPIO[7:0], REFCLK	2		VDDIO	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IN}	Input Current	VIN = 0 V or VDDIO	GPIO[7:0](1)	–20		20	µA
V_{OH}	High Level Output Voltage	I_{OH} = –4 mA	GPIO[7:0]	2.4		VDDIO	V
V_{OL}	Low Level Output Voltage	I_{OL} = 4 mA	GPIO[7:0], INTB	GND		0.4	V

(1) GPIO[7:0] Register 0xBE = 0xFF

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
I_{OS}	Output Short Circuit Current	VOUT = 0 V		GPIO[7:0]		–50		mA
I_{OZ}	TRI-STATE Output Current	VOUT = 0 V or VDDIO, PDB = LOW		GPIO[7:0]	–20		20	µA
I^2C SERIAL CONTROL BUS (VDDIO = 1.8 V ± 5% OR 3.3 V ± 10%)								
V_{IH}	Input High Level			I2C_SDA, I2C_SCL I2C_SDA2, I2C_SCL2	0.7 × VDDIO		VDDIO	V
V_{IL}	Input Low Level				GND		0.3 × VDDIO	V
V_{HY}	Input Hysteresis					>50		mV
V_{OL}	Output Low Level	I_{OL} = 4 mA	Standard-mode Fast-mode		0		0.4	V
		I_{OL} = 15 mA	Fast-mode Plus		0		0.4	V
I_{IN}	Input Current	VIN = 0 V or VDDIO			–10		10	µA
FPD-LINK III RECEIVER INPUT								
V_{ID}	Differential Input Voltage(2)	(Figure 2)		RIN0±, RIN1±, RIN2±, RIN3±	60			mV
V_{CM}	Common Mode Voltage					1.0		V
I_{IZ}	Power-down input current	PDB = LOW			–10		–10	µA
R_T	Internal Termination Resistance	Single-ended RIN+ or RIN-			40	50	60	Ω
		Differential across RIN+ and RIN-			80	100	120	Ω
FPD-LINK III BI-DIRECTIONAL CONTROL CHANNEL								
V_{OUT-BC}	Back Channel Single-Ended Output Voltage	R_L = 50 Ω Coaxial configuration Forward channel disabled		RIN0+, RIN1+ RIN2+, RIN3+	+190	+220	+260	mV
				RIN0-, RIN1- RIN2-, RIN3-	–190	–220	–260	
V_{OD-BC}	Back Channel Differential Output Voltage (RIN+) - (RIN-)	R_L = 100 Ω STP configuration Forward channel disabled		RIN0±, RIN1±, RIN2±, RIN3±	380	440	520	mV
HSTX DRIVER								
V_{CMTX}	HS transmit static common-mode voltage(2)			CSI0_D[3:0]P/N, CSI0_CLKP/N, CSI1_D[3:0]P/N, CSI1_CLKP/N	150	200	250	mV
$\lvert\Delta V_{CMTX(1,0)}\rvert$	V_{CMTX} mismatch when output is 1 or 0						5	mV_{P-P}
$\lvert V_{OD}\rvert$	HS transmit differential voltage				140	200	270	mV
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when output is 1 or 0						14	mV
V_{OHHS}	HS output high voltage						360	mV
Z_{OS}	Single-ended output impedance				40	50	62.5	Ω
ΔZ_{OS}	Mismatch in single-ended output impedance						10	%

(2) Specification is ensured by design and/or characterization and is not tested in production.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
LPTX DRIVER							
V_{OH}	High Level Output Voltage	I_{OH} = –4 mA	CSI0_D[3:0]P/N, CSI0_CLKP/N, CSI1_D[3:0]P/N, CSI1_CLKP/N	1.1	1.2	1.3	V
V_{OL}	Low Level Output Voltage	I_{OL} = 4 mA		–50		50	mV
Z_{OLP}	Output impedance(2)			110			Ω
POWER CONSUMPTION							
P_T	Total Power Consumption in Operation Mode	CSI-2 data rate = 1.6 Gbps 4 × FPD-Link III RX inputs CSI-2 TX = 2 × (4 data lanes + 1 CLK lane) <Non-Replicate> Default registers				1100	mW
SUPPLY CURRENT							
I_{DDT1}	DPHY TX Supply Current (includes load current)	CSI-2 data rate = 800 Mbps 4 × FPD-Link III RX inputs CSI-2 TX = 1 data lanes + 1 CLK lane <Non-Replicate> Default registers	VDD11		90	275	mA
			VDD18		177	240	
			VDDIO		10	50	
		CSI-2 data rate = 1.6 Gbps 4 × FPD-Link III RX inputs CSI-2 TX = 1 data lanes + 1 CLK lane <Non-Replicate> Default registers	VDD11		100	280	mA
			VDD18		177	240	
			VDDIO		10	50	
I_{DDT2}	DPHY TX Supply Current (includes load current)	CSI-2 data rate = 800 Mbps 4 × FPD-Link III RX inputs CSI-2 TX = 2 × (4 data lanes + 1 CLK lane) <Replicate Mode> Default registers	VDD11		105	285	mA
			VDD18		180	240	
			VDDIO		10	50	
		CSI-2 data rate = 1.6 Gbps 4 × FPD-Link III RX inputs CSI-2 TX = 2 × (4 data lanes + 1 CLK lane) <Replicate Mode> Default registers	VDD11		120	380	mA
			VDD18		180	240	
			VDDIO		10	50	
I_{DDZ}	Standby Current	PDB = LOW	VDD11			100	mA
			VDD18			1	
			VDDIO			3	

6.7 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
LVCMOS I/O							
t_{CLH}	LVCMOS Low-to-High Transition Time	VDDIO: 1.71 V to 1.89 V OR VDDIO: 3.0 V to 3.6 V C_L = 8 pF (lumped load) Default Registers (Figure 1)	GPIO[7:0]		2.5		ns
t_{CHL}	LVCMOS High-to-Low Transition Time		GPIO[7:0]		2.5		ns
FPD-LINK III RECEIVER INPUT							
t_{DDLT}	Deserializer Data Lock Time	With Adaptive Equalization (Figure 3)	RIN0±, RIN1±, RIN2±, RIN3±		15	22	ms
IJT	Input Jitter Tolerance(1)	Jitter Frequency > FPD3_PCLK(2) / 15 See Input Jitter Tolerance				0.4	UI

(1) Specification is ensured by design and/or characterization and is not tested in production.
(2) FPD3_PCLK is equivalent to PCLK frequency based on the operating MODE:
10-bit mode: PCLK_Freq. /2
12-bit HF mode: PCLK_Freq. x 2/3
12-bit LF mode: PCLK_Freq.

6.8 Recommended Timing for the Serial Control Bus

Over I^2C supply and temperature ranges unless otherwise specified.

PARAMETER		STANDARD-MODE		FAST-MODE		FAST-MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I^2C SERIAL CONTROL BUS (Figure 4)								
f_{SCL}	SCL Clock Frequency	>0	100	>0	400	>0	1000	kHz
t_{LOW}	SCL Low Period	4.7		1.3		0.5		µs
t_{HIGH}	SCL High Period	4.0		0.6		0.26		µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	4.0		0.6		0.26		µs
$t_{SU;STA}$	Set Up time for a start or a repeated start condition	4.7		0.6		0.26		µs
$t_{HD;DAT}$	Data Hold Time	0		0		0		µs
$t_{SU;DAT}$	Data Set Up Time	250		100		50		ns
$t_{SU;STO}$	Set Up Time for STOP Condition	4.0		0.6		0.26		µs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		µs
t_r	SCL & SDA Rise Time		1000		300		120	ns
t_f	SCL & SDA Fall Time		300		300		120	ns
C_b	Capacitive Load for Each Bus Line		400		400		550	pF
t_{SP}	Input Filter		-		50		50	ns

6.9 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
HSTX DRIVER							
$HSTX_{DBR}$	Data rate(1)		CSI0_D[3:0]P/N CSI1_D[3:0]P/N	400	800	1600	Mbps
fCLK	DDR Clock frequency(1)		CSI0_CLKP/N CSI1_CLKP/N	200	400	800	MHz
$\Delta V_{CMTX(HF)}$	Common mode voltage variations HF(1)	Above 450MHz	CSI0_D0P/N CSI0_D1P/N CSI0_D2P/N CSI0_D3P/N CSI0_CLKP/N CSI1_D0P/N CSI1_D1P/N CSI1_D2P/N CSI1_D3P/N CSI1_CLKP/N			15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common mode voltage variations LF(1)	Between 50 and 450MHz				25	mV_{RMS}
t_{RHS} t_{FHS}	20% to 80% Rise and Fall HS(1)	HS data rates ≤ 1 Gbps (UI ≥ 1 ns)				0.3	UI
		HS data rates > 1 Gbps (UI ≤ 1 ns) but less than 1.5 Gbps (UI ≥ 0.667 ns)				0.35	UI
		Applicable when supporting maximum HS data rates ≤ 1.5 Gbps.		100			ps
		Applicable for all HS data rates when supporting > 1.5 Gbps.				0.4	UI
		Applicable for all HS data rates when supporting > 1.5 Gbps.		50			ps
SDD_{TX}	TX differential return loss(1)	f_{LPMAX}	HS data rates <1.5 Gbps			-18	dB
		f_H				-9	dB
		f_{MAX}				-3	dB
		f_{LPMAX}	HS data rates >1.5 Gbps			-18	dB
		f_H				-4.5	dB
		f_{MAX}				-2.5	dB

(1) Specification is ensured by design and/or characterization and is not tested in production.

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
LPTX DRIVER							
t_{RLP}	Rise Time LP (1)(2)	15% to 85% rise time	CSI0_D0P/N CSI0_D1P/N CSI0_D2P/N CSI0_D3P/N CSI1_D0P/N CSI1_D1P/N CSI1_D2P/N CSI1_D3P/N CSI0_CLKP/N CSI1_CLKP/N			25	ns
t_{FLP}	Fall Time LP (1)(2)	15% to 85% fall time				25	ns
t_{REOT}	Rise Time Post-EoT (1) (2)	30%-85% rise time				35	ns
$t_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock (1) (2)	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state		40			ns
		All other pulses		20			ns
$t_{LP-PER-TX}$	Period of the LP exclusive-OR clock (1)			90			ns
DV/DtSR	Slew rate (1)(2)	C_{LOAD} = 0 pF				500	mV/ns
		C_{LOAD} = 5 pF				300	mV/ns
		C_{LOAD} = 20 pF				250	mV/ns
		C_{LOAD} = 70 pF				150	mV/ns
		C_{LOAD} = 0 to 70 pF (Falling Edge Only)		30			mV/ns
		C_{LOAD} = 0 to 70 pF (Rising Edge Only)		30			mV/ns
		C_{LOAD} = 0 to 70 pF (Rising Edge Only) (3)(4)		30 - 0.075×(VO,INST - 700)			mV/ns
		C_{LOAD} = 0 to 70 pF (Rising Edge Only) (5)(6)		25 - 0.0625×(VO,INST - 500)			mV/ns
C_{LOAD}	Load capacitance (1)(2)			0		70	pF
CSI-2 TIMING SPECIFICATIONS — DATA-CLOCK TIMING (Figure 6, Figure 7)							
UI_{INST}	UI instantaneous (1)	In 1, 2, 3, or 4 Lane Configuration HS Data rate = 400 Mbps	CSI0_D0P/N CSI0_D1P/N CSI0_D2P/N CSI0_D3P/N CSI1_D0P/N CSI1_D1P/N CSI1_D2P/N CSI1_D3P/N CSI0_CLKP/N CSI1_CLKP/N		2.5		ns
		In 1, 2, 3, or 4 Lane Configuration HS Data rate = 800 Mbps			1.25		ns
		In 1, 2, 3, or 4 Lane Configuration HS Data rate = 1.6 Gbps			0.625		ns
ΔUI	UI variation (1)	UI ≥ 1 ns (Figure 5)		-10%		10%	UI
		UI < 1 ns (Figure 5)		-5%		5%	UI
$t_{SKEW(TX)}$	Data to Clock Skew (measured at transmitter) (1) Skew between clock and data from ideal center	HS Data rate ≤ 1 Gbps (Figure 5)		-0.15		0.15	UI_{INST}
		1 Gbps ≤ HS Data rate ≤ 1.5 Gbps (Figure 5)		-0.2		0.2	UI_{INST}
$t_{SKEW(TX)}$ static	Static Data to Clock Skew (1)	HS Data rate > 1.5 Gbps		-0.2		0.2	UI_{INST}
$t_{SKEW(TX)}$ dynamic	Dynamic Data to Clock Skew (1)	HS Data rate > 1.5 Gbps		-0.15		0.15	UI_{INST}

(2) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2ns delay.
(3) When the output voltage is between 700 mV and 930 mV
(4) Applicable when the supported data rate ≤ 1.5 Gbps
(5) When the output voltage is between 550 mV and 790 mV
(6) Applicable when the supported data rate > 1.5 Gbps.

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
CSI-2 TIMING SPECIFICATIONS - GLOBAL OPERATION (Figure 6, Figure 7)							
$t_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX(1)		CSI0_D0P/N CSI0_D1P/N CSI0_D2P/N CSI0_D3P/N CSI1_D0P/N CSI1_D1P/N CSI1_D2P/N CSI1_D3P/N CSI0_CLKP/N CSI1_CLKP/N	60			ns
$t_{CLK-POST}$	HS exit(1)			60 + 52×UI_{INST}			ns
$t_{CLK-PRE}$	Time HS clock shall be driver prior to any associated Data Lane beginning the transition from LP to HS mode(1)			8			UI_{INST}
$t_{CLK-PREPARE}$	Clock Lane HS Entry(1)			38		95	ns
$t_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions(1)			95		300	ns
$t_{CLK-TERM-EN}$	Time-out at Clock Lane Display Module to enable HS Termination(1)			Time for Dn to reach VTERM-EN		38	ns
$t_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst(1)			60			ns
$t_{CLK-PREPARE}$ + $t_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock(1)			300			ns
$t_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination(1)			Time for Dn to reach V-TERM-EN		35 + 4×UI_{INST}	ns
t_{EOT}	Transmitted time interval from the start of $t_{HS-TRAIL}$ to the start of the LP-11 state following a HS burst(1)					105 + 12×UI_{INST}	ns
$t_{HS-EXIT}$	Time that the transmitter drives LP=11 following a HS burst(1)			100			ns
$t_{HS-PREPARE}$	Data Lane HS Entry(1)			40 + 4×UI_{INST}		85 + 6×UI_{INST}	ns
$t_{HS-PREPARE}$ + $t_{HS-ZERO}$	$t_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence(1)			145 + 10×UI_{INST}			ns
$t_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $t_{HS-SETTLE}$ (1)			85 + 6×UI_{INST}		145 + 10×UI_{INST}	ns

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.(1)			40		55 + 4×UI_{INST}	ns
$t_{HS-TRAIL}$	Data Lane HS Exit(1)			60 + 4×UI_{INST}			ns
t_{LPX}	Transmitted length of LP state(1)			50			ns
t_{WAKEUP}	Recovery Time from Ultra Low Power State (ULPS)(1)			1			ms

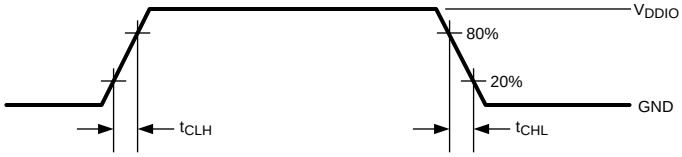


Figure 1. LVCMOS Transition Times

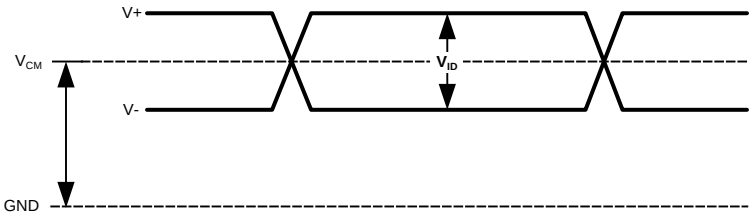


Figure 2. FPD-Link III Receiver VID

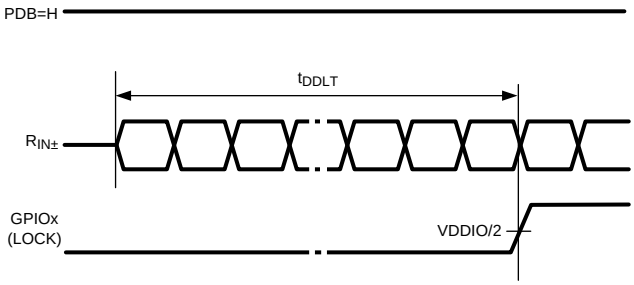


Figure 3. Deserializer Data Lock Time

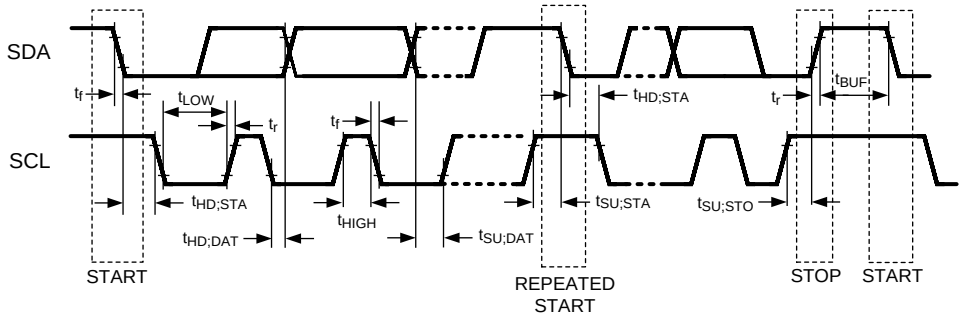


Figure 4. I2C Serial Control Bus Timing

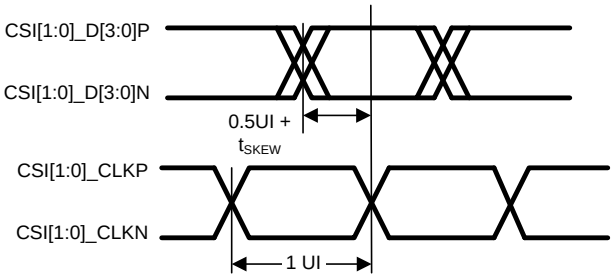


Figure 5. Clock and Data Timing in HS Transmission

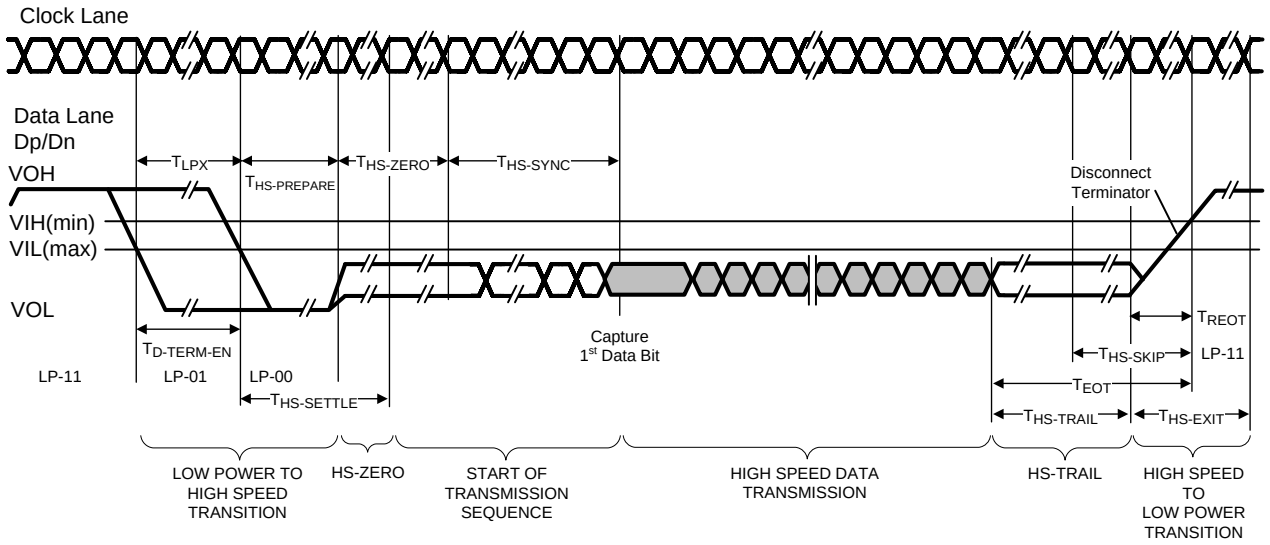


Figure 6. High Speed Data Transmission Burst

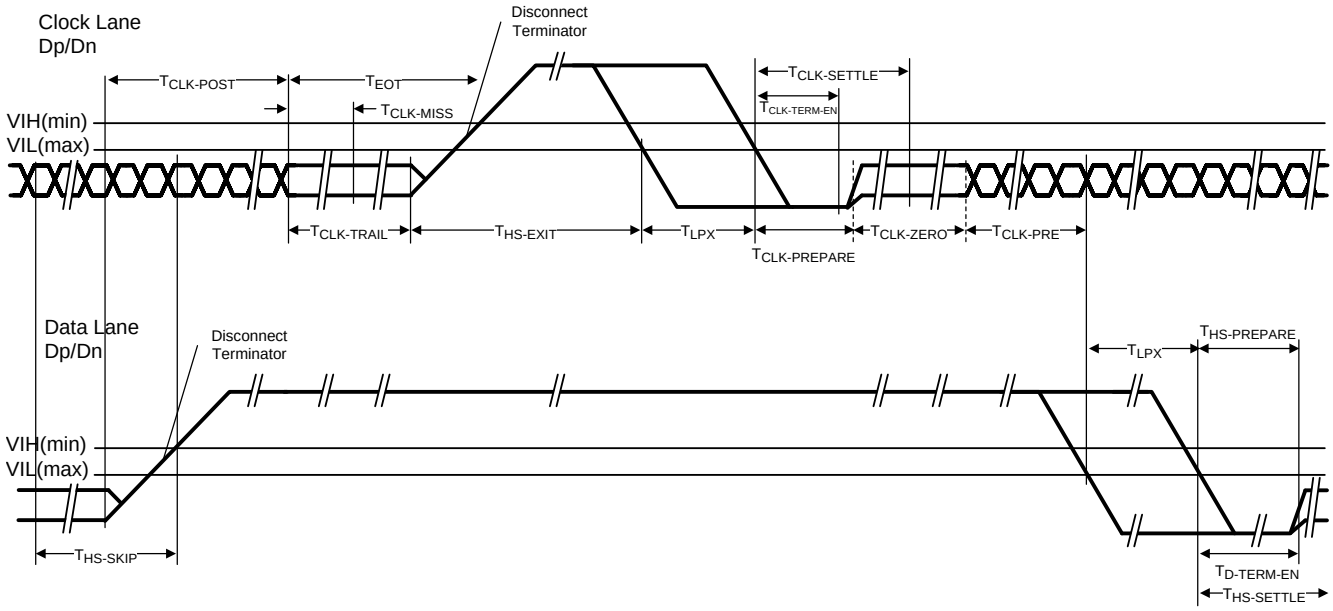


Figure 7. Switching the Clock Lane between Clock Transmission and Low-Power Mode

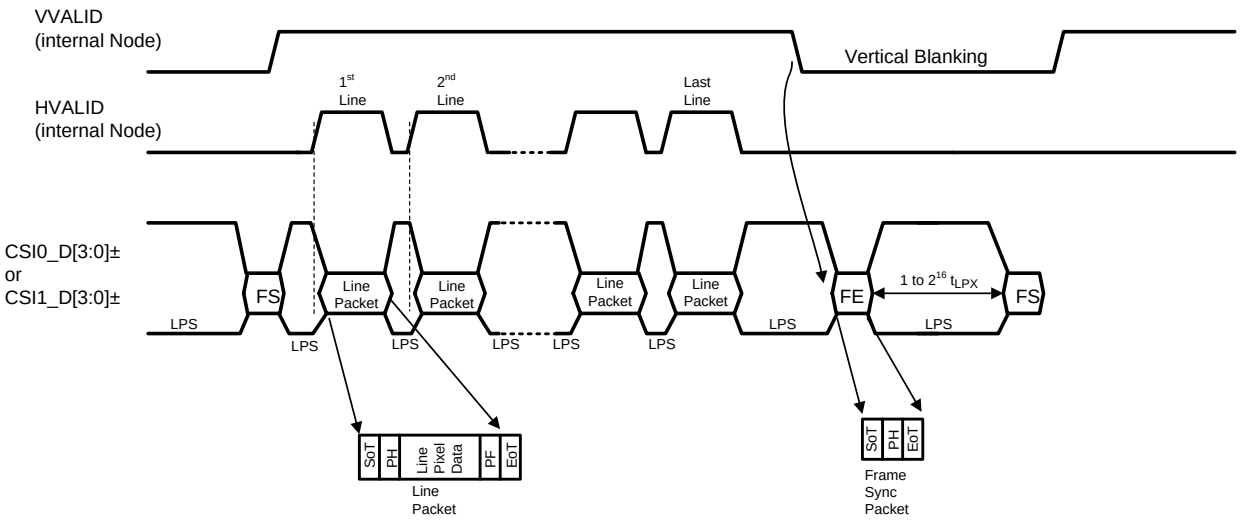


Figure 8. Long Line Packets and Short Frame Sync Packets

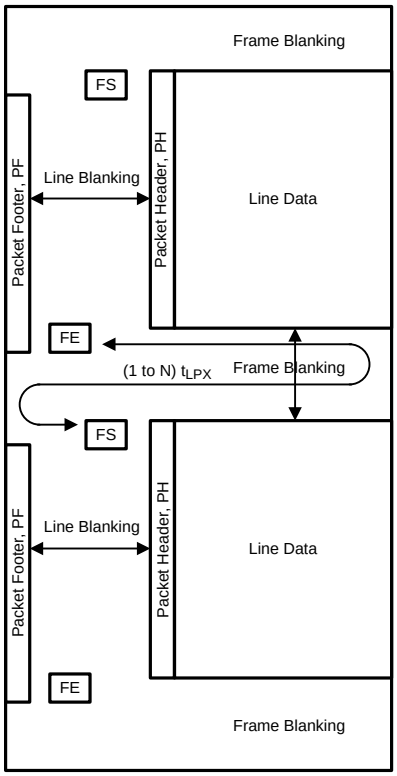
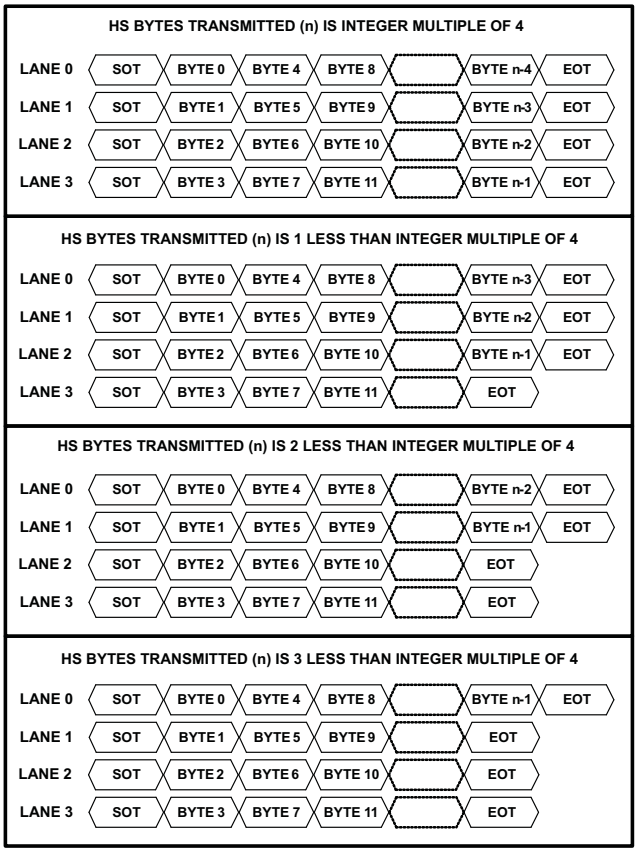
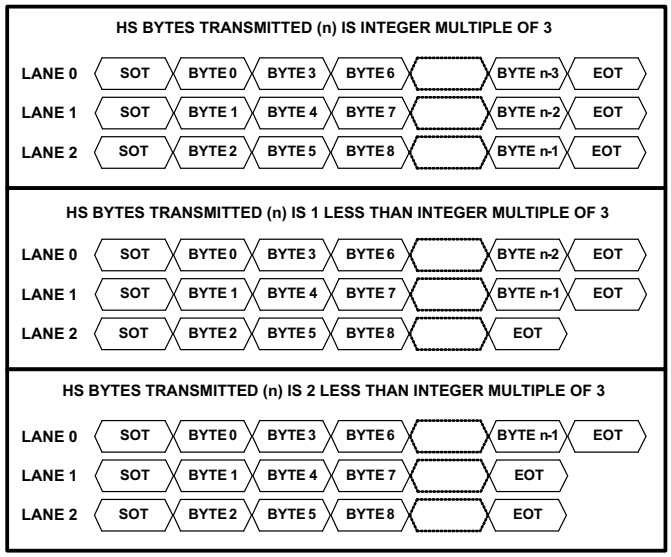


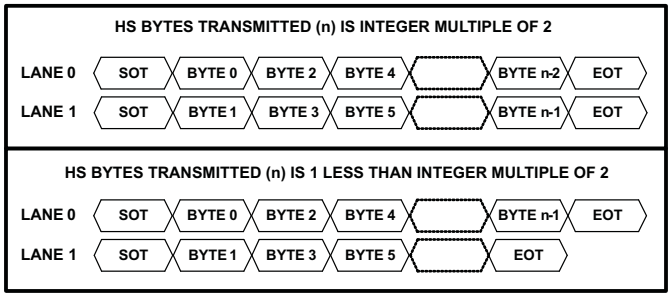
Figure 9. CSI-2 General Frame Format



4 CSI-2 Data Lane Configuration (default)



3 CSI-2 Data Lane Configuration



2 CSI-2 Data Lane Configuration

Figure 10. 4 MIPI Data Lane Configuration

7 Typical Characteristics

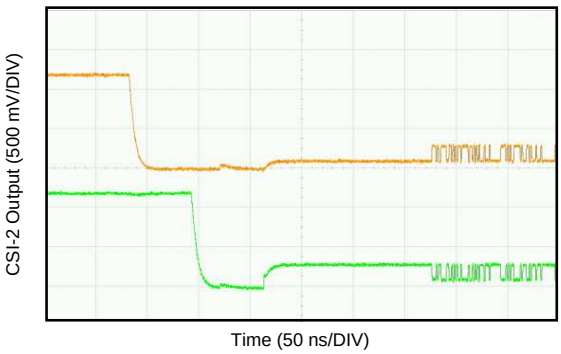


Figure 11. CSI-2 Start of Transmission (SoT)

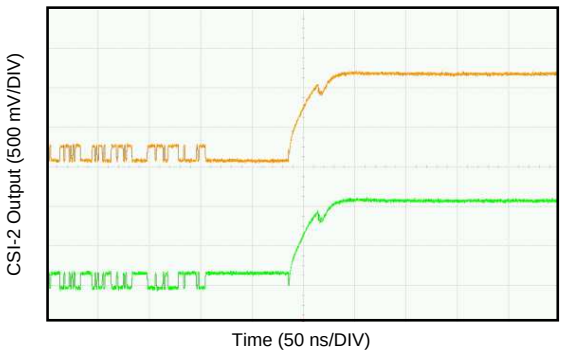


Figure 12. CSI-2 End of Transmission (EoT)

8 Detailed Description

8.1 Overview

The DS90UB964-Q1 is a camera hub that accepts four camera inputs from a FPD-Link III interface. The device combines data streams from multiple camera sources onto one or two MIPI CSI-2 port(s) with up to 4 data lanes each port.

8.2 Functional Block Diagram

The DS90UB964-Q1 is a camera hub that aggregates up to four inputs acquired from a FPD-Link III stream and transmitted over a MIPI camera serial interface (CSI-2). When coupled with DS90UB913AQ/913Q/933Q FPD-Link III serializers, the DS90UB964-Q1 receives data streams from multiple imagers to be multiplexed on the same CSI-2 links.

The DS90UB964-Q1 provides two MIPI CSI-2 ports, configuration with 4 lanes per port up to 1.6 Gbps per lane. The second MIPI CSI-2 output port is available to provide additional bandwidth, or offers a second replicated output. The DS90UB964-Q1 can support multiple data formats (programmable as RAW, YUV, RGB) and different camera resolutions. The CSI-2 Tx module accommodates both image data and non-image data (including synchronization or embedded data packets).

The DS90UB964-Q1 CSI-2 interface combines each of the camera data streams into packets designated for each virtual channel. The output generated is composed of virtual channels to separate different streams to be interleaved. Each virtual channel is identified by a unique channel identification number in the packet header.

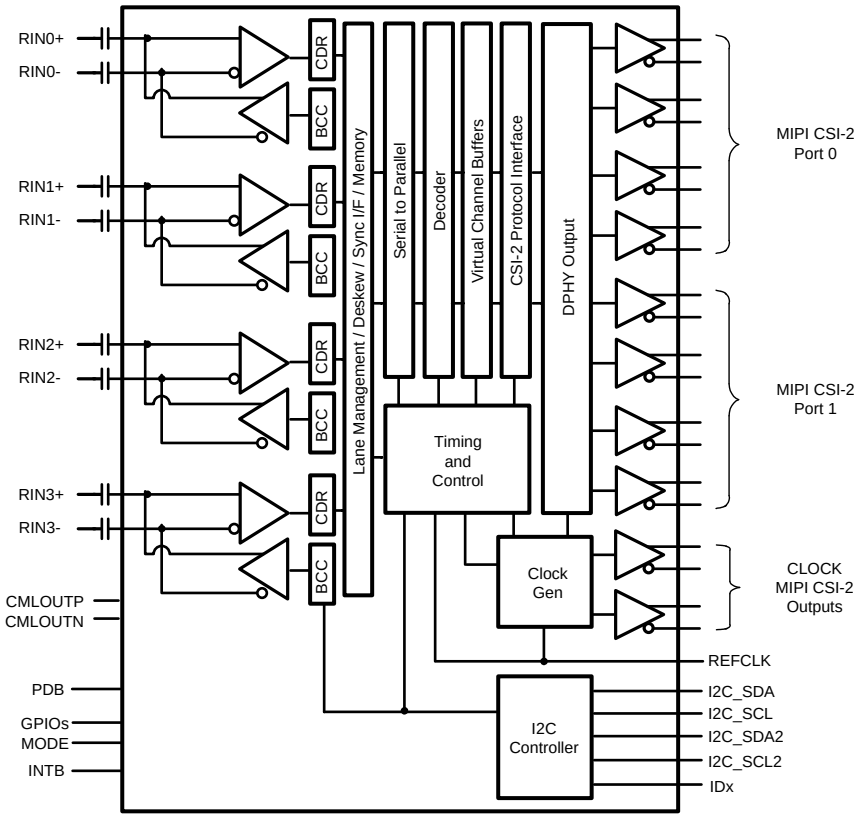


Figure 13. Functional Block Diagram

8.3 Feature Description

The DS90UB964-Q1 provides a 4:2 hub for camera applications. The device includes 4 FPD-Link III inputs for camera data streams from up to 4 serializers. The interfaces are compatible to DS90UB913AQ/913Q/933Q serializers. Data received from the 4 input ports is aggregated onto one or two 4-lane CSI-2 interfaces.

8.4 Device Functional Modes

DS90UB964-Q1 operating modes:

- RAW10 (DS90UB913AQ/913Q/933Q compatible)
- RAW12 LF (DS90UB913AQ/913Q/933Q compatible)
- RAW12 HF (DS90UB913AQ/913Q/933Q compatible)

The modes control the FPD-Link III receiver operation of the device. In each of the cases, the output format for the device is CSI-2 via one or two CSI-2 transmit ports.

Each port can be individually configured for RAW modes of operation.

The DS90UB964-Q1 includes forwarding control to allow multiple video streams from any of the received ports to be mapped to either of the CSI-2 ports.

The input mode of operation is controlled by the FPD3_MODE (Register 0x6D[1:0]) setting in the Port Configuration register. The input mode may also be controlled by the MODE strap pin.

8.4.1 RAW Mode

In Raw mode, the DS90UB964-Q1 receives RAW10 or RAW12 data from a DS90UB913AQ/913Q/933Q serializer. The data is translated into a RAW10 or RAW12 CSI-2 video stream for forwarding on one of the CSI-2 transmit ports. For each input port, the CSI-2 packet header VC-ID and Data Type are programmable.

8.4.2 MODE Pin

Configuration of the device may be done via the MODE input strap pin, or via the configuration register bits. A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE input (V_{R2}) and V_{DD18} to select one of the 6 possible selected modes. Possible configurations are:

- FPD-Link III Coaxial or STP
- 12-bit LF / 12-bit HF / 10-bit DVP modes (DS90UB913AQ/913Q/933Q compatible)

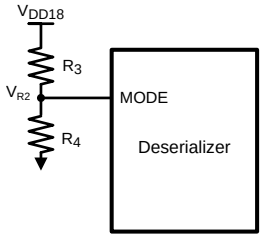


Figure 14. MODE Pin Connection Diagram

Table 2. Configuration Select (MODE)

NO.	TARGET VOLTAGE			SUGGESTED R3 kΩ (1% tol)	SUGGESTED R4 kΩ (1% tol)	COAX	RX MODE
	V_{R2} min (V)	V_{R2} typ (V)	V_{R2} max (V)				
0	0	0	0.237	OPEN	40.2	0	RESERVED
1	0.293	0.367	0.440	118	30.9	0	RAW12 LF (DS90UB913A/913/933 compatible)
2	0.507	0.579	0.650	107	51.1	0	RAW12 HF (DS90UB913A/913/933 compatible)
3	0.716	0.783	0.849	113	88.7	0	RAW10 (DS90UB913A/913/933 compatible)
4	0.924	0.992	1.059	82.5	102	1	RESERVED
5	1.139	1.205	1.271	68.1	137	1	RAW12 LF (DS90UB913A/933 compatible)
6	1.350	1.416	1.481	56.2	210	1	RAW12 HF (DS90UB913A/933 compatible)
7	1.561	VDD18	VDD18	13.3	OPEN	1	RAW10 (DS90UB913A/933 compatible)

The strapped values can be viewed and/or modified in the following locations:

- Coaxial – Port Configuration COAX_MODE (Register 0x6D[2])
- RX Mode – Port Configuration FPD3_MODE (Register 0x6D[1:0])

8.4.3 REFCLK

A valid 25 MHz (default) reference clock is required on the REFCLK pin 5 for proper operation. REFCLK input must be continuous. The REFCLK frequency defines all internal clock timers including the back channel rate, I2C timers, CSI-2 datarate, FrameSync signal parameters, etc. Min stop time (stop at high or stop at low) is 20 uS, otherwise it is required to reset using PDB. During normal operation if REFCLK input is removed and then re-applied this may cause CSI-2 output to be disrupted.

The REFCLK LVCMOS input oscillator specifications are listed in Table 3.

Table 3. REFCLK Oscillator Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE CLOCK					
Frequency tolerance				±100	ppm
Duty cycle		40%	50%	60%	
Rise/Fall Time	10% - 90%			8	ns
Jitter	500 kHz - 50 MHz		50	80	ps p-p
Frequency		23		25	MHz

8.4.4 Input Jitter Tolerance

Input jitter tolerance is the ability of the receiver's CDR PLL to track and recover the incoming serial data stream. Jitter tolerance at a specific frequency is the maximum jitter permissible before data errors occur. The following shows the allowable total jitter of the receiver inputs and must be less than the values in the chart.

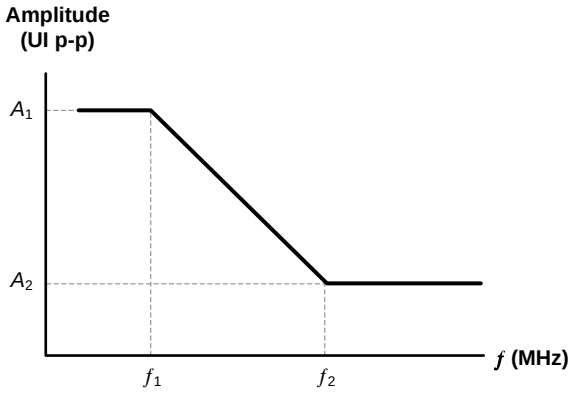


Figure 15. Input Jitter Tolerance Plot

Table 4. Input Jitter Tolerance Limit

INTERFACE	JITTER AMPLITUDE (UI p-p)		FREQUENCY (MHz) (1)	
FPD3	A1	A2	ƒ1	ƒ2
	1	0.4	FPD3_PCLK / 80	FPD3_PCLK / 15

(1) FPD3_PCLK is equivalent to PCLK frequency based on the operating MODE:
10-bit mode: PCLK_Freq. /2
12-bit HF mode: PCLK_Freq. x 2/3
12-bit LF mode: PCLK_Freq.

8.4.5 Adaptive Equalizer

The receiver inputs provide an adaptive equalization filter in order to compensate for signal degradation from the interconnect components. In order to determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, ISI, crosstalk, etc. need to be taken into consideration. The equalization status and configuration are selected via AEQ registers 0xD2–0xD5.

Each RX receiver incorporates an adaptive equalizer (AEQ), which continuously monitors cable characteristics for long-term cable aging and temperature changes. The AEQ attempts to optimize the equalization setting of the RX receiver.

If the deserializer loses LOCK, the adaptive equalizer will reset and perform the LOCK algorithm again to reacquire the serial data stream being sent by the serializer.

8.4.6 Channel Monitor Loop-Through Output Driver

The DS90UB964-Q1 includes an internal **C**hannel **M**onitor **L**oop-through output on the CMLOUTP/N pins. A buffered loop-through output driver is provided on the CMLOUTP/N for observing jitter after equalization for each of the four RX receive channels. The CMLOUT monitors the post EQ stage thus providing the recovered input of the deserializer signal. The measured serial data width on the CMLOUT loop-through is the total jitter including the internal driver, AEQ, back channel echo, etc. Each channel also has its own CMLOUT monitor and can be used for debug purposes. This CMLOUT is useful in identifying gross signal conditioning issues.

Table 6 includes details on selecting the corresponding RX receiver of CMLOUTP/N configuration.

Table 5. CML Monitor Output Driver

PARAMETER		TEST CONDITIONS	PIN	MIN	TYP	MAX	UNIT
E_W	Differential Output Eye Opening	R_L = 100 Ω (Figure 16)	CMLOUTP, CMLOUTN	0.45			UI(1)

(1) UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with serializer input PCLK frequency.
10-bit mode: 1 UI = 1 / (PCLK_Freq. /2 x 28)
12-bit HF mode: 1 UI = 1 / (PCLK_Freq. x 2/3 x 28)
12-bit LF mode: 1 UI = 1 / (PCLK_Freq. x 28)

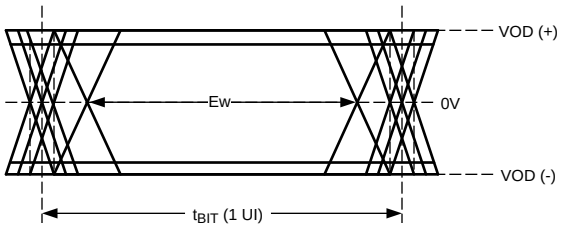


Figure 16. CMLOUT Output Driver

Table 6. Channel Monitor Loop-Through Output Configuration

	FPD3 RX Port 0	FPD3 RX Port 1	FPD3 RX Port 2	FPD3 RX Port 3
ENABLE MAIN LOOPTHRU DRIVER	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80
SELECT CHANNEL MUX	0xB1 = 0x01 0xB2 = 0x01	0xB1 = 0x01 0xB2 = 0x02	0xB1 = 0x01 0xB2 = 0x04	0xB1 = 0x01 0xB2 = 0x08
SELECT RX PORT	0xB0 = 0x04 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02	0xB0 = 0x08 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02	0xB0 = 0x0C 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02	0xB0 = 0x10 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02

8.4.6.1 Code Example for CMLOUT FPD3 RX Port 0:

```
WriteI2C(0xB0,0x14)   # FPD3 RX Shared, page 0
WriteI2C(0xB1,0x00)   # Offset 0 (reg_0_sh)
WriteI2C(0xB2,0x80)   # Enable loop throu driver
WriteI2C(0xB1,0x01)   # Select Drive Mux
WriteI2C(0xB2,0x01)   #
WriteI2C(0xB0,0x04)   # FPD3 RX Port 0, page 0
WriteI2C(0xB1,0x0F)   #
WriteI2C(0xB2,0x01)   # Loop through select
WriteI2C(0xB1,0x10)   #
WriteI2C(0xB2,0x02)   # Enable CML data output
```

8.4.7 GPIO Support

The DS90UB964-Q1 supports 8 pins which are programmable for use in multiple options through the GPIOx_PIN_CTL registers.

8.4.7.1 Back Channel GPIO

The DS90UB964-Q1 can input data on the GPIO pins to send on the back channel to remote serializers. Each GPIO pin can be programmed for input mode. In addition, the back channel for each FPD3 port can be programmed to send any of the 8 GPIO pin data. The same GPIO pin can be connected to multiple back channel GPIO signals.

In addition to sending GPIO from pins, an internally generated FrameSync signal may be sent on any of the back-channel GPIOs.

For each port, the following GPIO control is available through the BC_GPIO_CTL0 register 0x6E and BC_GPIO_CTL1 register 0x6F.

8.4.7.2 GPIO Pin Status

GPIO pin status may be read through the GPIO_PIN_STS register 0x0E. This register provides the status of the GPIO pin independent of whether the GPIO pin is configured as an input or output.

8.4.7.3 Other GPIO Pin Controls

Each GPIO pin can has a input disable and a pulldown disable. By default, the GPIO pin input paths are enabled and the internal pulldown circuit in the GPIO is enabled. The GPIO_INPUT_CTL register 0x0F and GPIO_PD_CTL register 0xBE allow control of the input enable and the pulldown respectively. For most applications, there is no need to modify the default register settings.

8.4.8 RAW Mode LV/FV Controls

The Raw modes provide FrameValid (FV) and LineValid (LV) controls for the video framing. The FV is equivalent to a Vertical Sync (VSYNC) while the LineValid is equivalent to a Horizontal Sync (HSYNC) input to the DS90UB913AQ/913Q/933Q device.

The DS90UB964-Q1 allows setting the polarity of these signals by register programming. The FV and LV polarity are controlled on a per-port basis and can be independently set in the PORT_CONFIG2 register 0x7C.

To prevent false detection of FrameValid, FV must be asserted for a minimum number of clocks prior to first video line to be considered valid. The minimum FrameValid time is programmable in the FV_MIN_TIME register 0xBC. Since the measurement is in FPD3 clocks, the minimum FrameValid setup to LineValid timing at the Serializer will vary based on operating mode.

A minimum FV to LV timing is required when processing video frames at the serializer input. If the FV to LV minimum setup is not met (by default), the first video line is discarded. Optionally, a register control (PORT_CONFIG:DISCARD_1ST_ON_ERR) forwards the first video line missing some number of pixels at the start of the line.

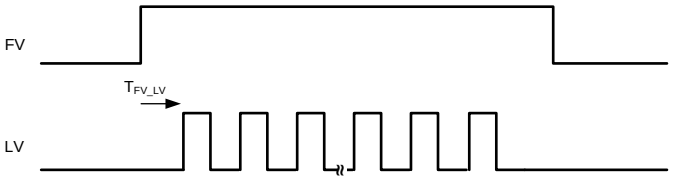


Figure 17. Minimum FV to LV

Table 7. Minimum FV to LV Setup Requirement (in Serializer PCLKs)

MODE	FV_MIN_TIME Conversion Factor	Absolute Min (FV_MIN_TIME = 0)	Default (FV_MIN_TIME = 128)
RAW12 LF	1	2	130
RAW12 HF	1.5	3	195
RAW10	2	5	261

For other settings of FV_MIN_TIME, the required FV to LV setup in Serializer PCLKs can be determined by:

Absolute Min + (FV_MIN_TIME * Conversion factor)

8.4.9 CSI-2 Protocol Layer

The DS90UB964-Q1 implements High-Speed mode to forward CSI-2 Low Level Protocol data. This includes features as described in the Low Level Protocol section of the MIPI CSI-2 Specification. It supports short and long packet formats.

The feature set of the protocol layer implemented by the CSI-2 TX is:

- Transport of arbitrary data (payload-independent)
- 8-bit word size
- Support for up to four interleaved virtual channels on the same link
- Special packets for frame start, frame end, line start and line end information
- Descriptor for the type, pixel depth and format of the Application Specific Payload data
- 16-bit Checksum Code for error detection

Figure 18 shows the CSI-2 protocol layer with short and long packets.

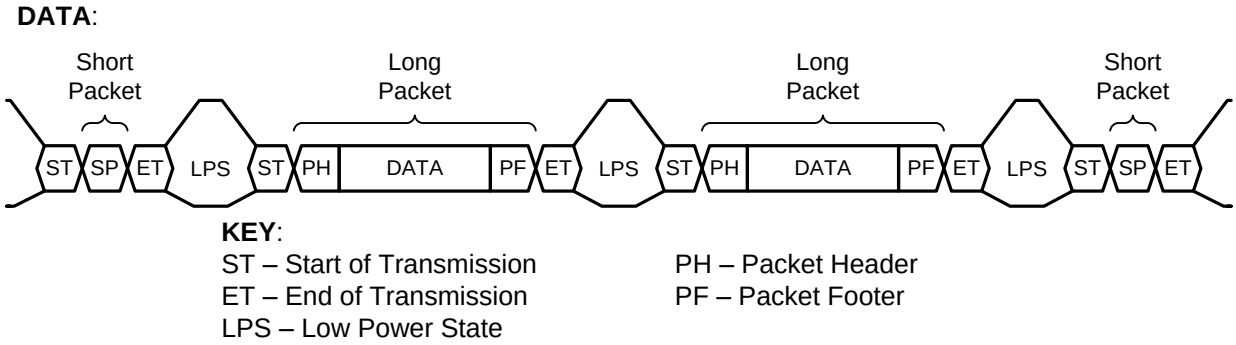


Figure 18. CSI-2 Protocol Layer With Short and Long Packets

8.4.10 CSI-2 Short Packet

The short packet provides frame or line synchronization. Figure 19 shows the structure of a short packet. A short packet is identified by data types 0x00 to 0x0F.

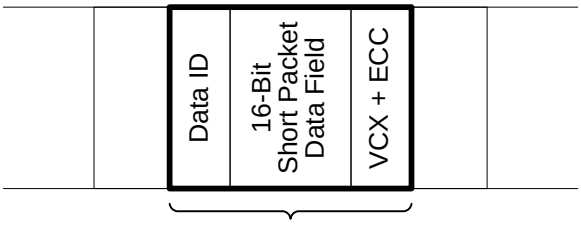


Figure 19. CSI-2 Short Packet Structure

8.4.11 CSI-2 Long Packet

A long packet consists of three elements: a 32-bit packet header (PH), an application-specific data payload with a variable number of 8-bit data words, and a 16-bit packet footer (PF). The packet header is further composed of three elements: an 8-bit data identifier, a 16-bit word count field, and an 8-bit ECC. The packet footer has one element, a 16-bit checksum. Figure 20 shows the structure of a long packet.

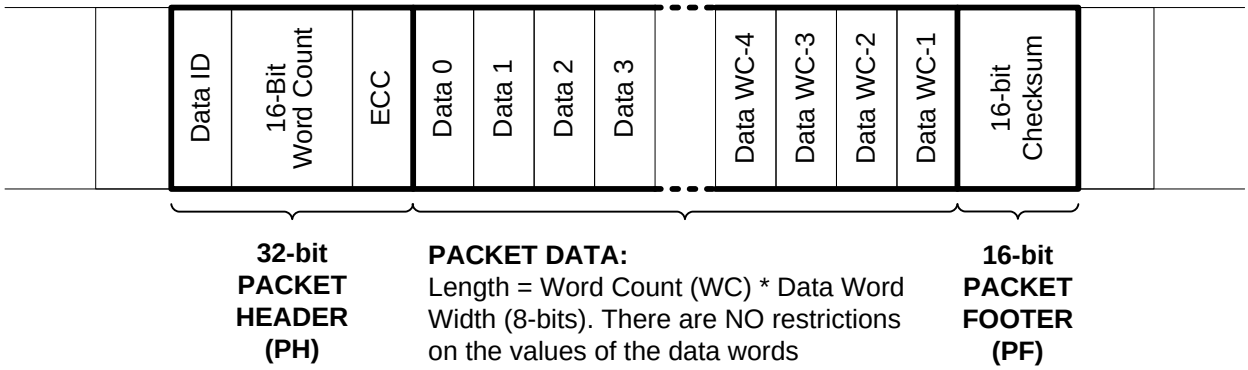


Figure 20. CSI-2 Long Packet Structure

Table 8. CSI-2 Long Packet Structure Description

PACKET PART	FIELD NAME	SIZE (BIT)	DESCRIPTION
Header	VC / Data ID	8	Contains the virtual channel identifier and the data-type information.
	Word Count	16	Number of data words in the packet data. A word is 8 bits.
	ECC	8	ECC for data ID and WC field. Allows 1-bit error recovery and 2-bit error detection.
Data	Data	WC * 8	Application-specific payload (WC words of 8 bits).
Footer	Checksum	16	16-bit cyclic redundancy check (CRC) for packet data.

8.4.12 CSI-2 Data Identifier

The DS90UB964-Q1 MIPI CSI-2 protocol interface transmits the data identifier byte containing the values for the virtual channel ID (VC) and data type (DT) for the application specific payload data, as shown in Figure 21. The virtual channel ID is contained in the 2 MSBs of the data identifier byte and identify the data as directed to one of four virtual channels. The value of the data type is contained in the 6 LSBs of the data identifier byte.

For each RX Port, register defines with which channel and data type the context is associated:

- 0x70 RAW10 Mode and 0x71 RAW12 Mode
- RAW1x_VC[7:6] field defines the associated virtual ID transported by the CSI-2 protocol from the camera sensor.
- RAW1x_ID[5:0] field defines the associated data type. The data type is a combination of the data type

transported by the CSI-2 protocol.

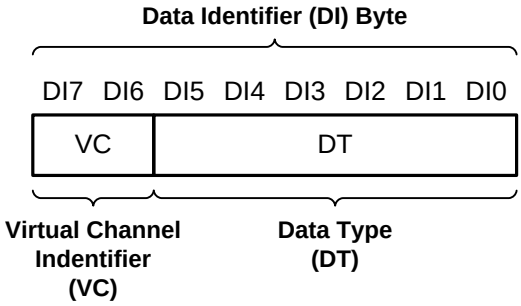


Figure 21. CSI-2 Data Identifier Structure

8.4.13 Virtual Channel and Context

The CSI-2 protocol layer transports virtual channels. The purpose of virtual channels is to separate different data flows interleaved in the same data stream. Each virtual channel is identified by a unique channel identification number in the packet header. Therefore, a CSI-2 TX context can be associated with a virtual channel and a data type. Virtual channels are defined by a 2-bit field. This channel identification number is encoded in the 2-bit code.

The CSI-2 TX transmits the channel identifier number and multiplexes the interleaved data streams. The CSI-2 TX supports up to four concurrent virtual channels.

8.4.14 CSI-2 Mode Virtual Channel Mapping

The CSI-2 Mode provides per-port Virtual Channel ID mapping. For each FPD-Link III input port, separate mapping may be done for each input VC-ID to any of the four VC-ID values. The mapping is controlled by the VC_ID_MAP register. This function sends the output as a time-multiplexed CSI-2 stream, where the video sources are differentiated by the virtual channel.

8.4.14.1 Example 1

The DS90UB964-Q1 is receiving data from cameras attached to each port. Each port is sending a video stream using VC-ID of 0. The DS90UB964-Q1 can be configured to re-map the incoming VC-IDs to ensure each video stream has a unique ID. The direct implementation would map incoming VC-ID of 0 for RX Port 0, VC-ID of 1 for RX Port 1, VC-ID of 2 for RX Port 2, and VC-ID of 3 for RX Port 3.

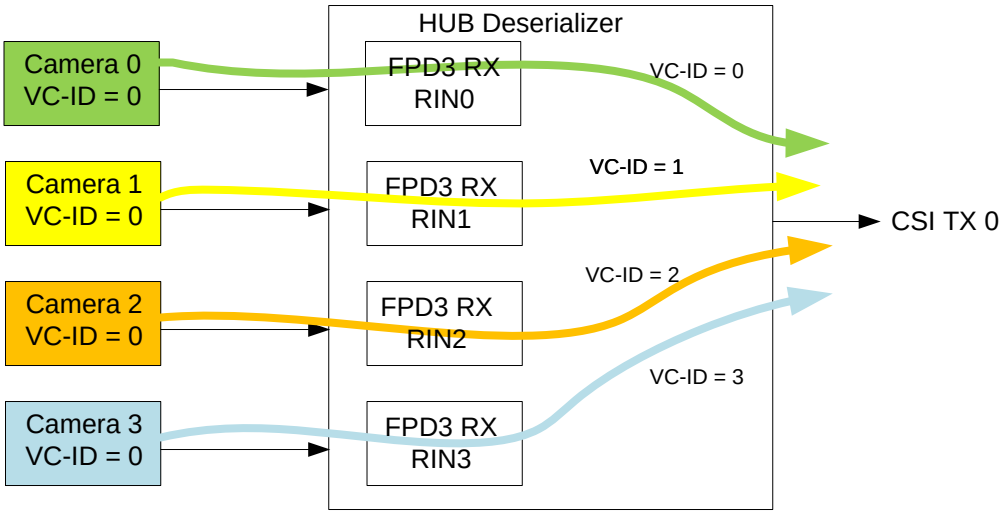


Figure 22. VC-ID Mapping Example 1

8.4.14.2 Example 2

The DS90UB964-Q1 is receiving data from cameras attached to each port. Each port is sending a video stream using VC-ID of 0. The DS90UB964-Q1 can be configured to re-map the incoming VC-IDs and distribute to different CSI Transmitters. This implementation maps incoming VC-ID of 0 for RX Port 0, VC-ID of 1 for RX Port 1, VC-ID of 0 for RX Port 2, and VC-ID of 1 for RX Port 3. RX Ports 0 and 1 are assigned to CSI Transmitter 0 which RX Ports 2 and 3 are assigned to CSI Transmitter 1.

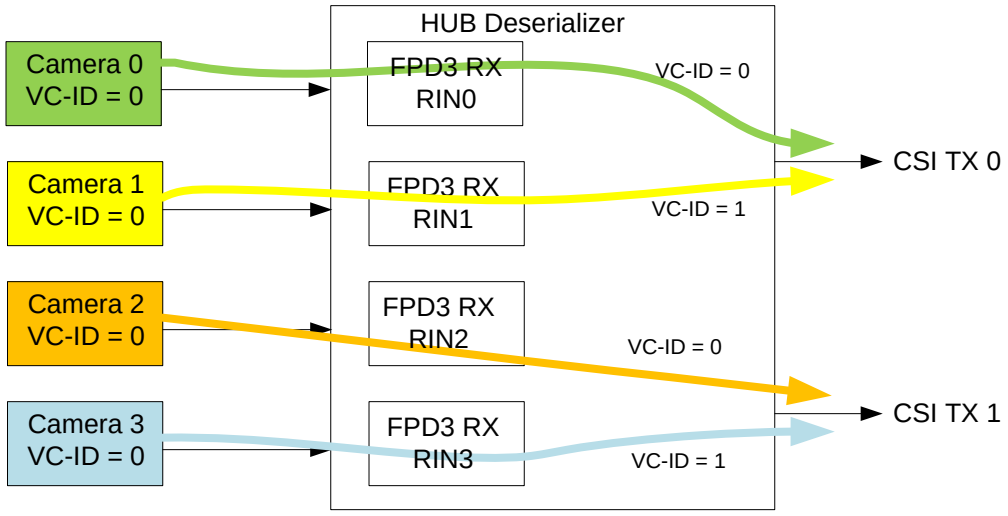


Figure 23. VC-ID Mapping Example 2

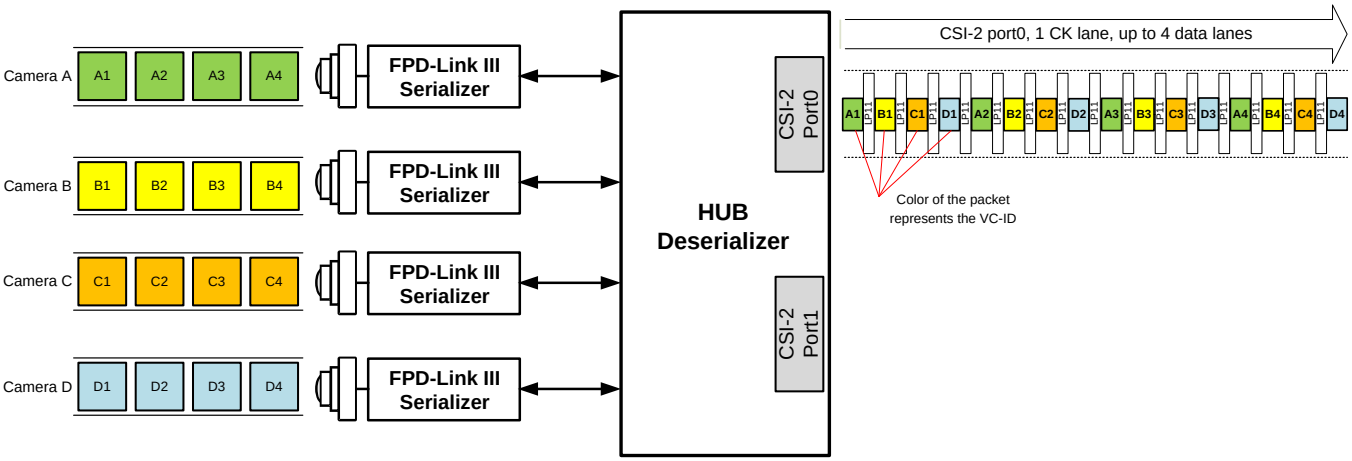


Figure 24. Four Camera Data onto CSI-2 With Virtual Channels (VC-ID)

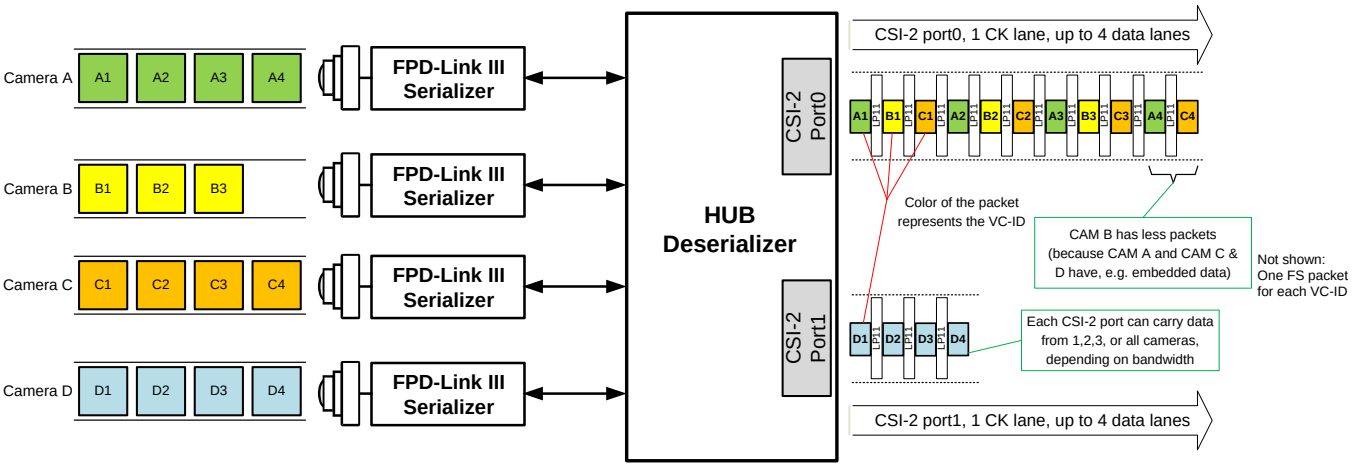


Figure 25. Four Camera Data onto CSI-2 With Virtual Channels (VC-ID) With Different Frame Size

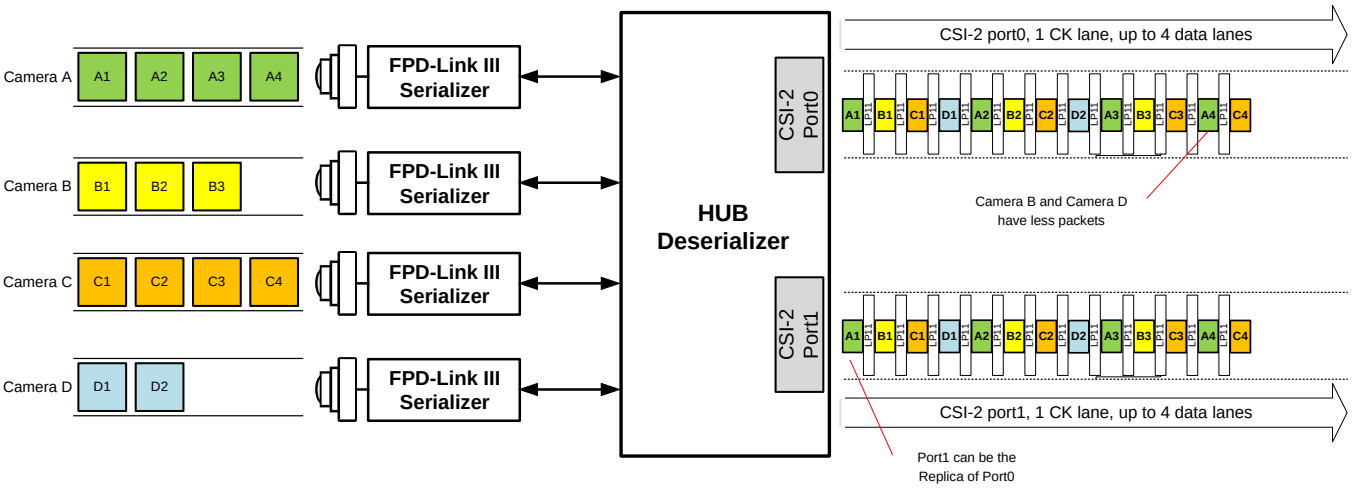


Figure 26. Four Camera Data onto 1xCSI-2 Replicated With Virtual Channels (VC-ID) With Different Frame Size

8.4.15 CSI-2 Transmitter Frequency

The CSI-2 Transmitters may operate at 400 or 800 Mbps or 1.6 Gbps. This operation is controlled via the CSI_PLL_CTL 0x1F register.

CSI_PLL_CTL[1:0]	CSI-2 TX Frequency	REFCLK Frequency
00	1.6 Gbps	25 MHz
	1.472 Gbps	23 MHz
01	Reserved	Reserved
10	800 Mbps	25 MHz
11	400 Mbps	25 MHz

When configuring to 800 Mbps or 1.6 Gbps, the CSI-2 timing parameters are automatically set based on the CSI_PLL_CTL 0x1F register. In the case of 400 Mbps, the respective CSI-2 timing parameters registers must be programmed, and the appropriate override bit needs to be set. To enable CSI-2 400 Mbps mode, set the following registers:

```
# Set CSI Timing parameters
WriteI2C(0xB0,0x2)    # set auto-increment, page 0
WriteI2C(0xB1,0x40)   # CSI Port 0
```

```
WriteI2C(0xB2,0x83)   # TCK Prep
WriteI2C(0xB2,0x8D)   # TCK Zero
WriteI2C(0xB2,0x87)   # TCK Trail
WriteI2C(0xB2,0x87)   # TCK Post
WriteI2C(0xB2,0x83)   # THS Prep
WriteI2C(0xB2,0x86)   # THS Zero
WriteI2C(0xB2,0x84)   # THS Trail
WriteI2C(0xB2,0x86)   # THS Exit
WriteI2C(0xB2,0x84)   # TLPX

# Set CSI Timing parameters
WriteI2C(0xB0,0x2)    # set auto-increment, page 0
WriteI2C(0xB1,0x60)   # CSI Port 1
WriteI2C(0xB2,0x83)   # TCK Prep
WriteI2C(0xB2,0x8D)   # TCK Zero
WriteI2C(0xB2,0x87)   # TCK Trail
WriteI2C(0xB2,0x87)   # TCK Post
WriteI2C(0xB2,0x83)   # THS Prep
WriteI2C(0xB2,0x86)   # THS Zero
WriteI2C(0xB2,0x84)   # THS Trail
WriteI2C(0xB2,0x86)   # THS Exit
WriteI2C(0xB2,0x84)   # TLPX
```

8.4.16 Video Buffers

The DS90UB964-Q1 implements four video line buffer/FIFO, one for each RX channel. The video buffers provide storage of data payload and forward requirements for sending multiple video streams on the CSI-2 transmit ports. The total line buffer memory size is a 16-kB block for each RX port.

The CSI-2 transmitter waits for an entire packet to be available before pulling data from the video buffers.

8.4.17 CSI-2 Line Count and Line Length

The DS90UB964-Q1 counts the number of lines (long packets) to determine line count on LINE_COUNT_1/0 registers 0x73–74. For line length, DS90UB964-Q1 generates the word count field in the CSI-2 header on LINE_LEN_1/0 registers 0x75–0x76.

8.4.18 FrameSync Operation

A frame synchronization signal (FrameSync) can be sent via the back-channel using any of the back channel GPIOs. The signal can be generated in two different methods. The first option offers sending the external FrameSync using one of the available GPIO pins on the DS90UB964-Q1 and mapping that GPIO to a back channel GPIO on one or more of the FPD-Link III ports.

The second option is to have the DS90UB964-Q1 internally generate a FrameSync signal to send via GPIO to one or more of the attached Serializers.

FrameSync signaling on the four back channels is synchronous. Thus, the FrameSync signal arrives at each of the four serializers with limited skew.

8.4.18.1 External FrameSync Control

In External FrameSync mode, an external signal is input to the DS90UB964-Q1 via one of the GPIO pins on the device. The external FrameSync signal may be propagated to one or more of the attached FPD3 Serializers via a GPIO signal in the back channel.

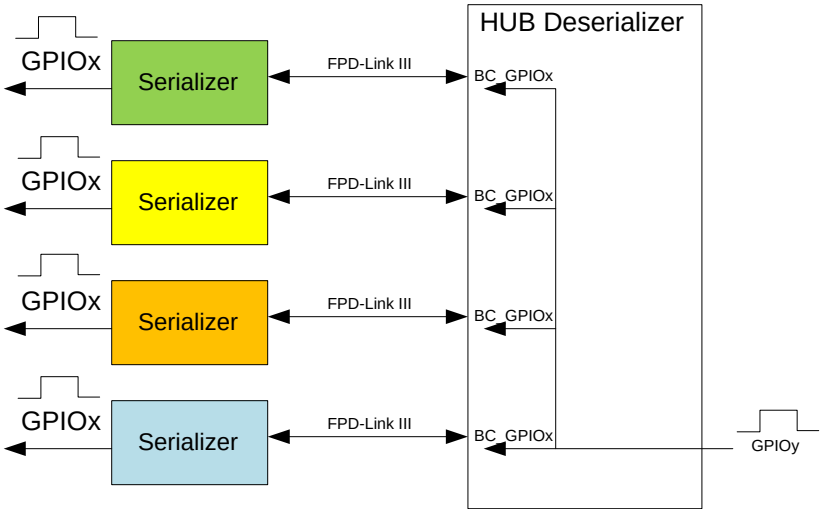


Figure 27. External FrameSync

Enabling the external FrameSync mode is done by setting the FS_MODE control in the FS_CTL register to a value between 0x8 (GPIO0 pin) to 0xF (GPIO7 pin). Set FS_GEN_ENABLE to 0 for this mode.

To send the FrameSync signal on a port's BC_GPIOx signal, the BC_GPIO_CTL0 or BC_GPIO_CTL1 register should be programmed for that port to select the FrameSync signal.

8.4.18.2 Internally Generated FrameSync

In Internal FrameSync mode, an internally generated FrameSync signal is sent to one or more of the attached FPD3 Serializers via a GPIO signal in the back channel.

FrameSync operation is controlled by the FS_CTL 0x18, FS_HIGH_TIME_x, and FS_LOW_TIME_x 0x19–0x1A registers. The resolution of the FrameSync generator clock (FS_CLK_PD) is derived from the back channel frame period (BC_FREQ_SELECT register). For each 2.5 Mbps back-channel , the frame period is 12 µs (30 bits * 400 ns/bit).

Once enabled, the FrameSync signal is sent continuously based on the programmed conditions.

Enabling the internal FrameSync mode is done by setting the FS_GEN_ENABLE control in the FS_CTL register to a value of 1. The FS_MODE field controls the clock source used for the FrameSync generation. The FS_GEN_MODE field configures whether the duty cycle of the FrameSync is 50/50 or whether the high and low periods are controlled separately. The FrameSync high and low periods are controlled by the FS_HIGH_TIME and FS_LOW_TIME registers.

The accuracy of the internally generated FrameSync is directly dependent on the accuracy of the 25 MHz oscillator used as the reference clock.

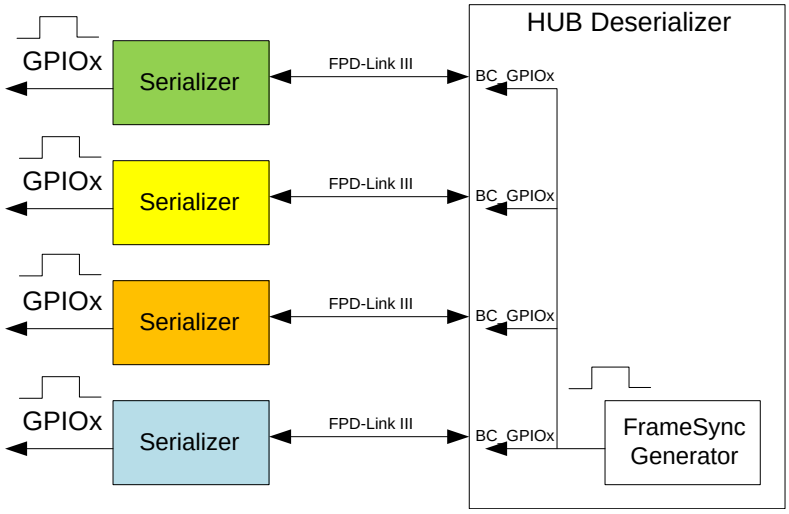
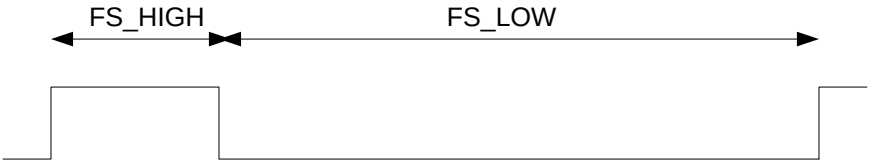


Figure 28. Internal FrameSync



FS_LOW = FS_LOW_TIME * FS_CLK_PD
FS_HIGH = FS_HIGH_TIME * FS_CLK_PD
where FS_CLK_PD is the resolution of the FrameSync generator clock

Figure 29. Internal FrameSync Signal

The following example shows generation of a FrameSync signal at 60 pulses per second. Mode settings:

- Programmable High/Low periods: FS_GEN_MODE 0x18[1]=0
- Use port 0 back channel frame period: FS_MODE 0x18[7:4]=0x0
- Back channel rate of 2.5 Mbps: BC_FREQ_SELECT for port 0 0x58[2:0]=0x0
- Initial FS state of 0: FS_INIT_STATE 0x18[2]=0

Based on mode settings, the FrameSync is generated based upon FS_CLK_PD of 12 us.

The total period of the FrameSync is (1 sec / 60 hz) / 12 µs or approximately 1,389 counts.

For a 10% duty cycle, set the high time to 139 (0x008A) cycles, and the low time to 1,250 (0x04E1) cycles:

- FS_HIGH_TIME_1: 0x19=0x00
- FS_HIGH_TIME_0: 0x1A=0x8A
- FS_LOW_TIME_1: 0x1B=0x04
- FS_LOW_TIME_0: 0x1C=0xE1

8.4.18.2.1 Code Example for Internally Generated FrameSync

```
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x10,0x91) # FrameSync signal; Device Status; Enabled
WriteI2C(0x58,0x58) # BC FREQ SELECT: 2.5 Mbps
```

```
WriteI2C(0x19,0x00) # FS_HIGH_TIME_1
WriteI2C(0x1A,0x8A) # FS_HIGH_TIME_0
WriteI2C(0x1B,0x04) # FS_LOW_TIME_1
WriteI2C(0x1C,0xE1) # FS_LOW_TIME_0
WriteI2C(0x18,0x01) # Enable FrameSync
```

8.4.19 CSI-2 Forwarding

Video stream forwarding is handled by the forwarding control in the DS90UB964-Q1 on FWD_CTL1 register 0x20. The forwarding control pulls data from the video buffers for each FPD3 RX port and forwards the data to one of the CSI-2 output interfaces. It also handles generation of transitions between LP and HS modes as well as sending of Synchronization frames. The forwarding control monitors each of the video buffers for packet and data availability.

Forwarding from input ports may be disabled using per-port controls. Each of the forwarding engines may be configured to pull data from any of the four video buffers, although a buffer may only be assigned to one CSI-2 Transmitter at a time. The two forwarding engines operate independently. Video buffers are assigned to the CSI-2 Transmitters using the mapping bits in the FWD_CTL1 register 0x20[7:4].

8.4.19.1 Best-Effort Round Robin CSI-2 Forwarding

By default, the round-robin (RR) forwarding of packets use standard CSI-2 method of video stream determination. No special ordering of CSI-2 packets are specified, effectively relying on the Virtual Channel Identifier (VC) and Data Type (DT) fields to distinguish video streams. Each image sensor is assigned a VC-ID to identify the source. Different data types within a virtual channel is also supported in this mode.

The forwarding engine forwards packets as they become available to the forwarding engine. In the case where multiple packets may be available to transmit, the forwarding engine typically operates in an RR fashion based on the input port from which the packets are received.

Best-effort CSI-2 RR forwarding has the following characteristics and capabilities:

- Uses Virtual Channel ID to differentiate each video stream
- Separate Frame Synchronization packets for each VC
- No synchronization requirements

This mode of operation allows input RX ports to have different video characteristics and there is no requirement that the video be synchronized between ports. The attached video processor would be required to properly decode the various video streams based on the VC and DT fields.

Best-effort forwarding is enabled by setting the CSIx_RR_FWD bits in the FWD_CTL2 register 0x21.

8.4.19.2 Synchronized Forwarding

In cases with multiple input sources, synchronized forwarding offers synchronization of all incoming data stored within the buffer. If packets arrive within a certain window, the forwarding control may be programmed to attempt to synchronize the video buffer data. In this mode, it attempts to send each channel synchronization packets in order (C0, C1, C2, C3) as well as sending packet data in the same order. In the following sections, Camera 0 (C0), Camera 1 (C1), Camera 2 (C2), and Camera 3 (C3) refers to the camera connected at FPD3 RX port 0, RX port 1, RX port 2, and RX port 3 respectively. The following describe only the 4-port operation, but other possible port combinations apply.

The forwarding engine for each CSI-2 Transmitter can be configured independently and synchronize up to all four video sources.

Requirements:

- Video arriving at input ports should be synchronized within approximately 1 video line period
- All enabled ports should have valid, synchronized video
- Each port must have identical video parameters, including number and size of video lines, presence of synchronization packets, etc.

The forwarding engine attempts to send the video synchronized. If synchronization fails, the CSI-2 transmitter stops forwarding packets and attempt to restart sending synchronized video at the next FrameStart indication. Packets are discarded as long as the forwarding engine is unable to send the synchronized video.

Status is provided to indicate when the forwarding engine is synchronized. In addition, a flag is used to indicate that synchronization has been lost (status is cleared on a read).

Three options are available for Synchronized forwarding:

- Basic Synchronized forwarding
- Line-Interleave forwarding
- Line-Concatenated forwarding

Synchronized forwarding modes are selected by setting the CSIx_SYNC_FWD controls in the FWD_CTL2 register. To enable synchronized forwarding the following order of operations is recommended:

1. Disable Best-effort forwarding by clearing the CSIx_RR_FWD bits in the FWD_CTL2 register
2. Enable forwarding per Receive port by clearing the FWD_PORTx_DIS bits in the FWD_CTL1 register
3. Enable Synchronized forwarding in the FWD_CTL2 register

8.4.19.3 Basic Synchronized Forwarding

During Basic Synchronized Forwarding each forwarded frame is an independent CSI-2 video frame including FrameStart (FS), video lines, and FrameEnd (FE) packets. Each forwarded stream may have a unique VC ID. If the forwarded streams do not have a unique VC-ID, the receiving process may use the frame order to differentiate the video stream packets.

The forwarding engine attempts to send the video synchronized. If synchronization fails, the CSI-2 transmitter stops forwarding packets and attempts to restart sending synchronized video at the next FS indication. Packets are discarded as long as the forwarding engine is unable to send the synchronized video.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – FS1 – FS2 – FS3 – C0L1 – C1L1 – C2L1 – C3L1 – C0L2 – C1L2 – C2L2 – C3L2 – C0L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... C0LN – C1LN – C2LN – C3LN – FE0 – FE1 – FE2 – FE3

Notes:

FSx FrameStart for Camera X

FEx FrameEnd for Camera X

CxLy Line Y for Camera X video frame

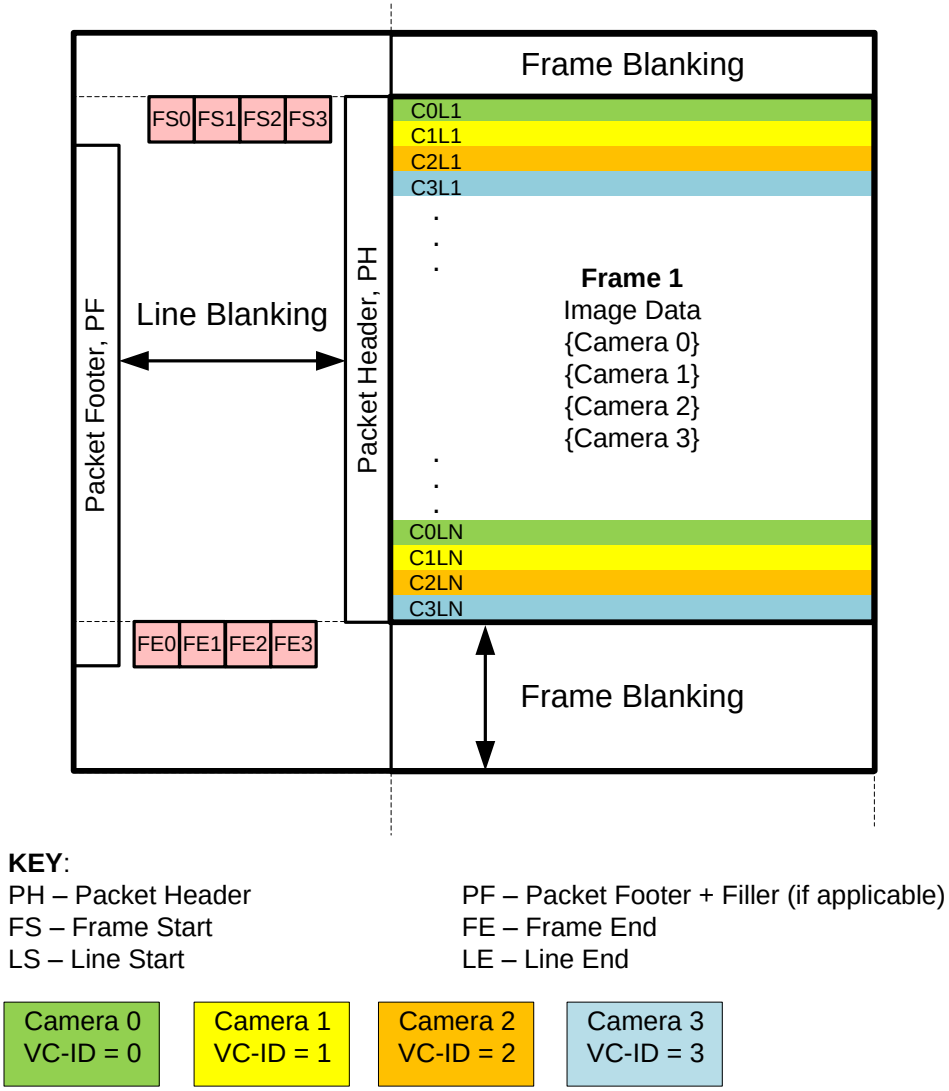
CxLN Last line for Camera X video frame

Each packet includes the virtual channel ID assigned to receive port for each camera.

8.4.19.3.1 Code Example for Basic Synchronized Forwarding

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x70,0x1F) # RAW10_datatype_yuv422b10_VC0

# "*** RX1 VC=1 ***"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x70,0x5F) # RAW10_datatype_yuv422b10_VC1

# "*** RX2 VC=2 ***"
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0x70,0x9F) # RAW10_datatype_yuv422b10_VC2

# "*** RX3 VC=3 ***"
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0x70,0xDF) # RAW10_datatype_yuv422b10_VC3

#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI0 select

#  "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI0 4L

#  "***Basic_FWD"
```

```
WriteI2C(0x21,0x14) # Synchronized Basic_FWD

#  "***FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0
```



**Blanking intervals do not provide accurate synchronization timing*

Figure 30. Basic Synchronized Format

8.4.19.4 Line-Interleave Forwarding

In synchronized forwarding, the forwarding engine may be programmed to send only one of each synchronization packet. For example, if forwarding from all four input ports, only one FS, FE packet is sent for each video frame. The synchronization packets for the other 3 ports is dropped. The video line packets for each video stream are sent as individual packets. This effectively merges the frames from N video sources into a single frame that has N times the number of video lines.

In this mode, all video streams must also have the same VC, although this is not checked by the forwarding engine. This is useful when connected to a controller that does not support multiple VCs. The receiving processor must process the image based on order of video line reception.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – C0L1 – C1L1 – C2L1 – C3L1 – C0L2 – C1L2 – C2L2 – C3L2 – C0L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... C0LN – C1LN – C2LN – C3LN – FE0

Notes:

FSx FrameStart for Camera X

FEx FrameEnd for Camera X

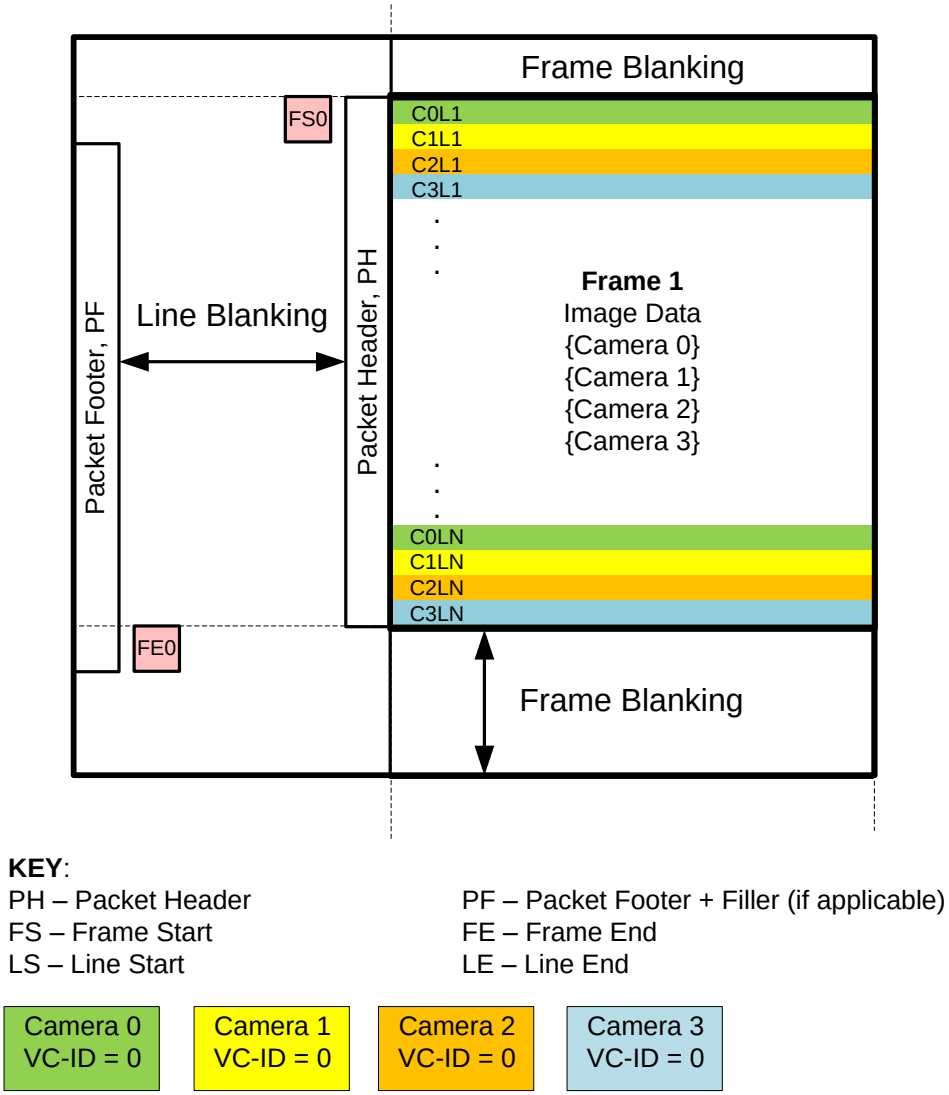
CxLy Line Y for Camera X video frame

CxLN Last line for Camera X video frame

All packets would have the same VC ID.

8.4.19.4.1 Code Example for Line-Interleave Forwarding

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4c,0x01) # RX0
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0

# "*** RX1 VC=0 ***"
WriteI2C(0x4c,0x12) # RX1
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0

# "*** RX2 VC=0 ***"
WriteI2C(0x4c,0x24) # RX2
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0

# "*** RX3 VC=0 ***"
WriteI2C(0x4c,0x38) # RX3
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0

#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI0 select

#  "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI0 4L

# "*** CSI0_SYNC_FWD synchronous forwarding with line interleaving ***"
WriteI2C(0x21,0x28) # synchronous forwarding with line interleaving

#  "*** FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0
```



**Blanking intervals do not provide accurate synchronization timing*

Figure 31. Line-Interleave Format

8.4.19.5 Line-Concatenated Forwarding

In synchronized forwarding, the forwarding engine may be programmed to merge video frames from multiple sources into a single video frame by concatenating video lines. Each of the cameras for each RX carry different data streams that get concatenated into one CSI-2 stream. For example, if forwarding from all four input ports, only one FS, an FE packet is sent for each video frame. The synchronization packets for the other 3 ports are dropped. In addition, the video lines from each camera are combined into a single line. The controller must separate the single video line into the separate components based on position within the concatenated video line.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – C0L1,C1L1,C2L1,C3L1 – C0L2,C1L2,C2L2,C3L2 – C0L3,C1L3,C2L3,C3L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... C0LN,C1LN,C2LN,C3LN – FE0

Notes:

FSx FrameStart for Camera X

FEx FrameEnd for Camera X

CxLy Line Y for Camera X video frame

CxLN Last line for Camera X video frame

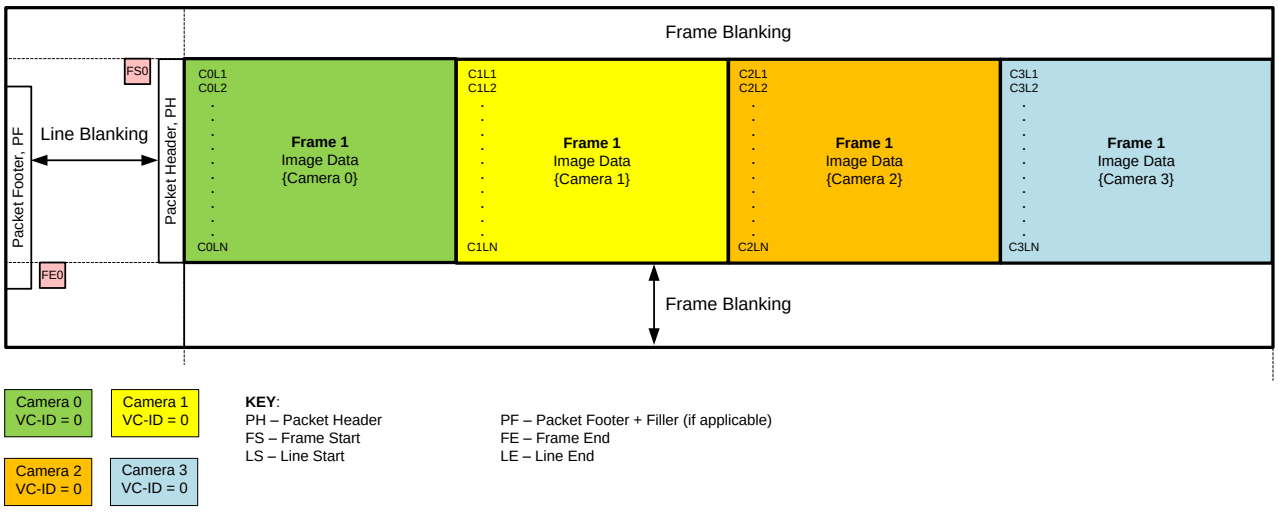
C0L1,C1L1,C2L1,C3L1 indicates concatenation of the first video line from each camera into a single video line. This packet has a modified header and footer that matches the concatenated line data.

Packets would have the same VC ID, based on the VC ID for the lowest number camera port being forwarded.

Lines are concatenated on a byte basis without padding between video line data.

8.4.19.5.1 Code Example for Line-Concatenate Forwarding

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4c,0x01) # RX0
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0

# "*** RX1 VC=0 ***"
WriteI2C(0x4c,0x12) # RX1
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0

# "*** RX2 VC=0 ***"
WriteI2C(0x4c,0x24) # RX2
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0

# "*** RX3 VC=0 ***"
WriteI2C(0x4c,0x38) # RX3
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0

#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI0 select

#  "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI0 4L

# "*** CSI0_SYNC_FWD synchronous forwarding with line concatenation ***"
WriteI2C(0x21,0x3c) # synchronous forwarding with line concatenation

#  "***FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0
```



**Blanking intervals do not provide accurate synchronization timing*

Figure 32. Line-Concatenated Format

8.4.19.6 CSI-2 Replicate Mode

In CSI-2 Replicate mode, both ports can be programmed to output the same data. The output from CSI-2 port 0 is also presented on CSI-2 port 1.

To configure this mode of operation, set the CSI_REPLICATE bit in the FWD_CTL2 register (Address 0x21).

8.4.19.7 CSI Transmitter Output Control

Two register controls allow control of CSI Transmitter outputs to disable the CSI Transmitter outputs. If the OUTPUT_SLEEP_STATE_SELECT (OSS_SEL) control is set to 0 in the GENERAL_CFG 0x02 register, the CSI Transmitter outputs are forced to the HS-0 state. If the OUTPUT_ENABLE (OEN) register bit is set to 0 in the GENERAL_CFG register, the CSI pins are set to the high-impedance state.

For normal operation (OSS_SEL and OEN both set to 1), the detection of activity on FPD3 inputs determines the state of the CSI outputs. The FPD3 inputs are considered active if the Receiver indicates valid lock to the incoming signal. For a CSI TX port, lock is considered valid if any Received port mapped to the TX port is indicating Lock.

Table 9. Table 19. CSI Output Control Options

PDB pin	OSS_SEL	OEN	FPD3 INPUT	CSI PIN STATE
0	X	X	X	Hi-Z
1	0	X	X	HS-0
1	1	0	X	Hi-Z
1	1	1	Inactive	Hi-Z
1	1	1	Active	Valid

8.5 Programming

8.5.1 Serial Control Bus

The DS90UB964-Q1 implements two I2C compatible serial control buses. Both I2C ports support local device configuration and incorporates a bi-directional control channel (BCC) that allows communication with a remote serializers as well as remote I2C slave devices.

The device address is set via a resistor divider connected to the IDx pin (R1 and R2 – see Figure 33).

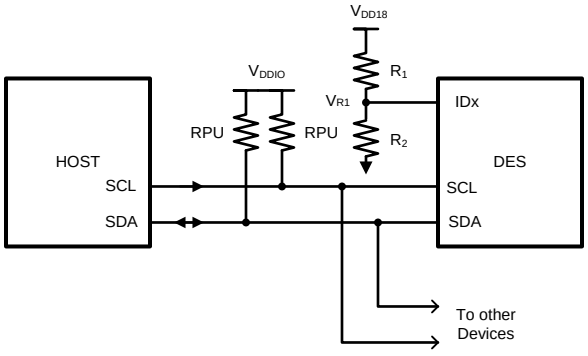


Figure 33. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to VDDIO. For most applications, TI recommends a 4.7 kΩ pullup resistor to VDDIO. However, the pull-up resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

The IDx pin configures the control interface to one of 8 possible device addresses. A pullup resistor and a pulldown resistor may be used to set the appropriate voltage ratio between the IDx input pin (V_{R1}) and VDD18, each ratio corresponding to a specific device address. See Table 10.

Programming (continued)

Table 10. Serial Control Bus Addresses for IDx

NO.	TARGET VOLTAGE			SUGGESTED R1 kΩ (1% tol)	SUGGESTED R2 kΩ (1% tol)	7-BIT ADDRESS	8-BIT ADDRESS
	V_{R1} min (V)	V_{R1} typ (V)	V_{R1} max (V)				
0	0	0	0.237	OPEN	40.2	0x30	0x60
1	0.293	0.367	0.440	118	30.9	0x32	0x64
2	0.507	0.579	0.650	107	51.1	0x34	0x68
3	0.716	0.783	0.849	113	88.7	0x36	0x6C
4	0.924	0.992	1.059	82.5	102	0x38	0x70
5	1.139	1.205	1.271	68.1	137	0x3A	0x74
6	1.350	1.416	1.481	56.2	210	0x3C	0x78
7	1.561	VDD18	VDD18	13.3	OPEN	0x3D	0x7A

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 34 .

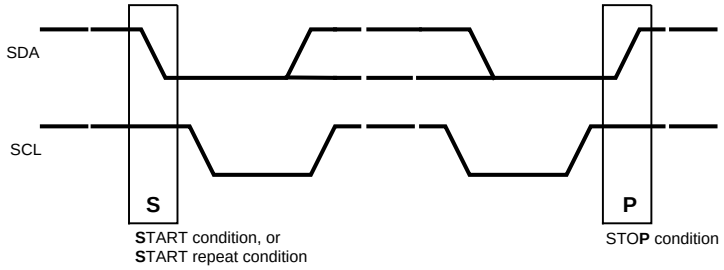


Figure 34. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it acknowledges (ACKs) the master by driving the SDA bus low. If the address does not match a device's slave address, it not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 35 and a WRITE is shown in Figure 36.

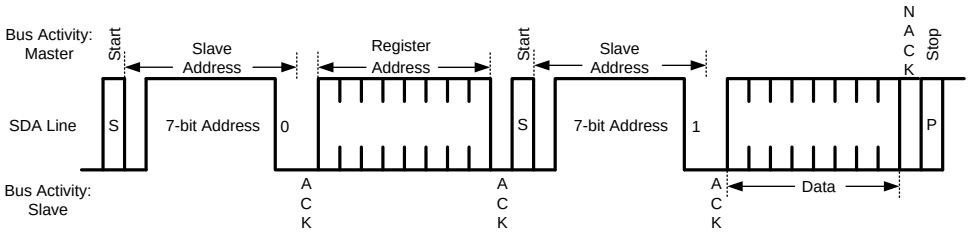


Figure 35. Serial Control Bus — READ

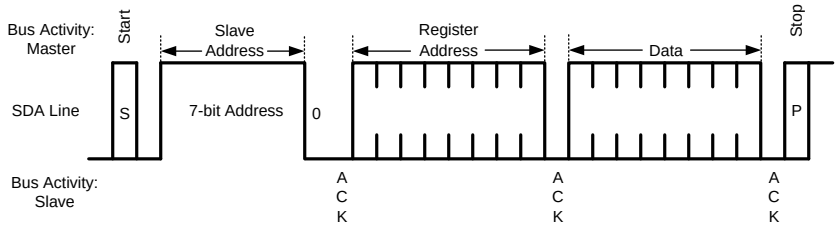


Figure 36. Serial Control Bus — WRITE

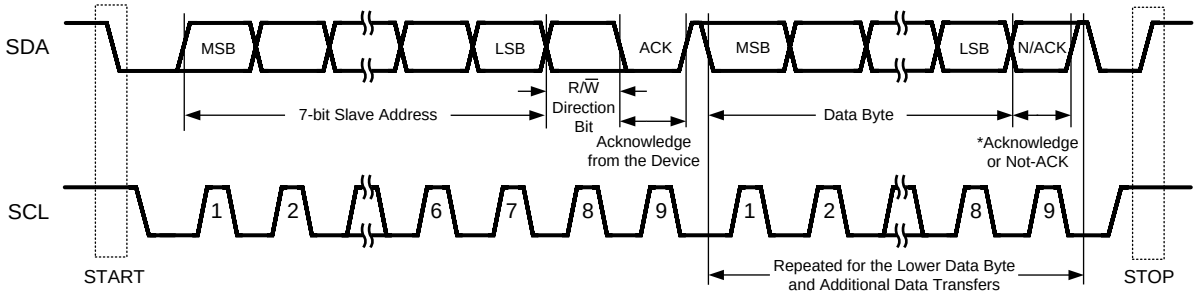


Figure 37. Basic Operation

The I2C Master located at the Deserializer must support I2C clock stretching. For more information on I2C interface requirements and throughput considerations, refer to *I2C Communication Over FPD-Link III with Bidirectional Control Channel* and *I2C over DS90UB913/4 FPD-Link III with Bidirectional Control Channel*.

8.5.2 Second I2C Port

The DS90UB964-Q1 includes a second I2C port that allows bi-directional control channel access to both local registers and remote devices. Remote device access is configured on BCCx_MAP register 0x0C[7:4].

The second I2C port uses the same I2C address as the primary I2C port. In addition, RX Port I2C IDs are also available for the second I2C port.

In general, TI recommends that the second I2C port be used in cases where the CSI TX ports are connected to separate processors. The second I2C port allows independent control of the DS90UB964-Q1 as well as remote devices by the second processor.

8.5.3 Broadcast Write to Remote Devices

The DS90UB964-Q1 provides a mechanism to broadcast I2C writes to remote devices (either remote slaves or serializers). For each Receive port, the SlaveID/Alias register pairs would be programmed with the same SlaveAlias value so they would each respond to the local I2C access. The SlaveID value would match the intended remote device address, either remote slave or serializers. For each receive port, on of the SlaveAlias registers is set with an Alias value. For each port, the SlaveID value is set to the address of the remote device. These values may be the same. To access the remote serializer registers rather than a remote slave, the serializer ID (SER_IDx or SER_IDy) would be used as the SlaveID value.

8.5.3.1 Code Example for Broadcast Write

```
#  "FPD3_PORT_SEL Boardcast RX0/1/2/3"
WriteI2C(0x4c,0x0f) # RX_PORT0 read; RX0/1/2/3 write

#  "enable pass throu"
WriteI2C(0x58,0x58) # enable pass throu

WriteI2C(0x5c,0x18) # "SER_ALIAS_ID"

WriteI2C(0x5d,0x60) # "SlaveID[0]"

WriteI2C(0x65,0x60) # "SlaveAlias[0]"
```

```
WriteI2C(0x7c,0x01) # "FV_POLARITY"

WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
```

8.5.4 Interrupt Support

Interrupts can be brought out on the INTB pin as controlled by the INTERRUPT_CTL 0x23 and INTERRUPT_STS 0x24 registers. The main interrupt control registers provide control and status for interrupts from the individual sources. Sources include each of the four FPD3 Receive ports as well as each of the two CSI-2 Transmit ports. Clearing interrupt conditions requires reading the associated status register for the source. The setting of the individual interrupt status bits is not dependent on the related interrupt enable controls. The interrupt enable controls whether an interrupt is generated based on the condition, but does not prevent the interrupt status assertion.

For an interrupt to be generated based on one of the interrupt status assertions, both the individual interrupt enable and the INT_EN control must be set in the INTERRUPT_CTL 0x23 register. For example, to generate an interrupt if IS_RX0 is set, both the IE_RX0 and INT_EN bits must be set. If IE_RX0 is set but INT_EN is not, the INT status is indicated in the INTERRUPT_STS register, and the INTB pin does not indicate the interrupt condition.

See the INTERRUPT_CTL 0x23 and INTERRUPT_STS 0x24 register for details.

8.5.4.1 Code Example to Enable Interrupts

```
#  "RX01/2/3/4 INTERRUPT_CTL enable"
WriteI2C(0x23,0xBF) # RX all & INTB PIN EN

# Individual RX01/2/3/4 INTERRUPT_CTL enable
# "RX0 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x23,0x81) # RX0 & INTB PIN EN

# "RX1 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x23,0x82) # RX1 & INTB PIN EN

# "RX2 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0x23,0x84) # RX2 & INTB PIN EN

# "RX3 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0x23,0x88) # RX3 & INTB PIN EN
```

8.5.4.2 FPD-Link III Receive Port Interrupts

For each FPD-Link III Receive port, multiple options are available for generating interrupts. Interrupt generation is controlled via the PORT_ICR_HI 0xD8 and PORT_ICR_LO 0xD9 registers. In addition, the PORT_ISR_HI 0xDA and PORT_ISR_LO 0xDB registers provide read-only status for the interrupts. Clearing of interrupt conditions is handled by reading the RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS registers. The status bits in the PORT_ISR_HI/LO registers are copies of the associated bits in the main status registers.

To enable interrupts from one of the Receive port interrupt sources:

1. Enable the interrupt source by setting the appropriate interrupt enable bit in the PORT_ICR_HI or PORT_ICR_LO register
2. Set the RX Port X Interrupt control bit (IE_RXx) in the INTERRUPT_CTL register
3. Set the INT_EN bit in the INTERRUPT_CTL register to allow the interrupt to assert the INTB pin low

To clear interrupts from one of the Receive port interrupt sources:

1. (optional) Read the INTERRUPT_STS register to determine which RX Port caused the interrupt
2. (optional) Read the PORT_ISR_HI and PORT_ISR_LO registers to determine source of interrupt
3. Read the appropriate RX_PORT_STS1, RX_PORT_STS2, or CSI_RX_STS register to clear the interrupt.

The first two steps are optional. The interrupt could be determined and cleared by just reading the status registers.

8.5.4.3 Code Example to Readback Interrupts

```
INTERRUPT_STS = ReadI2C(0x24) # 0x24 INTERRUPT_STS


if ((INTERRUPT_STS & 0x80) >> 7):
    print "# GLOBAL INTERRUPT DETECTED "
if ((INTERRUPT_STS & 0x40) >> 6):
    print "# RESERVED "
if ((INTERRUPT_STS & 0x20) >> 5):
    print "# IS_CSI_TX1 DETECTED "
if ((INTERRUPT_STS & 0x10) >> 4):
    print "# IS_CSI_TX0 DETECTED "
if ((INTERRUPT_STS & 0x08) >> 3):
    print "# IS_RX3 DETECTED "
if ((INTERRUPT_STS & 0x04) >> 2):
    print "# IS_RX2 DETECTED "
if ((INTERRUPT_STS & 0x02) >> 1):
    print "# IS_RX1 DETECTED "
if ((INTERRUPT_STS & 0x01) ):
    print "# IS_RX0 DETECTED "

# "################################################"
#  "RX0 status"
# "################################################"

WriteReg(0x4C,0x01) # RX0
PORT_ISR_LO = ReadI2C(0xDB)

print "0xDB PORT_ISR_LO : ", hex(PORT_ISR_LO) # readout; cleared by RX_PORT_STS2

if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "

################################################

PORT_ISR_HI = ReadI2C(0xDA)

print "0xDA PORT_ISR_HI : ", hex(PORT_ISR_HI) # readout; cleared by RX_PORT_STS2

if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "

################################################

RX_PORT_STS1 = ReadI2C(0x4D) # R/COR

if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
```

```
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "

################################################

RX_PORT_STS2 = ReadI2C(0x4E)

if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "

################################################

# "################################################"
#  "RX1 status"
# "################################################"


WriteReg(0x4C,0x12) # RX1
PORT_ISR_LO = ReadI2C(0xDB) # PORT_ISR_LO readout; cleared by RX_PORT_STS2

if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "

################################################

PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2

if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "

################################################
```

```
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR

if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "

################################################

RX_PORT_STS2 = ReadI2C(0x4E)

if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "

################################################

# "################################################"
#  "RX2 status"
# "################################################"

WriteReg(0x4C,0x24) # RX2
PORT_ISR_LO = ReadI2C(0xDB) # readout; cleared by RX_PORT_STS2

if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "

################################################

PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2
```

```
if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "

################################################

RX_PORT_STS1 = ReadI2C(0x4D) # R/COR

if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "

################################################

RX_PORT_STS2 = ReadI2C(0x4E)

if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "

################################################


# "################################################"
#  "RX3 status"
# "################################################"

WriteReg(0x4C,0x38) # RX3
PORT_ISR_LO = ReadI2C(0xDB) # readout; cleared by RX_PORT_STS2

if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
```

```
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "

################################################

PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2

if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "

################################################

RX_PORT_STS1 = ReadI2C(0x4D) # R/COR

if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "

################################################

RX_PORT_STS2 = ReadI2C(0x4E)

if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "

################################################
```

8.5.4.4 CSI-2 Transmit Port Interrupts

The following interrupts are available for each CSI Transmit Port:

- Pass indication
- Synchronized status

- Deassertion of Pass indication for an input port assigned to the CSI TX Port
- Loss of Synchronization between input video streams
- RX Port Interrupt – interrupts from RX Ports mapped to this CSI Transmit port

See the CSI_TX_ICR address 0x36 and CSI_TX_ISR address 0x37 registers for details.

The setting of the individual interrupt status bits is not dependent on the related interrupt enable controls. The interrupt enable controls whether an interrupt is generated based on the condition, but does not prevent the interrupt status assertion.

8.5.5 Timestamp – Video Skew Detection

The DS90UB964-Q1 implements logic to detect skew between video signaling from attached cameras. For each input port, the DS90UB964-Q1 provides the ability to capture a time-stamp for both a start-of-frame and start-of-line event. Comparison of timestamps can provide information on the relative skew between the ports. Start-of-frame timestamps are generated at the active edge of the Vertical Sync signal in Raw mode. Start-of-line timestamps are generated at the start of reception of the Nth line of video data after the start-of-frame for either mode of operation. The function does not use the Line Start (LS) packet or Horizontal Sync controls to determine the start of lines.

The skew detection can run in either a FrameSync mode or free-run mode.

Skew detection can be individually enabled for each RX port.

For start-of-line timestamps, a line number must be programmed. The same line number is used for all 4 channels. Prior to reading timestamps, the TS_FREEZE bit for each port that will be read should be set. This will prevent overwrite of the timestamps by the detection circuit until all timestamps have been read. The freeze condition will be released automatically once all frozen timestamps have been read. The freeze bits can also be cleared if it does not read all the timestamp values.

The TS_STATUS register includes the following:

- Flags to indicate multiple start-of-frame per FrameSync period
- Flag to indicate Timestamps Ready
- Flags to indicate Timestamps valid (per port) – if ports are not synchronized, all ports may not indicate valid timestamps

The Timestamp Ready flag will be cleared when the TS_FREEZE bit is cleared.

8.5.6 Pattern Generation

The DS90UB964-Q1 supports an internal pattern generation feature to provide a simple way to generate video test patterns for the CSI-2 transmitter outputs. Two types of patterns are supported: Reference Color Bar pattern and Fixed Color patterns.

The Pattern Generator is programmable with the following options:

- Number of color bars (1, 2, 4, or 8)
- Number of bytes per line
- Number of bytes per color bar
- CSI DataType field and VC-ID
- Number of active video lines per frame
- Number of total lines per frame (active plus blanking)
- Line period
- Vertical front porch – number of blank lines prior to FrameEnd packet
- Vertical back porch – number of blank lines following FrameStart packet

8.5.6.1 Code Example for Pattern Generator

```
#Patgen Fixed Colorbar 1280x720p30

WriteI2C(0x32,0x01) # CSI0 sel and CSI0 enable
WriteI2C(0x33,0x01)

WriteI2C(0xB0,0x00) # Indirect Pattern Gen Registers
```

```
WriteI2C(0xB1,0x01) # PGEN_CTL
WriteI2C(0xB2,0x01)

WriteI2C(0xB1,0x02) # PGEN_CFG
WriteI2C(0xB2,0x33)

WriteI2C(0xB1,0x03) # PGEN_CSI_DI
WriteI2C(0xB2,0x24)

WriteI2C(0xB1,0x04) # PGEN_LINE_SIZE1
WriteI2C(0xB2,0x0F)

WriteI2C(0xB1,0x05) # PGEN_LINE_SIZE0
WriteI2C(0xB2,0x00)

WriteI2C(0xB1,0x06) # PGEN_BAR_SIZE1
WriteI2C(0xB2,0x01)

WriteI2C(0xB1,0x07) # PGEN_BAR_SIZE0
WriteI2C(0xB2,0xE0)

WriteI2C(0xB1,0x08) # PGEN_ACT_LPF1
WriteI2C(0xB2,0x02)

WriteI2C(0xB1,0x09) # PGEN_ACT_LPF0
WriteI2C(0xB2,0xD0)

WriteI2C(0xB1,0x0A) # PGEN_TOT_LPF1
WriteI2C(0xB2,0x04)

WriteI2C(0xB1,0x0B) # PGEN_TOT_LPF0
WriteI2C(0xB2,0x1A)

WriteI2C(0xB1,0x0C) # PGEN_LINE_PD1
WriteI2C(0xB2,0x0C)

WriteI2C(0xB1,0x0D) # PGEN_LINE_PD0
WriteI2C(0xB2,0x67)

WriteI2C(0xB1,0x0E) # PGEN_VBP
WriteI2C(0xB2,0x21)

WriteI2C(0xB1,0x0F) # PGEN_VFP
WriteI2C(0xB2,0x0A)
```

8.5.7 BIST

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high speed serial link and the back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

8.5.7.1 BIST Configuration and Status

The BIST mode is enabled by BIST configuration register 0xB3. The test may select either an external PCLK or the internal oscillator clock (OSC) frequency in the Serializer. In the absence of PCLK, the user can select the internal OSC frequency at the deserializer through the BIST configuration register. When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a continuous stream of a pseudo-random sequence and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame. While the lock indications are required to identify the beginning of proper data reception, for any link failures or data corruption, the best indication is the contents of the error counter in the BIST_ERR_COUNT register 0x57 for each RX port.

8.6 Register Description

The DS90UB964-Q1 implements the following register blocks, accessible via I2C as well as the bi-directional control channel:

- Main Registers
- FPD3 RX Port Registers (separate register block for each of the four RX ports)
- CSI-2 Port Registers (separate register block for each of the CSI-2 ports)

Table 11. Main Register Map Descriptions

ADDRESS RANGE	DESCRIPTION	ADDRESS MAP			
0x00-0x31	Digital Shared Registers	Shared			
0x32-0x3A	Digital CSI-2 Registers (paged, broadcast write allowed)	CSI-2 TX Port 0 *R: 0x32[4]=0* *W: 0x32[0]=1*		CSI-2 TX Port 1 *R: 0x32[4]=1* *W: 0x32[1]=1*	
0x4C-0x7F	Digital RX Port Registers (paged, broadcast write allowed)	FPD3 RX Port 0 *R: 0x4C[5:4]=00* *W: 0x4C[0]=1*	FPD3 RX Port 1 *R: 0x4C[5:4]=01* *W: 0x4C[1]=1*	FPD3 RX Port 2 *R: 0x4C[5:4]=10* *W: 0x4C[2]=1*	FPD3 RX Port 3 *R: 0x4C[5:4]=11* *W: 0x4C[3]=1*
0x80-0x9F	Reserved	Reserved			
0xA0-0xAF	Reserved	Reserved			
0xB0-0xB2	Indirect Access Registers	Shared			
0xB0-0xBF	Digital Share Registers	Shared			
0xC0-0xCF	Reserved	Reserved			
0xD0-0xDF	Digital RX Port Debug Registers	FPD3 RX Port 0	FPD3 RX Port 1	FPD3 RX Port 2	FPD3 RX Port 3
0xE0-0xEF	Reserved	Reserved			
0xF0-0xF5	FPD3 RX ID	Shared			
0xF8-0xFB	Port I2C Addressing	Shared			
0xF6-0xF7 0xFC-0xFF	Reserved	Reserved			

LEGEND:

- RW = Read Write
- RW/SC = RW/SC = Read Write access/Self Clearing bit
- R = Read Only, Permanent value
- R/COR = Read Only, Clear On Read

8.7 Register Maps

Table 12. Serial Control Bus Registers

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x00	I2C_DEVICE_ID	7:1	DEVICE_ID	RW	Strap	7-bit I2C ID of Deserializer. This field always indicates the current value of the I2C ID. When bit 0 of this register is 0, this field is read-only and show the strapped ID. When bit 0 of this register is 1, this field is read/write and can be used to assign any valid I2C ID.
			0	DES_ID	RW	0	0: Device ID is from strap 1: Register I2C Device ID overrides strapped value
Share	0x01	RESET_CTL	7:6	RESERVED	R	0x0	Reserved
			5	RESERVED	RW	0	Reserved
			4:3	RESERVED	R	0x0	Reserved
			2	RESTART_AUTOLOAD	RW/SC	0	Restart ROM Auto-load Setting this bit to 1 causes a re-load of the ROM. This bit is self-clearing. Software may check for Auto-load complete by checking the CFG_INIT_DONE bit in the DEVICE_STS register.
			1	DIGITAL RESET1	RW/SC	0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation
			0	DIGITAL RESET0	RW/SC	0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation
Share	0x02	GENERAL_CFG	7:5	RESERVED	R	0x0	Reserved
			4	OUTPUT_EN_MODE	RW	1	Output Enable Mode If set to 0, the CSI TX output port is forced to the high-impedance state if no assigned RX ports have an active Receiver lock. If set to 1, the CSI TX output port will continue in normal operation if no assigned RX ports have an active Receiver lock. CSI TX operation will remain under register control via the CSI_CTL register for each port. If no assigned RX ports have an active Receiver lock, this will result in the CSI Transmitter entering the LP-11 state.
			3	OUTPUT_ENABLE	RW	1	Output Enable Control (in conjunction with Output Sleep State Select) If OUTPUT_SLEEP_STATE_SEL is set to 1 and this bit is set to 0, the CSI TX outputs is forced into a high impedance state.
			2	OUTPUT_SLEEP_STATE_SEL	RW	1	OSS Select to control output state when LOCK is low (used in conjunction with Output Enable) When this bit is set to 0, the CSI TX outputs is forced into a HS-0 state.
			1	RX_PARITY_CHECKER_EN	RW	1	FPD3 Receiver Parity Checker Enable When enabled, the parity check function is enabled for the FPD3 receiver. This allows detection of errors on the FPD3 receiver data bits. 0: Disable 1: Enable

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			0	FORCE_REFCLK_DET	RW	0	Force indication of external reference clock 0: Normal operation, reference clock detect circuit indicates the presence of an external reference clock 1: Force reference clock to be indicated present
Share	0x03	REV_MASK_ID	7:4	REVISION_ID	R	0x0	Revision ID 0010: DS90UB964-Q1 A0 0011: DS90UB964-Q1 A1
			3:0	MASK_ID	R	0x0	Mask ID
Share	0x04	DEVICE_STS	7	CFG_CKSUM_STS	R	1	Config Checksum Passed This bit is set following initialization if the Configuration data in the eFuse ROM had a valid checksum
			6	CFG_INIT_DONE	R	1	Power-up initialization complete This bit is set after Initialization is complete. Configuration from eFuse ROM has completed.
			5:0	RESERVED	R	0x2	Reserved
Share	0x05	PAR_ERR_THOLD_HI	7:0	PAR_ERR_THOLD_HI	RW	0x1	FPD3 Parity Error Threshold High byte This register provides the 8 most significant bits of the Parity Error Threshold value. For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag is set in the RX_PORT_STS1 register.
Share	0x06	PAR_ERR_THOLD_LO	7:0	PAR_ERR_THOLD_LO	RW	0x0	FPD3 Parity Error Threshold Low byte This register provides the 8 least significant bits of the Parity Error Threshold value. For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag is set in the RX_PORT_STS1 register.
Share	0x07	BCC Watchdog Control	7:1	BCC WATCHDOG TIMER	RW	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bi-directional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
			0	BCC WATCHDOG TIMER DISABLE	RW	0	Disable Bi-directional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation
Share	0x08	I2C Control 1	7	LOCAL WRITE DISABLE	RW	0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C master attached to the Serializer. Setting this bit does not affect remote access to I2C slaves at the Deserializer.
			6:4	I2C SDA HOLD	RW	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
			3:0	I2C FILTER DEPTH	RW	0xC	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that is rejected. Units are 5 nanoseconds.

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x09	I2C Control 2	7:4	SDA Output Setup	RW	0x1	Remote Ack SDA Output Setup When a Control Channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. Setting this value will increase setup time in units of 640ns. The nominal output setup time value for SDA to SCL when this field is 0 is 80ns.
			3:2	SDA Output Delay	RW	0x0	SDA Output Delay This field configures additional delay on the SDA output relative to the falling edge of SCL. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 240ns 01: 280ns 10: 320ns 11: 360ns
			1	I2C BUS TIMER SPEEDUP	RW	0	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
			0	I2C BUS TIMER DISABLE	RW	0	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL
Share	0x0A	SCL High Time	7:0	SCL HIGH TIME	RW	0x79	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the reference clock at 25 MHz + 100ppm. The delay includes 5 additional oscillator clock periods. Min_delay = 39.996ns * (SCL_HIGH_TIME + 5)
Share	0x0B	SCL Low Time	7:0	SCL LOW TIME	RW	0x79	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bi-directional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the reference clock at 25 MHz + 100ppm. The delay includes 5 additional clock periods. Min_delay = 39.996ns * (SCL_LOW_TIME+ 5)
Share	0x0C	RX_PORT_CTL	7	BCC3_MAP	RW	0	Map Control Channel 3 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1
			6	BCC2_MAP	RW	0	Map Control Channel 2 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			5	BCC1_MAP	RW	0	Map Control Channel 1 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1
			4	BCC0_MAP	RW	0	Map Control Channel 0 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1
			3	PORT3_EN	RW	1	Port 3 Receiver Enable 0: Disable Port 3 Receiver 1: Enable Port 3 Receiver
			2	PORT2_EN	RW	1	Port 2 Receiver Enable 0: Disable Port 2 Receiver 1: Enable Port 2 Receiver
			1	PORT1_EN	RW	1	Port 1 Receiver Enable 0: Disable Port 1 Receiver 1: Enable Port 1 Receiver
			0	PORT0_EN	RW	1	Port 0 Receiver Enable 0: Disable Port 0 Receiver 1: Enable Port 0 Receiver
Share	0x0D	IO_CTL	7	SEL3P3V	RW	0	3.3V I/O Select on pins INTB, I2C, GPIO 0: 1.8V I/O Supply 1: 3.3V I/O Supply If IO_SUPPLY_MODE_OV is 0, a read of this register will return the detected I/O voltage level.
			6	IO_SUPPLY_MODE_OV	RW	0	Override I/O Supply Mode bit If set to 0, the detected voltage level is used for both SEL3P3V and IO_SUPPLY_MODE controls. If set to 1, the values written to the SEL3P3V and IO_SUPPLY_MODE fields is used.
			5:4	IO_SUPPLY_MODE	RW	0x0	I/O Supply Mode 00: 1.8V 11: 3.3V If IO_SUPPLY_MODE_OV is 0, a read of this register will return the detected I/O voltage level.
			3:0	RESERVED	RW	0x9	Reserved
Share	0x0E	GPIO_PIN_STS	7:0	GPIO_STS	R	0x0	GPIO Pin Status This register reads the current values on each of the 8 GPIO pins. Bit 7 reads GPIO7 and bit 0 reads GPIO0.
Share	0x0F	GPIO_INPUT_CTL	7	GPIO7_INPUT_EN	RW	1	GPIO7 Input Enable 0: Disabled 1: Enabled
			6	GPIO6_INPUT_EN	RW	1	GPIO6 Input Enable 0: Disabled 1: Enabled
			5	GPIO5_INPUT_EN	RW	1	GPIO5 Input Enable 0: Disabled 1: Enabled
			4	GPIO4_INPUT_EN	RW	1	GPIO4 Input Enable 0: Disabled 1: Enabled
			3	GPIO3_INPUT_EN	RW	1	GPIO3 Input Enable 0: Disabled 1: Enabled

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			2	GPIO2_INPUT_EN	RW	1	GPIO2 Input Enable 0: Disabled 1: Enabled
			1	GPIO1_INPUT_EN	RW	1	GPIO1 Input Enable 0: Disabled 1: Enabled
			0	GPIO0_INPUT_EN	RW	1	GPIO0 Input Enable 0: Disabled 1: Enabled
Share	0x10	GPIO0_PIN_CTL	7:5	GPIO0_OUT_SEL	RW	0x0	GPIO0 Output Select Determines the output data for the selected source. If GPIO0_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO0_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO0_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO0_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI TX Port Interrupt 11 : Reserved
			4:2	GPIO0_OUT_SRC	RW	0x0	GPIO0 Output Source Select Selects output source for GPIO0 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI TX Port 0 111 : CSI TX Port 1
			1	GPIO0_OUT_VAL	RW	0	GPIO0 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO0_OUT_EN	RW	0	GPIO0 Output Enable 0: Disabled 1: Enabled

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x11	GPIO1_PIN_CTL	7:5	GPIO1_OUT_SEL	RW	0x0	GPIO1 Output Select Determines the output data for the selected source. If GPIO1_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO1_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO1_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO1_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI TX Port Interrupt 111 : Reserved
			4:2	GPIO1_OUT_SRC	RW	0x0	GPIO1 Output Source Select Selects output source for GPIO1 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI TX Port 0 111 : CSI TX Port 1
			1	GPIO1_OUT_VAL	RW	0	GPIO1 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO1_OUT_EN	RW	0	GPIO1 Output Enable 0: Disabled 1: Enabled

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x12	GPIO2_PIN_CTL	7:5	GPIO2_OUT_SEL	RW	0x0	GPIO2 Output Select Determines the output data for the selected source. If GPIO2_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO2_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO2_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO2_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI TX Port Interrupt 111 : Reserved
			4:2	GPIO2_OUT_SRC	RW	0x0	GPIO2 Output Source Select Selects output source for GPIO2 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI TX Port 0 111 : CSI TX Port 1
			1	GPIO2_OUT_VAL	RW	0	GPIO2 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO2_OUT_EN	RW	0	GPIO2 Output Enable 0: Disabled 1: Enabled

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x13	GPIO3_PIN_CTL	7:5	GPIO3_OUT_SEL	RW	0x0	GPIO3 Output Select Determines the output data for the selected source. If GPIO3_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO3_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO2_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO3_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI TX Port Interrupt 111 : Reserved
			4:2	GPIO3_OUT_SRC	RW	0x0	GPIO3 Output Source Select Selects output source for GPIO3 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 101 : Reserved 110 : CSI TX Port 0 111 : CSI TX Port 1
			1	GPIO3_OUT_VAL	RW	0	GPIO3 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO3_OUT_EN	RW	0	GPIO3 Output Enable 0: Disabled 1: Enabled

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x14	GPIO4_PIN_CTL	7:5	GPIO4_OUT_SEL	RW	0x0	GPIO4 Output Select Determines the output data for the selected source. If GPIO4_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO4_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO2_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO4_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI TX Port Interrupt 111 : Reserved
			4:2	GPIO4_OUT_SRC	RW	0x0	GPIO4 Output Source Select Selects output source for GPIO4 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI TX Port 0 111 : CSI TX Port 1
			1	GPIO4_OUT_VAL	RW	0	GPIO4 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO4_OUT_EN	RW	0	GPIO4 Output Enable 0: Disabled 1: Enabled

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x15	GPIO5_PIN_CTL	7:5	GPIO5_OUT_SEL	RW	0x0	GPIO5 Output Select Determines the output data for the selected source. If GPIO5_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO5_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO5_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO5_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI TX Port Interrupt 111 : Reserved
			4:2	GPIO5_OUT_SRC	RW	0x0	GPIO5 Output Source Select Selects output source for GPIO5 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI TX Port 0 111 : CSI TX Port 1
			1	GPIO5_OUT_VAL	RW	0	GPIO5 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO5_OUT_EN	RW	0	GPIO5 Output Enable 0: Disabled 1: Enabled

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x16	GPIO6_PIN_CTL	7:5	GPIO6_OUT_SEL	RW	0x0	GPIO6 Output Select Determines the output data for the selected source. If GPIO6_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO6_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO6_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO6_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI TX Port Interrupt 111 : Reserved
			4:2	GPIO6_OUT_SRC	RW	0x0	GPIO6 Output Source Select Selects output source for GPIO6 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI TX Port 0 111 : CSI TX Port 1
			1	GPIO6_OUT_VAL	RW	0	GPIO6 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO6_OUT_EN	RW	0	GPIO6 Output Enable 0: Disabled 1: Enabled

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x17	GPIO7_PIN_CTL	7:5	GPIO7_OUT_SEL	RW	0x0	GPIO7 Output Select Determines the output data for the selected source. If GPIO7_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO7_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO7_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO7_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI TX Port Interrupt 111 : Reserved
			4:2	GPIO7_OUT_SRC	RW	0x0	GPIO7 Output Source Select Selects output source for GPIO7 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI TX Port 0 111 : CSI TX Port 1
			1	GPIO7_OUT_VAL	RW	0	GPIO7 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO7_OUT_EN	RW	0	GPIO7 Output Enable 0: Disabled 1: Enabled

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x18	FS_CTL	7:4	FS_MODE	RW	0x0	FrameSync Mode 0000: Internal Generated FrameSync, use Back-channel frame clock from port 0 0001: Internal Generated FrameSync, use Back-channel frame clock from port 1 0010: Internal Generated FrameSync, use Back-channel frame clock from port 2 0011: Internal Generated FrameSync, use Back-channel frame clock from port 3 01xx: Internal Generated FrameSync, use 25MHz clock 1000: External FrameSync from GPIO0 1001: External FrameSync from GPIO1 1010: External FrameSync from GPIO2 1011: External FrameSync from GPIO3 1100: External FrameSync from GPIO4 1101: External FrameSync from GPIO5 1110: External FrameSync from GPIO6 1111: External FrameSync from GPIO7
			3	FS_SINGLE	RW/SC	0	Generate Single FrameSync pulse When this bit is set, a single FrameSync pulse is generated. The system should wait for the full duration of the desired pulse before generating another pulse. When using this feature, the FS_GEN_ENABLE bit should remain set to 0. This bit is self-clearing and will always return 0.
			2	FS_INIT_STATE	RW	0	Initial State This register controls the initial state of the FrameSync signal. 0: FrameSync initial state is 0 1: FrameSync initial state is 1
			1	FS_GEN_MODE	RW	0	FrameSync Generation Mode This control selects between Hi/Lo and 50/50 modes. In Hi/Lo mode, the FrameSync generator will use the FS_HIGH_TIME and FS_LOW_TIME register values to separately control the High and Low periods for the generated FrameSync signal. In 50/50 mode, the FrameSync generator will use the values in the FS_HIGH_TIME_0, FS_LOW_TIME_1 and FS_LOW_TIME_0 registers as a 24-bit value for both the High and Low periods of the generated FrameSync signal. 0: Hi/Lo 1: 50/50
			0	FS_GEN_ENABLE	RW	0	FrameSync Generation Enable 0: Disabled 1: Enabled
Share	0x19	FS_HIGH_TIME_1	7:0	FRAMESYNC_HIGH_TIME_1	RW	0x0	FrameSync High Time bits 15:8 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.
Share	0x1A	FS_HIGH_TIME_0	7:0	FRAMESYNC_HIGH_TIME_0	RW	0x0	FrameSync High Time bits 7:0 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x1B	FS_LOW_TIME_1	7:0	FRAMESYNC_LOW_TIME_1	RW	0x0	FrameSync Low Time bits 15:8 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.
Share	0x1C	FS_LOW_TIME_0	7:0	FRAMESYNC_LOW_TIME_0	RW	0x0	FrameSync Low Time bits 7:0 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.
Share	0x1D	MAX_FRM_HI	7:0	MAX_FRAME_HI	RW	0x0	CSI-2 Maximum Frame Count bits 15:8 In RAW mode operation, the FPD3 Receiver will create CSI-2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field is generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and will always be 0. If Maximum Frame Count value is non-zero, the frame number will increment for each from 1 up to the Maximum Frame Count value before resetting to 1.
Share	0x1E	MAX_FRM_LO	7:0	MAX_FRAME_LO	RW	0x04	CSI-2 Maximum Frame Count bits 7:0 In RAW mode operation, the FPD3 Receiver will create CSI-2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field is generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and will always be 0. If Maximum Frame Count value is non-zero, the frame number will increment for each from 1 up to the Maximum Frame Count value before resetting to 1.
Share	0x1F	CSI_PLL_CTL	7:3	RESERVED	R	0x0	Reserved
			2	RESERVED	RW	0	Reserved
			1:0	CSI_TX_SPEED	RW	10	CSI Transmitter Speed select: (See CSI-2 Transmitter Frequency) Controls the CSI Transmitter frequency. 00 : 1.5 / 1.6 Gbps serial rate 01 :Reserved 10 : 800 Mbps serial rate 11 : 400 Mbps serial rate
Share	0x20	FWD_CTL1	7	FWD_PORT3_DIS	RW	1	Disable forwarding of RX Port 3 0: Forwarding enabled 1: Forwarding disabled
			6	FWD_PORT2_DIS	RW	1	Disable forwarding of RX Port 2 0: Forwarding enabled 1: Forwarding disabled
			5	FWD_PORT1_DIS	RW	1	Disable forwarding of RX Port 1 0: Forwarding enabled 1: Forwarding disabled
			4	FWD_PORT0_DIS	RW	1	Disable forwarding of RX Port 0 0: Forwarding enabled 1: Forwarding disabled
			3	RX3_MAP	RW	0	Map RX Port 3 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			2	RX2_MAP	RW	0	Map RX Port 2 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping
			1	RX1_MAP	RW	0	Map RX Port 1 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping
			0	RX0_MAP	RW	0	Map RX Port 0 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping
Share	0x21	FWD_CTL2	7	CSI_REPLICATE	RW	0	CSI Replicate Mode When set to a 1, the CSI output from port 0 will also be generated on CSI port 1. The same output data is presented on both ports.
			6	FWD_SYNC_AS_AVAIL	RW	0	Synchronized Forwarding As Available During Synchronized Forwarding, each forwarding engine will wait for video data to be available from each enabled port, prior to sending the video line. Setting this bit to a 1 will allow sending the next video line as it becomes available. For example if RX Ports 0 and 1 are being forwarded, port 0 video line is forwarded when it becomes available, rather than waiting until both ports 0 and ports 1 have video data available. This operation may reduce the likelihood of buffer overflow errors in some conditions. This bit will have no affect in video line concatenation mode and only affects video lines (long packets) rather than synchronization packets. This bit applies to both CSI output ports
			5:4	CSI1_SYNC_FWD	RW	0x0	Enable synchronized forwarding for CSI output port 1 (See Synchronized Forwarding) 00: Synchronized forwarding disabled 01: Basic Synchronized forwarding enabled 10: Synchronous forwarding with line interleaving 11: Synchronous forwarding with line concatenation Only one of CSI1_RR_FWD and CSI1_SYNC_FWD must be enabled at a time.
			3:2	CSI0_SYNC_FWD	RW	0x0	Enable synchronized forwarding for CSI output port 0 (Synchronized Forwarding) 00: Synchronized forwarding disabled 01: Basic Synchronized forwarding enabled 10: Synchronous forwarding with line interleaving 11: Synchronous forwarding with line concatenation Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be enabled at a time.

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			1	CSI1_RR_FWD	RW	1	Enable best-effort forwarding for CSI output port 1. When this mode is enabled, no attempt is made to synchronize the video traffic. When multiple sources have data available to forward, the data will tend to be forwarded in a round-robin fashion. 0: Round robin forwarding disabled 1: Round robin forwarding enabled Only one of CSI1_RR_FWD and CSI1_SYNC_FWD must be enabled at a time.
			0	CSI0_RR_FWD	RW	1	Enable best-effort forwarding for CSI output port 0. When this mode is enabled, no attempt is made to synchronize the video traffic. When multiple sources have data available to forward, the data will tend to be forwarded in a round-robin fashion. 0: Round robin forwarding disabled 1: Round robin forwarding enabled Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be enabled at a time.
Share	0x22	FWD_STS	7:4	RESERVED	R	0x0	Reserved
			3	FWD_SYNC_FAIL1	R/COR	0	Forwarding synchronization failed for CSI output port 1 During Synchronized forwarding, this flag indicates a failure of synchronized video has been detected. For this bit to be set, the forwarding process must have previously been successful at sending at least one synchronized video frame. 0: No failure 1: Synchronization failure This bit is cleared on read.
			2	FWD_SYNC_FAIL0	R/COR	0	Forwarding synchronization failed for CSI output port 0 During Synchronized forwarding, this flag indicates a failure of synchronized video has been detected. For this bit to be set, the forwarding process must have previously been successful at sending at least one synchronized video frame. 0: No failure 1: Synchronization failure This bit is cleared on read.
			1	FWD_SYNC1	R	0	Forwarding synchronized for CSI output port 1 During Synchronized forwarding, this bit indicates that the forwarding engine is currently able to provide synchronized video from enabled Receive ports. This bit will always be 0 if Synchronized forwarding is disabled. 0: Video is not synchronized 1: Video is synchronized
			0	FWD_SYNC0	R	0	Forwarding synchronized for CSI output port 0 During Synchronized forwarding, this bit indicates that the forwarding engine is currently able to provide synchronized video from enabled Receive ports. This bit will always be 0 if Synchronized forwarding is disabled. 0: Video is not synchronized 1: Video is synchronized
Share	0x23	INTERRUPT_CTL	7	INT_EN	RW	0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			6	RESERVED	R	0	Reserved
			5	IE_CSI_TX1	RW	0	CSI Transmit Port 1 Interrupt: Enable interrupt from CSI Transmitter Port 1.
			4	IE_CSI_TX0	RW	0	CSI Transmit Port 1 Interrupt: Enable interrupt from CSI Transmitter Port 0.
			3	IE_RX3	RW	0	RX Port 3 Interrupt: Enable interrupt from Receiver Port 3.
			2	IE_RX2	RW	0	RX Port 2 Interrupt: Enable interrupt from Receiver Port 2.
			1	IE_RX1	RW	0	RX Port 1 Interrupt: Enable interrupt from Receiver Port 1.
			0	IE_RX0	RW	0	RX Port 0 Interrupt: Enable interrupt from Receiver Port 0.
Share	0x24	INTERRUPT_STS	7	INT	R	0	Global Interrupt: Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INT_EN bit in the INTERRUPT_CTL register but does depend on the IE_xxx bits. For example, if IE_RX0 and IS_RX0 are both asserted, the INT bit is set to 1.
			6	RESERVED	R	0	Reserved
			5	IS_CSI_TX1	R	0	CSI Transmit Port 1 Interrupt: An interrupt has occurred for CSI Transmitter Port 1. This interrupt is cleared upon reading the CSI_TX_ISR register for CSI Transmit Port 1.
			4	IS_CSI_TX0	R	0	CSI Transmit Port 0 Interrupt: An interrupt has occurred for CSI Transmitter Port 0. This interrupt is cleared upon reading the CSI_TX_ISR register for CSI Transmit Port 0.
			3	IS_RX3	R	0	RX Port 3 Interrupt: This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
			2	IS_RX2	R	0	RX Port 2 Interrupt: An interrupt has occurred for Receive Port 2. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
			1	IS_RX1	R	0	RX Port 1 Interrupt: 0x An interrupt has occurred for Receive Port 1. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
			0	IS_RX0	R	0	RX Port 0 Interrupt: An interrupt has occurred for Receive Port 0. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x25	TS_CONFIG	7	RESERVED	R	0	Reserved
			6	FS_POLARITY	RW	0	Framesync Polarity Indicates active edge of FrameSync signal 0: Rising edge 1: Falling edge
			5:4	TS_RES_CTL	RW	0x0	Timestamp Resolution Control 00: 40 ns 01: 80 ns 10: 160 ns 11: 1.0 us
			3	TS_AS_AVAIL	RW	0	Timestamp Ready Control 0: Normal operation 1: Indicate timestamps ready as soon as all port timestamps are available
			2	RESERVED	R	0	Reserved
			1	TS_FREERUN	RW	0	FreeRun Mode 0: FrameSync mode 1: FreeRun mode
			0	TS_MODE	RW	0	Timestamp Mode 0: Line start 1: Frame start
Share	0x26	TS_CONTROL	7:5	RESERVED	R	0x0	Reserved
			4	TS_FREEZE	RW	0	Freeze Timestamps 0: Normal operation 1: Freeze timestamps Setting this bit will freeze timestamps and clear the TS_READY flag. The TS_FREEZE bit should be cleared after reading timestamps to resume operation.
			3	TS_ENABLE3	RW	0	Timestamp Enable RX Port 3 0: Disabled 1: Enabled
			2	TS_ENABLE2	RW	0	Timestamp Enable RX Port 2 0: Disabled 1: Enabled
			1	TS_ENABLE1	RW	0	Timestamp Enable RX Port 1 0: Disabled 1: Enabled
			0	TS_ENABLE0	RW	0	Timestamp Enable RX Port 0 0: Disabled 1: Enabled
Share	0x27	TS_LINE_HI	7:0	TS_LINE_HI	RW	0x0	Timestamp Line, upper 8 bits This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number should be set to a value greater than 1. During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start
Share	0x28	TS_LINE_LO	7:0	TS_LINE_LO	RW	0x0	Timestamp Line, lower 8 bits This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number should be set to a value greater than 1. During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start
Share	0x29	TS_STATUS	7:5	RESERVED	R	0x0	Reserved

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			4	TS_READY	R	0	Timestamp Ready This flag indicates when timestamps are ready to be read. This flag is cleared when the TS_FREEZE bit is set.
			3	TS_VALID3	R	0	Timestamp Valid, RX Port 3
			2	TS_VALID2	R	0	Timestamp Valid, RX Port 2
			1	TS_VALID1	R	0	Timestamp Valid, RX Port 1
			0	TS_VALID0	R	0	Timestamp Valid, RX Port 0
Share	0x2A	TIMESTAMP_P0_HI	7:0	TIMESTAMP_P0_HI	R	0x0	Timestamp, upper 8 bits, RX Port 0
Share	0x2B	TIMESTAMP_P0_LO	7:0	TIMESTAMP_P0_LO	R	0x0	Timestamp, lower 8 bits, RX Port 0
Share	0x2C	TIMESTAMP_P1_HI	7:0	TIMESTAMP_P1_HI	R	0x0	Timestamp, upper 8 bits, RX Port 1
Share	0x2D	TIMESTAMP_P1_LO	7:0	TIMESTAMP_P1_LO	R	0x0	Timestamp, lower 8 bits, RX Port 1
Share	0x2E	TIMESTAMP_P2_HI	7:0	TIMESTAMP_P2_HI	R	0x0	Timestamp, upper 8 bits, RX Port 2
Share	0x2F	TIMESTAMP_P2_LO	7:0	TIMESTAMP_P2_LO	R	0x0	Timestamp, lower 8 bits, RX Port 2
Share	0x30	TIMESTAMP_P3_HI	7:0	TIMESTAMP_P3_HI	R	0x0	Timestamp, upper 8 bits, RX Port 3
Share	0x31	TIMESTAMP_P3_LO	7:0	TIMESTAMP_P3_LO	R	0x0	Timestamp, lower 8 bits, RX Port 3
Share	0x32	CSI_PORT_SEL	7:5	RESERVED	R	0x0	Reserved
			4	TX_READ_PORT	RW	0	Select TX port for register read This field selects one of the two TX port register blocks for readback. This applies to the subsequent registers prefixed "CSI". 0: Port 0 registers 1: Port 1 registers
			3:2	RESERVED	R	0x0	Reserved
			1	TX_WRITE_PORT_1	RW	0	Write Enable for TX port 1 registers This bit enables writes to TX port 1 registers. Any combination of TX port registers can be written simultaneously. This applies to the subsequent registers prefixed "CSI". 0: Writes disabled 1: Writes enabled
			0	TX_WRITE_PORT_0	RW	0	Write Enable for TX port 0 registers This bit enables writes to TX port 0 registers. Any combination of TX port registers can be written simultaneously. This applies to the subsequent registers prefixed "CSI". 0: Writes disabled 1: Writes enabled
CSI	0x33	CSI_CTL	7	RESERVED	R	0	Reserved
			6	CSI_CAL_EN	RW	0	Enable initial CSI Skew-Calibration sequence When the initial skew-calibration sequence is enabled, the CSI Transmitter will send the sequence at initialization, prior to sending any HS data. This bit should be set when operating at 1.6 Gbps CSI speed (as configured in the CSI_PLL register). 0: Disabled 1: Enabled
			5:4	CSI_LANE_COUNT	RW	0x0	CSI lane count 00: 4 lanes 01: 3 lanes 10: 2 lanes 11: 1 lane

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			3:2	CSI_ULP	RW	0	Force LP00 state on data/clock lanes 00: Normal operation 01: LP00 state forced only on data lanes 10: Reserved 11: LP00 state forced on data and clock lanes
			1	CSI_CONTS_CLOCK	RW	0	Enable CSI continuous clock mode 0: Disabled 1: Enabled
			0	CSI ENABLE	RW	0	Enable CSI output 0: Disabled 1: Enabled
CSI	0x34	CSI_CTL2	7:4	RESERVED	R	0x0	Reserved
			3	CSI_PASS_MODE	RW	0	CSI PASS indication mode Determines whether the CSI Pass indication is for a single port or all enabled ports. 0 : Assert PASS if at least one enabled Receive port is providing valid video data 1 : Assert PASS only if ALL enabled Receive ports are providing valid video data
			2	CSI_CAL_INV	RW	0	CSI Calibration Inverted Data pattern During the CSI skew-calibration pattern, the CSI Transmitter will send a sequence of 01010101 data (first bit 0). Setting this bit to a 1 will invert the sequence to 10101010 data.
			1	CSI_CAL_SINGLE	RW	0	Enable single periodic CSI Skew-Calibration sequence Setting this bit will send a single skew-calibration sequence from the CSI Transmitter. The skew-calibration sequence is the 1010 bit sequence required for periodic calibration. The calibration sequence is sent at the next idle period on the CSI interface. This bit is self-clearing and will reset to 0 after the calibration sequence is sent.
			0	CSI_CAL_PERIODIC	RW	0	Enable periodic CSI Skew-Calibration sequence When the periodic skew-calibration sequence is enabled, the CSI Transmitter will send the periodic skew-calibration sequence following the sending of Frame End packets. 0: Disabled 1: Enabled
CSI	0x35	CSI_STS	7:5	RESERVED	R	0x0	Reserved
			4	TX_PORT_NUM	R	0	TX Port Number This read-only field indicates the number of the currently selected TX read port.
			3:2	RESERVED	R	0x0	Reserved
			1	TX_PORT_SYNC	R	0	TX Port Synchronized This bit indicates the CSI Transmit Port is able to properly synchronize input data streams from multiple sources. This bit is 0 if synchronization is disabled via the FWD_CTL2 register. 0 : Input streams are not synchronized 1 : Input streams are synchronized

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			0	TX_PORT_PASS	R	0	TX Port Pass Indicates valid data is available on at least one port, or on all ports if configured for all port status via the CSI_PASS_MODE bit in the CSI_CTL2 register. The function differs based on mode of operation. In asynchronous operation, the TX_PORT_PASS indicates the CSI port is actively delivering valid video data. The status is cleared based on detection of an error condition that interrupts transmission. During Synchronized forwarding, the TX_PORT_PASS indicates valid data is available for delivery on the CSI TX output. Data may not be delivered if ports are not synchronized. The TX_PORT_SYNC status is a better indicator that valid data is being delivered to the CSI transmit port.
CSI	0x36	CSI_TX_ICR	7:5	RESERVED	R	0x0	Reserved
			4	IE_RX_PORT_INT	RW	0	RX Port Interrupt Enable Enable interrupt based on receiver port interrupt for the RX Ports being forwarded to the CSI Transmit Port.
			3	IE_CSI_SYNC_ERROR	RW	0	CSI Sync Error interrupt Enable Enable interrupt on CSI Synchronization enable.
			2	IE_CSI_SYNC	RW	0	CSI Synchronized interrupt Enable Enable interrupts on CSI Transmit Port assertion of CSI Synchronized Status.
			1	IE_CSI_PASS_ERROR	RW	0	CSI RX Pass Error interrupt Enable Enable interrupt on CSI Pass Error
			0	IE_CSI_PASS	RW	0	CSI Pass interrupt Enable Enable interrupt on CSI Transmit Port assertion of CSI Pass.
CSI	0x37	CSI_TX_ISR	7:5	RESERVED	R	0x0	Reserved
			4	IS_RX_PORT_INT	R/COR	0	RX Port Interrupt A Receiver port interrupt has been generated for one of the RX Ports being forwarded to the CSI Transmit Port. A read of the associated port receive status registers will clear this interrupt. See the PORT_ISR_HI and PORT_ISR_LO registers for details.
			3	IS_CSI_SYNC_ERROR	R/COR	0	CSI Sync Error interrupt A synchronization error has been detected for multiple video stream inputs to the CSI Transmitter.
			2	IS_CSI_SYNC	R/COR	0	CSI Synchronized interrupt CSI Transmit Port assertion of CSI Synchronized Status. Current status for CSI Sync can be read from the TX_PORT_SYNC flag in the CSI_STS register.
			1	IS_CSI_PASS_ERROR	R/COR	0	CSI RX Pass Error interrupt A deassertion of CSI Pass has been detected on one of the RX Ports being forwarded to the CSI Transmit Port
			0	IS_CSI_PASS	R/COR	0	CSI Pass interrupt CSI Transmit Port assertion of CSI Pass detected. Current status for the CSI Pass indication can be read from the TX_PORT_PASS flag in the CSI_STS register

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x42	AEQ_CTL	7	RESERVED	R	0	Reserved
			6:4	AEQ_ERR_CTL		0x0	AEQ Error Control Setting any of these bits will enable FPD3 error checking during the Adaptive Equalization process. Errors are accumulated over 1/2 of the period of the timer set by the ADAPTIVE_EQ_RELOCK_TIME filed in the AEQ_TEST register. If the number of errors is greater than the programmed threshold (AEQ_ERR_THOLD), the AEQ will attempt to increase the EQ setting. The errors may also be checked as part of EQ setting validation if AEQ_2STEP_EN is set. The following errors are checked based on this three bit field: [2] FPD3 clk1/clk0 errors [1] DCA sequence errors [0] Parity errors
			3	RESERVED	RW	0	Reserved
			2	AEQ_2STEP_EN	RW	0	AEQ 2-step enable This bit enables a two-step operation as part of the Adaptive EQ algorithm. If disabled, the state machine will wait for a programmed period of time, then check status to determine if setting is valid. If enabled, the state machine will wait for 1/2 the programmed period, then check for errors over an additional 1/2 the programmed period. If errors occur during the 2nd step, the state machine will immediately move to the next setting. 0 : Wait for full programmed delay, then check instantaneous lock value 1 : Wait for 1/2 programmed time, then check for errors over 1/2 programmed time. The programmed time is controlled by the ADAPTIVE_EQ_RELOCK_TIME field in the AEQ_TEST register
			1	AEQ_OUTER_LOOP	RW	0	AEQ outer loop control This bit controls whether the Equalizer or SFILTER adaption is the outer loop when the AEQ adaption includes SFILTER adaption. 0 : AEQ is inner loop, SFILTER is outer loop 1 : AEQ is outer loop, SFILTER is inner loop
			0	AEQ_SFILTER_EN	RW	1	Enable SFILTER Adaption with AEQ Setting this bit allows SFILTER adaption as part of the Adaptive Equalizer algorithm.
Share	0x43	AEQ_ERR_THOLD	7:0	AEQ_ERR_THRESHOLD	RW	0x1	AEQ Error Threshold This register controls the error threshold to determine when to re-adapt the EQ settings. This register should not be programmed to a value of 0.
Share	0x4C	FPD3_PORT_SEL	7:6	PHYS_PORT_NUM	R	0x0 Port#	Physical port number This field provides the physical port connection when reading from a remote device via the Bi-directional Control Channel. When accessed via local I2C interfaces, the value returned is always 0. When accessed via Bi-directional Control Channel, the value returned is the port number of the Receive port connection.

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			5:4	RX_READ_PORT	RW	0x0 Port#	Select RX port for register read This field selects one of the four RX port register blocks for readback. This applies to all paged FPD3 Receiver port registers. 00: Port 0 registers 01: Port 1 registers 10: Port 2 registers 11: Port 3 registers When accessed via local I2C interfaces, the default setting is 0. When accessed via Bi-directional Control Channel, the default value is the port number of the Receive port connection.
			3	RX_WRITE_PORT_3	RW	0 1 for RX Port 3	Write Enable for RX port 3 registers This bit enables writes to RX port 3 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bi-directional Control Channel, the default value is 1 if accessed over RX port 3.
			2	RX_WRITE_PORT_2	RW	0 1 for RX Port 2	Write Enable for RX port 2 registers This bit enables writes to RX port 2 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bi-directional Control Channel, the default value is 1 if accessed over RX port 2.
			1	RX_WRITE_PORT_1	RW	0 1 for RX Port 1	Write Enable for RX port 1 registers This bit enables writes to RX port 1 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bi-directional Control Channel, the default value is 1 if accessed over RX port 1.
			0	RX_WRITE_PORT_0	RW	0 1 for RX Port 0	Write Enable for RX port 0 registers This bit enables writes to RX port 0 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bi-directional Control Channel, the default value is 1 if accessed over RX port 0.
RX	0x4D	RX_PORT_STS1	7:6	RX_PORT_NUM	R	0x0	RX Port Number This read-only field indicates the number of the currently selected RX read port.
			5	BCC_CRC_ERROR	R/COR	0	Bi-directional Control Channel CRC Error Detected This bit indicates a CRC error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read.

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			4	LOCK_STS_CHG	R/COR	0	Lock Status Changed This bit is set if a change in receiver lock status has been detected since the last read of this register. Current lock status is available in the LOCK_STS bit of this register This bit is cleared on read.
			3	BCC_SEQ_ERROR	R/COR	0	Bi-directional Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read.
			2	PARITY_ERROR	R	0	FPD3 parity errors detected This flag is set when the number of parity errors detected is greater than the threshold programmed in the PAR_ERR_THOLD registers. 1: Number of FPD3 parity errors detected is greater than the threshold 0: Number of FPD3 parity errors is below the threshold This bit is cleared when the RX_PAR_ERR_HI/LO registers are cleared.
			1	PORT_PASS	R	0	Receiver PASS indication This bit indicates the current status of the Receiver PASS indication. The requirements for setting the Receiver PASS indication are controlled by the PORT_PASS_CTL register. 1: Receive input has met PASS criteria 0: Receive input does not meet PASS criteria
			0	LOCK_STS	R	0	FPD-Link III receiver is locked to incoming data 1: Receiver is locked to incoming data 0: Receiver is not locked
RX	0x4E	RX_PORT_STS2	7	LINE_LEN_UNSTABLE	R/COR	0	Line Length Unstable If set, this bit indicates the line length was detected as unstable during a previous video frame. The line length is considered to be stable if all the lines in the video frame have the same length. This flag will remain set until read.
			6	LINE_LEN_CHG	R/COR	0	Line Length Changed 1: Change of line length detected 0: Change of line length not detected This bit is cleared on read.
			5	FPD3_ENCODE_ERROR	R/COR	0	FPD3 Encoder error detected If set, this flag indicates an error in the FPD-Link III encoding has been detected by the FPD-Link III receiver. This bit is cleared on read. Note, to detect FP3 Encoder errors, the LINK_ERROR_COUNT must be enabled with a LINK_ERR_THRESH value greater than 1. Otherwise, the loss of Receiver Lock will prevent detection of the Encoder error.
			4	BUFFER_ERROR	R/COR	0	Packet buffer error detected. If this bit is set, an overflow condition has occurred on the packet buffer FIFO. 1: Packet Buffer error detected 0: No Packet Buffer errors detected This bit is cleared on read.
			3	RESERVED	R	0	Reserved

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			2	FREQ_STABLE	R	0	Frequency measurement stable
			1	NO_FPD3_CLK	R	0	No FPD-Link III input clock detected
			0	LINE_CNT_CHG	R/COR	0	Line Count Changed 1: Change of line count detected 0: Change of line count not detected This bit is cleared on read.
RX	0x4F	RX_FREQ_HIGH	7:0	FREQ_CNT_HIGH	R	0x0	Frequency Counter High Byte (MHz) The Frequency counter reports the measured frequency for the FPD3 Receiver. This portion of the field is the integer value in MHz.
RX	0x50	RX_FREQ_LOW	7:0	FREQ_CNT_LOW	R	0x0	Frequency Counter Low Byte (1/256 MHz) The Frequency counter reports the measured frequency for the FPD3 Receiver. This portion of the field is the fractional value in 1/256 MHz.
RX	0x55	RX_PAR_ERR_HI	7:0	PAR ERROR BYTE 1	R	0x0	Number of FPD3 parity errors – 8 most significant bits The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register is cleared upon reading the RX_PAR_ERR_LO register.
RX	0x56	RX_PAR_ERR_LO	7:0	PAR ERROR BYTE 0	R	0x0	Number of FPD3 parity errors – 8 least significant bits The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register is cleared on read.
RX	0x57	BIST_ERR_COUNT	7:0	BIST ERROR COUNT	R	0x0	Bist Error Count Returns BIST error count
RX	0x58	BCC_CONFIG	7	I2C PASS THROUGH ALL	RW	0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
			6	I2C PASS THROUGH	RW	0	I2C Pass-Through to Serializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled
			5	AUTO ACK ALL	RW	0	Automatically Acknowledge all I2C writes independent of the forward channel lock state or status of the remote Acknowledge 1: Enable 0: Disable
			4	BC_ALWAYS_ON	RW	1	Back channel enable 1: Back channel is always enabled independent of I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL 0: Back channel enable requires setting of either I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL This bit may only be written via a local I2C master.

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			3	BC CRC GENERATOR ENABLE	RW	1	Back Channel CRC Generator Enable 0: Disable 1: Enable
			2:0	BC FREQ SELECT	RW, Strap	0x0	Back Channel Frequency Select 000: 2.5 Mbps (default for DS90UB913AQ/913Q/933Q compatibility) 001: 1.5625 Mbps 010 - 111 : Reserved Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Deserializer should first be programmed to Auto-Ack operation to avoid a control channel timeout due to lack of response from the Serializer.
RX	0x59	RESERVED	7:0	RESERVED	RW	0x0	Reserved
RX	0x5A	RESERVED	7:0	RESERVED	RW	0x0	Reserved
RX	0x5B	SER_ID	7:1	SER ID	RW	0x0	Remote Serializer ID This field is normally loaded automatically from the remote Serializer.
			0	FREEZE DEVICE ID	RW	0	Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID is frozen at the value written.
RX	0x5C	SER_ALIAS_ID	7:1	SER ALIAS ID	RW	0x0	7-bit Remote Serializer Alias ID Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction is remapped to the address specified in the Slave ID register. A value of 0 in this field disables access to the remote I2C Slave.
			0	SER AUTO ACK	RW	0	Automatically Acknowledge all I2C writes to the remote Serializer independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable
RX	0x5D	SlaveID[0]	7:1	SLAVE ID0	RW	0x0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
			0	RESERVED	R	0	Reserved.
RX	0x5E	SlaveID[1]	7:1	SLAVE ID1	RW	0x0	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
			0	RESERVED	R	0	Reserved.

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
RX	0x5F	SlaveID[2]	7:1	SLAVE ID2	RW	0x0	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
			0	RESERVED	R	0	Reserved.
RX	0x60	SlaveID[3]	7:1	SLAVE ID3	RW	0x0	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
			0	RESERVED	R	0	Reserved.
RX	0x61	SlaveID[4]	7:1	SLAVE ID4	RW	0x0	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
			0	RESERVED	R	0	Reserved.
RX	0x62	SlaveID[5]	7:1	SLAVE ID5	RW	0x0	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
			0	RESERVED	R	0	Reserved.
RX	0x63	SlaveID[6]	7:1	SLAVE ID6	RW	0x0	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
			0	RESERVED	R	0	Reserved.
RX	0x64	SlaveID[7]	7:1	SLAVE ID7	RW	0x0	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
			0	RESERVED	R	0	Reserved.

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
RX	0x65	SlaveAlias[0]	7:1	SLAVE ALIAS ID0	RW	0x0	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
			0	SLAVE AUTO ACK 0	RW	0	Automatically Acknowledge all I2C writes to the remote Slave 0 independent of the forward channel lock state or status of the remote Serializer Acknowledge1: Enable0: Disable
RX	0x66	SlaveAlias[1]	7:1	SLAVE ALIAS ID1	RW	0x0	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
			0	SLAVE AUTO ACK 1	RW	0	Automatically Acknowledge all I2C writes to the remote Slave 1 independent of the forward channel lock state or status of the remote Serializer Acknowledge1: Enable0: Disable
RX	0x67	SlaveAlias[2]	7:1	SLAVE ALIAS ID2	RW	0x0	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
			0	SLAVE AUTO ACK 2	RW	0	Automatically Acknowledge all I2C writes to the remote Slave 2 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable
RX	0x68	SlaveAlias[3]	7:1	SLAVE ALIAS ID3	RW	0x0	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.
			0	SLAVE AUTO ACK 3	RW	0	Automatically Acknowledge all I2C writes to the remote Slave 3 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable
RX	0x69	SlaveAlias[4]	7:1	SLAVE ALIAS ID4	RW	0x0	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			0	SLAVE AUTO ACK 4	RW	0	Automatically Acknowledge all I2C writes to the remote Slave 4 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable
RX	0x6A	SlaveAlias[5]	7:1	SLAVE ALIAS ID5	RW	0x0	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
			0	SLAVE AUTO ACK 5	RW	0	Automatically Acknowledge all I2C writes to the remote Slave 5 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable
RX	0x6B	SlaveAlias[6]	7:1	SLAVE ALIAS ID6	RW	0x0	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
			0	SLAVE AUTO ACK 6	RW	0	Automatically Acknowledge all I2C writes to the remote Slave 6 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable
RX	0x6C	SlaveAlias[7]	7:1	SLAVE ALIAS ID7	RW	0x0	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
			0	SLAVE AUTO ACK 7	RW	0	Automatically Acknowledge all I2C writes to the remote Slave 7 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable
RX	0x6D	PORT_CONFIG	7:4	RESERVED	RW	0x7	Reserved
			3	DISCARD_1ST_LINE_ON_ERR	RW	1	In RAW Mode, Discard first video line if FV to LV setup time is not met. 0 : Forward truncated 1st video line 1 : Discard truncated 1st video line
			2	COAX_MODE	RW	Strap	Enable coax cable mode 0: Shielded twisted pair (STP) mode 1: Coax mode

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			1:0	FPD3_MODE	RW	Strap	FPD3 Input Mode 00: Reserved 01: RAW12 Low Frequency Mode (DS90UB913AQ/913Q/933Q compatible) 10: RAW12 High Frequency Mode(DS90UB913AQ/913Q/933Q compatible) 11: RAW10 Mode (DS90UB913AQ/913Q/933Q compatible)
RX	0x6E	BC_GPIO_CTL0	7:4	BC_GPIO1_SEL	RW	0x8	Back channel GPIO1 Select: Determines the data sent on GPIO1 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO1_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved
			3:0	BC_GPIO0_SEL	RW	0x8	Back channel GPIO0 Select: Determines the data sent on GPIO0 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO0_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved
RX	0x6F	BC_GPIO_CTL1	7:4	BC_GPIO3_SEL	RW	0x8	Back channel GPIO3 Select: Determines the data sent on GPIO3 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO3_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved
			3:0	BC_GPIO2_SEL	RW	0x8	Back channel GPIO2 Select: Determines the data sent on GPIO2 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO2_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved
RX	0x70	RAW10_ID	7:6	RAW10_VC	RW	<RX Port #>	RAW10 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW10 data. The field value defaults to the FPD-Link III receive port number (0, 1, 2, or 3)
			5:0	RAW10_DT	RW	0x2B	RAW10 DT This field configures the CSI data type used in RAW10 mode. The default of 0x2B matches the CSI specification.
RX	0x71	RAW12_ID	7:6	RAW12_VC	RW	<RX Port #>	RAW12 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW12 data. The field value defaults to the FPD-Link III receive port number (0, 1, 2, or 3)

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			5:0	RAW12_DT	RW	0x2C	RAW12 DT This field configures the CSI data type used in RAW12 mode. The default of 0x2C matches the CSI specification.
RX	0x72	RESERVED	7:0	Reserved	RW	0x0	Reserved
RX	0x73	LINE_COUNT_1	7:0	LINE_COUNT_HI	R	0x0	High byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value is frozen until read.
RX	0x74	LINE_COUNT_0	7:0	LINE_COUNT_LO	R	0x0	Low byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value is frozen until read. In addition, when reading the LINE_COUNT registers, the LINE_COUNT_LO is latched upon reading LINE_COUNT_HI to ensure consistency between the two portions of the Line Count.
RX	0x75	LINE_LEN_1	7:0	LINE_LEN_HI	R	0	High byte of Line Length The Line Length reports the line length recorded during the most recent video frame. If line length is not stable during the frame, this register will report the length of the last line in the video frame. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value is frozen until read.
RX	0x76	LINE_LEN_0	7:0	LINE_LEN_LO	R	0	Low byte of Line Length The Line Length reports the lenth of the most recent video line. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value is frozen until read. In addition, when reading the LINE_LEN registers, the LINE_LEN_LO is latched upon reading LINE_LEN_HI to ensure consistency between the two portions of the Line Length.
RX	0x77	FREQ_DET_CTL	7:6	FREQ_HYST	RW	0x3	Frequency Detect Hysteresis The Frequency detect hysteresis setting allows ignoring minor fluctuations in frequency. A new frequency measurement will be captured only if the measured frequency differs from the current measured frequency by more than the FREQ_HYST setting. The FREQ_HYST setting is in MHz.
			5:4	FREQ_STABLE_THR	RW	0x0	Frequency Stable Threshold The Frequency detect circuit can be used to detect a stable clock frequency. The Stability Threshold determines the amount of time required for the clock frequency to stay within the FREQ_HYST range to be considered stable: 00 : 40us 01 : 80us 10 : 320us 11 : 1.28ms

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			3:0	FREQ_LO_THR	RW	0x5	Frequency Low Threshold Sets the low threshold for the Clock frequency detect circuit in MHz. This value is used to determine if the clock frequency is too low for proper operation.
RX	0x78	MAILBOX_1	7:0	MAILBOX_0	RW	0x0	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.
RX	0x79	MAILBOX_2	7:0	MAILBOX_1	RW	0x01	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.
RX	0x7C	PORT_CONFIG2	7:6	RAW10_8BIT_CTL	RW	0x0	Raw10 8-bit mode When Raw10 Mode is enabled for the port, the input data is processed as 8-bit data and packed accordingly for transmission over CSI. 00 : Normal Raw10 Mode 01 : Reserved 10 : 8-bit processing using upper 8 bits 11 : 8-bit processing using lower 8 bits
			5	DISCARD_ON_PAR_ERR	RW	0	Discard frames on Parity Error 0 : Forward packets with parity errors 1 : Truncate Frames if a parity error is detected
			4	DISCARD_ON_LINE_SIZE	RW	0	Discard frames on Line Size 0 : Allow changes in Line Size within packets 1 : Truncate Frames if a change in line size is detected
			3	DISCARD_ON_FRAME_SIZE	RW	0	Discard frames on change in Frame Size When enabled, a change in the number of lines in a frame will result in truncation of the packet. The device will resume forwarding video frames based on the PASS_THRESHOLD setting in the PORT_PASS_CTL register. 0 : Allow changes in Frame Size 1 : Truncate Frames if a change in frame size is detected
			2	RESERVED	RW	0	Reserved
			1	LV_POLARITY	RW	0	LineValid Polarity This register indicates the expected polarity for the LineValid indication received in Raw mode. 1 : LineValid is low for the duration of the video frame 0 : LineValid is high for the duration of the video frame
			0	FV_POLARITY	RW	0	FrameValid Polarity This register indicates the expected polarity for the FrameValid indication received in Raw mode. 1 : FrameValid is low for the duration of the video frame 0 : FrameValid is high for the duration of the video frame
RX	0x7D	PORT_PASS_CTL	7	PASS_DISCARD_EN	RW	0	Pass Discard Enable Discard packets if PASS is not indicated. 0 : Ignore PASS for forwarding packets 1 : Discard packets when PASS is not true

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			6	PASS_FREEZE	RW	0	Pass Freeze Control This register controls whether the device will include video freeze detection in qualification of the Pass indication: 0 : Ignore video freeze detection 1 : Include video freeze detection When enabled, Pass is deasserted upon detection of a frozen image based on the controls in the VIDEO_FREEZE register. Pass will not be reasserted until a new video image is detected and the PASS_THRESHOLD setting is met.
			5	PASS_LINE_CNT	RW	0	Pass Line Count Control This register controls whether the device will include line count in qualification of the Pass indication: 0 : Don't check line count 1 : Check line count When checking line count, Pass is deasserted upon detection of a change in the number of video lines per frame. Pass will not be reasserted until the PASS_THRESHOLD setting is met.
			4	PASS_LINE_SIZE	RW	0	Pass Line Size Control This register controls whether the device will include line size in qualification of the Pass indication: 0 : Don't check line size 1 : Check line size When checking line size, Pass is deasserted upon detection of a change in video line size. Pass will not be reasserted until the PASS_THRESHOLD setting is met.
			3	PASS_PARITY_ERR	RW	0	Parity Error Mode If this bit is set to 0, the port Pass indication is deasserted for every parity error detected on the FPD3 Receive interface. If this bit is set to a 1, the port Pass indication is cleared on a parity error and remain clear until the PASS_THRESHOLD is met.
			2	PASS_WDOG_DIS	RW	0	RX Port Pass Watchdog disable When enabled, if the FPD Receiver does not detect a valid frame end condition within two video frame periods, the Pass indication is deasserted. The watchdog timer will not have any effect if the PASS_THRESHOLD is set to 0. 0 : Enable watchdog timer for RX Pass 1 : Disable watchdog timer for RX Pass
			1:0	PASS_THRESHOLD	RW	0x0	Pass Threshold Register This register controls the number of valid frames before asserting the port Pass indication. If set to 0, PASS is asserted after Receiver Lock detect. If non-zero, PASS is asserted following reception of the programmed number of valid frames.
Share	0xB0	IND_ACC_CTL	7:6	RESERVED	R	0x0	Reserved

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			5:2	IA_SEL	RW	0x0	Indirect Access Register Select: Selects target for register access 0000 : CSI-2 Pattern Generator & Timing Registers (See Table 14) 0001 : FPD3 RX Port 0 Reserved Registers 0010 : FPD3 RX Port 1 Reserved Registers 0011 : FPD3 RX Port 2 Reserved Registers 0100 : FPD3 RX Port 3 Reserved Registers 0101 : FPD3 RX Shared Reserved Registers 0110 : Simultaneous write to FPD3 RX Reserved Registers 0111 : CSI-2 Reserved Registers
			1	IA_AUTO_INC	RW	0	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1
			0	IA_READ	RW	0	Indirect Access Read: Setting this allows generation of a read strobe to the selected register block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes will also be asserted following a read of the IND_ACC_DATA register. This function is only required for blocks that need to pre-fetch register data.
Share	0xB1	IND_ACC_ADDR	7:0	IA_ADDR	RW	0x0	Indirect Access Register Offset: This register contains the 8-bit register offset for the indirect access.
Share	0xB2	IND_ACC_DATA	7:0	IA_DATA	RW	0x0	Indirect Access Data: Writing this register will cause an indirect write of the IND_ACC_DATA value to the selected analog block register. Reading this register will return the value of the selected block register
Share	0xB3	BIST Control	7:6	BIST_OUT_MODE	RW	0x0	BIST Output Mode 00 : No toggling 01 : Alternating 1/0 toggling 1x : Toggle based on BIST data
			5:4	RESERVED	RW	0x0	Reserved
			3	BIST PIN CONFIG	RW	1	Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through bits 2:0 in this register
			2:1	BIST CLOCK SOURCE	RW	0	BIST Clock Source This register field selects the BIST Clock Source at the Serializer. These register bits are automatically written to the CLOCK SOURCE bits (register offset 0x14) in the Serializer after BIST is enabled. See the appropriate Serializer register descriptions for details.
			0	BIST_EN	RW	0	BIST Control 1: Enabled 0: Disabled
Share	0xB8	MODE_IDX_STS	7	IDX_DONE	R	1	IDX Done If set, indicates the IDX decode has completed and latched into the IDX status bits.
			6:4	IDX	R	Strap	IDX Decode 3-bit decode from IDX pin

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			3	MODE_DONE	R	1	MODE Done If set, indicates the MODE decode has completed and latched into the MODE status bits.
			2:0	MODE	R	Strap	MODE Decode 3-bit decode from MODE pin
Share	0xB9	LINK_ERROR_COUNT	7:6	RESERVED	R	0x0	Reserved
			5	LINK_SFIL_WAIT	RW	0	During SFILTER adaption, setting this bit will cause the Lock detect circuit to ignore errors during the SFILTER wait period after the SFILTER control is updated. 1: Errors during SFILTER Wait period will be ignored 0: Errors during SFILTER Wait period will not be ignored and may cause loss of Lock
			4	LINK_ERR_COUNT_EN	RW	0	Enable serial link data integrity error count 1: Enable error count 0: DISABLE
			3:0	LINK_ERR_THRESH	RW	0x3	Link error count threshold. The Link Error Counter monitors the forward channel link and determines when link will be dropped. The link error counter is pixel clock based. clk0, clk1, parity, and DCA are monitored for link errors. If the error counter is enabled, the deserializer will lose lock once the error counter reaches the LINK_ERR_THRESH value. If the link error counter is disabled, the deserilizer will lose lock after one error. The control bits in DIGITAL_DEBUG_2 register can be used to disable error conditions individually.
Share	0xBC	FV_MIN_TIME	7:0	FRAME_VALID_MIN	RW	0x80	Frame Valid Minimum Time This register controls the minimum time the FrameValid (FV) should be active before the Raw mode FPD3 receiver generates a FrameStart packet. Duration is in FPD3 clock periods.
Share	0xBE	GPIO_PD_CTL	7	GPIO7_PD_DIS	RW	0	GPIO7 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
			6	GPIO6_PD_DIS	RW	0	GPIO6 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
			5	GPIO5_PD_DIS	RW	0	GPIO5 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			4	GPIO4_PD_DIS	RW	0	GPIO4 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
			3	GPIO3_PD_DIS	RW	0	GPIO3 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
			2	GPIO2_PD_DIS	RW	0	GPIO2 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
			1	GPIO1_PD_DIS	RW	0	GPIO1 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
			0	GPIO0_PD_DIS	RW	0	GPIO0 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
RX	0xD0	PORT_DEBUG	7	RESERVED	R	0	Reserved
			6	RESERVED	RW	0	Reserved
			5	SER_BIST_ACT	R	0	Serializer BIST active This register indicates the Serializer is in BIST mode. If the Deserializer is not in BIST mode, this could indicate an error condition.
			4:0	RESERVED	RW	0x0	Reserved
RX	0xD2	AEQ TEST	7:5	ADAPTIVE_EQ_RELOCK_TIME	RW	0x4	Time to wait for lock before incrementing the EQ to next setting 000 : 164 us 001 : 328 us 010 : 655 us 011 : 1.31 ms 100 : 2.62 ms 101 : 5.24 ms 110 : 10.5ms 111 : 21.0 ms

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			4	AEQ_1ST_LOCK_MODE	RW	0	AEQ First Lock Mode This register bit controls the Adaptive Equalizer algorithm operation at initial Receiver Lock. 0 : Initial AEQ lock may occur at any value 1 : Initial Receiver lock will restart AEQ at 0, providing a more deterministic initial AEQ value
			3	AEQ_RESTART	RW/SC	0	Set high to restart AEQ adaptation from initial value. This bit is self clearing. Adaption is restarted.
			2	SET_AEQ_FLOOR	RW	0	AEQ adaptation starts from a pre-set floor value rather than from zero - good in long cable situations
			1:0	RESERVED	R	0x0	Reserved
RX	0xD3	AEQ_STATUS	7:6	RESERVED	R	0x0	Reserved
			5:3	EQ_STATUS_1	R	0x0	Adaptive EQ Status 1
			2:0	EQ_STATUS_2	R	0x0	Adaptive EQ Status 2
RX	0xD4	ADAPTIVE EQ BYPASS	7:5	EQ STAGE 1 SELECT VALUE	RW	0x3	EQ select value [5:3] - Used if adaptive EQ is bypassed.
			4	AEQ_LOCK_MODE	RW	0	Adaptive Equalizer lock mode When set to a 1, Receiver Lock status requires the Adaptive Equalizer to complete adaption. When set to a 0, Receiver Lock is based only on the Lock circuit itself. AEQ may not have stabilized.
			3:1	EQ STAGE 2 SELECT VALUE	RW	0x0	EQ select value [2:0] - Used if adaptive EQ is bypassed.
			0	ADAPTIVE EQ BYPASS	RW	0	1: Disable adaptive EQ 0: Enable adaptive EQ
RX	0xD5	AEQ_MIN_MAX	7:4	AEQ_MAX	RW	0xF	Adaptive Equalizer Maximum value This register sets the maximum value for the Adaptive EQ algorithm.
			3:0	ADAPTIVE EQ FLOOR VALUE	RW	0x8	When AEQ floor is enabled by register {reg_35[5:4]} the starting setting is given by this register.
RX	0xD8	PORT_ICR_HI	7:2	RESERVED	R	0x0	Reserved
			2	IE_FPD3_ENC_ERR	RW	0	Interrupt on FPD-Link III Receiver Encoding Error When enabled, an interrupt is generated on detection of an encoding error on the FPD-Link III interface for the receive port as reported in the FPD3_ENC_ERROR bit in the RX_PORT_STS2 register
			1	IE_BCC_SEQ_ERR	RW	0	Interrupt on BCC SEQ Sequence Error When enabled, an interrupt is generated if a Sequence Error is detected for the Bi-directional Control Channel forward channel receiver as reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register.
			0	IE_BCC_CRC_ERR	RW	0	Interrupt on BCC CRC error detect When enabled, an interrupt is generated if a CRC error is detected on a Bi-directional Control Channel frame received over the FPD-Link III forward channel as reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register.
RX	0xD9	PORT_ICR_LO	7	RESERVED	RW	0	Reserved

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			6	IE_LINE_LEN_CHG	RW	0	Interrupt on Video Line length When enabled, an interrupt is generated if the length of the video line changes. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register.
			5	IE_LINE_CNT_CHG	RW	0	Interrupt on Video Line count When enabled, an interrupt is generated if the number of video lines per frame changes. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register.
			4	IE_BUFFER_ERR	RW	0	Interrupt on Receiver Buffer Error When enabled, an interrupt is generated if the Receive Buffer overflow is detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register.
			3	RESERVED	RW	0	Reserved
			2	IE_FPD3_PAR_ERR	RW	0	Interrupt on FPD-Link III Receiver Parity Error When enabled, an interrupt is generated on detection of parity errors on the FPD-Link III interface for the receive port. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register.
			1	IE_PORT_PASS	RW	0	Interrupt on change in Port PASS status When enabled, an interrupt is generated on a change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register.
			0	IE_LOCK_STS	RW	0	Interrupt on change in Lock Status When enabled, an interrupt is generated on a change in lock status. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register.
RX	0xDA	PORT_ISR_HI	7:3	Reserved	R	0x0	Reserved
			2	IS_FPD3_ENC_ERR	R	0	FPD-Link III Receiver Encode Error Interrupt Status An encoding error on the FPD-Link III interface for the receive port has been detected. Status is reported in the FPD3_ENC_ERROR bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
			1	IS_BCC_SEQ_ERR	R	0	BCC CRC Sequence Error Interrupt Status A Sequence Error has been detected for the Bi-directional Control Channel forward channel receiver. Status is reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
			0	IS_BCC_CRC_ERR	R	0	BCC CRC error detect Interrupt Status A CRC error has been detected on a Bi-directional Control Channel frame received over the FPD-Link III forward channel. Status is reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
RX	0xDB	PORT_ISR_LO	7	RESERVED	R	0	Reserved

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			6	IS_LINE_LEN_CHG	R	0	Video Line Length Interrupt Status A change in video line length has been detected. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
			5	IS_LINE_CNT_CHG	R	0	Video Line Count Interrupt Status A change in number of video lines per frame has been detected. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
			4	IS_BUFFER_ERR	R	0	Receiver Buffer Error Interrupt Status A Receive Buffer overflow has been detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register.This interrupt condition is cleared by reading the RX_PORT_STS2 register.
			3	RESERVED	R	0	Reserved
			2	IS_FPD3_PAR_ERR	R	0	FPD-Link III Receiver Parity Error Interrupt Status A parity error on the FPD-Link III interface for the receive port has been detected. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
			1	IS_PORT_PASS	R	0	Port Valid Interrupt Status A change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
			0	IS_LOCK_STS	R	0	Lock Interrupt Status A change in lock status has been detected. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
Share	0xF0	FPD3_RX_ID0	7:0	FPD3_RX_ID0	R	0x5F	FPD3_RX_ID0: First byte ID code: '_'
Share	0xF1	FPD3_RX_ID1	7:0	FPD3_RX_ID1	R	0x55	FPD3_RX_ID1: 2nd byte of ID code: 'U'
Share	0xF2	FPD3_RX_ID2	7:0	FPD3_RX_ID2	R	0x42	FPD3_RX_ID2: 3rd byte of ID code: 'B'
Share	0xF3	FPD3_RX_ID3	7:0	FPD3_RX_ID3	R	0x39	FPD3_RX_ID3: 4th byte of ID code: '9'
Share	0xF4	FPD3_RX_ID4	7:0	FPD3_RX_ID4	R	0x36	FPD3_RX_ID4: 5th byte of ID code: '6'
Share	0xF5	FPD3_RX_ID5	7:0	FPD3_RX_ID5	R	0x34	FPD3_RX_ID5: 6th byte of ID code: '4'
Share	0xF8	I2C_RX0_ID	7:1	RX_PORT0_ID	RW	0x0	7-bit Receive Port 0 I2C ID Configures the decoder for detecting transactions designated for Receiver port 0 registers. This provides a simpler method of accessing device registers specifically for port 0 without having to use the paging function to select the register page. A value of 0 in this field disables the Port0 decoder.
			0	RESERVED	R	0	Reserved

Register Maps (continued)

Table 12. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0xF9	I2C_RX1_ID	7:1	RX_PORT1_ID	RW	0x0	7-bit Receive Port 1 I2C ID Configures the decoder for detecting transactions designated for Receiver port 1 registers. This provides a simpler method of accessing device registers specifically for port 1 without having to use the paging function to select the register page. A value of 0 in this field disables the Port1 decoder.
			0	RESERVED	R	0	Reserved
Share	0xFA	I2C_RX2_ID	7:1	RX_PORT2_ID	RW	0x0	7-bit Receive Port 2 I2C ID Configures the decoder for detecting transactions designated for Receiver port 2 registers. This provides a simpler method of accessing device registers specifically for port 2 without having to use the paging function to select the register page. A value of 0 in this field disables the Port2 decoder.
			0	RESERVED	R	0	Reserved
Share	0xFB	I2C_RX3_ID	7:1	RX_PORT3_ID	RW	0x0	7-bit Receive Port 3 I2C ID Configures the decoder for detecting transactions designated for Receiver port 3 registers. This provides a simpler method of accessing device registers specifically for port 3 without having to use the paging function to select the register page. A value of 0 in this field disables the Port3 decoder.
			0	RESERVED	R	0	Reserved

8.7.1 Indirect Access Registers

Several functional blocks include register sets contained in the Indirect Access map (Table 13); i.e. Pattern Generator, CSI-2 timing, and Analog controls. Register access is provided via an indirect access mechanism through the Indirect Access registers (IND_ACC_CTL, IND_ACC_ADDR, and IND_ACC_DATA). These registers are located at offsets 0xB0-0xB2 in the main register space.

The indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Write the data value to the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 will write additional data bytes to subsequent register offset locations

For reads, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Read from the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 will read additional data bytes from subsequent register offset locations.

Table 13. Indirect Register Map Description

IA Select 0xB0[5:2]	Page/Block	Indirect Registers	Address Range	Description
0000	0	Digital Page 0 Indirect Registers	0x01-0x1F	Pattern Gen Registers
			0x40-0x51	CSI TX port 0 Timing Registers
			0x60-0x71	CSI TX port 1 Timing Registers
0001	1	FPD3 Channel 0 Reserved Registers	0x00-0x14	Reserved
0010	2	FPD3 Channel 1 Reserved Registers	0x00-0x14	Reserved
0011	3	FPD3 Channel 2 Reserved Registers	0x00-0x14	Reserved
0100	4	FPD3 Channel 3 Reserved Registers	0x00-0x14	Reserved
0101	5	FPD3 Share Reserved Registers	0x00-0x04	Reserved
0110	6	Write All FPD3 Reserved Registers	0x00-0x14	Reserved
0111	7	CSI TX Reserved Registers	0x00-0x1D	Reserved

Table 14. Digital Page 0 Indirect Registers

Indirect Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Block 0	0x00	Reserved	7:0	RESERVED	R	0x0	Reserved
	0x01	PGEN_CTL	7:1	RESERVED	RW	0x0	Reserved
			0	PGEN_ENABLE	RW	0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator
	0x02	PGEN_CFG	7	PGEN_FIXED_EN	RW	0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0 : Send Color Bar Pattern 1 : Send Fixed Color Pattern
			6	RESERVED	RW	0	Reserved
			5:4	NUM_CBARS	RW	0x3	Number of Color Bars 00 : 1 Color Bar 01 : 2 Color Bars 10 : 4 Color Bars 11 : 8 Color Bars
			3:0	BLOCK_SIZE	RW	0x3	Block Size For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 15.
	0x03	PGEN_CSI_DI	7:6	PGEN_CSI_VC	RW	0x0	CSI Virtual Channel Identifier This field controls the value sent in the CSI packet for the Virtual Channel Identifier
			5:0	PGEN_CSI_DT	RW	0x24	CSI Data Type This field controls the value sent in the CSI packet for the Data Type. The default value (0x24) indicates RGB888.
	0x04	PGEN_LINE_SIZE1	7:0	PGEN_LINE_SIZE[15:8]	RW	0x07	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.
	0x05	PGEN_LINE_SIZE0	7:0	PGEN_LINE_SIZE[7:0]	RW	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.
	0x06	PGEN_BAR_SIZE1	7:0	PGEN_BAR_SIZE[15:8]	RW	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.
	0x07	PGEN_BAR_SIZE0	7:0	PGEN_BAR_SIZE[7:0]	RW	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.
	0x08	PGEN_ACT_LPF1	7:0	PGEN_ACT_LPF[15:8]	RW	0x01	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.
	0x09	PGEN_ACT_LPF0	7:0	PGEN_ACT_LPF[7:0]	RW	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.
	0x0A	PGEN_TOT_LPF1	7:0	PGEN_TOT_LPF[15:8]	RW	0x02	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking
	0x0B	PGEN_TOT_LPF0	7:0	PGEN_TOT_LPF[7:0]	RW	0x0D	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

Table 14. Digital Page 0 Indirect Registers (continued)

Indirect Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
	0x0C	PGEN_LINE_PD1	7:0	PGEN_LINE_PD[15:8]	RW	0x0C	Line Period Most significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.
	0x0D	PGEN_LINE_PD0	7:0	PGEN_LINE_PD[7:0]	RW	0x67	Line Period Least significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.
	0x0E	PGEN_VBP	7:0	PGEN_VBP	RW	0x21	Vertical Back Porch This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.
	0x0F	PGEN_VFP	7:0	PGEN_VFP	RW	0x0A	Vertical Front Porch This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.
	0x10	PGEN_COLOR0	7:0	PGEN_COLOR0	RW	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0.For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.
	0x11	PGEN_COLOR1	7:0	PGEN_COLOR1	RW	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1.For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.
	0x12	PGEN_COLOR2	7:0	PGEN_COLOR2	RW	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2.For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.
	0x13	PGEN_COLOR3	7:0	PGEN_COLOR3	RW	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3.For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.
	0x14	PGEN_COLOR4	7:0	PGEN_COLOR4	RW	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4.For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.
	0x15	PGEN_COLOR5	7:0	PGEN_COLOR5	RW	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5.For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

Table 14. Digital Page 0 Indirect Registers (continued)

Indirect Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
	0x16	PGEN_COLOR6	7:0	PGEN_COLOR6	RW	0x0F	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6.For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.
	0x17	PGEN_COLOR7	7:0	PGEN_COLOR7	RW	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7.For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.
	0x18	PGEN_COLOR8	7:0	PGEN_COLOR8	RW	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.
	0x19	PGEN_COLOR9	7:0	PGEN_COLOR9	RW	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.
	0x1A	PGEN_COLOR10	7:0	PGEN_COLOR10	RW	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.
	0x1B	PGEN_COLOR11	7:0	PGEN_COLOR11	RW	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.
	0x1C	PGEN_COLOR12	7:0	PGEN_COLOR12	RW	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.
	0x1D	PGEN_COLOR13	7:0	PGEN_COLOR13	RW	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.
	0x1E	PGEN_COLOR14	7:0	PGEN_COLOR14	RW	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.
	0x1F	RESERVED	7:0	RESERVED	RW	0x0	Reserved
	0x40	CSI0_TCK_PREP	7	MR_TCK_PREP_OV	RW	0	Override CSI Tck-prep parameter 0: Tck-prep is automatically determined 1: Override Tck-prep with value in bits 6:0 of this register
			6:0	MR_TCK_PREP	R RW	0x0	Tck-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x41	CSI0_TCK_ZERO	7	MR_TCK_ZERO_OV	RW	0	Override CSI Tck-zero parameter 0: Tck-zero is automatically determined 1: Override Tck-zero with value in bits 6:0 of this register
			6:0	MR_TCK_ZERO	R RW	0x0	Tck-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

Table 14. Digital Page 0 Indirect Registers (continued)

Indirect Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
	0x42	CSI0_TCK_TRAIL	7	MR_TCK_TRAIL_OV	RW	0	Override CSI Tck-trail parameter 0: Tck-trail is automatically determined 1: Override Tck-trail with value in bits 6:0 of this register
			6:0	MR_TCK_TRAIL	R RW	0x0	Tck-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x43	CSI0_TCK_POST	7	MR_TCK_POST_OV	RW	0	Override CSI Tck-post parameter 0: Tck-post is automatically determined 1: Override Tck-post with value in bits 6:0 of this register
			6:0	MR_TCK_POST	R RW	0x0	Tck-post value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x44	CSI0_THS_PREP	7	MR_THS_PREP_OV	RW	0	Override CSI Ths-prep parameter 0: Ths-prep is automatically determined 1: Override Ths-prep with value in bits 6:0 of this register
			6:0	MR_THS_PREP	R RW	0x0	Ths-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x45	CSI0_THS_ZERO	7	MR_THS_ZERO_OV	RW	0	Override CSI Ths-zero parameter 0: Ths-zero is automatically determined 1: Override Ths-zero with value in bits 6:0 of this register
			6:0	MR_THS_ZERO	R RW	0x0	Ths-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x46	CSI0_THS_TRAIL	7	MR_THS_TRAIL_OV	RW	0	Override CSI Ths-trail parameter 0: Ths-trail is automatically determined 1: Override Ths-trail with value in bits 6:0 of this register
			6:0	MR_THS_TRAIL	R RW	0x0	Ths-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x47	CSI0_THS_EXIT	7	MR_THS_EXIT_OV	RW	0	Override CSI Ths-exit parameter 0: Ths-exit is automatically determined 1: Override Ths-exit with value in bits 6:0 of this register
			6:0	MR_THS_EXIT	R RW	0x0	Ths-exit value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

Table 14. Digital Page 0 Indirect Registers (continued)

Indirect Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
	0x48	CSI0_TPLX	7	MR_TPLX_OV	RW	0	Override CSI Tplx parameter 0: Tplx is automatically determined 1: Override Tplx with value in bits 6:0 of this register
			6:0	MR_TPLX	R RW	0x0	Tplx value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x60	CSI1_TCK_PREP	7	MR_TCK_PREP_OV	RW	0	Override CSI Tck-prep parameter 0: Tck-prep is automatically determined 1: Override Tck-prep with value in bits 6:0 of this register
			6:0	MR_TCK_PREP	R RW	0x0	Tck-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x61	CSI1_TCK_ZERO	7	MR_TCK_ZERO_OV	RW	0	Override CSI Tck-zero parameter 0: Tck-zero is automatically determined 1: Override Tck-zero with value in bits 6:0 of this register
			6:0	MR_TCK_ZERO	R RW	0x0	Tck-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x62	CSI1_TCK_TRAIL	7	MR_TCK_TRAIL_OV	RW	0	Override CSI Tck-trail parameter 0: Tck-trail is automatically determined 1: Override Tck-trail with value in bits 6:0 of this register
			6:0	MR_TCK_TRAIL	R RW	0x0	Tck-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x63	CSI1_TCK_POST	7	MR_TCK_POST_OV	RW	0	Override CSI Tck-post parameter 0: Tck-post is automatically determined 1: Override Tck-post with value in bits 6:0 of this register
			6:0	MR_TCK_POST	R RW	0x0	Tck-post value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x64	CSI1_THS_PREP	7	MR_THS_PREP_OV	RW	0	Override CSI Ths-prep parameter 0: Ths-prep is automatically determined 1: Override Ths-prep with value in bits 6:0 of this register
			6:0	MR_THS_PREP	R RW	0x0	Ths-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

Table 14. Digital Page 0 Indirect Registers (continued)

Indirect Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
	0x65	CSI1_THS_ZERO	7	MR_THS_ZERO_OV	RW	0	Override CSI Ths-zero parameter 0: Ths-zero is automatically determined 1: Override Ths-zero with value in bits 6:0 of this register
			6:0	MR_THS_ZERO	R RW	0x0	Ths-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x66	CSI1_THS_TRAIL	7	MR_THS_TRAIL_OV	RW	0	Override CSI Ths-trail parameter 0: Ths-trail is automatically determined 1: Override Ths-trail with value in bits 6:0 of this register
			6:0	MR_THS_TRAIL	R RW	0x0	Ths-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x67	CSI1_THS_EXIT	7	MR_THS_EXIT_OV	RW	0	Override CSI Ths-exit parameter 0: Ths-exit is automatically determined 1: Override Ths-exit with value in bits 6:0 of this register
			6:0	MR_THS_EXIT	R RW	0x0	Ths-exit value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.
	0x68	CSI1_TPLX	7	MR_TPLX_OV	RW	0	Override CSI Tplx parameter 0: Tplx is automatically determined 1: Override Tplx with value in bits 6:0 of this register
			6:0	MR_TPLX	R RW	0x0	Tplx value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

LEGEND:
- RW = Read Write
- RW/SC = RW/SC = Read Write access/Self Clearing bit
- R/P = Read Only, Permanent value
- R/COR = Read Only, Clear On Read

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90UB964-Q1 is a highly integrated camera hub chip which includes four FPD-Link III inputs targeted at ADAS applications, such as front/rear/surround-view cameras, camera monitoring systems, and sensor fusion.

9.1.1 Power Over Coax

See application report *Sending Power over Coax in DS90UB913A Designs* for more details.

9.2 Typical Application

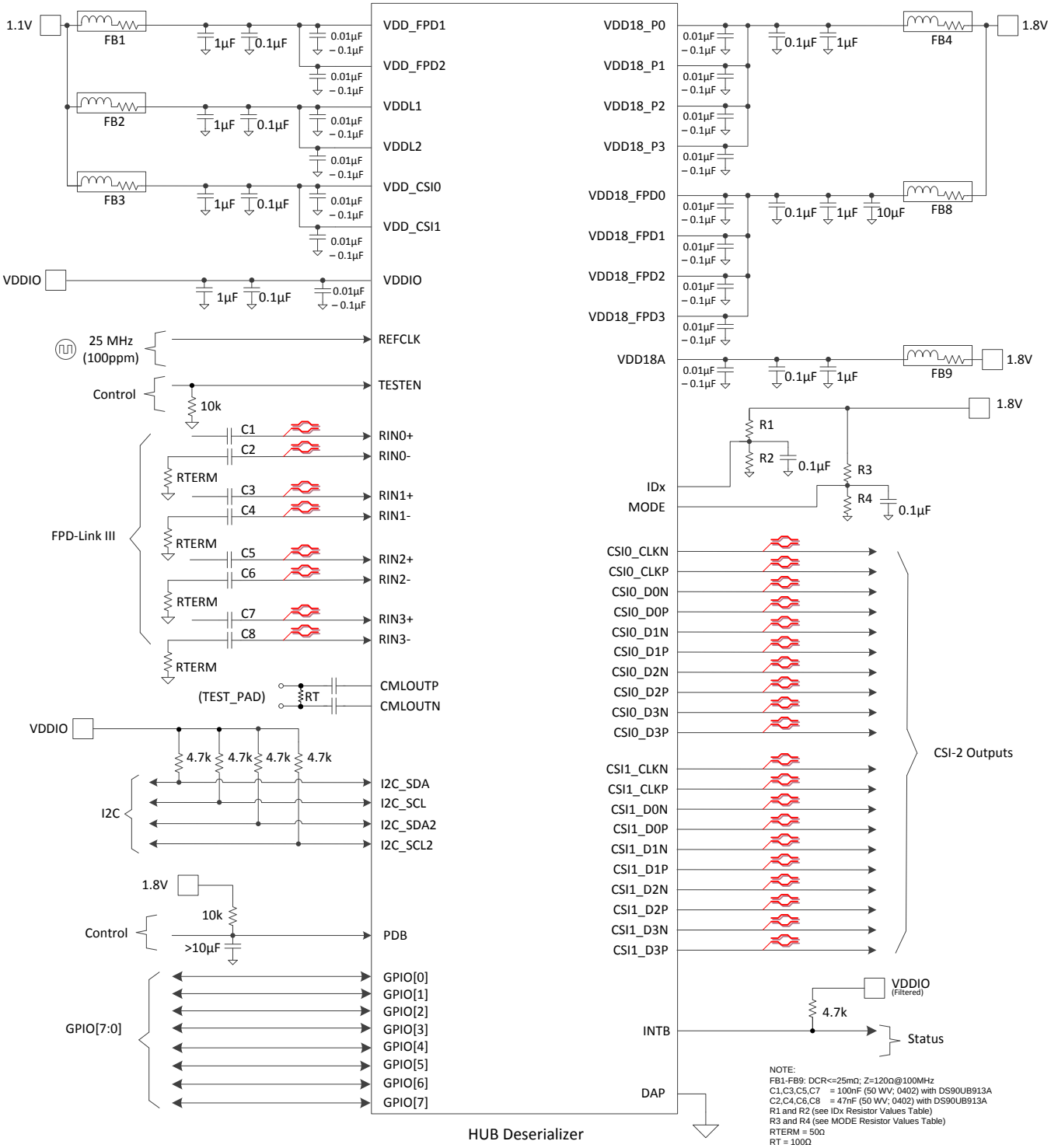


Figure 38. Typical Connection Diagram (Coaxial)

Typical Application (continued)

9.2.1 Design Requirements

For the typical design application, use use the parameters listed in Table 15.

Table 15. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V or 3.3 V
VDD11	1.1 V
VDD18	1.8 V
AC Coupling Capacitor for STP with 913AQ/913Q/933Q: RIN[3:0]±	100 nF (50 WV 0402)
AC Coupling Capacitor for Coaxial with 913AQ/933Q: RIN[3:0]+	100 nF (50 WV 0402)
AC Coupling Capacitor for Coaxial with 913AQ/933Q: RIN[3:0]-	47 nF (50 WV 0402)

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in Figure 39. For applications utilizing single-ended 50-Ω coaxial cable, terminate the unused data pins (RIN0–, RIN1–, RIN2–, RIN3–) with an AC-coupling capacitor and a 50-Ω resistor.

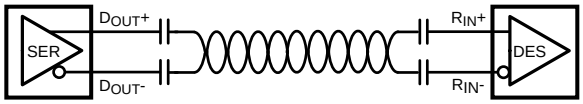


Figure 39. AC-Coupled Connection (STP)

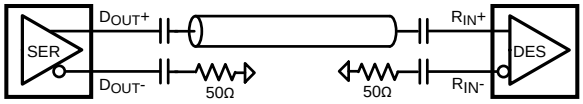


Figure 40. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, use the smallest available package for the AC-coupling capacitor to help minimize degradation of signal quality due to package parasitics.

9.2.2 Detailed Design Procedure

Figure 44 and Figure 44 show typical applications of the DS90UB964-Q1 for multi-camera surround view system. From Figure 38, the FPD-Link III must have an external 0.100 µF / 0.47 µF AC coupling capacitors for coaxial interconnects. The same AC coupling capacitor values should be matched on the paired serializer boards. The deserializer has an internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, 0.1µF or 0.01µF capacitors should be used for each of the core supply pins for local device bypassing. Ferrite beads are placed on the VDD18 and VDD11 supplies for effective noise suppression.

9.2.3 Application Curves

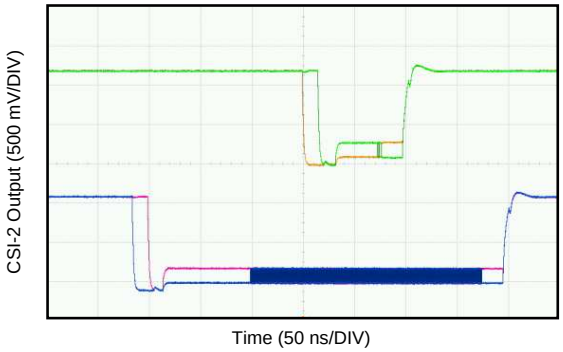


Figure 41. CSI-2 DATA and CLK Output

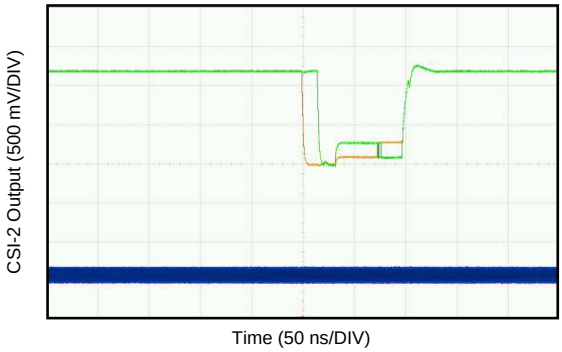


Figure 42. CSI-2 DATA and Continuous CLK Output

9.3 System Examples

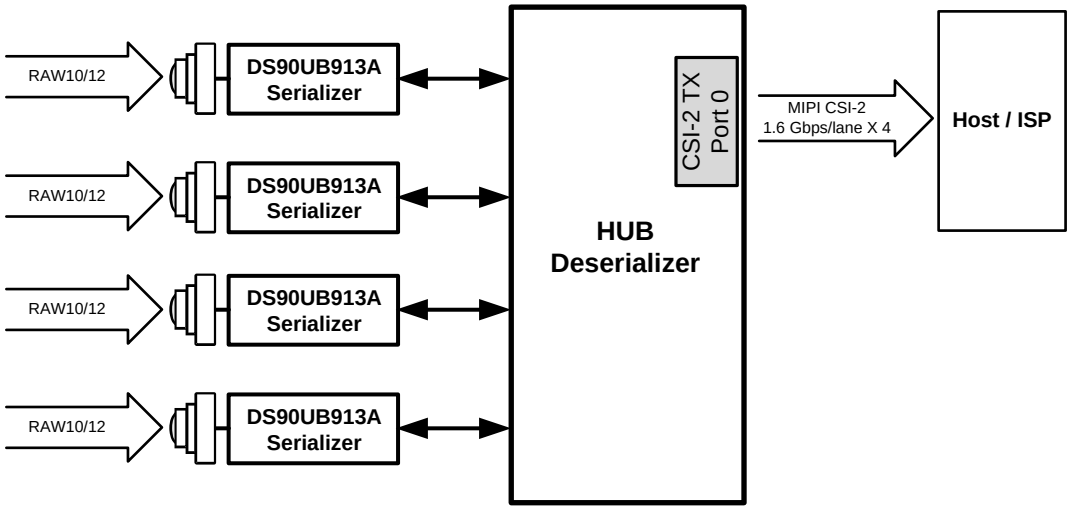


Figure 43. Four DS90UB913A Camera Data onto CSI-2 over 1 port

System Examples (continued)

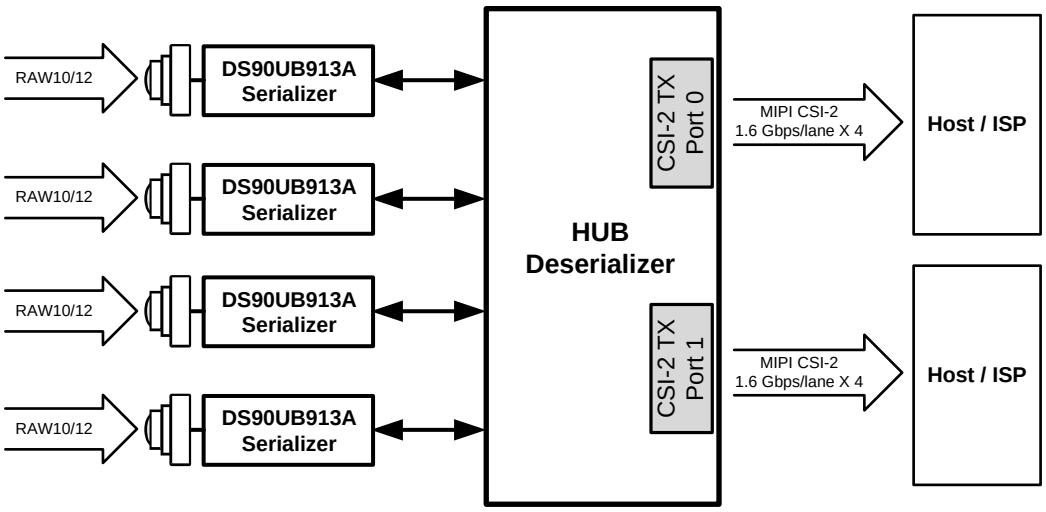


Figure 44. Four DS90UB913A Camera Data onto CSI-2 over 2 ports

10 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. *Table 1* provides guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

10.1 VDD Power Supply

Each VDD power supply pin must have a 10 nF (or 100 nF) capacitor to ground connected as close as possible to DS90UB964-Q1 device. TI recommends having additional decoupling capacitors (0.1 µF, 1 µF, and 10 µF) on i and also recommends having the pins connected to a solid power plane.

10.2 Power-Up Sequencing

The power-up sequence for the DS90UB964-Q1 is as follows:

Table 16. Timing Diagram for the Power-Up Sequence

PARAMETER		MIN	TYP	MAX	UNIT	NOTES
T0	VDD11 to VDD18 to VDDIO	0			ms	
T1	VDD11 rise time	0.05			ms	@10/90%
T2	VDD11 to VDD18	0			ms	
T3	VDD18 rise time	0.2	1		ms	@10/90%
T4	VDD18 to VDDIO	0			ms	
T5	VDDIO rise time	0.2	1		ms	@10/90%
T6	VDDIO to PDB	0			ms	
T7	PDB pulse width	2			ms	Hard reset

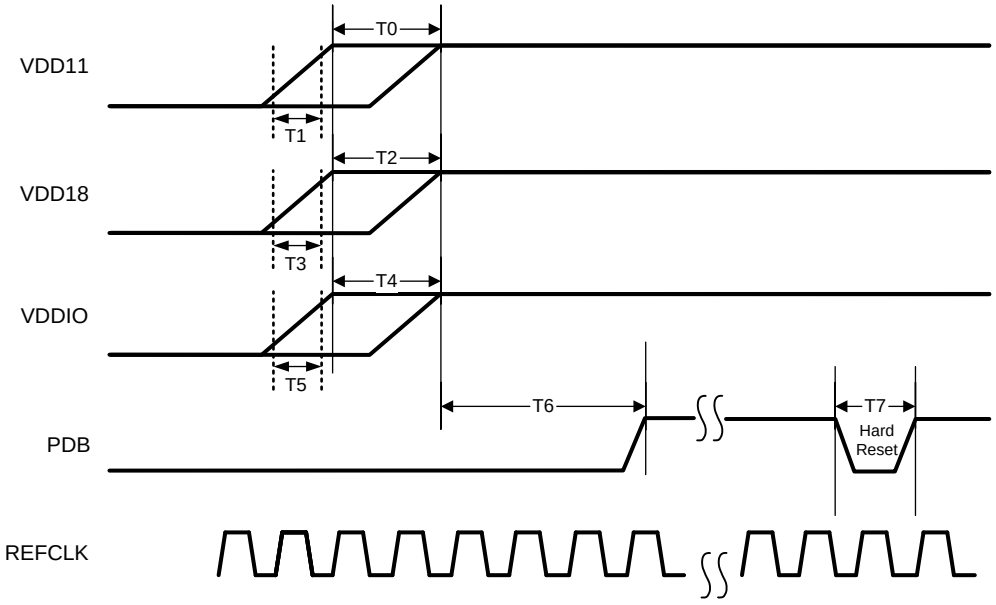


Figure 45. Power-Up Sequencing

10.3 PDB Pin

The PDB pin is active HIGH and must remain LOW while the VDD pin power supplies are in transition. An external RC network on the PDB pin may be connected to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to VDD18, a 10-kΩ pullup and a > 10-µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until both power supplies have reached steady state.

PDB Pin (continued)

Table 17. PDB Pin Pulse Width

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PDB						
tLRST	PDB Reset Low Pulse		2			ms

10.4 Ground

TI recommends that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. Connect the thermal pad of the DS90UB964-Q1 to this plane with vias.

11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power/ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Ceramic capacitors may be in the 2.2-µF to 10-µF range. The voltage rating of the ceramic capacitors must be at least 5× the power supply voltage being used

TI recommends surface-mount capacitorsdue to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50-µF to 100-µF range, which smooths low frequency switching noise. TI recommends connectingpower and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs

Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Differential impedance of 100 Ω are typically recommended for STP interconnect and single-ended impedance of 50 Ω for coaxial interconnect. The closely coupled lines help to ensure that coupled noise appears as common-mode and thus is rejected by the receivers. The tightly coupled lines aso radiate less.

11.1.1 CSI-2 Guidelines

1. Route CSI0_D*P/N and CSI1_D*P/N pairs with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).
2. Keep away from other high-speed signals.
3. Keep length difference between a differential pair to 5 mils of each other.
4. Length matching should be near the location of mismatch.
5. Match trace lengths between pairs to be < 25 mils.
6. Each pair should be separated at least by 3 times the signal trace width.
7. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend should be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
8. Route all differential pairs on the same layer.
9. Keep the number of VIAS to a minimum — TI recommends keeping the VIA count to 2 or fewer.
10. Keep traces on layers adjacent to ground plane.
11. Do NOT route differential pairs over any plane split.
12. Adding Test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

11.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the VQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP.

Example PCB layout is used to demonstrate both proper routing and proper solder techniques when designing in the Deserializer.

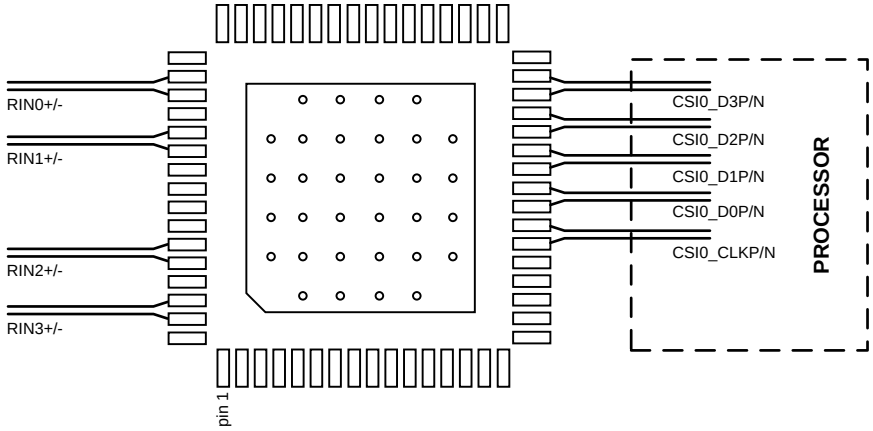


Figure 46. Simplified Layout Example

Figure 47 shows a PCB layout example are derived from the layout design of the DS90UB96X-Q1EVM Evaluation Board. The graphic and layout description are used to determine proper routing when designing the board. The high speed FPD-Link III traces routed differentially up to the connector. A 100Ω differential characteristic impedance and 50Ω single-ended characteristic impedance traces are maintained as much as possible for both STP and coaxial applications. For the layout of a coaxial interconnects, coupled traces should be used with the RINx- termination near to the connector.

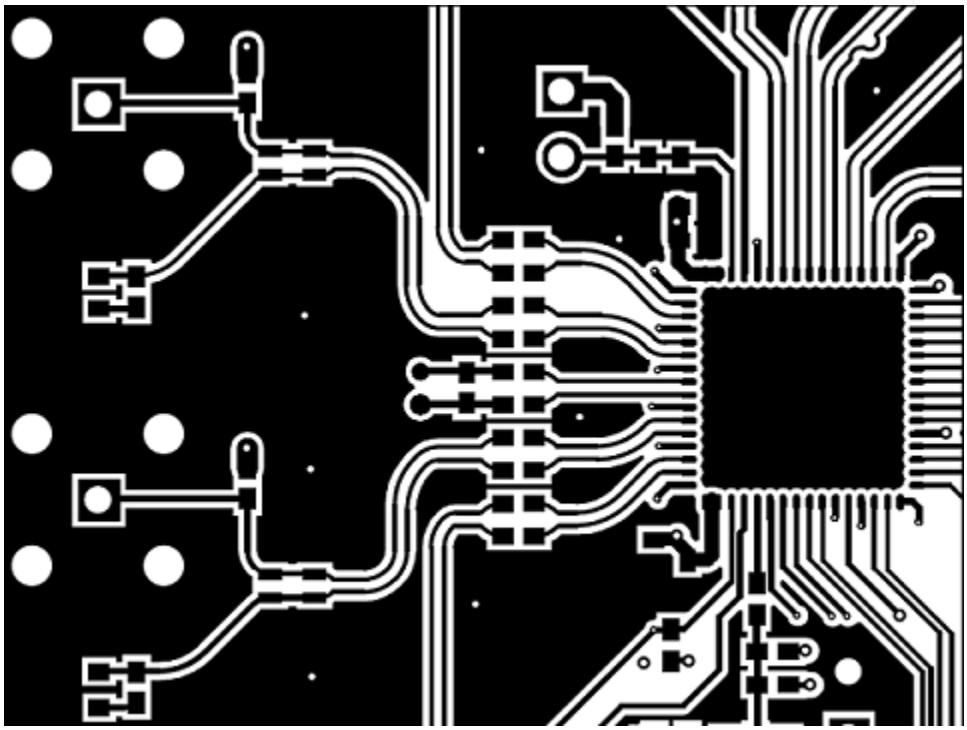
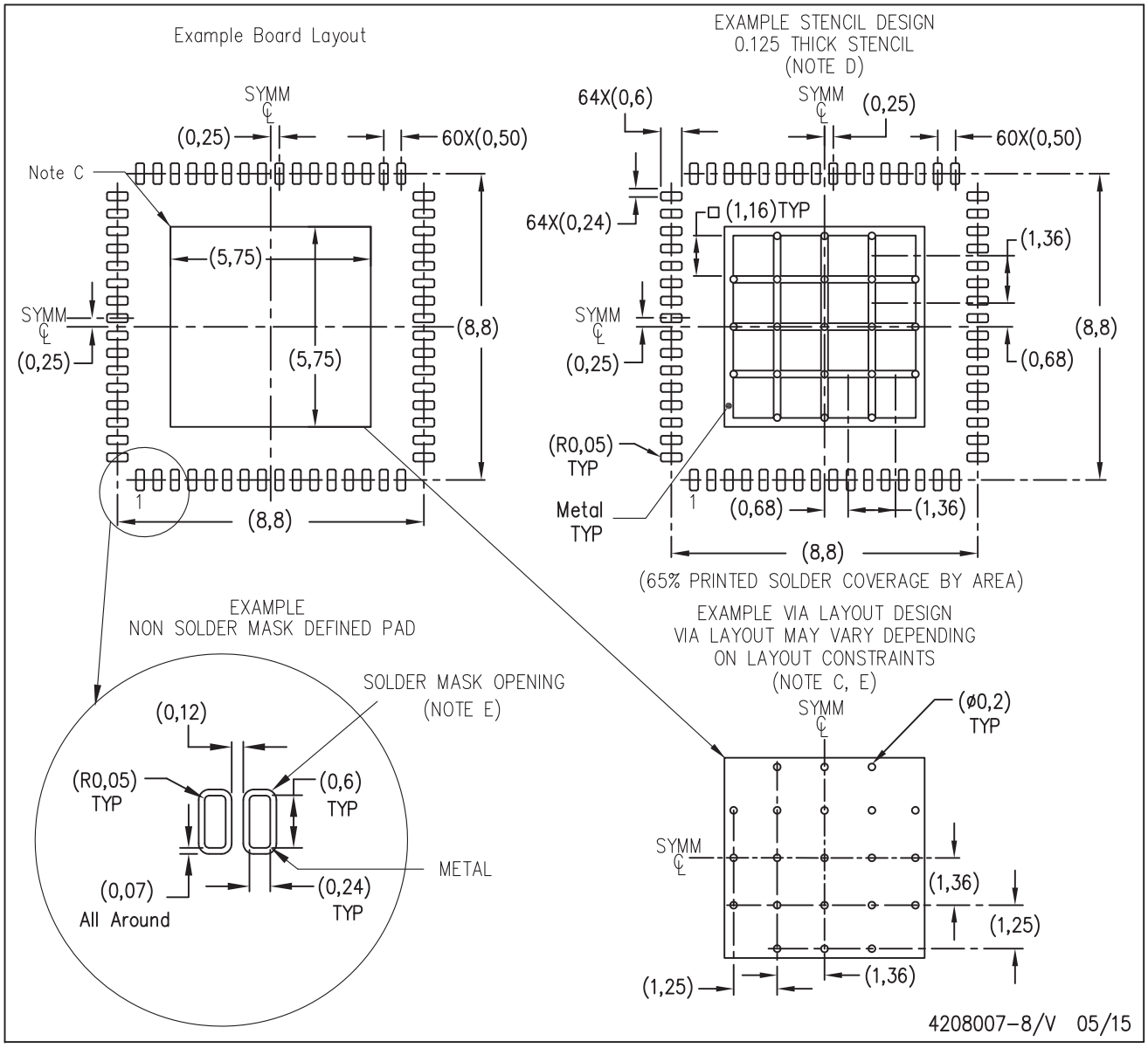


Figure 47. DS90UB964-Q1 Example PCB Layout

Layout Example (continued)

LAND PATTERN DATA

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Sending Power over Coax in DS90UB913A Designs*
- *I2C over DS90UB913/4 FPD-Link III with Bidirectional Control Channel*
- *I2C Communication Over FPD-Link III with Bidirectional Control Channel*
- *I2C Bus Pull-Up Resistor Calculation*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UB964TRGCRQ1	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB964Q	Samples
DS90UB964TRGCTQ1	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB964Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

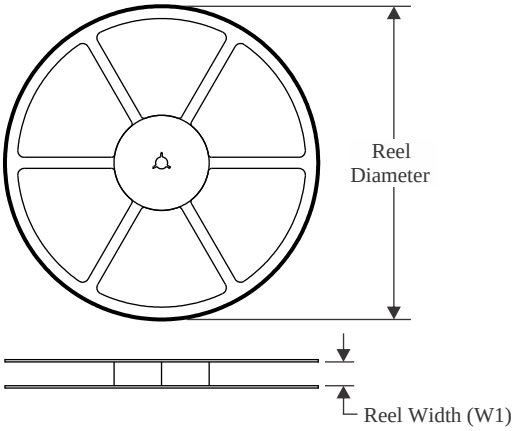
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

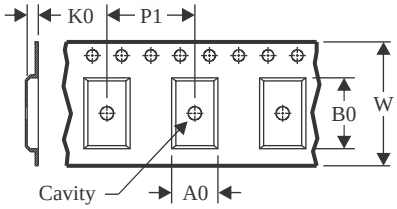
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

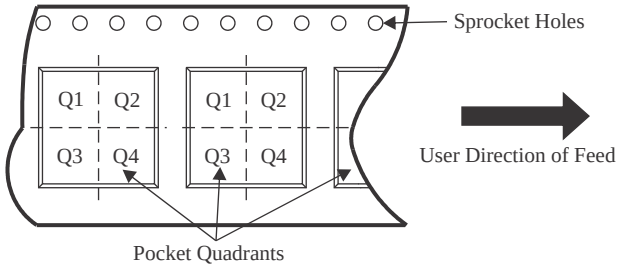


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

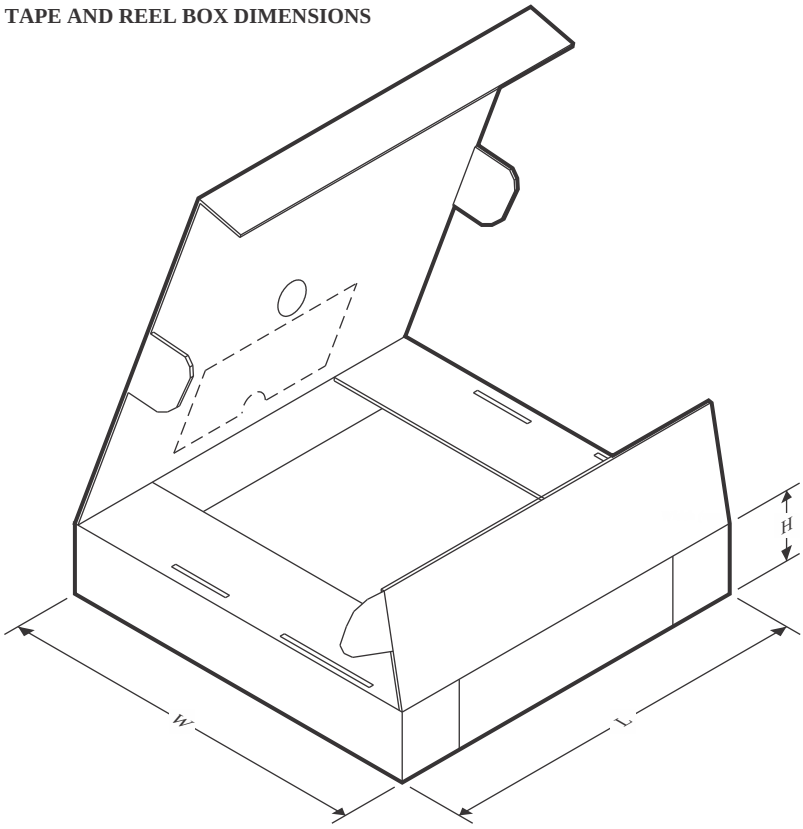
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB964TRGCRQ1	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS90UB964TRGCTQ1	VQFN	RGC	64	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB964TRGCRQ1	VQFN	RGC	64	2000	356.0	356.0	35.0
DS90UB964TRGCTQ1	VQFN	RGC	64	250	208.0	191.0	35.0

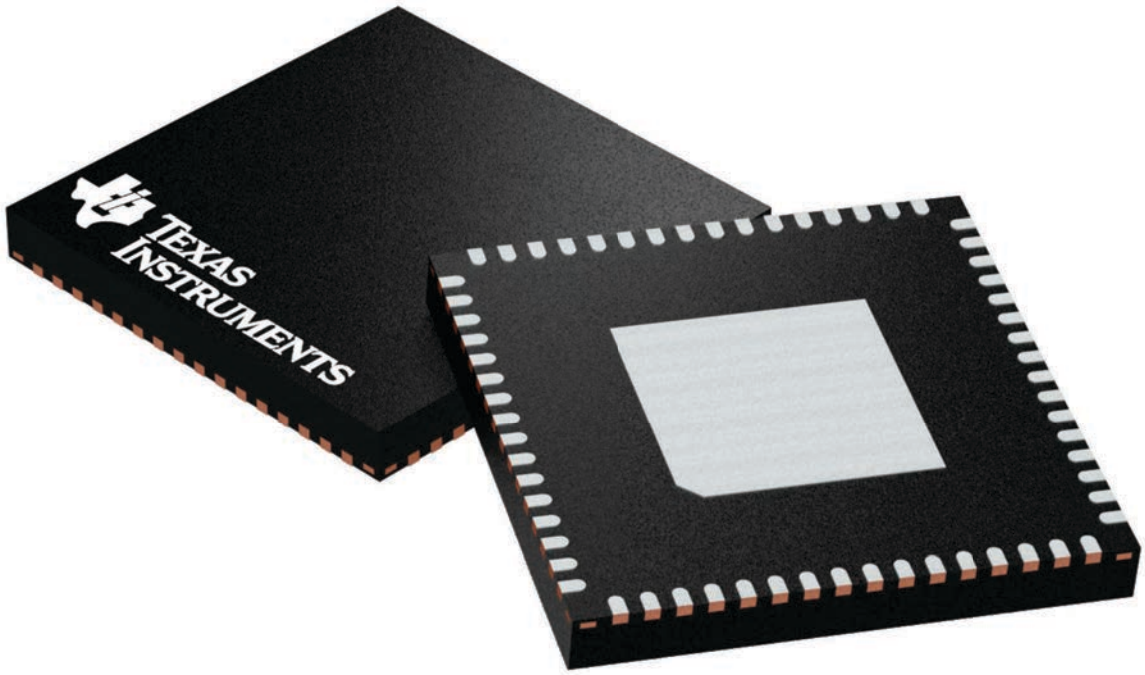
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

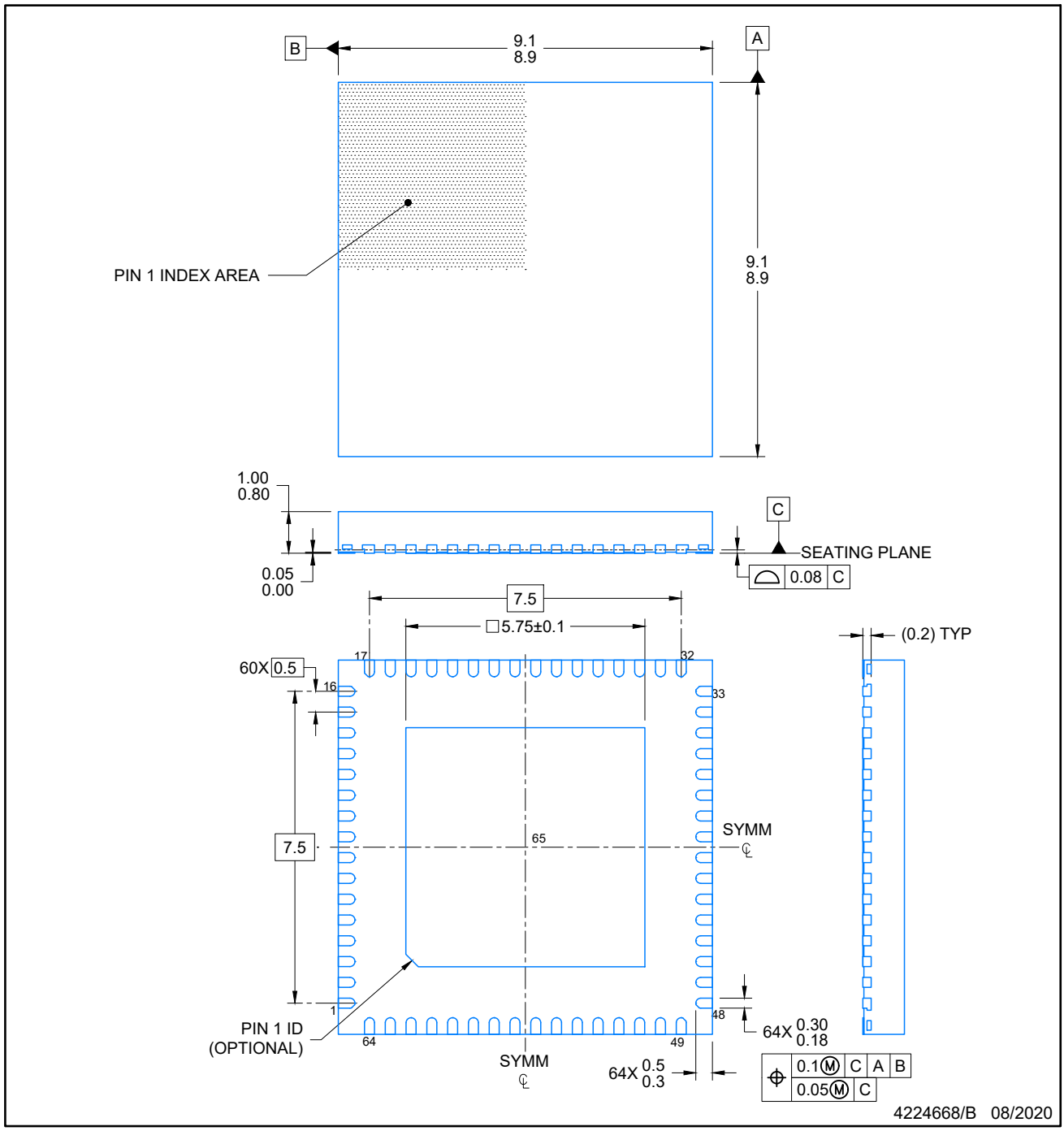
4224597/A

PACKAGE OUTLINE

RGC0064K

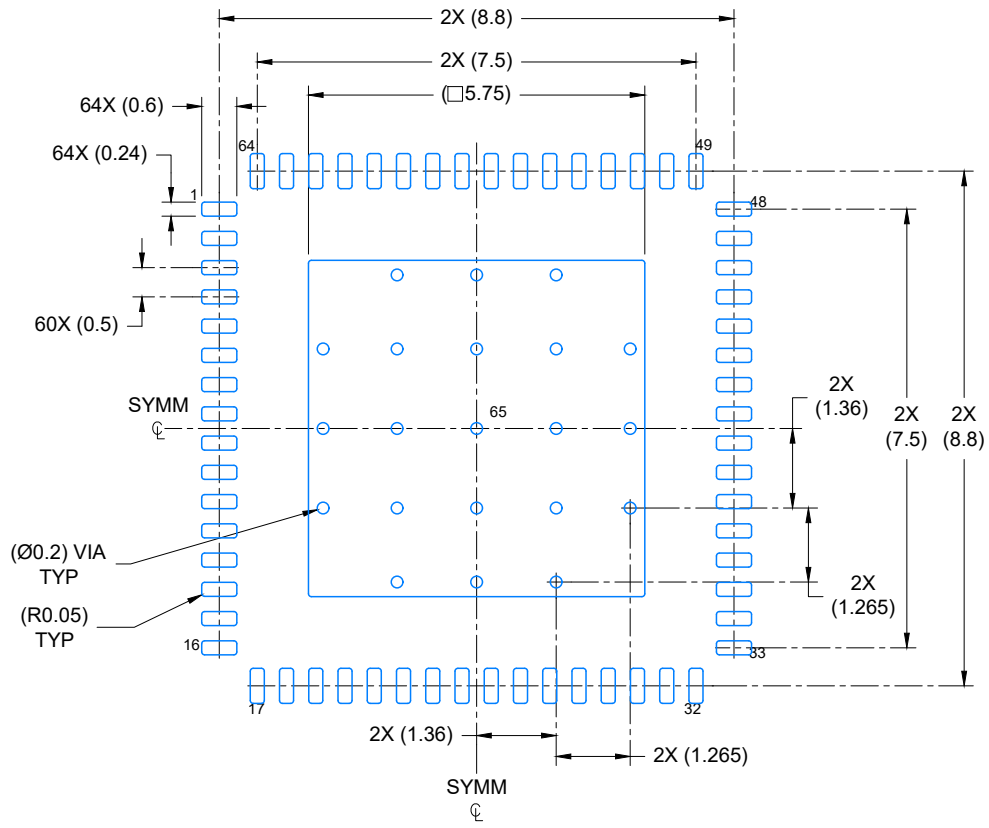
VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

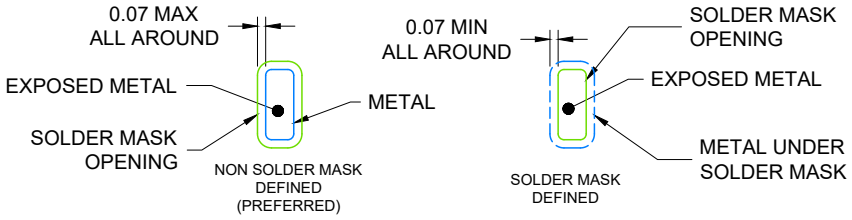


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

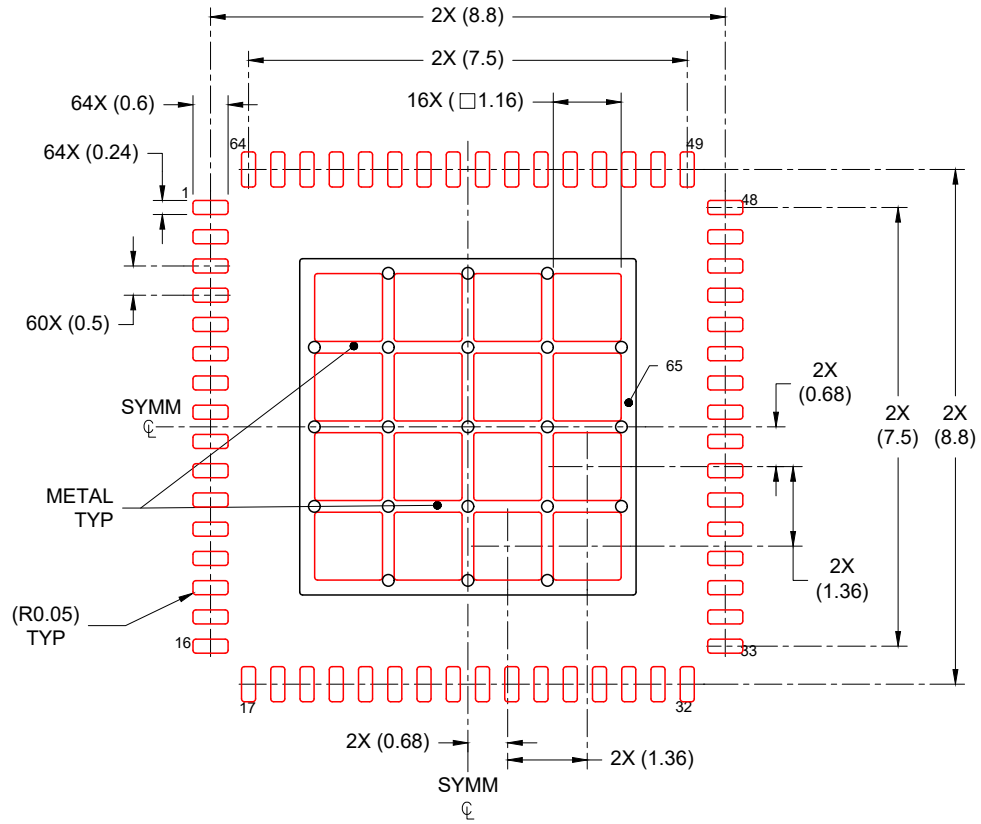


SOLDER MASK DETAILS

4224668/B 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED COVERAGE BY AREA
SCALE: 8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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