

FEATURES

- Operation: 400 MHz to 2700 MHz**
- Gain of 16.9 dB at 880 MHz**
- OIP3 of 45.0 dBm at 880 MHz**
- P1dB of 25.4 dBm at 880 MHz**
- Noise figure: 4.1 dB at 880 MHz**
- Power supply voltage: 3.3 V to 5 V**
- Power supply current: 44 mA to 104 mA**
- Dynamically adjustable bias**
- No bias resistor required**
- Thermally efficient, MSL-1 rated SOT-89 package**
- Operating temperature range: -40°C to +105°C**
- ESD rating of ±4 kV (Class 3A)**

APPLICATIONS

- Wireless infrastructure**
- Automated test equipment**
- ISM/AMR applications**

GENERAL DESCRIPTION

The **ADL5320** incorporates a dynamically adjustable biasing circuit that allows for the customization of OIP3 and P1dB performance from 3.3 V to 5 V without the need for an external bias resistor. This feature gives the designer the ability to tailor driver amplifier performance to the specific needs of the design. This feature also creates the opportunity for dynamic biasing of the driver amplifier, where a variable supply is used to allow for full 5 V biasing under large signal conditions and then can reduce the supply voltage when signal levels are smaller and lower power consumption is desirable. This scalability reduces the need to evaluate and inventory multiple driver amplifiers for different output power requirements from 22 dBm to 26 dBm output power levels.

The **ADL5320** is also rated to operate across the wide temperature range of -40°C to +105°C for reliable performance in designs that experience higher temperatures, such as power amplifiers. The ¼ watt driver amplifier also covers the 400 MHz to 2700 MHz wide frequency range and only requires a few external components to be tuned to a specific band within that wide range. This high performance, broadband RF driver amplifier is well suited for a variety of wired and wireless applications including cellular infrastructure, ISM band power amplifiers, defense equipment, and instrumentation equipment. A fully populated evaluation board is available.

FUNCTIONAL BLOCK DIAGRAM

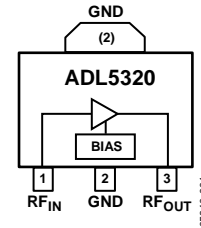


Figure 1.

The **ADL5320** also delivers excellent adjacent channel power ratio (ACPR) vs. output power and bias voltage. The driver can deliver greater than 17 dBm of output power at 2140 MHz while achieving an ACPR of -55 dBc at 5 V. If the bias is reduced to 3.3 V, the -55 dBc ACPR output power reduces to 9 dBm.

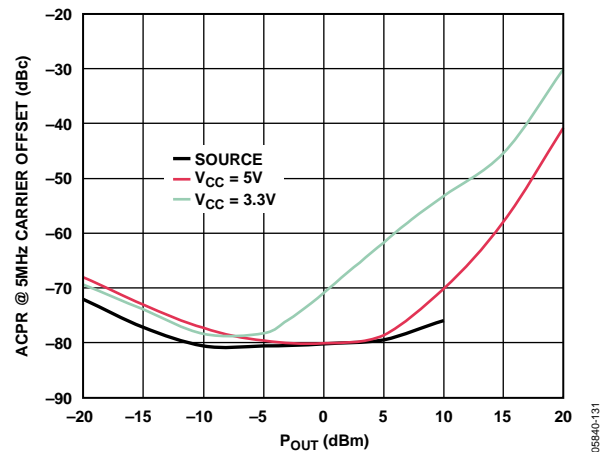


Figure 2. ACPR vs. Output Power, Single Carrier W-CDMA TM1-64 at 2140 MHz

Rev. B

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REVISION HISTORY

10/13—Rev. A to Rev. B

| | |
|--|------------|
| Changed 1805 MHz to 2110 MHz | Throughout |
| Changes to Figure 27 | 10 |
| Changes to Figure 34 and Table 6..... | 12 |
| Changes to Figure 35..... | 13 |
| Changes to Matching Procedures Section..... | 14 |
| Added Optimizing OP1dB Section, Table 10, Table 11, Table 12, and Figure 39; Renumbered Sequentially..... | 15 |
| Changes to Evaluation Board Section | 16 |
| Updated Outline Dimensions | 18 |
| Changes to Ordering Guide | 18 |

6/12—Rev. 0 to Rev. A

| | |
|--|---|
| Changes to Features Section and General Description Section..... | 1 |
| Added Application Section and Figure 2; Renumbered Sequentially | 1 |
| Changes to Specifications Section | 3 |
| Deleted θ_{JC} (Junction to Paddle) Parameter, Table 3..... | 5 |

| | |
|--|----|
| Changes to Operating Temperature Range Parameter, Table 3 | 5 |
| Added Thermal Resistance Section and Table 4; Renumbered Sequentially | 5 |
| Added EPAD Notation to Figure 3 | 6 |
| Added Figure 27 | 10 |
| Added High Temperature and 3.3 V Operation Section and Figure 28 to Figure 33 | 11 |
| Added Applications Information Section and Figure 35 | 12 |
| Changes to Soldering Information and Recommended PCB Land Pattern | 12 |
| Changed –82 dBc to –80 dBc in W-CDMA ACPR Performance Section..... | 14 |
| Added Figure 39 | 14 |
| Updated Outline Dimensions | 17 |

2/08—Revision 0: Initial Version

SPECIFICATIONS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | 3.3 V | | | 5 V | | | Unit |
|-------------------------------|--|-------|------------|------|------|------------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| OVERALL FUNCTION | | | | | | | | |
| Frequency Range | | 400 | | 2700 | 400 | | 2700 | MHz |
| FREQUENCY = 880 MHz | | | | | | | | |
| Gain ¹ | | | 15.6 | | 16.3 | 16.9 | 17.5 | dB |
| vs. Frequency | ± 50 MHz | | ± 0.2 | | | ± 0.3 | | dB |
| vs. Temperature | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | | ± 0.6 | | | ± 0.6 | | dB |
| vs. Supply | 3.2 V to 3.4 V, 4.75 V to 5.25 V | | ± 0.2 | | | ± 0.1 | | dB |
| Output 1 dB Compression Point | | | 21.5 | | | 25.4 | | dBm |
| Output Third-Order Intercept | $\Delta f = 1$ MHz, $P_{\text{OUT}} = 10$ dBm per tone | | 34 | | | 45 | | dBm |
| Noise Figure | | | 3.2 | | | 4.1 | | dB |
| FREQUENCY = 2140 MHz | | | | | | | | |
| Gain ¹ | | | 12.2 | | 12.4 | 13.2 | 14.0 | dB |
| vs. Frequency | ± 50 MHz | | ± 0.3 | | | ± 0.33 | | dB |
| vs. Temperature | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | | ± 0.7 | | | ± 0.8 | | dB |
| vs. Supply | 3.2 V to 3.4 V, 4.75 V to 5.25 V | | ± 0.15 | | | ± 0.06 | | dB |
| Output 1 dB Compression Point | | | 22.6 | | | 25.7 | | dBm |
| Output Third-Order Intercept | $\Delta f = 1$ MHz, $P_{\text{OUT}} = 10$ dBm per tone | | 32 | | | 42 | | dBm |
| Noise Figure | | | 3.7 | | | 4.4 | | dB |
| FREQUENCY = 2600 MHz | | | | | | | | |
| Gain ¹ | | | 10.7 | | 11.5 | 12.5 | 13.4 | dB |
| vs. Frequency | ± 100 MHz | | ± 0.2 | | | ± 0.6 | | dB |
| vs. Temperature | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | | ± 0.6 | | | ± 1.1 | | dB |
| vs. Supply | 3.2 V to 3.4 V, 4.75 V to 5.25 V | | ± 0.2 | | | ± 0.1 | | dB |
| Output 1 dB Compression Point | | | 25.7 | | | 27.4 | | dBm |
| Output Third-Order Intercept | $\Delta f = 1$ MHz, $P_{\text{OUT}} = 10$ dBm per tone | | 29 | | | 37 | | dBm |
| Noise Figure | | | 4.1 | | | 5.1 | | dB |
| POWER INTERFACE | Pin RF_{OUT} | | | | | | | |
| Supply Voltage | | | 3.3 | | 4.5 | 5 | 5.5 | V |
| Supply Current | | | 44 | | | 104 | 124 | mA |
| vs. Temperature | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | | ± 5.0 | | | ± 6.0 | | mA |
| Power Dissipation | $V_{\text{SUP}} = 3.3$ V, $V_{\text{SUP}} = 5$ V | | 145 | | | 520 | | mW |

¹ Guaranteed maximum and minimum specified limits on this parameter are based on six sigma calculations.

TYPICAL SCATTERING PARAMETERS

VSUP = 5 V and T_A = 25°C; the effects of the test fixture have been de-embedded up to the pins of the device.

Table 2.

| Freq (MHz) | S11 | | S21 | | S12 | | S22 | |
|------------|----------------|-----------|----------------|-----------|----------------|-----------|----------------|-----------|
| | Magnitude (dB) | Angle (°) | Magnitude (dB) | Angle (°) | Magnitude (dB) | Angle (°) | Magnitude (dB) | Angle (°) |
| 400 | -1.42 | -179.88 | +14.16 | +134.74 | -32.56 | +13.47 | -3.42 | +176.22 |
| 500 | -1.38 | +175.04 | +13.97 | +126.21 | -32.02 | +8.58 | -3.71 | +175.38 |
| 550 | -1.42 | +173.05 | +13.81 | +122.24 | -31.84 | +6.81 | -3.84 | +175.10 |
| 600 | -1.48 | +171.25 | +13.66 | +118.41 | -31.70 | +5.25 | -3.96 | +174.89 |
| 650 | -1.54 | +169.59 | +13.49 | +114.71 | -31.56 | +3.85 | -4.08 | +174.74 |
| 700 | -1.62 | +168.11 | +13.32 | +111.12 | -31.43 | +2.63 | -4.19 | +174.71 |
| 750 | -1.70 | +166.66 | +13.17 | +107.64 | -31.29 | +1.35 | -4.30 | +174.74 |
| 800 | -1.80 | +165.36 | +13.05 | +104.27 | -31.16 | +0.20 | -4.41 | +174.89 |
| 850 | -1.90 | +163.99 | +12.94 | +100.86 | -31.01 | -0.95 | -4.52 | +175.10 |
| 900 | -2.01 | +162.65 | +12.84 | +97.48 | -30.85 | -2.23 | -4.62 | +175.37 |
| 950 | -2.13 | +161.32 | +12.73 | +94.09 | -30.69 | -3.43 | -4.71 | +175.78 |
| 1000 | -2.27 | +159.98 | +12.65 | +90.72 | -30.52 | -4.80 | -4.81 | +176.29 |
| 1050 | -2.43 | +158.61 | +12.62 | +87.34 | -30.32 | -6.24 | -4.89 | +176.85 |
| 1100 | -2.63 | +157.11 | +12.59 | +83.90 | -30.15 | -7.92 | -4.98 | +177.52 |
| 1150 | -2.84 | +155.60 | +12.56 | +80.41 | -29.95 | -9.61 | -5.06 | +178.29 |
| 1200 | -3.09 | +153.91 | +12.55 | +76.75 | -29.74 | -11.56 | -5.12 | +179.17 |
| 1250 | -3.39 | +152.08 | +12.56 | +73.03 | -29.54 | -13.63 | -5.18 | -179.85 |
| 1300 | -3.73 | +150.14 | +12.57 | +69.24 | -29.33 | -15.87 | -5.25 | -178.72 |
| 1350 | -4.13 | +147.98 | +12.61 | +65.23 | -29.12 | -18.39 | -5.28 | -177.52 |
| 1400 | -4.59 | +145.57 | +12.66 | +61.05 | -28.91 | -21.17 | -5.29 | -176.26 |
| 1450 | -5.13 | +143.05 | +12.72 | +56.75 | -28.69 | -24.17 | -5.27 | -174.93 |
| 1500 | -5.76 | +140.31 | +12.79 | +52.20 | -28.48 | -27.48 | -5.19 | -173.52 |
| 1550 | -6.48 | +137.18 | +12.83 | +47.46 | -28.28 | -31.05 | -5.12 | -172.60 |
| 1600 | -7.36 | +133.46 | +12.89 | +42.49 | -28.10 | -34.99 | -5.06 | -171.45 |
| 1650 | -8.45 | +129.65 | +12.93 | +37.41 | -27.95 | -39.05 | -4.94 | -170.38 |
| 1700 | -9.74 | +125.36 | +12.98 | +32.12 | -27.81 | -43.45 | -4.80 | -169.52 |
| 1750 | -11.32 | +120.71 | +12.99 | +26.74 | -27.70 | -48.12 | -4.65 | -168.95 |
| 1800 | -13.34 | +115.47 | +12.99 | +21.16 | -27.61 | -53.06 | -4.47 | -168.68 |
| 1850 | -16.00 | +109.24 | +12.97 | +15.43 | -27.56 | -58.23 | -4.30 | -168.76 |
| 1900 | -19.89 | +100.84 | +12.93 | +9.57 | -27.55 | -63.67 | -4.14 | -169.26 |
| 1950 | -26.68 | +83.39 | +12.86 | +3.65 | -27.58 | -69.38 | -3.99 | -170.11 |
| 2000 | -33.34 | -26.40 | +12.76 | -2.46 | -27.65 | -75.33 | -3.86 | -171.37 |
| 2050 | -23.21 | -71.32 | +12.64 | -8.60 | -27.75 | -81.44 | -3.74 | -172.97 |
| 2100 | -18.39 | -83.50 | +12.49 | -14.83 | -27.89 | -87.92 | -3.65 | -175.01 |
| 2150 | -15.39 | -92.08 | +12.31 | -21.09 | -28.07 | -94.55 | -3.58 | -177.37 |
| 2200 | -13.26 | -100.04 | +12.11 | -27.46 | -28.29 | -101.56 | -3.54 | +179.90 |
| 2250 | -11.63 | -107.86 | +11.88 | -33.90 | -28.54 | -108.80 | -3.50 | +176.83 |
| 2300 | -10.31 | -115.84 | +11.62 | -40.49 | -28.82 | -116.46 | -3.47 | +173.43 |
| 2350 | -9.20 | -123.94 | +11.33 | -47.09 | -29.15 | -124.41 | -3.44 | +169.75 |
| 2400 | -8.23 | -132.24 | +11.01 | -53.81 | -29.50 | -132.81 | -3.42 | +165.83 |
| 2450 | -7.38 | -140.88 | +10.64 | -60.65 | -29.89 | -141.70 | -3.40 | +161.63 |
| 2500 | -6.61 | -149.66 | +10.24 | -67.57 | -30.31 | -150.89 | -3.36 | +157.29 |
| 2550 | -5.89 | -158.59 | +9.78 | -74.53 | -30.76 | -160.57 | -3.31 | +152.82 |
| 2600 | -5.23 | -167.51 | +9.27 | -81.60 | -31.23 | -170.68 | -3.24 | +148.32 |
| 2650 | -4.62 | -176.26 | +8.70 | -88.50 | -31.73 | +178.90 | -3.17 | +143.81 |
| 2700 | -4.05 | +175.18 | +8.07 | -95.43 | -32.22 | +168.34 | -3.09 | +139.40 |

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|--|-----------------|
| Supply Voltage, VSUP | 6.5 V |
| Input Power (50 Ω Impedance) | 20 dBm |
| Internal Power Dissipation (Paddle Soldered) | 683 mW |
| Maximum Junction Temperature | 150°C |
| Operating Temperature Range | -40°C to +105°C |
| Storage Temperature Range | -65°C to +150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 4 lists the junction-to-air thermal resistance (θ_{JA}) and the junction-to-paddle thermal resistance (θ_{JC}) for the ADL5320.

Table 4. Thermal Resistance

| Package Type | θ_{JA} ¹ | θ_{JC} ² | Unit |
|---------------|----------------------------|----------------------------|------|
| 3-Lead SOT-89 | 35 | 11 | °C/W |

¹ Measured on Analog Devices, Inc., evaluation board. For more information about board layout, see the Soldering Information and Recommended PCB Land Pattern section.

² Based on simulation with JEDEC standard JESD51.

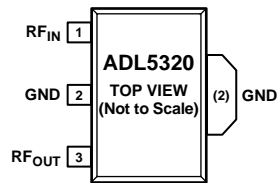
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. THE EXPOSED PAD IS INTERNALLY CONNECTED TO GND. SOLDER TO A LOW IMPEDANCE GROUND PLANE.

05944-002

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-------------------|---|
| 1 | RF _{IN} | RF Input. Requires a dc blocking capacitor. |
| 2 | GND | Ground. Connect to a low impedance ground plane. |
| 3 | RF _{OUT} | RF Output and Supply Voltage. DC bias is provided to this pin through an inductor that is connected to the external power supply. RF path requires a dc blocking capacitor. |
| | Exposed Paddle | Expose Paddle. Internally connected to GND. Solder to a low impedance ground plane. |

TYPICAL PERFORMANCE CHARACTERISTICS

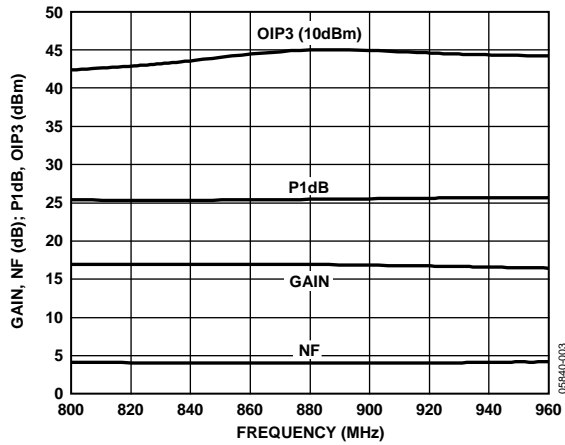


Figure 4. Gain, P1dB, OIP3, and Noise Figure vs. Frequency, 800 MHz to 960 MHz

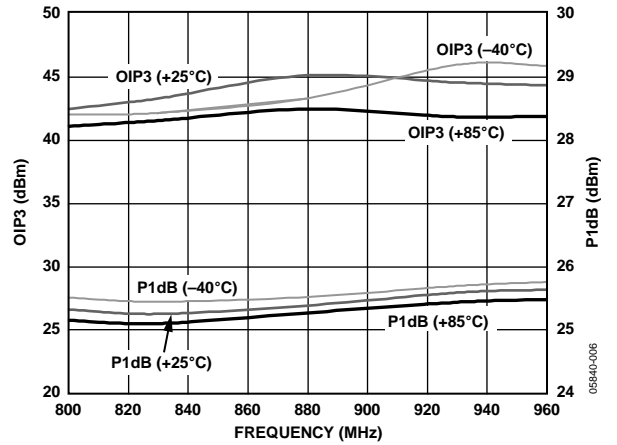


Figure 7. OIP3 and P1dB vs. Frequency and Temperature, 800 MHz to 960 MHz

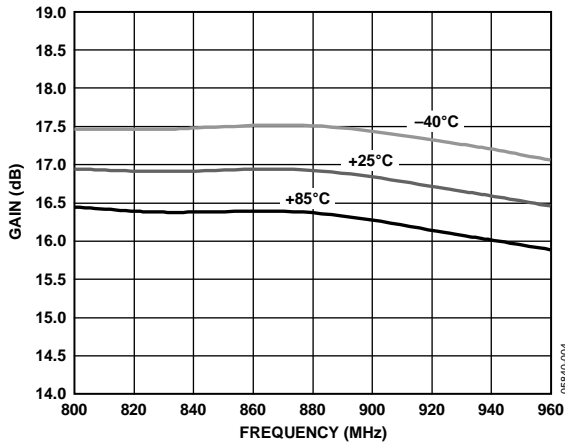


Figure 5. Gain vs. Frequency and Temperature, 800 MHz to 960 MHz

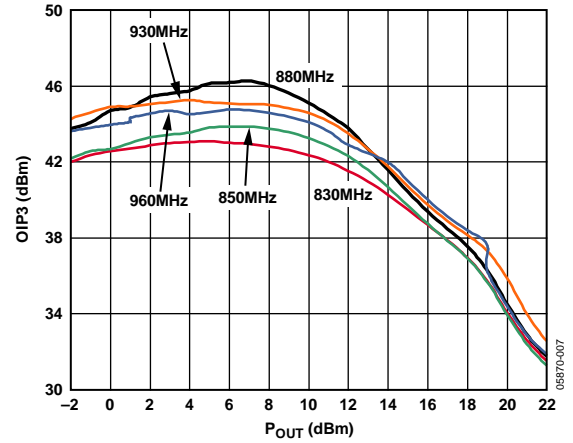


Figure 8. OIP3 vs. P_{OUT} and Frequency, 800 MHz to 960 MHz

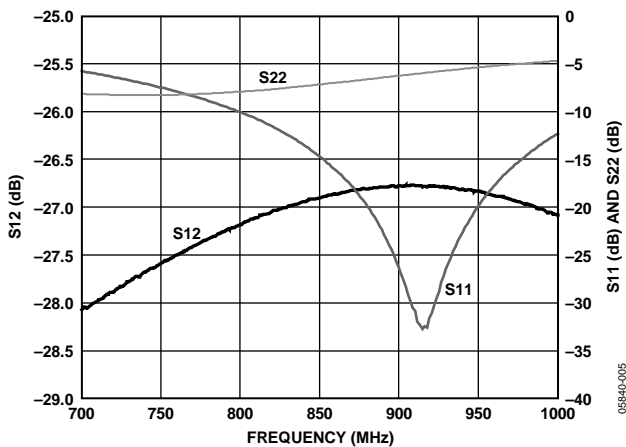


Figure 6. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency, 800 MHz to 960 MHz

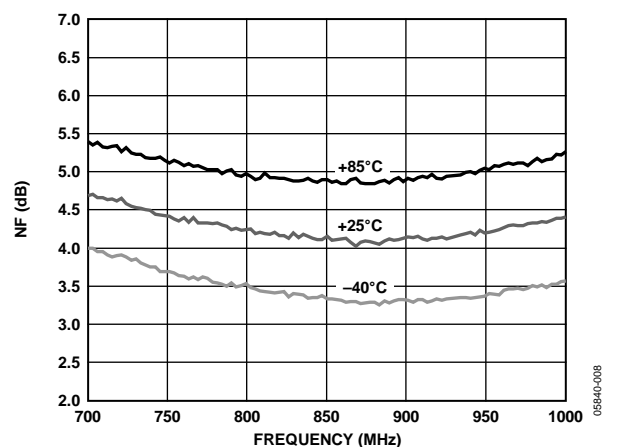


Figure 9. Noise Figure vs. Frequency and Temperature, 800 MHz to 960 MHz

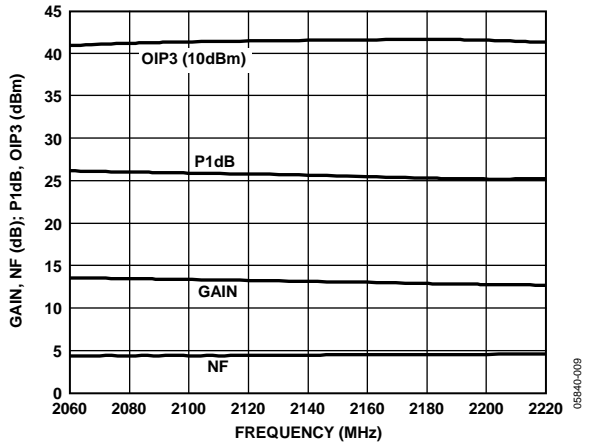


Figure 10. Gain, P1dB, OIP3, and Noise Figure vs. Frequency, 2060 MHz to 2200 MHz

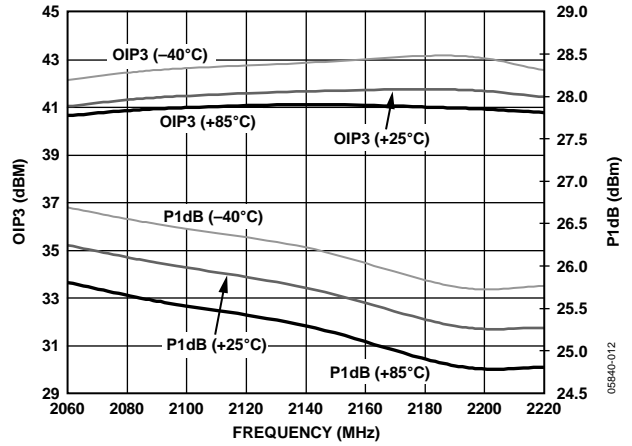


Figure 13. OIP3 and P1dB vs. Frequency and Temperature, 2060 MHz to 2200 MHz

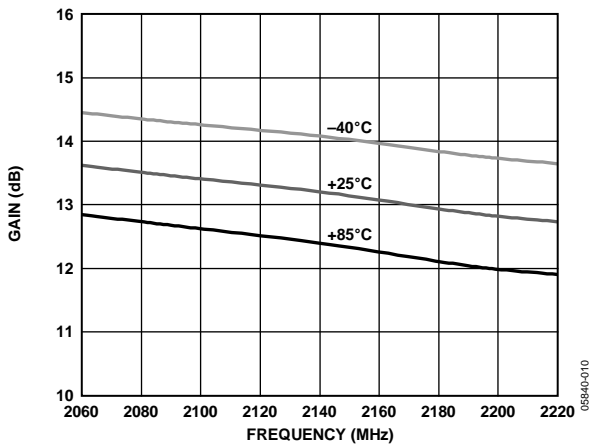


Figure 11. Gain vs. Frequency and Temperature, 2060 MHz to 2200 MHz

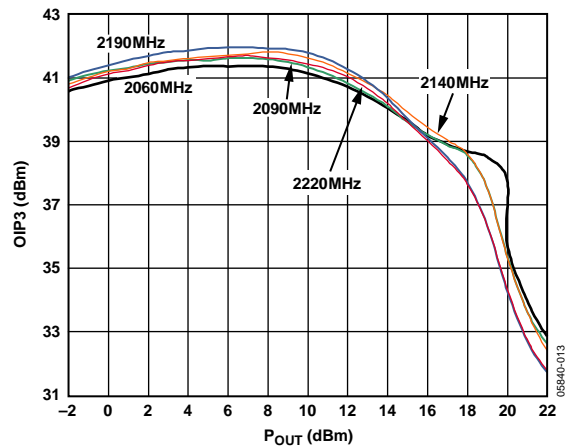


Figure 14. OIP3 vs. P_{OUT} and Frequency, 2060 MHz to 2200 MHz

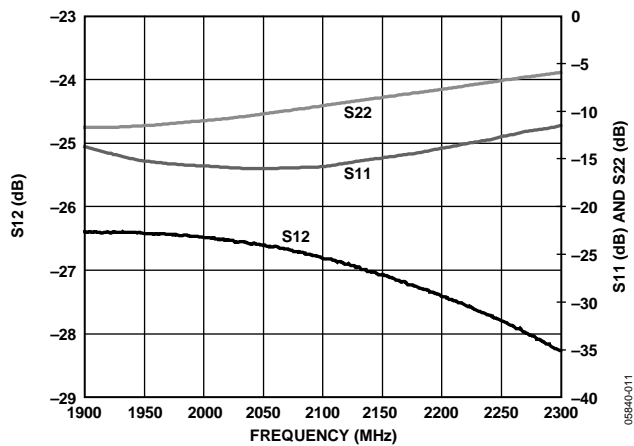


Figure 12. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency, 2060 MHz to 2200 MHz

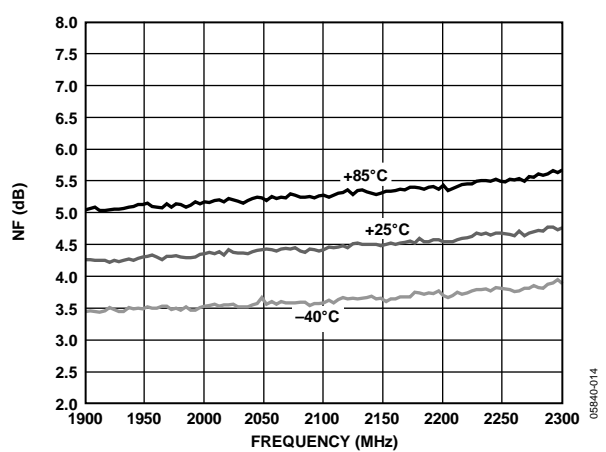


Figure 15. Noise Figure vs. Frequency and Temperature, 2060 MHz to 2200 MHz

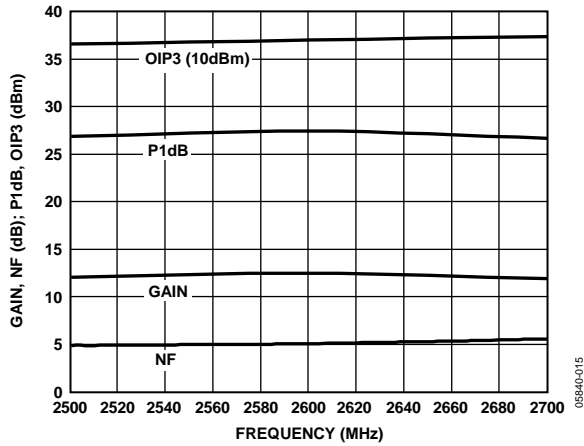


Figure 16. Gain, P1dB, OIP3, and Noise Figure vs. Frequency, 2500 MHz to 2700 MHz

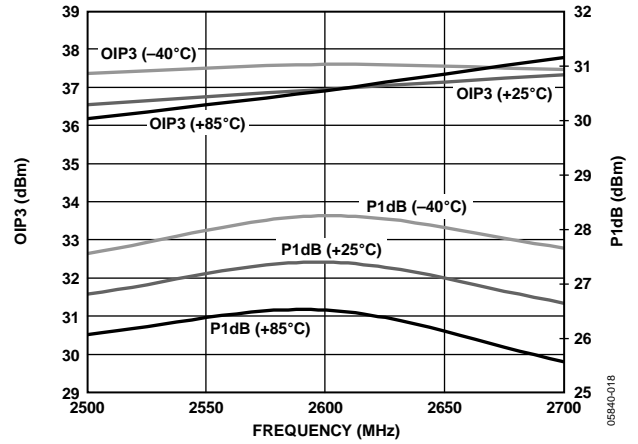


Figure 19. OIP3 and P1dB vs. Frequency and Temperature, 2500 MHz to 2700 MHz

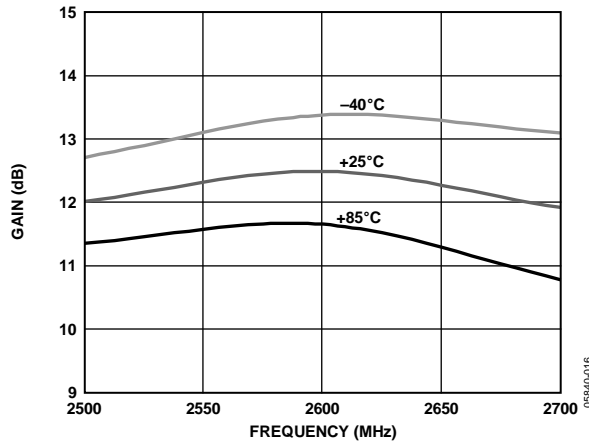


Figure 17. Gain vs. Frequency and Temperature, 2500 MHz to 2700 MHz

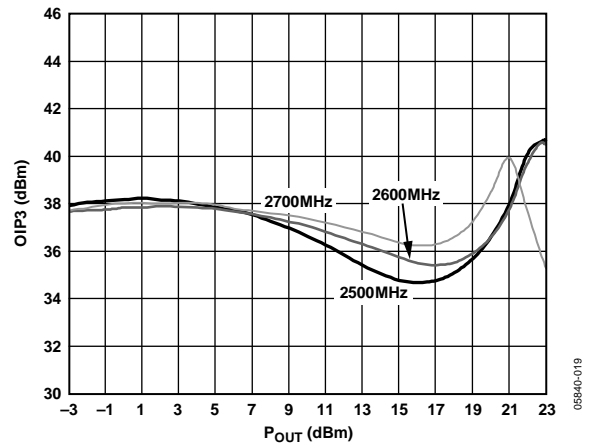


Figure 20. OIP3 vs. P_{OUT} and Frequency, 2500 MHz to 2700 MHz

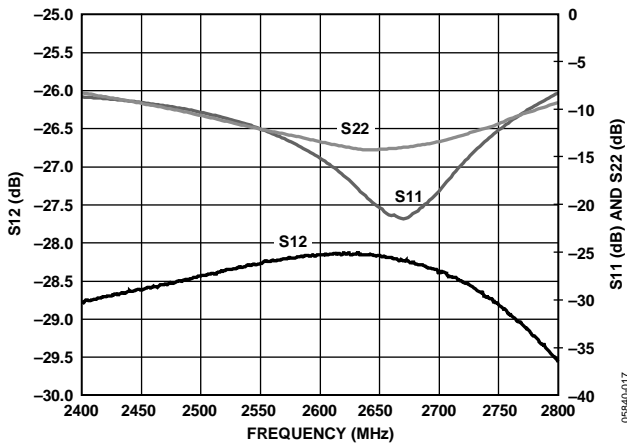


Figure 18. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency, 2500 MHz to 2700 MHz

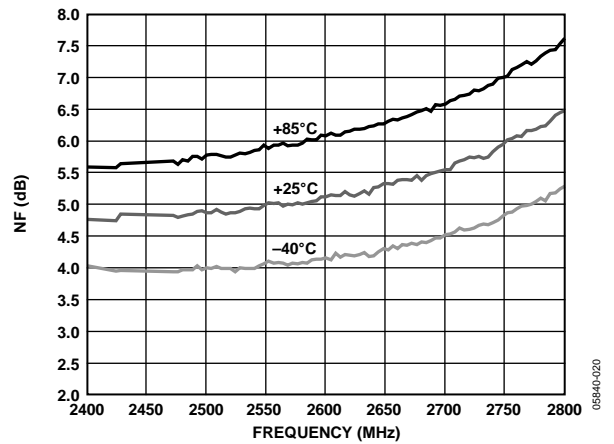


Figure 21. Noise Figure vs. Frequency and Temperature, 2500 MHz to 2700 MHz

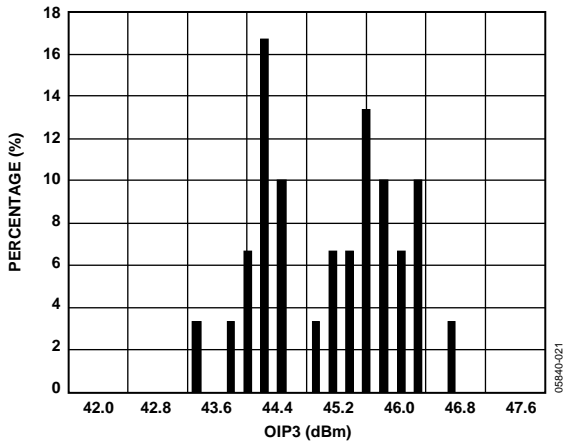


Figure 22. OIP3 Distribution at 880 MHz

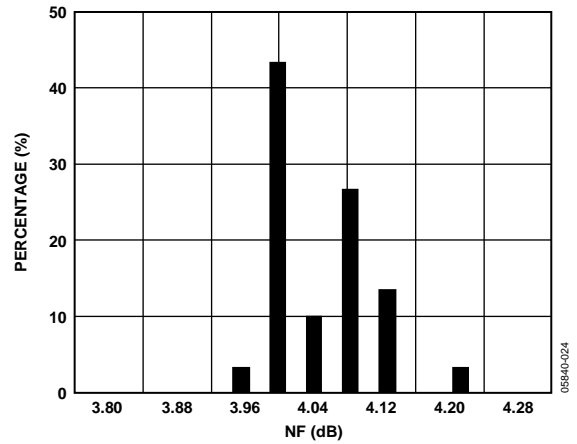


Figure 25. Noise Figure Distribution at 880 MHz

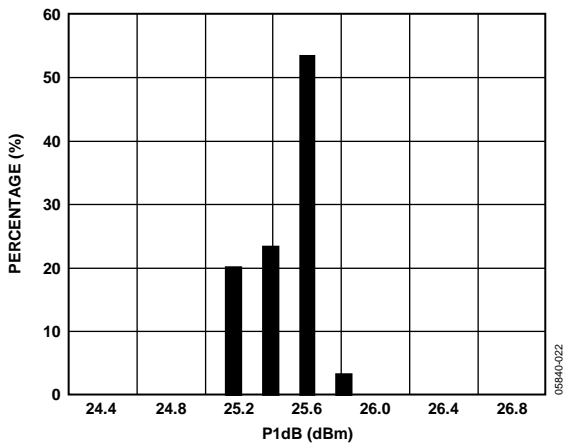


Figure 23. P1dB Distribution at 880 MHz

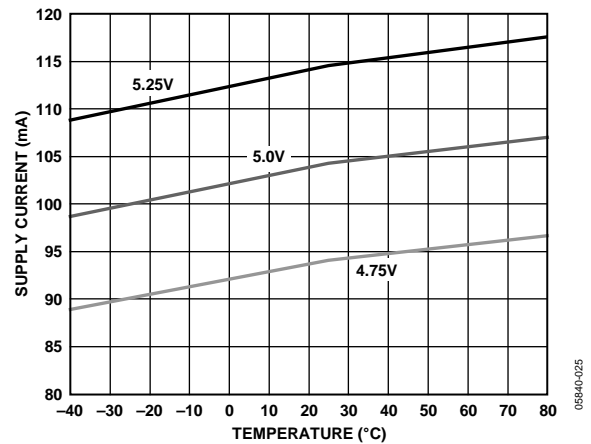


Figure 26. Supply Current vs. Supply Voltage and Temperature (Using 880 MHz Matching Components)

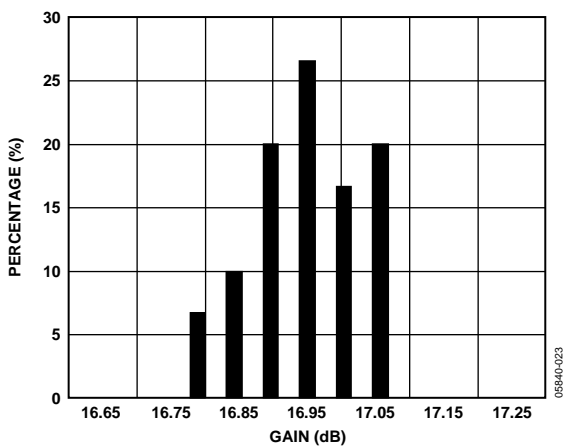


Figure 24. Gain Distribution at 880 MHz

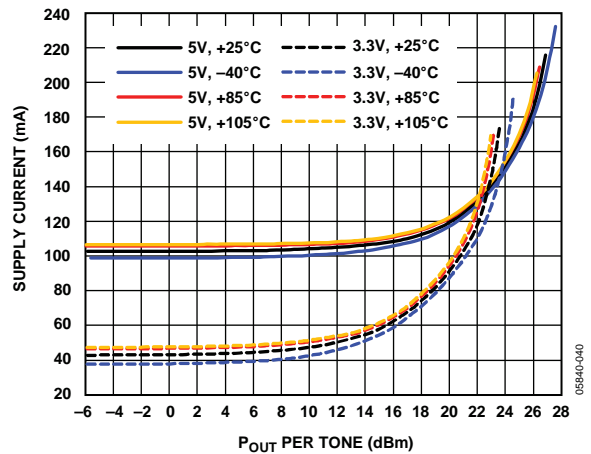


Figure 27. Supply Current vs. P_{OUT} and Temperature (2140 MHz Matching Components)

HIGH TEMPERATURE AND 3.3 V OPERATION

The ADL5320 has excellent performance at temperatures higher than 85°C. At 105°C, the gain and P1dB decrease by 0.2 dB, the OIP3 decreases by 0.4 dB, and the noise figure increases by 0.2 dB, compared with the data at 85°C. Figure 28, Figure 29, and Figure 30 show the performance at 105°C.

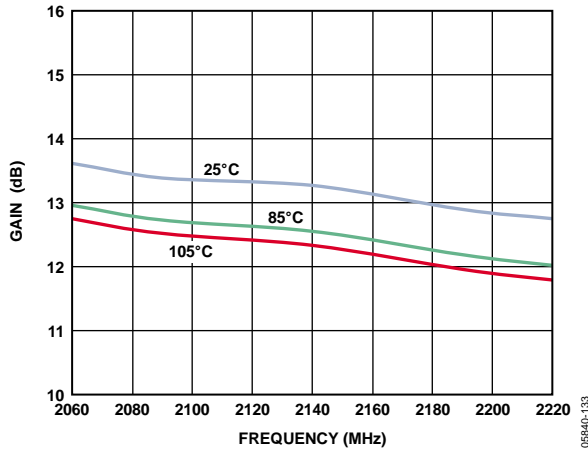


Figure 28. Gain vs. Frequency and Temperature, 5 V Supply, 2060 MHz to 2200 MHz

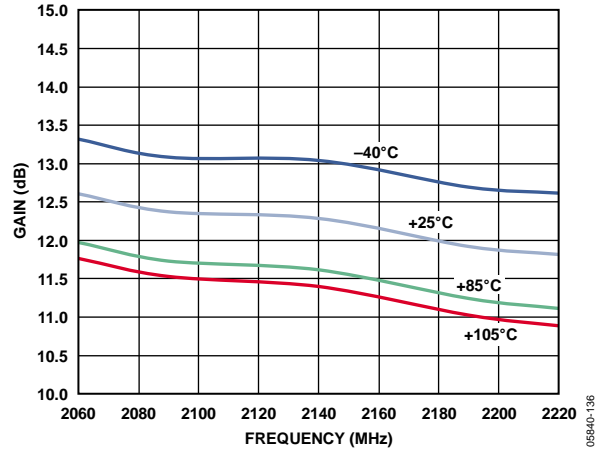


Figure 31. Gain vs. Frequency and Temperature, 3.3 V Supply, 2060 MHz to 2200 MHz

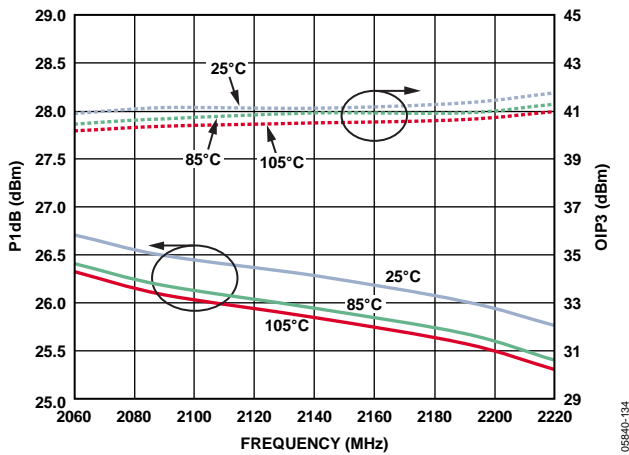


Figure 29. OIP3 and P1dB vs. Frequency and Temperature, 5 V Supply, 2060 MHz to 2200 MHz

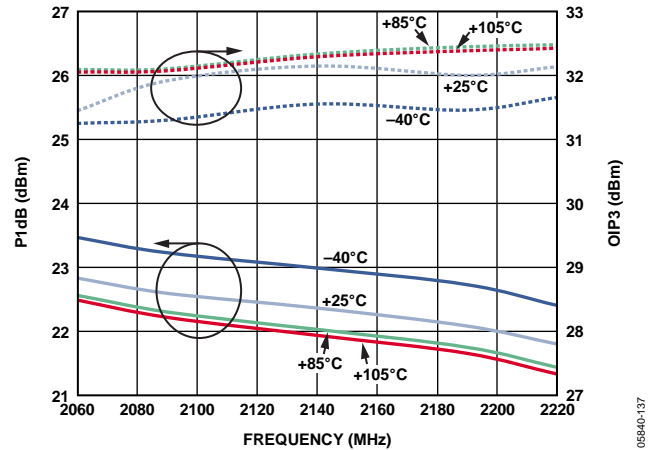


Figure 32. OIP3 and P1dB vs. Frequency and Temperature, 3.3 V Supply, 2060 MHz to 2200 MHz

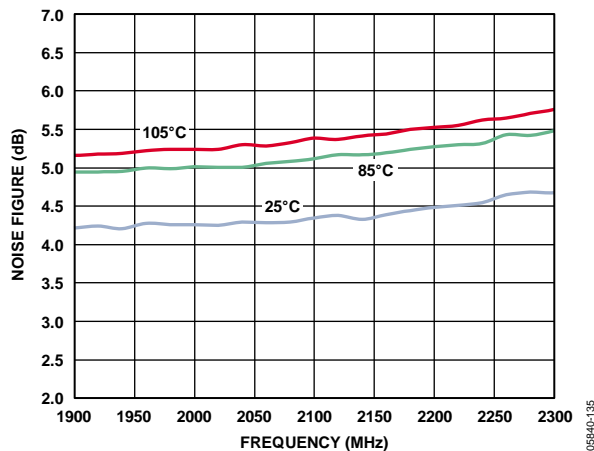


Figure 30. Noise Figure vs. Frequency and Temperature, 5 V Supply, 2060 MHz to 2200 MHz

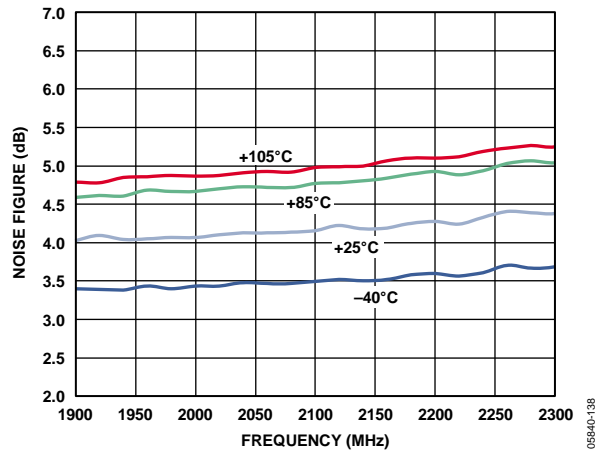


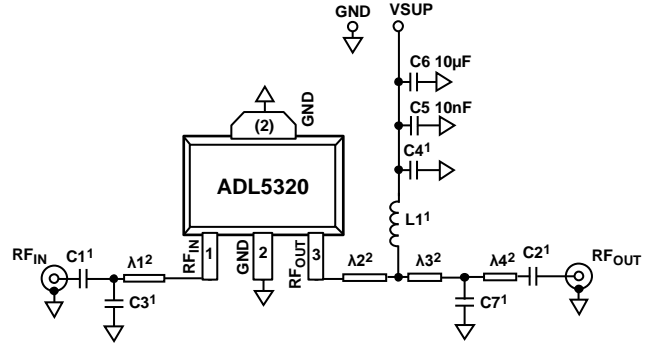
Figure 33. Noise Figure vs. Frequency and Temperature, 3.3 V Supply, 2060 MHz to 2200 MHz

APPLICATIONS INFORMATION

BASIC LAYOUT CONNECTIONS

The basic connections for operating the [ADL5320](#) are shown in Figure 34. Table 6 lists the required matching components. Capacitors C1, C2, C3, C4, and C7 are Murata GRM155 series (0402 size) and Inductor L1 is a Coilcraft 0603CS series (0603 size). For all frequency bands, the placement of C3 and C7 are critical. From 2300 MHz to 2700 MHz, the placement of C2 is also important. Table 7 lists the recommended component placement for various frequencies.

A 5 V dc bias is supplied through L1 which is connected to RF_{OUT} (Pin 3). In addition to C4, 10 nF and 10 μF power supply decoupling capacitors are also required. The typical current consumption for the [ADL5320](#) is 110 mA.



¹SEE TABLE 6 FOR FREQUENCY SPECIFIC COMPONENTS.
²SEE TABLE 7 FOR RECOMMENDED COMPONENT SPACING.

Figure 34. Basic Connections

05640-026

Table 6. Recommended Components for Basic Connections

| Frequency (MHz) | C1 (pF) | C2 (pF) | C3 (pF) | C4 (pF) | C5 (nF) | C6 (μF) | C7 (pF) | L1 (nH) |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| 450 to 500 | 100 | 100 | 18 | 100 | 10 | 10 | 6.8 | 47 |
| 800 to 960 | 47 | 47 | 6.8 | 100 | 10 | 10 | 2.2 | 47 |
| 2110 to 2170 | 22 | 22 | 0.5 | 22 | 10 | 10 | 1.5 | 15 |
| 2300 to 2400 | 12 | 2.2 | 1.2 | 12 | 10 | 10 | 1.0 | 15 |
| 2500 to 2700 | 12 | 1.0 | 1.8 | 12 | 10 | 10 | 0.5 | 15 |

Table 7. Matching Component Spacing

| Frequency (MHz) | λ1 (mils) | λ2 (mils) | λ3 (mils) | λ4 (mils) |
|-----------------|-----------|-----------|-----------|-----------|
| 450 to 500 | 391 | 75 | 364 | 50 |
| 800 to 960 | 200 | 75 | 100 | 350 |
| 2110 to 2170 | 300 | 75 | 175 | 275 |
| 2300 to 2400 | 225 | 75 | 125 | 125 |
| 2500 to 2700 | 142 | 75 | 89 | 75 |

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 35 shows the recommended land pattern for the ADL5320. To minimize thermal impedance, the exposed paddle on the SOT-89 package underside is soldered down to a ground plane along with Pin 2. If multiple ground layers exist, stitch them together using vias. For more information on land pattern design and layout, refer to the Application Note AN-772, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

The land pattern on the ADL5320 evaluation board provides a measured thermal resistance (θ_{JA}) of 35°C/W. To measure θ_{JA} , the temperature at the top of the SOT-89 package is found with an IR temperature gun. Thermal simulation suggests a junction temperature 10°C higher than the top of the package temperature. With additional ambient temperature and input/output power measurements, θ_{JA} can be determined.

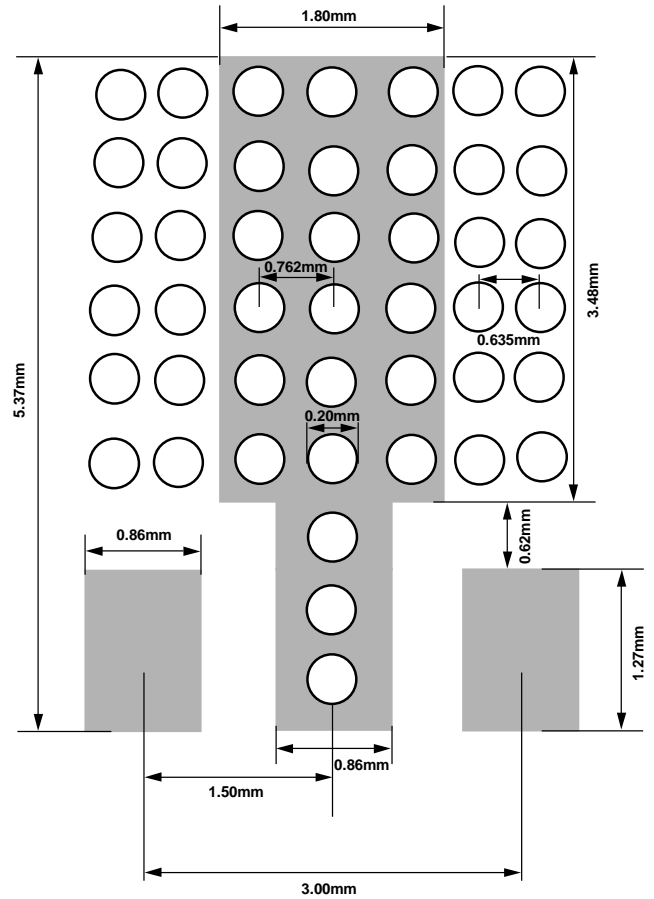


Figure 35. Recommended Land Pattern

08540041

MATCHING PROCEDURE

The ADL5320 is designed to achieve excellent gain and IP3 performance. To achieve this, both input and output matching networks must present specific impedance to the device. The matching components listed in Table 7 were chosen to provide -10 dB input return loss while maximizing OIP3. The load-pull plots (Figure 36, Figure 37, and Figure 38) show the load impedance points on the Smith chart where optimum OIP3, gain, and output power can be achieved. These load impedance values (that is, the impedance that the device sees when looking into the output matching network) are listed in Table 8 and Table 9 for maximum gain and maximum OIP3, respectively. The contours show how each parameter degrades as it is moved away from the optimum point.

From the data shown in Table 8 and Table 9, it becomes clear that maximum gain and maximum OIP3 do not occur at the same impedance. This can also be seen on the load-pull contours in Figure 36, Figure 37, and Figure 38. Thus, output matching generally involves compromising between gain and OIP3. In addition, the load-pull plots demonstrate that the quality of the output impedance match must be compromised to optimize gain and/or OIP3. In most applications, where line lengths are short and where the next device in the signal chain presents a low input return loss, compromising on the output match is acceptable.

To adjust the output match for operation at a different frequency or if a different trade-off between OIP3, gain, and output impedance is desired, the following procedure is recommended.

For example, to optimize the ADL5320 for optimum OIP3 and gain at 700 MHz, take the following steps:

1. Install the recommended tuning components for a 800 MHz to 960 MHz tuning band, but do not install C3 and C7.
2. Connect the evaluation board to a vector network analyzer so that input and output return loss can be viewed simultaneously.
3. Starting with the recommended values and positions for C3 and C7, adjust the positions of these capacitors along the transmission line until the return loss and gain are acceptable. Push-down capacitors that are mounted on small sticks can be used in this case as an alternative to soldering. If moving the component positions does not yield satisfactory results, then the values of C3 and C7 should be increased or decreased (most likely increased in this case as the user is tuning for a lower frequency). Repeat this process until the desired gain and return loss are achieved.
4. Once the desired gain and return loss are realized, OIP3 should be measured. Most likely, it will be necessary to go back and forth between return loss/gain and OIP3 measurements (probably compromising most on output return loss) until an acceptable compromise is achieved.

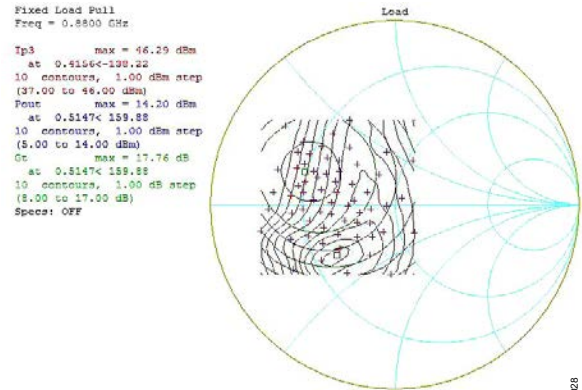


Figure 36. Load-Pull Contours, 880 MHz

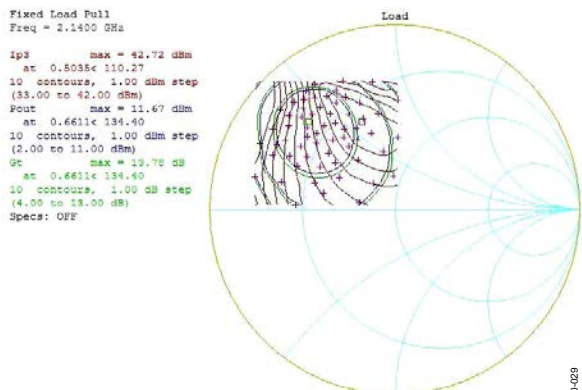


Figure 37. Load-Pull Contours, 2140 MHz

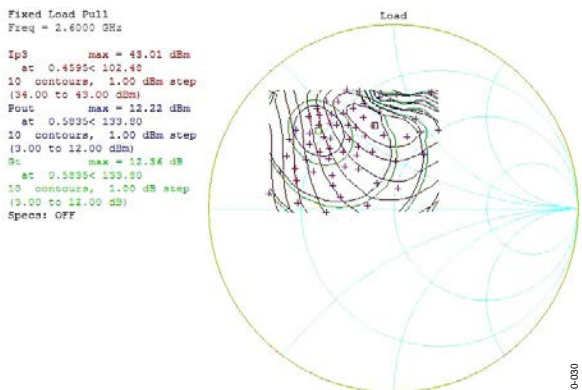


Figure 38. Load-Pull Contours, 2600 MHz

Table 8. Load Conditions for Gain_{MAX}

| Frequency (MHz) | Γ_{Load} (Magnitude) | Γ_{Load} (°) | Gain _{MAX} (dB) |
|-----------------|-----------------------------|---------------------|--------------------------|
| 880 | 0.5147 | 159.88 | 17.76 |
| 2140 | 0.6611 | 134.40 | 13.78 |
| 2600 | 0.5835 | 133.80 | 12.36 |

Table 9. Load Conditions for IP3_{MAX}

| Frequency (MHz) | Γ_{Load} (Magnitude) | Γ_{Load} (°) | IP3 _{MAX} (dBm) |
|-----------------|-----------------------------|---------------------|--------------------------|
| 880 | 0.4156 | -138.22 | 46.29 |
| 2140 | 0.5035 | +110.27 | 42.72 |
| 2600 | 0.4595 | +102.48 | 43.01 |

OPTIMIZING OP1dB

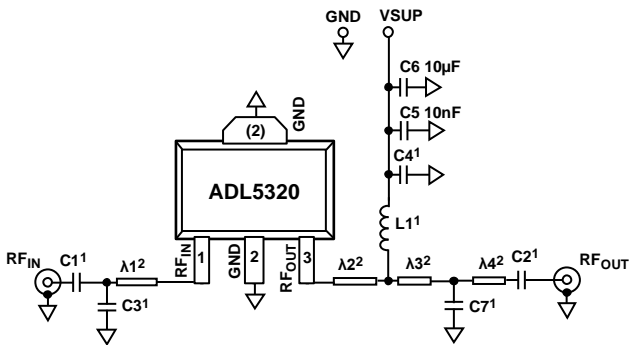
In some applications, power handling (P1dB) is a more important parameter than IP3. In such cases, it is possible to retune the output load to increase the compression point of the ADL5320. Table 10 shows the performance of the ADL5320 after tuning the output load for higher OP1dB. Table 11 lists the component spacing, and Table 12 lists the component values.

Table 10. OP1dB, Gain, and IP3 Results with Optimized OP1dB

| Frequency (MHz) | Gain (dB) | OIP3 (dBm) | OP1dB (dBm) |
|-----------------|-----------|------------|-------------|
| 880 | 17.9 | 36 | 28.5 |
| 2140 | 13.5 | 40 | 28 |
| 2600 | 12.4 | 35 | 28.2 |

Table 11. Matching Component Spacing for Optimized OP1dB

| Frequency (MHz) | $\lambda 1$ (mils) | $\lambda 2$ (mils) | $\lambda 3$ (mils) | $\lambda 4$ (mils) |
|-----------------|--------------------|--------------------|--------------------|--------------------|
| 800 to 960 | 200 | 75 | 339 | 100 |
| 2110 to 2170 | 300 | 75 | 89 | 275 |
| 2500 to 2700 | 142 | 75 | 89 | 75 |



¹SEE TABLE 12 FOR FREQUENCY SPECIFIC COMPONENTS.
²SEE TABLE 11 FOR RECOMMENDED COMPONENT SPACING.

Figure 39. Component Values and Spacing for Increased OP1dB

W-CDMA ACPR PERFORMANCE

Figure 40 shows a plot of adjacent channel power ratio (ACPR) vs. P_{OUT} for the ADL5320. The signal type being used is a single W-CDMA carrier (Test Model 1–64) at 2140 MHz. This signal is generated by a very low ACPR source. ACPR is measured at the output by a high dynamic range spectrum analyzer, which incorporates an instrument noise correction function.

The ADL5320 achieves an ACPR of –80 dBc at 0 dBm output, at which point device noise and not distortion is beginning to dominate the power in the adjacent channels. At an output power of 10 dBm, ACPR is still very low at –70 dBc, making the device particularly suitable for PA driver applications.

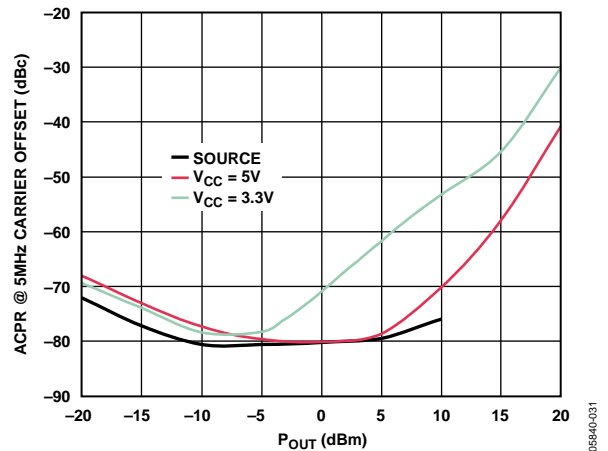


Figure 40. ACPR vs. P_{OUT}, Single Carrier W-CDMA (Test Model 1–64) at 2140 MHz Evaluation Board

Table 12. Matching Component Values for Optimized OP1dB

| Frequency (MHz) | C1 (pF) | C2 (pF) | C3 (pF) | C4 (pF) | C5 (nF) | C6 (μF) | C7 (pF) | L1 (nH) |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| 800 to 960 | 47 | 47 | 6.8 | 100 | 10 | 10 | 5.6 | 47 |
| 2110 to 2170 | 22 | 22 | 0.5 | 22 | 10 | 10 | 1.8 | 15 |
| 2500 to 2700 | 12 | 1.0 | 1.8 | 12 | 10 | 10 | 1.0 | 15 |

EVALUATION BOARD

The schematic of the ADL5320 evaluation board is shown in Figure 41. This evaluation board uses 25 mil wide traces and is made from FR4 material. The evaluation board comes tuned for operation in the 2110 MHz to 2170 MHz tuning band. Tuning options for other frequency bands are also provided in Table 13. The recommended placement for these components is provided in Table 14. The inputs and outputs should be ac-coupled with appropriately sized capacitors. DC bias is provided to the amplifier via an inductor connected to the RF_{OUT} pin. A bias voltage of 5 V is recommended.

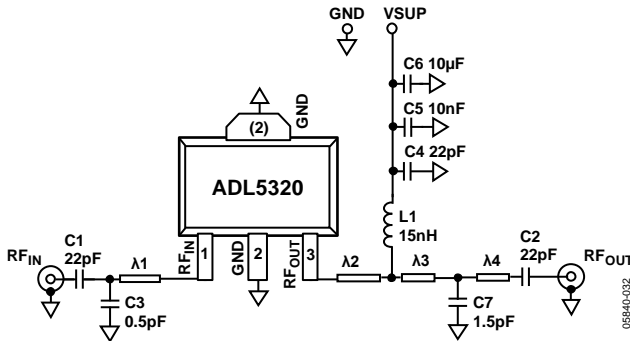


Figure 41. Evaluation Board, 2110 MHz to 2170 MHz

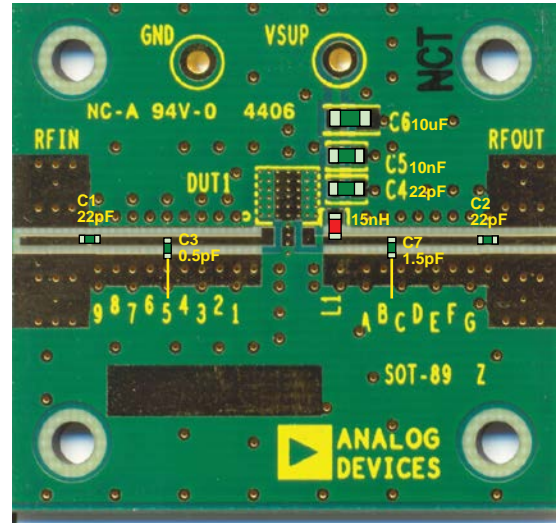


Figure 42. Evaluation Board Layout and Default Component Placement for Operation from 2110 MHz to 2170 MHz

Table 13. Evaluation Board Configuration Options

| Component | Function | 450 MHz to 500 MHz | 800 MHz to 960 MHz | 2110 MHz to 2170 MHz (Default Configuration) | 2300 MHz to 2400 MHz | 2500 MHz to 2700 MHz |
|------------|-----------------------------------|--|--|--|---|---|
| C1, C2 | AC coupling capacitors | 0402, 100 pF | 0402, 47 pF | 0402, 22pF | C1= 0402 12 pF, C2 = 0402 2.2 pF | C1 = 0402 12 pF, C2 = 0402 1.0 pF |
| C4, C5, C6 | Power supply bypassing capacitors | C4 = 0603 100 pF, C5 = 0603 10 nF, C6 = 1206 10 μF | C4 = 0603 100 pF, C5 = 0603 10 nF, C6 = 1206 10 μF | C4 = 0402 22pF, C5 = 0603 10 nF, C6 = 1206 10 μF | C4 = 0603 12 pF, C5 = 0603 10 nF, C6 = 1206 10 μF | C4 = 0603 12 pF, C5 = 0603 10 nF, C6 = 1206 10 μF |
| L1 | DC bias inductor | 0603, 47 nH | 0603, 47 nH | 0603, 15 nH | 0603, 15 nH | 0603, 15 nH |
| C3, C7 | Tuning capacitors | C3 = 0402 18 pF, C7 = 0402 6.8 pF | C3 = 0402 6.8 pF, C7 = 0402 2.2 pF | C3 = 0402 0.5 pF, C7 = 0402 1.5 pF | C3 = 0402 1.2 pF, C7 = 0402 1.0 pF | C3 = 0402 1.8 pF, C7 = 0402 0.5 pF |
| R1 | | | | | R1 = 0402 0 Ω | R1 = 0402 0 Ω |
| VSUP, GND | Power supply connections | VSUP red test loop, GND black test loop | VSUP red test loop, GND black test loop | VSUP red test loop, GND black test loop | VSUP red test loop, GND black test loop | VSUP red test loop, GND black test loop |

Table 14. Recommended Component Spacing on Evaluation Board

| Frequency (MHz) | λ1 (mils) | λ2 (mils) | λ3 (mils) | λ4 (mils) |
|-----------------|-----------|-----------|-----------|-----------|
| 450 to 500 | 391 | 75 | 364 | 50 |
| 800 to 960 | 200 | 75 | 100 | 350 |
| 2110 to 2170 | 300 | 75 | 175 | 275 |
| 2300 to 2400 | 225 | 75 | 125 | 125 |
| 2500 to 2700 | 142 | 75 | 89 | 75 |

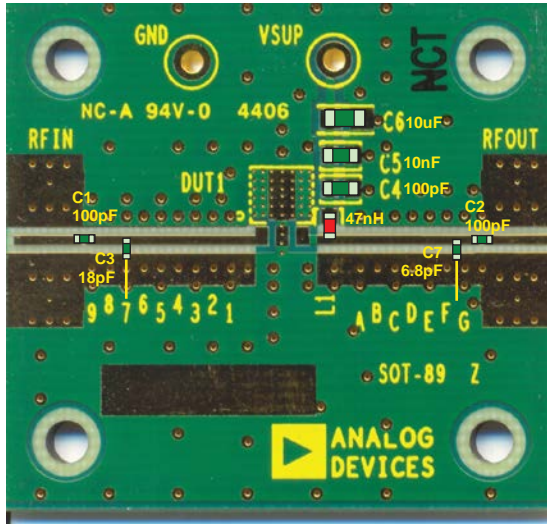


Figure 43. Evaluation Board Layout and Component Placement
450 MHz to 500 MHz Operation

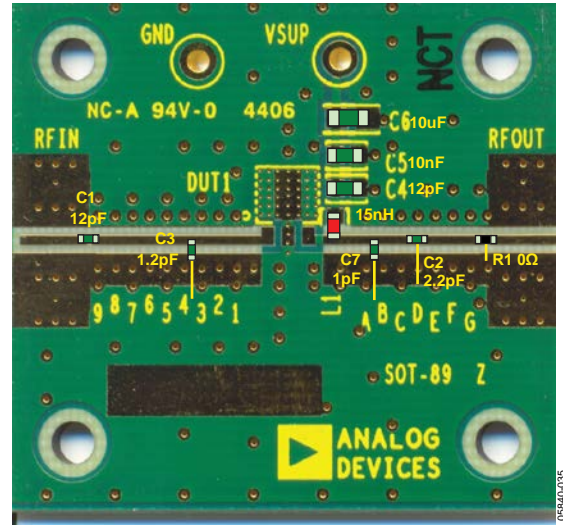


Figure 45. Evaluation Board Layout and Component Placement
2300 MHz to 2400 MHz Operation

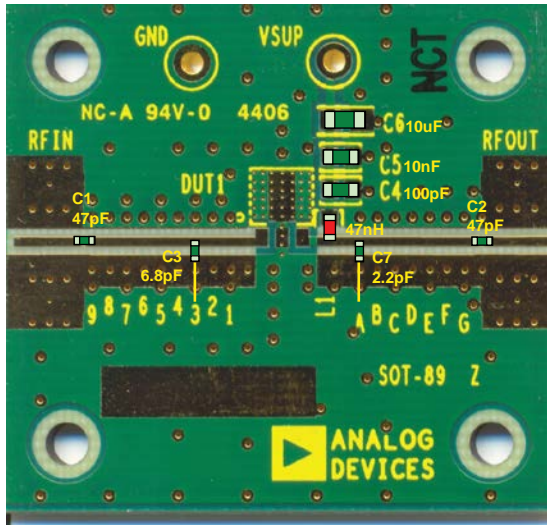


Figure 44. Evaluation Board Layout and Component Placement
800 MHz to 960 MHz Operation

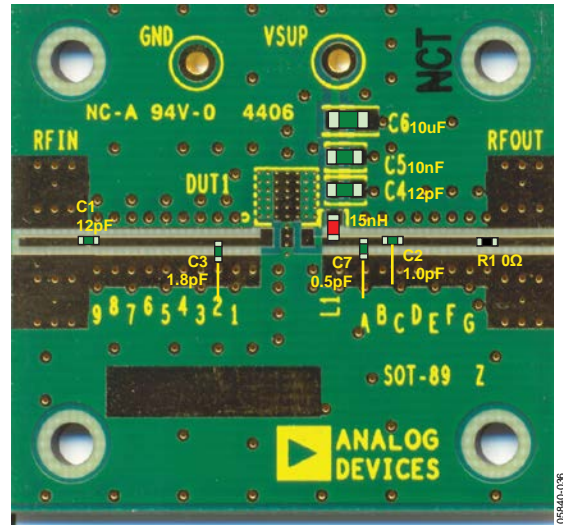
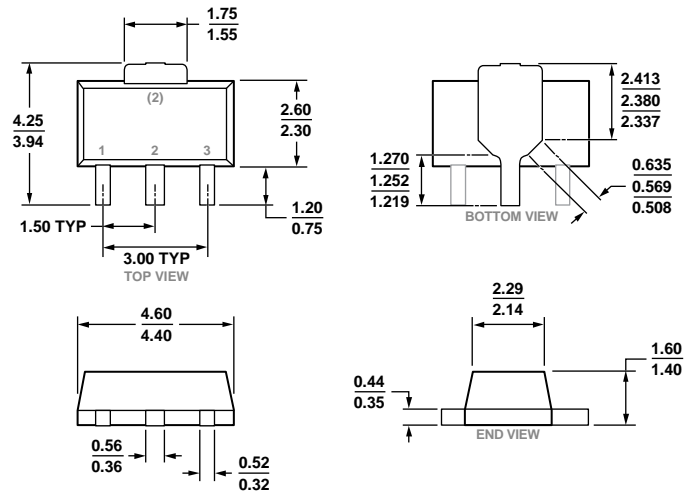


Figure 46. Evaluation Board Layout and Component Placement
2500 MHz to 2700 MHz Operation

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS TO-243

Figure 47. 3-Lead Small Outline Transistor Package [SOT-89] (RK-3)
Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---------------------------------|----------------|
| ADL5320ARKZ-R7 | -40°C to +105°C | 3-Lead SOT-89, 7" Tape and Reel | RK-3 |
| ADL5320-EVALZ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.

NOTES

NOTES