Texas Instruments

INA165x SoundPlus™ High Common-Mode Rejection Line Receivers

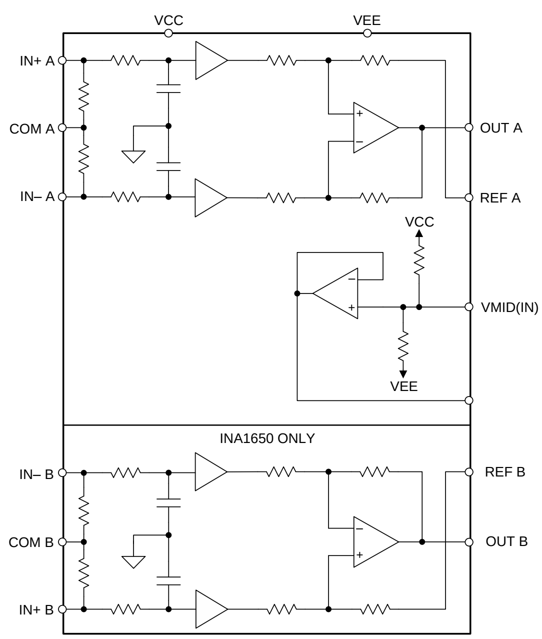
1 Features

- High Common-Mode Rejection: 91 dB (Typical)
- High Input Impedance: 1-MΩ Differential
- Ultra-Low Noise: –104.7 dBu, Unweighted
- Ultra-Low Total Harmonic Distortion + Noise: –120 dB THD+N (22 dBu, 22-kHz Bandwidth)
- Wide Bandwidth: 2.7 MHz
- Low Quiescent Current: 6 mA (INA1651, Typical)
- Short-Circuit Protection
- Integrated EMI Filters
- Wide Supply Range: ±2.25 V to ±18 V
- Available in Small 14-Pin TSSOP Package

2 Applications

- Differential Audio Interfaces
- Audio Input Circuitry
- Line Drivers
- Audio Power Amplifiers
- Audio Analyzers
- High-End Audio and Video (A/V) Receivers

INA165x Simplified Internal Schematic



3 Description

The dual-channel INA1650 and single-channel INA1651 (INA165x) SoundPlus™ audio line receivers achieve an extremely-high common-mode rejection ratio (CMRR) of 91 dB while maintaining an ultra-low THD+N of –120 dB at 1 kHz for 22-dBu signal levels. Precision matching of on-chip resistors give the INA165x devices excellent CMRR performance. These resistors have matching that is far superior compared to external components, and are immune to mismatches introduced by printed circuit board (PCB) layout. Unlike other line receiver products, the INA165x CMRR is characterized over temperature and tested in production to deliver consistent performance in a wide variety of applications.

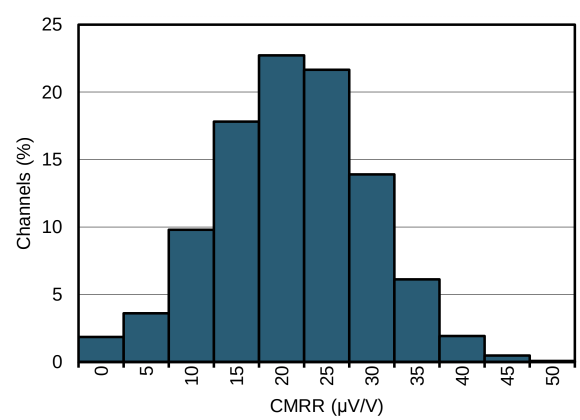
The INA165x devices operate over a very-wide-supply range of ±2.25 V to ±18 V, on 10.5 mA of supply current. In addition to the line-receiver channels, a buffered mid-supply reference output is included, making the INA165x configurable for dual- or single-supply applications. The mid-supply output can be used as a bias voltage for other analog circuitry in the signal chain. These devices are specified from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA1650	TSSOP (14)	4.40 mm × 5.00 mm
INA1651	TSSOP (14)	4.40 mm × 5.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

CMRR Histogram (5746 Channels)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2018) to Revision B — **Page**

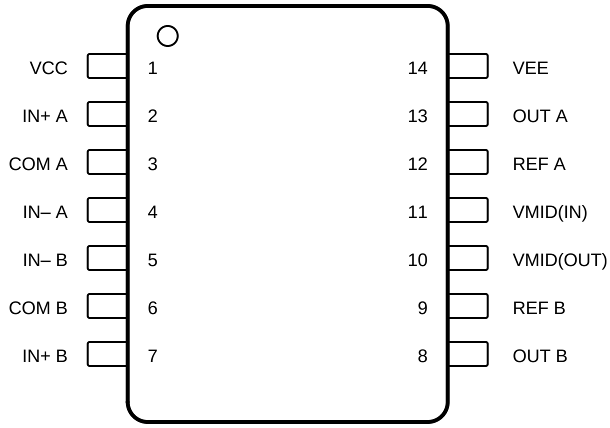
- Changed INA1651 device from product preview to production data (active) ... 1

Changes from Original (September 2018) to Revision A — **Page**

- Added new INA1651 as advance information ... 1

5 Pin Configuration and Functions

INA1650 PW Package
14-Pin TSSOP
Top View



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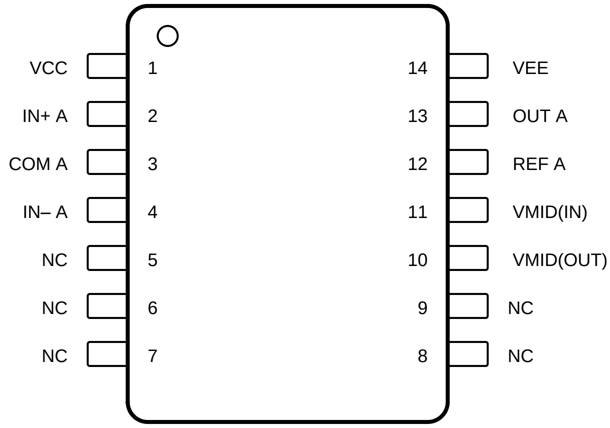
Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COM A	3	I	Input common, channel A
COM B	6	I	Input common, channel B
IN+ A	2	I	Noninverting input, channel A
IN– A	4	I	Inverting input, channel A
IN+ B	7	I	Noninverting input, channel B
IN– B	5	I	Inverting input, channel B
OUT A	13	O	Output, channel A
OUT B	8	O	Output, channel B
REF A	12	I	Reference input, channel A. This pin must be driven from a low impedance.
REF B	9	I	Reference input, channel B. This pin must be driven from a low impedance.
VCC	1	—	Positive (highest) power supply
VEE	14	—	Negative (lowest) power supply
VMID(IN)	11	I	Input node of internal supply divider. Connect a capacitor to this pin to reduce noise from the supply divider circuit.
VMID(OUT)	10	O	Buffered output of internal supply divider.

INA1651 PW Package
14-Pin TSSOP
Top View



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Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COM A	3	I	Input common, channel A
IN+ A	2	I	Noninverting input, channel A
IN– A	4	I	Inverting input, channel A
NC	5	—	No internal connection
NC	6	—	No internal connection
NC	7	—	No internal connection
NC	8	—	No internal connection
NC	9	—	No internal connection
OUT A	13	O	Output, channel A
REF A	12	I	Reference input, channel A. This pin must be driven from a low impedance.
VCC	1	—	Positive (highest) power supply
VEE	14	—	Negative (lowest) power supply
VMID(IN)	11	I	Input node of internal supply divider. Connect a capacitor to this pin to reduce noise from the supply divider circuit.
VMID(OUT)	10	O	Buffered output of internal supply divider.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)		40	V
	Input voltage (Signal inputs, enable, ground)	(V–) – 0.5	(V+) + 0.5	
	Input differential voltage		(V+) – (V–)	
Current	Input current (all pins except power-supply pins)		±10	mA
	Output short-circuit[2]	Continuous		
Temperature	Operating, T_A	–55	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2 (ground in symmetrical dual supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
INA1650				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	
INA1651				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		INA1650	INA1651	UNIT
		PW (TSSOP)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.0	99.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.6	29.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.4	42.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.6	42.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics:

at T_A = 25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
THD+N	Total harmonic distortion + noise	V_O = 3 V_{RMS}, f = 1kHz, 90-kHz measurement bandwidth, V_S = ±18 V		0.00039%		
				–108.1		dB
		V_{IN} = 22 dBu (9.7516 V_{RMS}) , F_{IN} = 1 kHz, V_S = ±18 V, 90-kHz measurement bandwidth		0.000174%		
				–115.2		dB
IMD	Intermodulation distortion	SMPTE and DIN two-tone, 4:1 (60 Hz and 7 kHz) V_O = 3 V_{RMS}, 90-kHz measurement bandwidth		0.0005%		
				–106.1		dB
		CCIF twin-tone (19 kHz and 20 kHz), V_O = 3 V_{RMS}, 90-kHz measurement bandwidth		0.00066%		
				–103.6		dB
AC PERFORMANCE						
BW	Small-signal bandwidth			2.7		MHz
SR	Slew rate			10		V/µs
	Full-power bandwidth (1)	V_O = 1 V_P		1.59		MHz
PM	Phase margin	C_L = 20 pF		71°		
		C_L = 200 pF		54°		
t_s	Settling time	To 0.01%, V_s = ±18 V, 10-V step		2.2		µs
	Overload recovery time			330		ns
	Channel separation	f = 1 kHz, REF and COM pins connected to ground		140		dB
		f = 1 kHz, REF and COM pins connected to VMID(OUT)		130		dB
	EMI/RFI filter corner frequency			80		MHz
NOISE						
	Output voltage noise	f = 20 Hz to 20 kHz, no weighting		4.5		μV_{RMS}
				–104.7		dBu
e_n	Output voltage noise density (2)	f = 100 Hz		47		nV/√Hz
		f = 1 kHz		31		
OFFSET VOLTAGE						
V_{OS}	Output offset voltage			±1	±3	mV
		T_A = –40°C to +125°C (2)			±4	
dV_{OS}/dT	Output offset voltage drift (2)	T_A = –40°C to +125°C		2	7	µV/°C
PSRR	Power-supply rejection ratio			2		µV/V
GAIN						
	Gain			1		V/V
	Gain error			0.04%	0.05%	
		T_A = –40°C to +125°C (2)		0.05%	0.06%	
	Gain nonlinearity	V_S = ±18 V, –10 V < V_O < 10 V (2)		1	5	ppm
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) + 0.25		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) + 0.25 V ≤ V_{CM} ≤ (V+) – 2 V, REF and COM pins connected to ground, V_S = ±18 V	85	91		dB
		T_A = –40°C to +125°C (2)	82	89		
		(V–) + 0.25 V ≤ V_{CM} ≤ (V+) – 2 V, REF and COM pins connected to VMID(OUT), V_S = ±18 V	82	86		
		T_A = –40°C to +125°C (2)	76	84		
CMRR	Common-mode rejection ratio	(V–) + 0.25 V ≤ V_{CM} ≤ (V+) – 2 V, REF and COM pins connected to ground, V_S = ±18 V, R_S mismatch = 20 Ω		84		dB

(1) Full-power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.

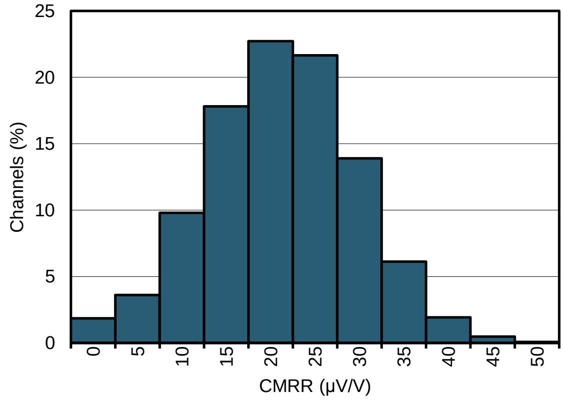
Electrical Characteristics: (continued)

at T_A = 25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT IMPEDANCE							
	Differential			850	1000	1150	kΩ
	Common-mode			212.5	250	287.5	kΩ
	Input resistance mismatch				0.01%	0.25%	
SUPPLY DIVIDER CIRCUIT							
	Nominal output voltage				[(V+) + (V–)] / 2		V
	Output voltage offset	VMID(IN) = ((V+) + (V–) / 2			2	4	mV
	Input impedance	VMID(IN) pin, f = 1 kHz			250		kΩ
	Output resistance	VMID(OUT) pin			0.35		Ω
	Output voltage noise	20 Hz to 20 kHz, C_{MID} = 1 µF			1.56		$µV_{RMS}$
	Output capacitive load limit	Phase margin > 45°, R_{ISO} = 0 Ω			150		pF
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	R_L = 2 kΩ		350		mV
			R_L = 600 Ω		1100		
		Negative rail	R_L = 2 kΩ		430		
			R_L = 600 Ω		1300		
Z_{OUT}	Output impedance	f ≤ 100 kHz, I_{OUT} = 0 A			< 1		Ω
I_{SC}	Short-circuit current	V_S = ±18 V			±75		mA
C_{LOAD}	Capacitive load drive				See Figure 19		pF
POWER SUPPLY							
I_Q	Quiescent current	I_{OUT} = 0 A, INA1651		4.6	6	6.9	mA
			T_A = –40°C to +125°C(2)			8	
		I_{OUT} = 0 A, INA1650		8	10.5	12	
			T_A = –40°C to +125°C(2)			14	

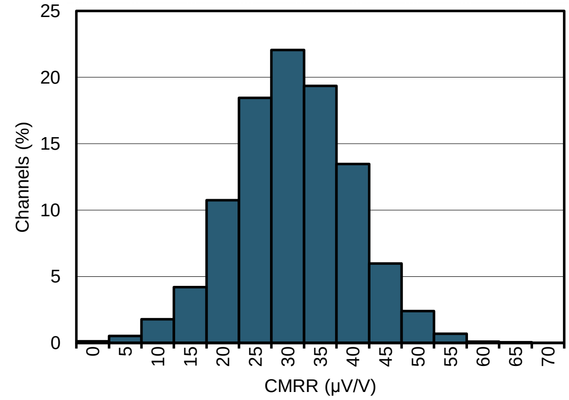
6.6 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)



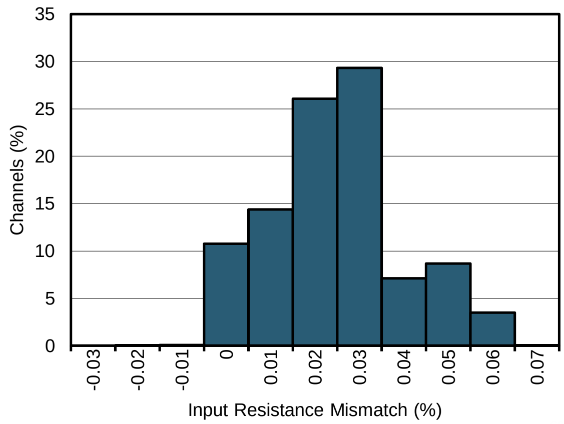
5746 Channels
V_{REF} Pins Connected to Ground

Figure 1. Common-Mode Rejection Ratio Distribution



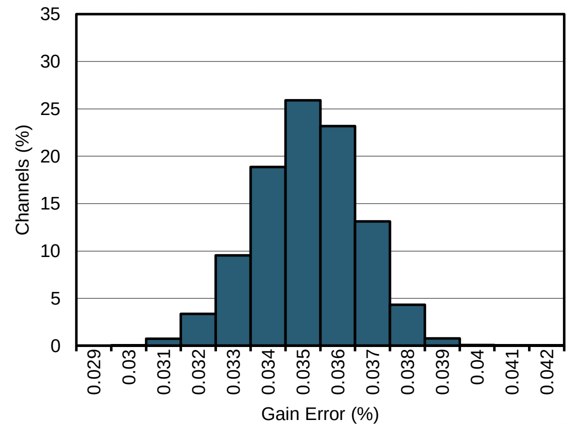
5746 Channels
V_{REF} Pins Connected to $V_{MID(OUT)}$

Figure 2. Common-Mode Rejection Ratio Distribution



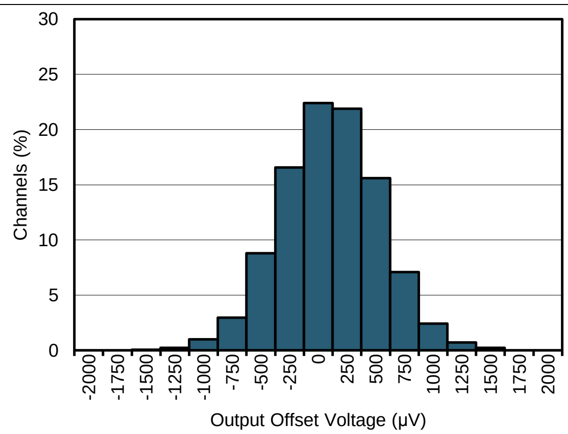
5746 Channels

Figure 3. Distribution of Mismatch in 500-kΩ Input Resistors



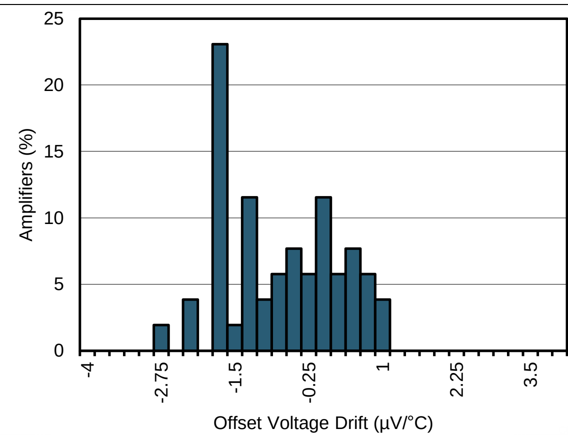
5746 Channels

Figure 4. Gain Error Distribution



5746 Channels

Figure 5. Offset Voltage Distribution



52 Channels

Figure 6. Offset Voltage Drift Distribution

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)

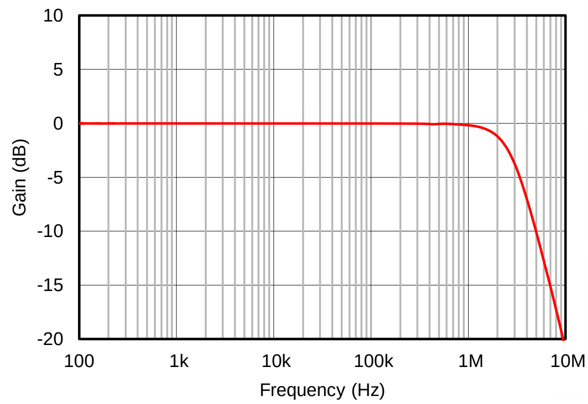


Figure 7. Frequency Response

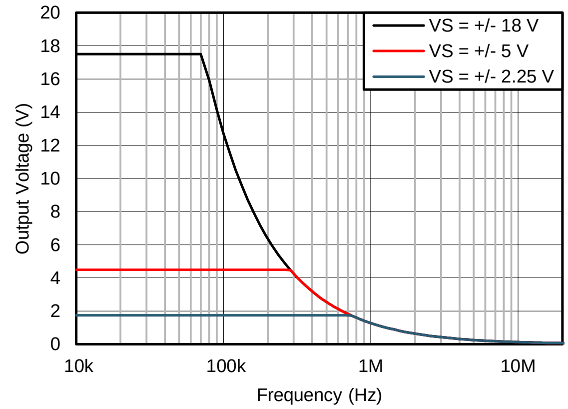


Figure 8. Maximum Output Voltage vs Frequency

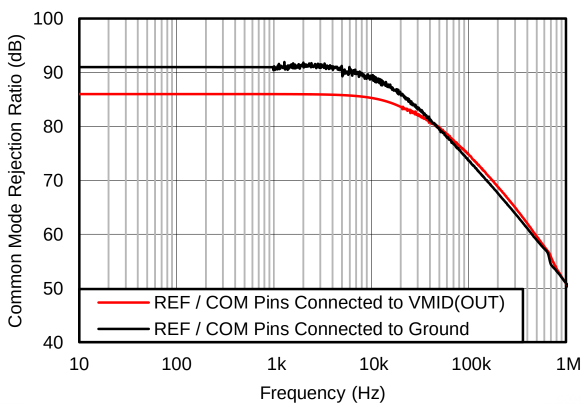


Figure 9. Common-Mode Rejection Ratio vs Frequency

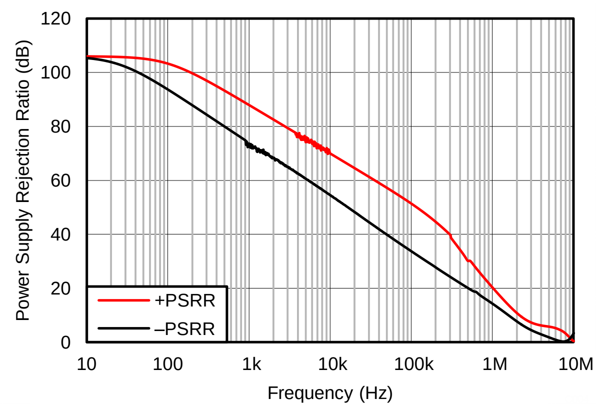


Figure 10. Power Supply Rejection Ratio vs Frequency

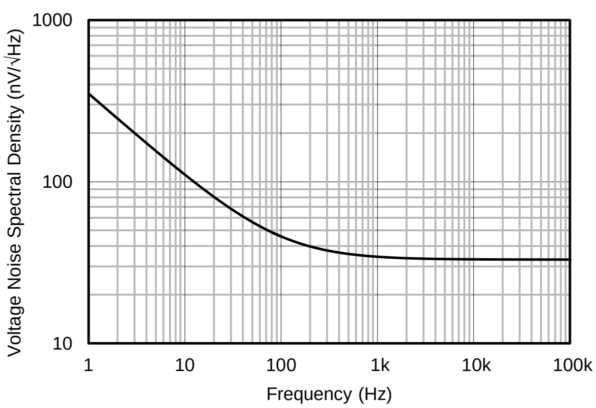
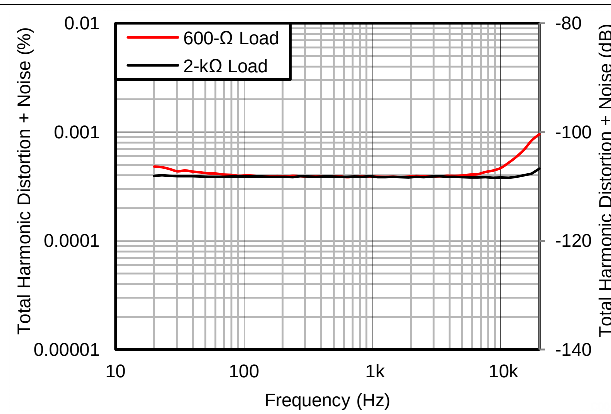


Figure 11. Voltage Noise Spectral Density

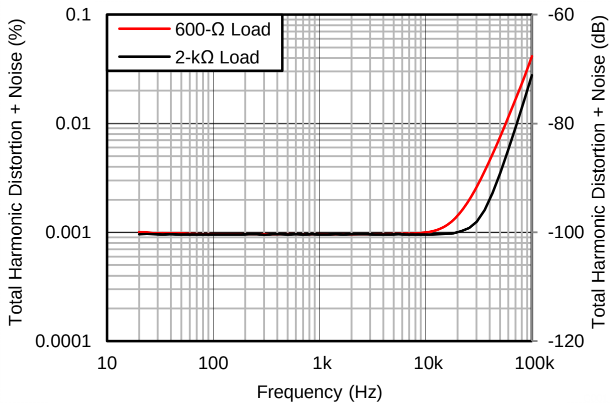


3 V_{RMS}, 90-kHz Measurement Bandwidth

Figure 12. THD+N vs Frequency

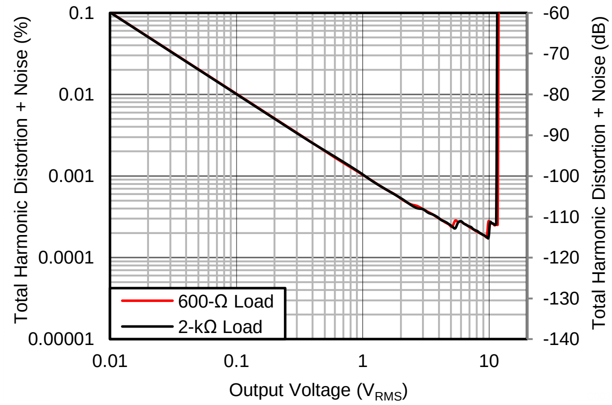
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)



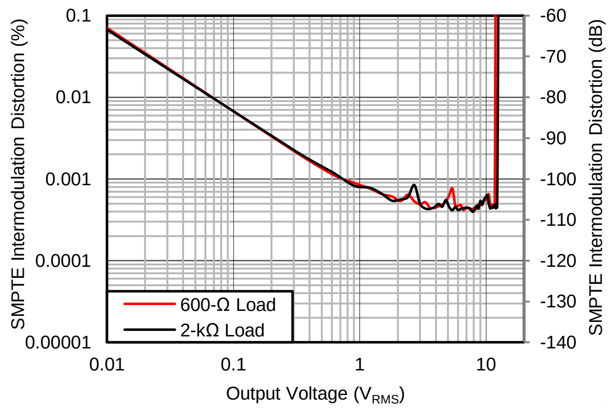
3 V_{RMS}, 500-kHz Measurement Bandwidth

Figure 13. THD+N vs Frequency



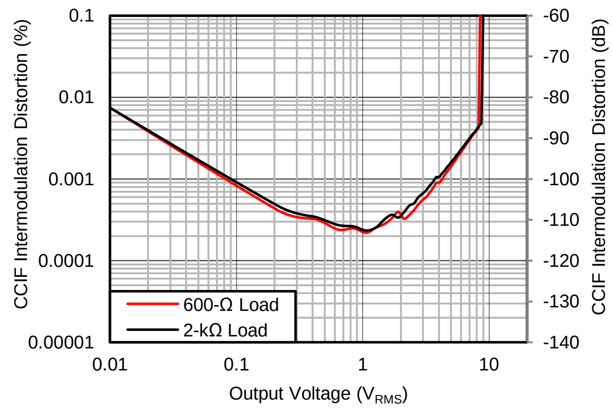
1 kHz, 90-kHz Measurement Bandwidth

Figure 14. THD+N vs Output Amplitude



SMPTE 4:1 60 Hz and 7 kHz, 90-kHz Measurement Bandwidth

Figure 15. SMPTE Intermodulation Distortion vs Output Amplitude



CCIF 19 kHz and 20 kHz, 90-kHz Measurement Bandwidth

Figure 16. CCIF Intermodulation Distortion vs Output Amplitude

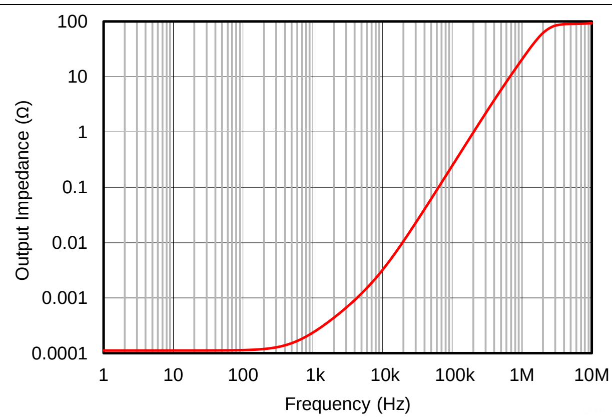
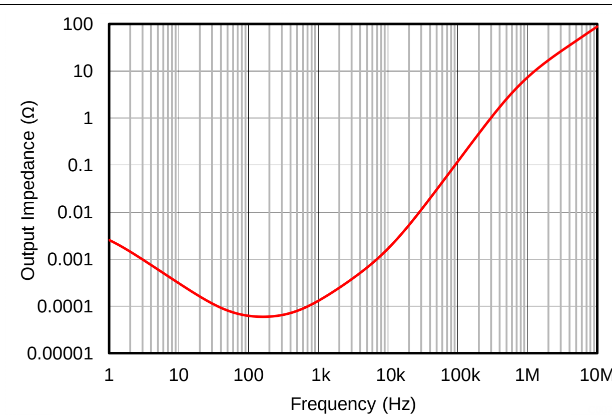


Figure 17. Signal Path Output Impedance vs Frequency

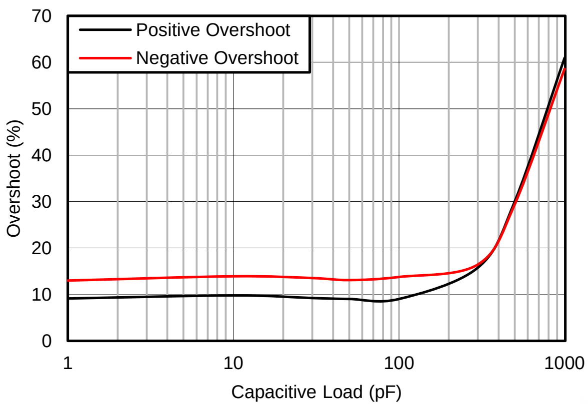


C_F = 1 µF

Figure 18. Supply Divider Output Impedance vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)



100-mV Input Step

Figure 19. Overshoot vs Capacitive Load

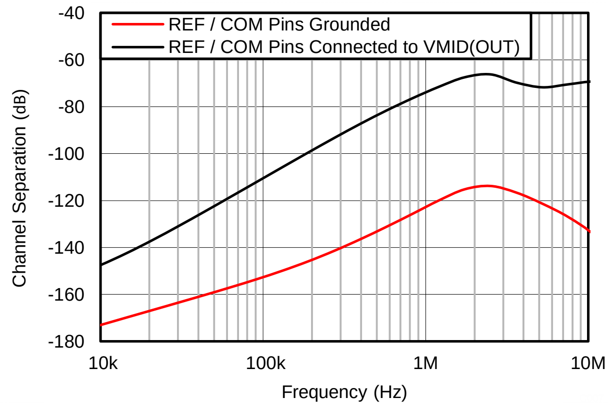
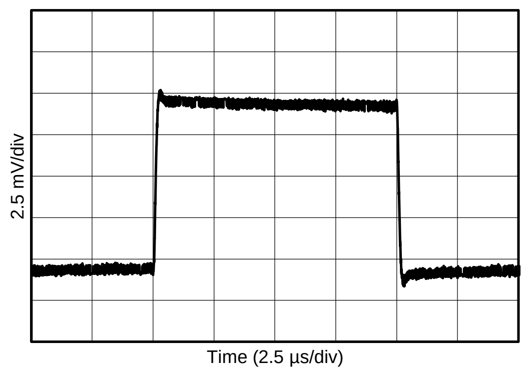
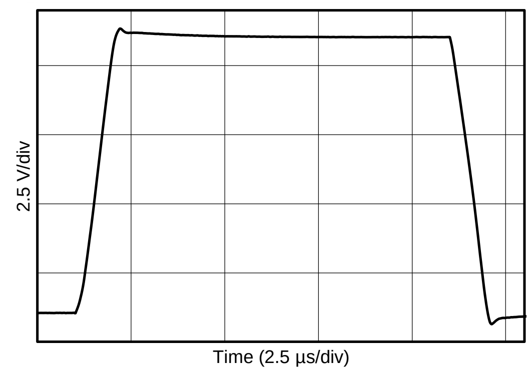


Figure 20. Channel Separation vs Frequency



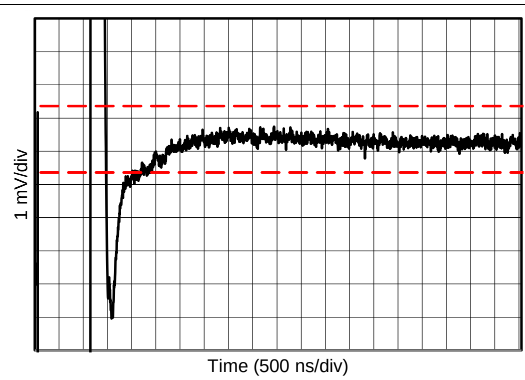
10-mV Input Step

Figure 21. Small-Signal Step Response



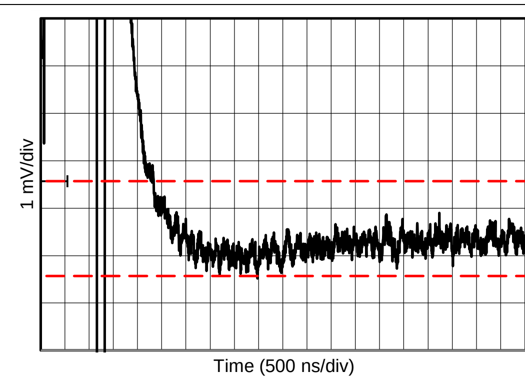
10-V Input Step

Figure 22. Large-Signal Step Response



10-V Input Step, 0.01% Settling = ± 1 mV

Figure 23. Rising-Edge Settling Time



10-V Input Step, 0.01% Settling = ± 1 mV

Figure 24. Falling-Edge Settling Time

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)

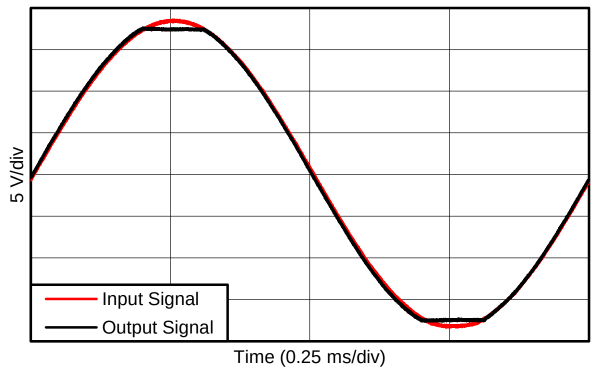
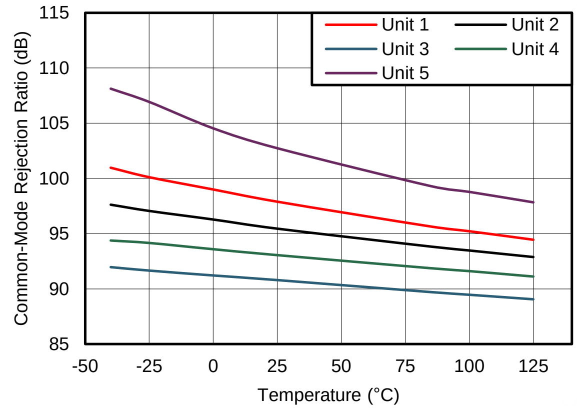
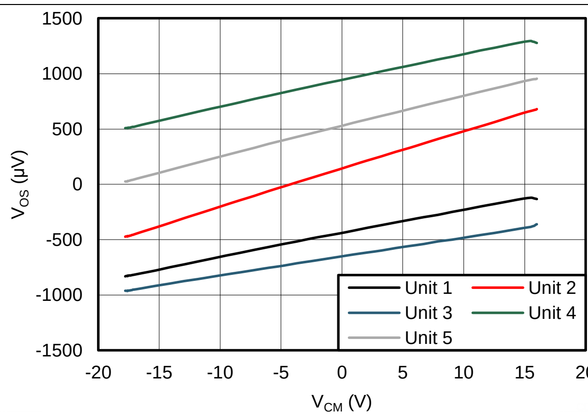


Figure 25. No Phase Reversal



5 Typical Units

Figure 26. CMRR vs Temperature



5 Typical Units

Figure 27. Output Offset Voltage vs Common-Mode Voltage

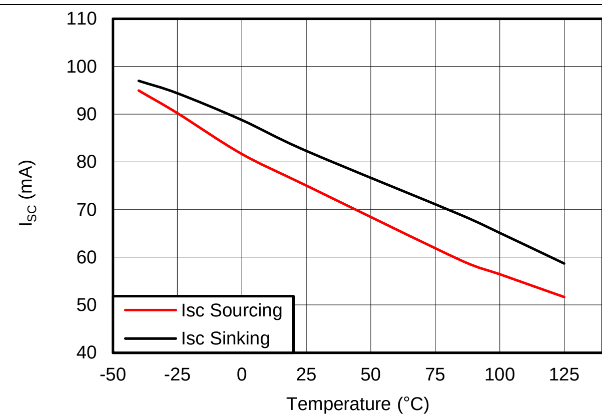


Figure 28. Short-Circuit Current vs Temperature

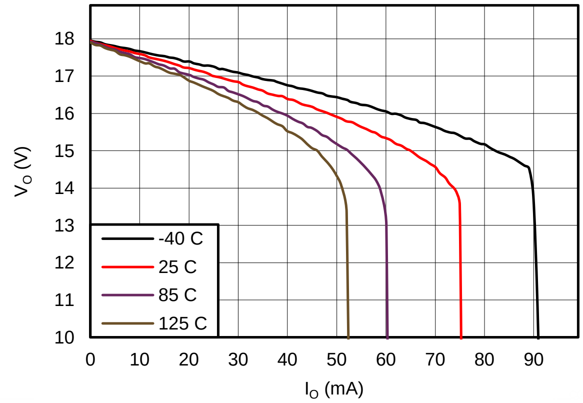


Figure 29. Positive Output Voltage vs Output Current

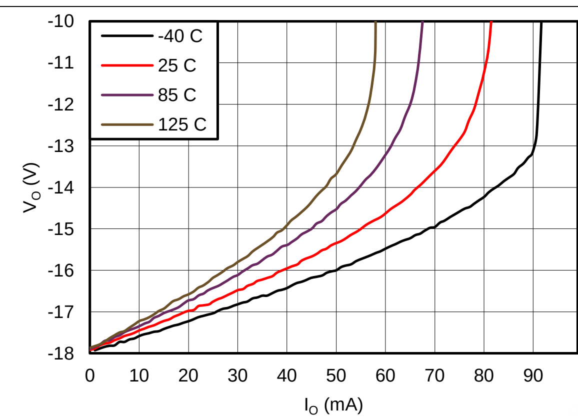


Figure 30. Negative Output Voltage vs Output Current

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)

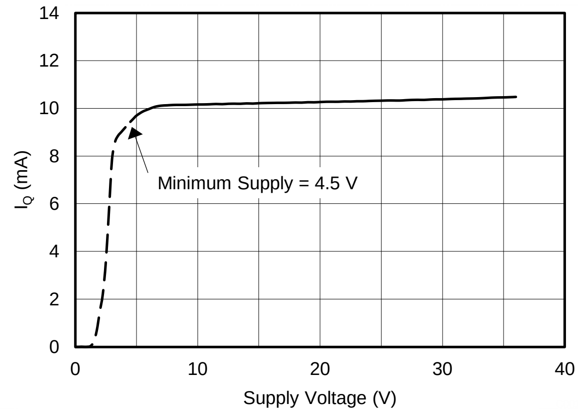


Figure 31. Power Supply Current vs Power Supply Voltage

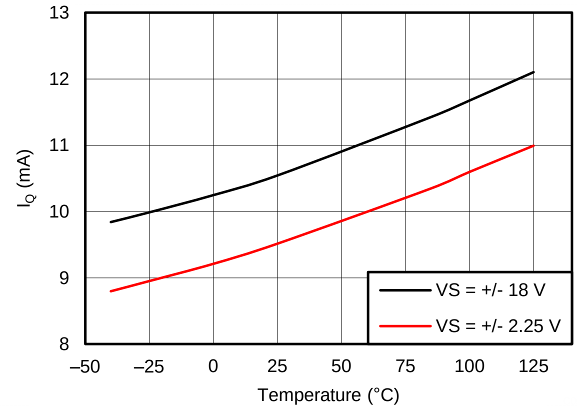


Figure 32. Power Supply Current vs Temperature

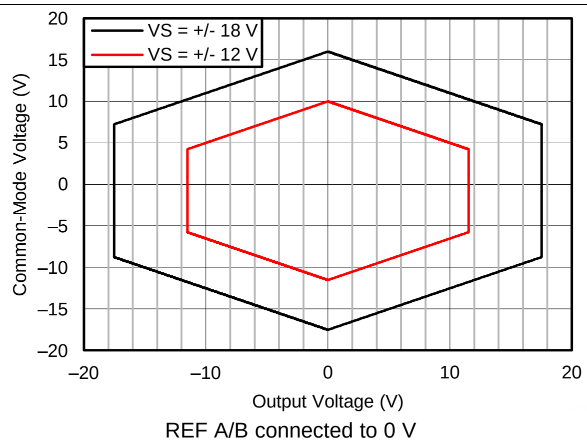


Figure 33. Input Common-Mode Voltage vs Output Voltage

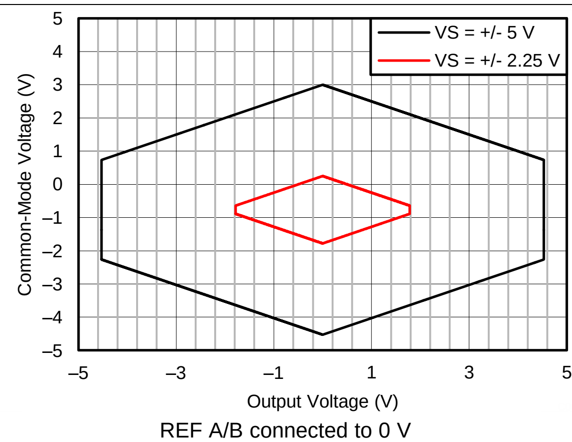


Figure 34. Input Common-Mode Voltage vs Output Voltage

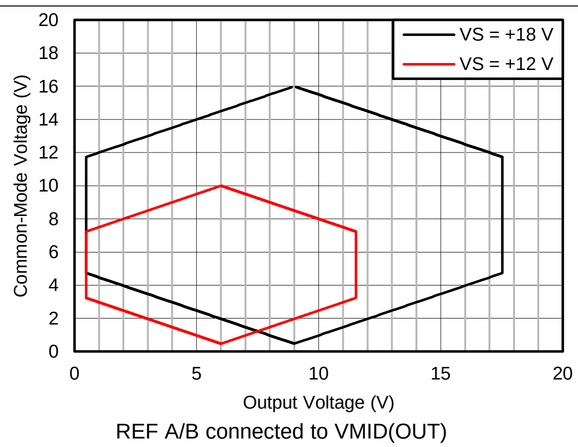


Figure 35. Input Common-Mode Voltage vs Output Voltage

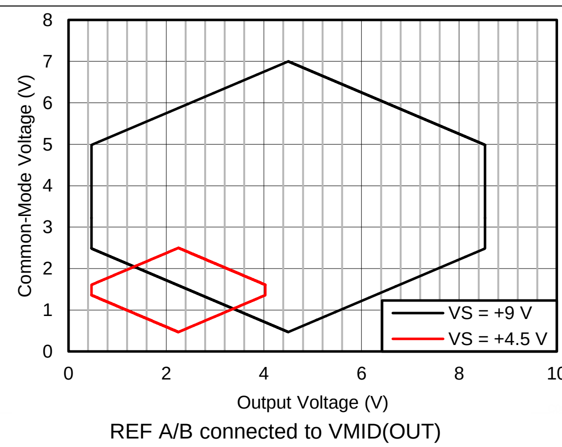


Figure 36. Input Common-Mode Voltage vs Output Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)

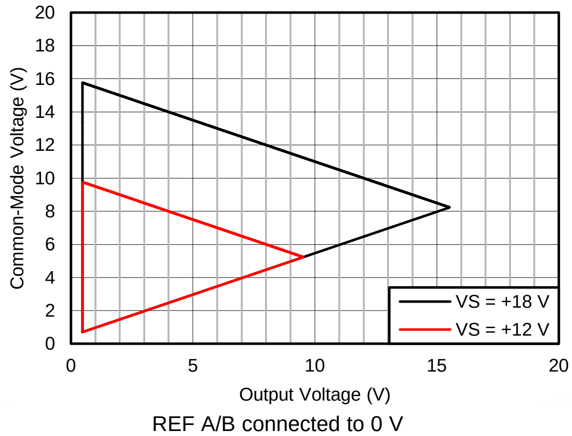


Figure 37. Input Common-Mode Voltage vs Output Voltage

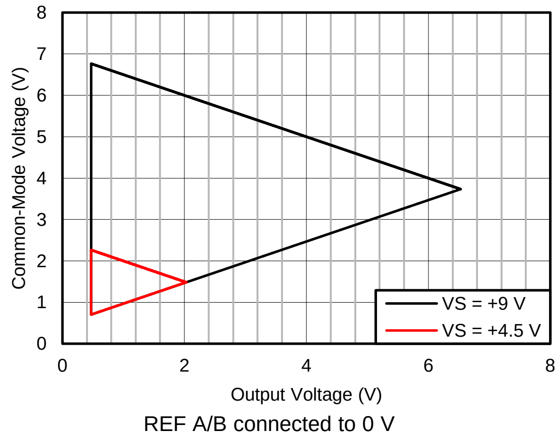


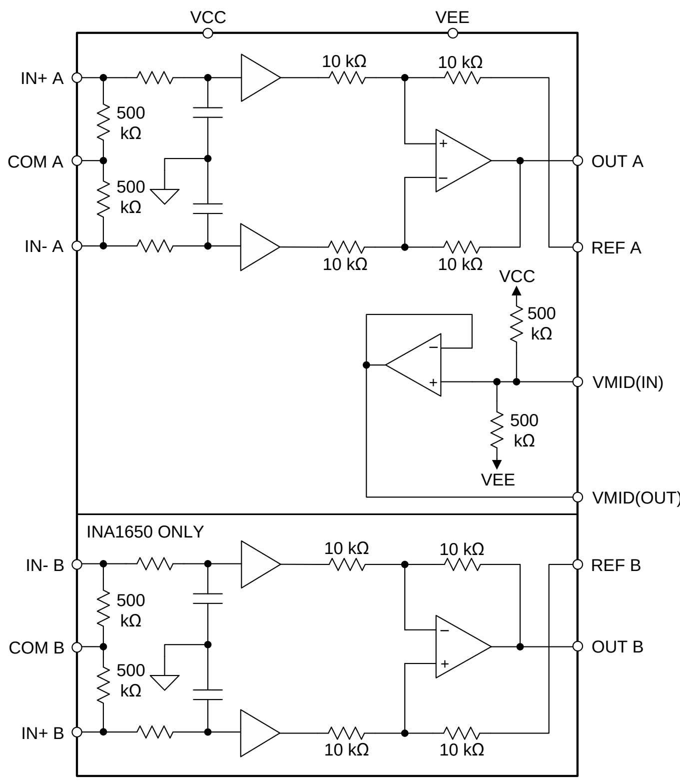
Figure 38. Input Common-Mode Voltage vs Output Voltage

7 Detailed Description

7.1 Overview

The INA165x combines high-performance audio operational amplifier cores with high-precision resistor networks to provide exceptional audio performance and rejection of noise which may be externally coupled into the audio signal path. The INA165x uses an instrumentation amplifier topology with a fixed unity gain to provide high input impedance and a high common-mode rejection ratio (CMRR). Unlike other line receiver products that use a simple four-resistor difference amplifier topology, the INA165x topology provides excellent CMRR even with mismatched source impedances.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Audio Signal Path

Figure 39 highlights the basic elements present in the audio signal pathway. The primary elements are: input biasing resistors, electromagnetic interference (EMI) filtering, input buffers, and a difference amplifier. The primary role of an audio line receiver is to convert a differential input signal into a single-ended output signal while rejecting noise that is common to both inputs (common-mode noise). The difference amplifier (which consists of an op amp and four matched 10-kΩ resistors) accomplishes this task. The basic transfer function of the circuit is shown in Equation 1:

$$V_{OUT} = \left(V_{IN+} - V_{IN-}\right) + V_{REF} \tag{1}$$

Feature Description (continued)

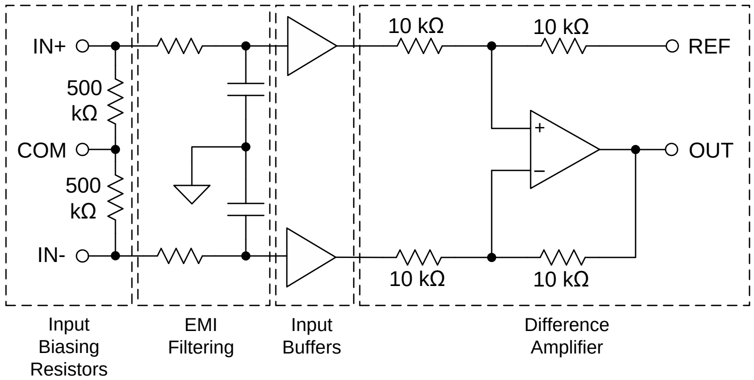


Figure 39. INA165x Audio Signal Path (Single Channel Shown)

The input buffers prevent external resistances (such as those from the PCB, connectors, or cables) from ruining the precise matching of the internal 10-kΩ resistors which would degrade the high common-mode rejection of the difference amplifier. As is typical of many amplifiers, a small bias current flows into or out of the buffer amplifier inputs. This current must flow to a common potential for the buffer to function properly. The input biasing resistors provide an internal pathway for this current to the COM pin. The COM pin can connect to ground in a dual-supply system or the output of the internal supply divider ($V_{MID(OUT)}$) in single-supply applications. Finally, EMI filtering is added to the input buffers to prevent high-frequency interference signals from propagating through the audio signal pathway.

7.3.2 Supply Divider

The INA165x integrates a supply-divider circuit which may bias the input common-mode voltage and output reference voltage to the halfway point between the applied power supply voltages. The nominal output voltage of the supply divider circuit is shown in Equation 2:

$$V_{MID(OUT)} = \frac{VCC + VEE}{2} \tag{2}$$

Figure 40 illustrates the internal topology of the supply-divider circuit. The supply divider consists of two 500-kΩ resistors connected between the VCC and VEE pins of the INA165x. The noninverting input of a buffer amplifier is connected to the midpoint of the voltage divider that is formed by the 500-kΩ resistors. The buffer amplifier provides a low-impedance output that is required to bias the REF pins without degrading the CMRR. For dual-supply applications where the supply divider circuit may not be used, no connection is required for the $V_{MID(IN)}$ or $V_{MID(OUT)}$ pins.

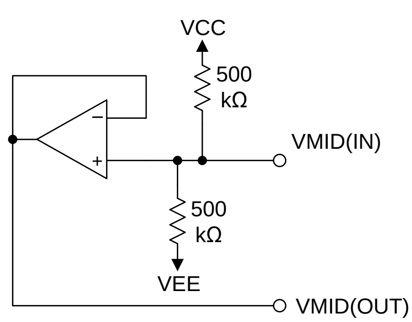


Figure 40. Internal Supply Divider Circuit

Feature Description (continued)

7.3.3 Electrical Overstress

Designers typically ask questions about the capability of an amplifier to withstand electrical overstress. These questions typically focus on the device inputs, but can involve the supply voltage pins or the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal ESD protection is built into these circuits to protect them from accidental ESD events both before and during product assembly. A good understanding of basic ESD circuitry and the relevance of circuitry to an electrical overstress event is helpful. Figure 41 illustrates the ESD circuits contained in the INA165x. The ESD protection circuitry involves several current-steering diodes that are connected from the input and output pins and routed back to the internal power-supply lines. This protection circuitry is intended to remain inactive during normal circuit operation. The input pins of the INA165x are protected with internal diodes that are connected to the power-supply rails. These diodes clamp the applied signal to prevent the input circuitry from damage. If the input signal voltage exceeds the power supplies by more than 0.3 V, limit the input signal current to less than 10 mA to protect the internal clamp diodes. A series input resistor can typically limit the current. Some signal sources are inherently current-limited and do not require limiting resistors.

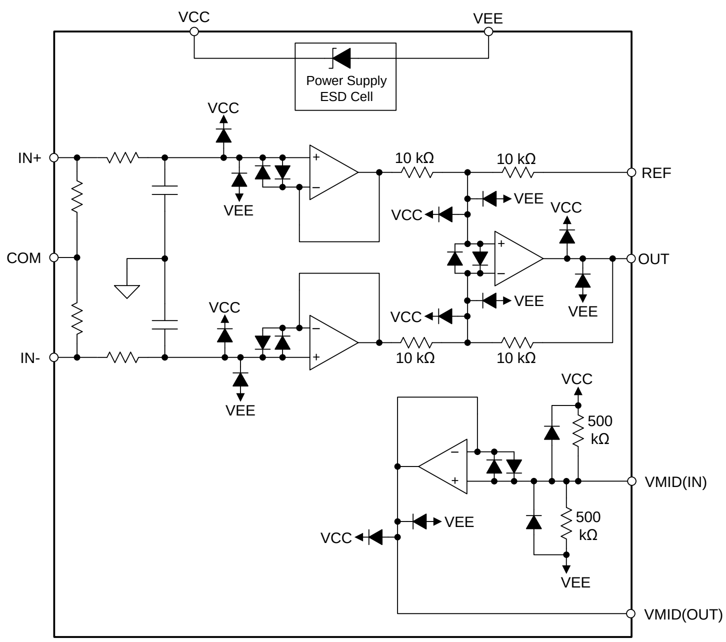


Figure 41. INA165x Internal ESD Protection Circuitry (Single Channel and Supply-Divider Shown for Simplicity)

7.3.4 Thermal Shutdown

If the junction temperature of the INA165x exceeds approximately 170ºC, a thermal shutdown circuit disables the amplifier to protect the device from damage. The amplifier is automatically re-enabled after the junction temperature falls below the shutdown threshold temperature. If the condition that caused excessive power dissipation is not removed, the amplifier oscillates between a shutdown and enabled state until the output fault is corrected.

7.4 Device Functional Modes

7.4.1 Single-Supply Operation

The INA165x can be used on single power supplies ranging from 4.5 V to 36 V. Use the COM and REF pins to level shift the internal voltages into a linear operating condition. Ideally, connecting the REF and COM pins to a midsupply potential (such as the $V_{MID(OUT)}$ pin) avoids saturating the output of the internal amplifiers.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Common-Mode Range

The linear input voltage range of the INA165x input circuitry extends from 350 mV inside the negative supply voltage to 2 V below the positive supply, and maintains 85-dB (minimum) common-mode rejection throughout this range. The INA165x operates over a wide range of power supplies and V_{REF} configurations; providing a comprehensive guide to common-mode range limits for all possible conditions is impractical. The common-mode range for most operating conditions is best calculated using the INA common-mode range calculating tool.

8.1.2 Common-Mode Input Impedance

The high CMRR of many line receivers can degrade by impedance mismatches in the system. Figure 42 shows a common-mode noise source (V_{CM}) connected to both inputs of a single channel of the INA165x. An external parasitic resistance (R_{EXT}) represents the mismatch in impedances between the common-mode noise source and the inputs of the INA165x. This mismatched impedance may be due to PCB layout, connectors, cabling, passive component tolerances, or the circuit topology. The presence of R_{EXT} in series with the IN+ input degrades the overall CMRR of the system because the voltage at IN+ is no longer equal to the voltage at IN–. Therefore, a portion of the common-mode noise converts to a differential signal and passes to the output.

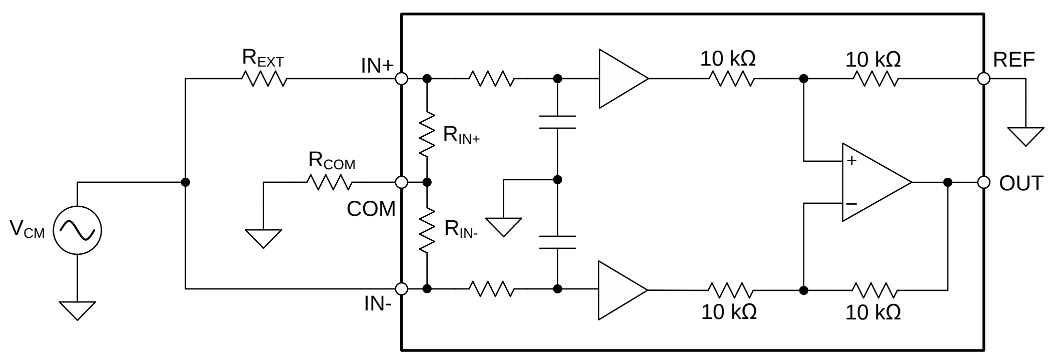


Figure 42. A Single Channel of the INA165x Shown With Source Impedance Mismatch (R_{EXT}) and Optional Resistor (R_{COM})

While the INA165x is significantly more resistant to these effects than typical line receivers, connecting a resistor (R_{COM}) from the COM pin to the system ground further improves CMRR performance. Figure 43 shows the CMRR of the INA165x (typical CMRR of 92 dB) for increasing source impedance mismatches. If the COM pin is connected directly to ground (R_{COM} equal to 0 Ω), a 20-Ω source impedance mismatch degrades the CMRR from 92 dB to 83.7 dB. However, if R_{COM} has a value of 1 MΩ, the CMRR only degrades to 89.6 dB, which is an improvement of approximately 6 dB.

Application Information (continued)

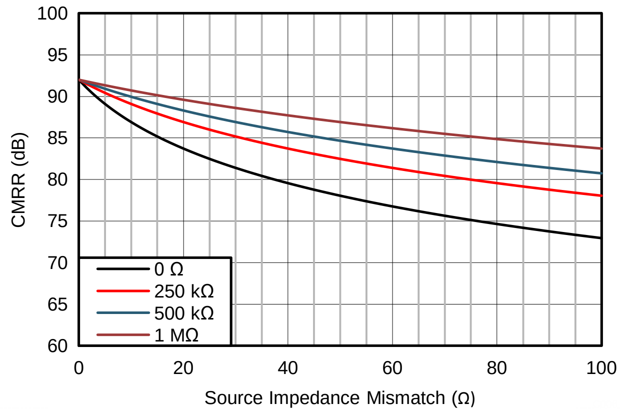


Figure 43. CMRR vs Source Impedance Mismatch for Different R_{COM} Values

R_{COM} does not need to be a high-precision resistor with a very tight tolerance. Low cost 5% or 1% resistors can be used with no degradation in overall performance. The addition of R_{COM} does not increase the noise of the audio signal path.

In single-supply systems where AC coupling is used at the inputs of the INA165x, adding R_{COM} lengthens the start-up time of the circuit. The input AC-coupling capacitors are charged to the midsupply voltage through the R_{COM} resistor, which may take a substantial amount of time if R_{COM} has a large value (such as 1 MΩ). Do not use R_{COM} in these systems if start-up time is a concern. In dual-supply systems with input AC-coupling capacitors, the capacitor voltage does not need to be charged to a midsupply point, since the capacitor voltage settles to ground by default. Therefore, R_{COM} does not increase start-up time in dual-supply systems.

8.1.3 Start-Up Time in Single-Supply Applications

The internal supply divider of the INA165x is constructed using two 500-kΩ resistors connected in series between the VCC and VEE pins. These resistors are matched on-chip to provide a reference voltage that is exactly one half of the power supply voltage. Noise from the power supplies and thermal noise from the resistors degrades the overall audio performance of the INA165x if allowed to enter the signal path. Therefore, TI recommends a filter capacitor (C_F) is connected to the VMID(IN) pin, as shown in Figure 44 The C_F capacitor forms a low-pass filter with the internal 500-kΩ resistors. Noise above the corner frequency of this filter is passed to ground and is removed from the audio signal path. The corner frequency of the filter is shown in Equation 3:

$$F_{-3dB} = \frac{1}{2 \cdot \pi \cdot 250\ k\Omega \cdot C_F} \tag{3}$$

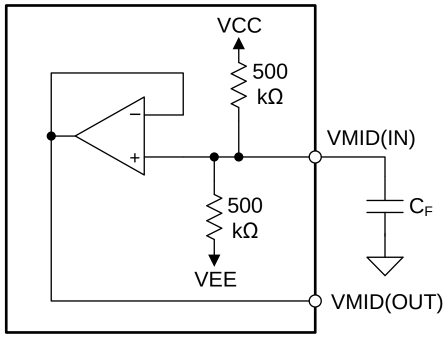


Figure 44. Connect a Capacitor (C_F) to the VMID(IN) Pin to Reduce Noise from the Voltage Divider

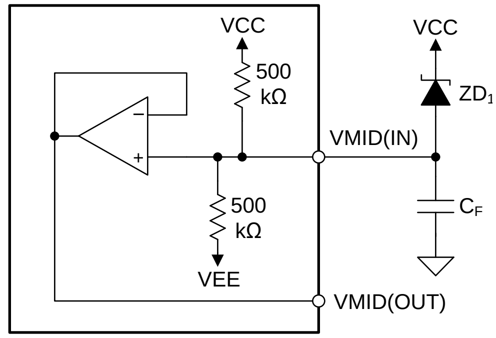


Figure 45. A Zener Diode (ZD1) Connected to the Positive Supply Can Decrease Start-Up Time

Application Information (continued)

When power is applied to the INA165x, the filter capacitor (C_F) charges through the internal 500-kΩ resistors. If the C_F capacitor has a large value, the time required for $V_{MID(OUT)}$ to reach the final midsupply voltage may be extensive. Adding a zener diode from the $V_{MID(IN)}$ pin to the positive power supply (as shown in Figure 45) reduces this time. The zener voltage must be slightly greater than one half of the power supply voltage.

Using large AC-coupling capacitors increases the start-up time of the line receiver circuit in single-supply applications. When power is applied, the AC-coupling capacitors begin to charge to the midsupply voltage applied to the COM pin through a current flowing through the input resistors as shown in Figure 46. The INA165x functions properly when the input common-mode voltage (and the capacitor voltage) is within the specified range. The time required for the input common-mode voltage to reach 98% of the final value is shown in Equation 4:

$$T_{98\%} = 4 \cdot R \cdot C_{IN} = 4 \cdot 500\ k\Omega \cdot C_{IN} \quad (4)$$

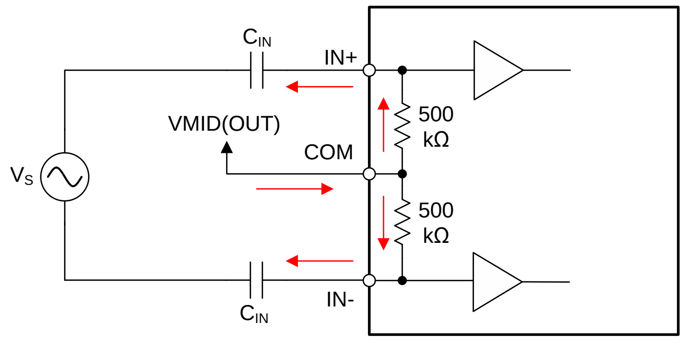


Figure 46. AC-Coupling Capacitors Charge to the Midsupply Voltage Through the Input Resistors

8.1.4 Input AC Coupling

The signal path in most audio systems is typically AC-coupled to avoid the propagation of DC voltages, which can potentially damage loudspeakers or saturate power amplifiers. The capacitor values must be selected to pass the desired bandwidth of audio signals. The high-pass corner frequency is calculated with Equation 5:

$$F_C = \frac{1}{2 \cdot \pi \cdot (2 \cdot R_{IN}) \cdot {C_{IN}}/{2}} = \frac{1}{2 \cdot \pi \cdot R_{IN} \cdot C_{IN}} \quad (5)$$

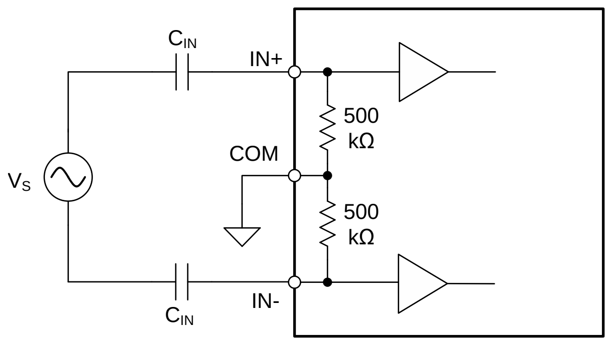


Figure 47. AC-Coupling Capacitors Form a High-Pass Filter With INA165x Input Resistors

Application Information (continued)

Although the input resistors of the INA165x are matched typically within 0.01%, large capacitors are usually mismatched. The mismatch in the values of the AC-coupling capacitors causes the corner frequencies at the two signal inputs (IN+ and IN–) to be different, which can degrade CMRR at low frequency. For this reason, TI recommends placing the high-pass corner frequency well below the audio bandwidth and to use a resistor in series with the COM pin (R_{COM}), as shown in Figure 42 if possible. See the Common-Mode Input Impedance section for more information on placing a resistor in series with the COM pin. Figure 48 shows the effect of a 5% mismatch in the values of the input AC-coupling capacitors with and without an R_{COM} resistor. Comparing CMRR at 100 Hz: 1-µF AC-coupling capacitors with a 5% mismatch degrade the CMRR to 75 dB, while 10-µF capacitors and a 1-MΩ R_{COM} resistor shows 92 dB of CMRR.

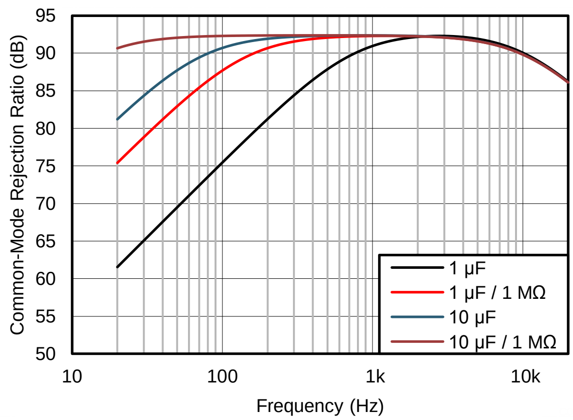


Figure 48. CMRR Degradation Due to a 5% Mismatch in AC-Coupling Capacitors

8.1.5 Supply Divider Capacitive Loading

The VMID(OUT) pin of the INA165x is stable with capacitive loads up to 150 pF. An isolation resistor (R_{ISO} in Figure 49), must be used if capacitive loads larger than 150 pF are connected to the VMID(OUT) pin. Figure 49 shows the recommended configuration of an isolation resistor in series with the capacitive load. The REF pins of the INA1650 must connect directly to the VMID(OUT) pin before the isolation resistor. Any resistance placed between the VMID(OUT) pin and the reference pins degrades the CMRR of the device. Figure 50 shows the recommended value for the isolation resistor for increasing capacitive loads.

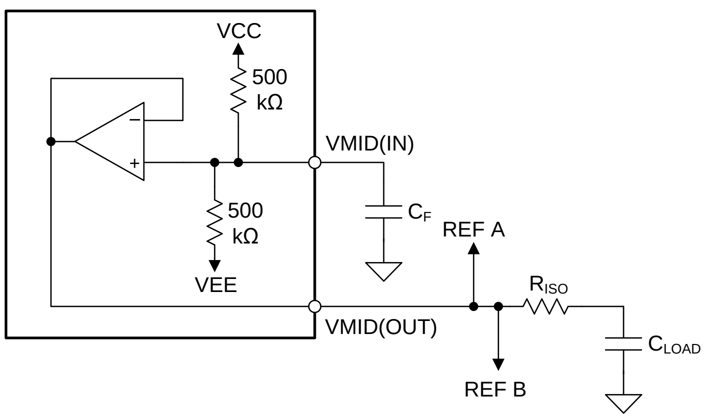


Figure 49. Place an Isolation Resistor Between the VMID(OUT) Pin and Large Capacitive Loads

Application Information (continued)

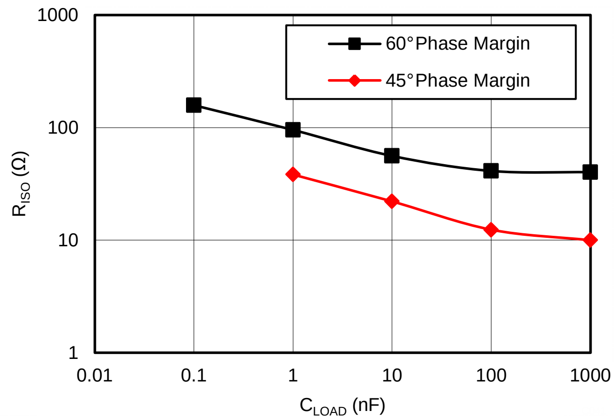


Figure 50. Recommended Isolation Resistor Value vs Capacitive Load

8.2 Typical Applications

The low noise and distortion of the INA165x make these devices an excellent choice for a variety of applications in professional and consumer audio products. However, these same performance metrics make the INA165x useful for industrial, test and measurement, and data-acquisition applications. The examples shown here are possible applications where the INA165x provide exceptional performance.

8.2.1 Line Receiver for Differential Audio Signals in a Split-Supply System

The INA165x devices are designed to require a minimum number of external components to achieve data sheet-level performance in audio line-receiver applications. Figure 51 shows the INA1650 used as a differential audio line receiver in split-supply systems that are common in professional audio applications. The line receiver recovers a differential audio signal which may have been affected by significant common-mode noise.

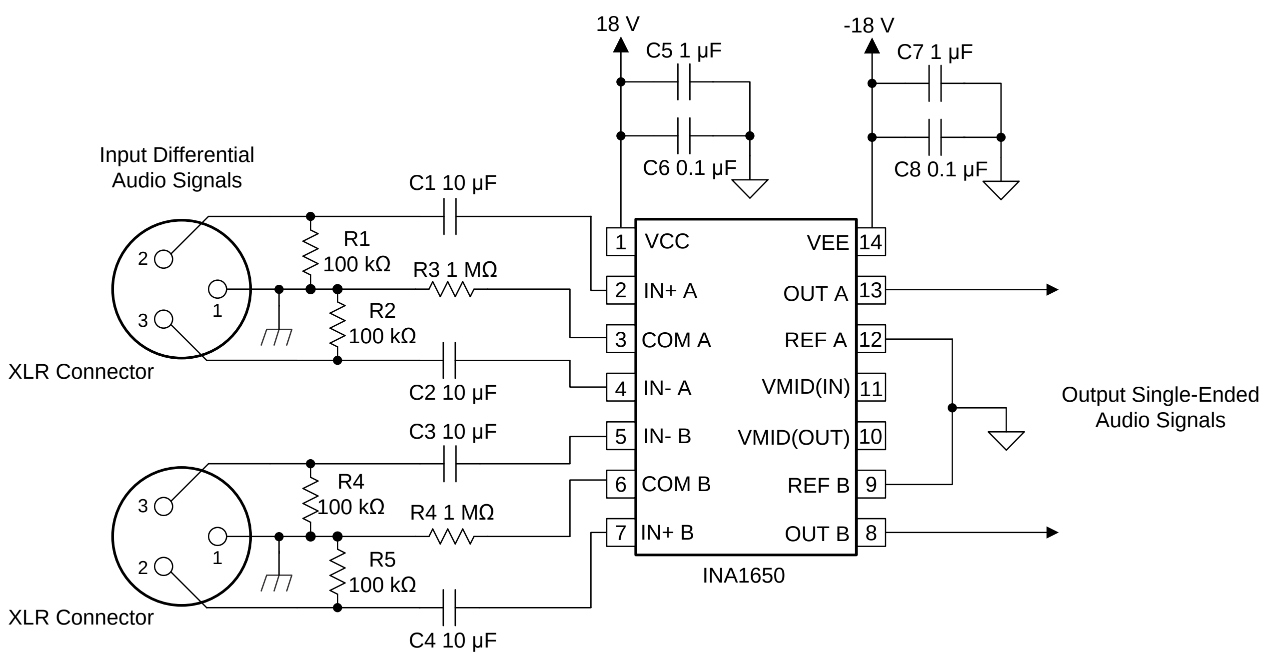


Figure 51. INA1650 Used as a Line Receiver for Differential Audio Signals in a Split-Supply System

Typical Applications (continued)

8.2.1.1 Design Requirements

- Power Supply Voltage: ±18 V
- Frequency Response: < 0.1 dB deviation from 20 Hz to 20 kHz
- Common-Mode Rejection Ratio: > 80 dB at 1 kHz
- THD+N: < –100 dB (4-dBu input signal, 1-kHz fundamental, 90-kHz measurement bandwidth)

8.2.1.2 Detailed Design Procedure

The passive components shown in Figure 51 are selected using the information given in the Application Information and Layout Guidelines sections. All 10-µF input AC-coupling capacitors (C1, C2, C3, and C4) maximize the CMRR performance at low frequency, as shown in Figure 48. The high-pass corner frequency for input signals meets the design requirement for frequency response, as Equation 6 shows:

$$F_C = \frac{1}{2 \cdot \pi \cdot R_{IN} \cdot C_{IN}} = \frac{1}{2 \cdot \pi \cdot (500\ k\Omega) \cdot (10\ \mu F)} = 0.032\ Hz \tag{6}$$

1-MΩ R_{COM} resistors (R3 and R4) further improve CMRR performance at low frequency. Resistors R1, R2, R4, and R5 provide a discharge pathway for the AC-coupling capacitors in the event that audio equipment with a DC offset voltage is connected to the inputs of the circuit. These resistors are optional and may degrade the CMRR performance with mismatches in source impedance. Finally, capacitors C5, C6, C7, and C8 provide a low-impedance pathway for power supply noise to pass to ground rather than interfering with the audio signal. No connection is necessary on the $V_{MID(IN)}$ and $V_{MID(OUT)}$ pins because the supply-divider circuit is not used in this particular application.

8.2.1.3 Application Curves

Figure 52 through Figure 57 illustrate the measured performance of the line receiver circuit. Figure 52 shows the measured frequency response. The gain of the circuit is 0 dB as expected with 0.1-dB magnitude variation at 10 Hz. The measured CMRR of the circuit (Figure 53) at 1 kHz equals 94 dB without any source impedance mismatch. Adding a 10-Ω source impedance mismatch degrades the CMRR at 1 kHz to 92 dB. The high-frequency degradation of CMRR shown in Figure 53 for the 10-Ω source impedance mismatch cases is due to the capacitance of the cables used for the measurement. The total harmonic distortion plus noise (THD+N) is plotted over frequency in Figure 54. For a 4-dBu (1.23 V_{RMS}) input signal level, the THD+N remains flat at –101.6 dB (0.0008%) over the measured frequency range. Increasing the signal level to 22 dBu further decreases the THD+N to –115.2 dB (0.00017%) at 1 kHz, but the THD+N rises above 7 kHz. Measuring the THD+N vs Output Amplitude (Figure 55) at 1 kHz shows a constant downward slope until the noise floor of the audio analyzer is reached at 5 V_{RMS}. The constant downward slope indicates that noise from the device dominates THD+N at this frequency instead of distortion harmonics. Figure 56 and Figure 57 confirm this conclusion. For a 4–dBu signal level, the second harmonic is barely visible above the noise floor at –140 dBu. Increasing the signal level to 22 dBu produces distortion harmonics above the noise floor. The largest harmonic in this case is the second at –111.2 dBu, or –133.2 dB relative to the fundamental.

Typical Applications (continued)

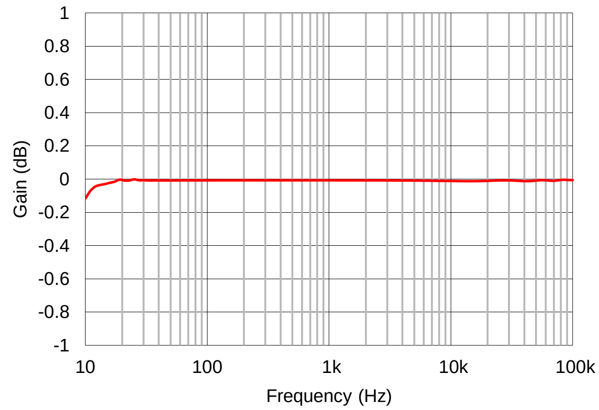
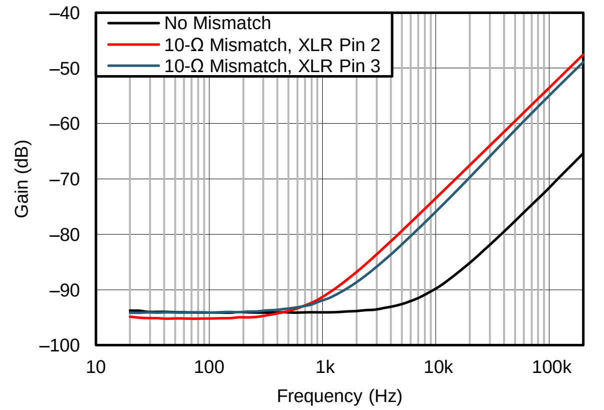
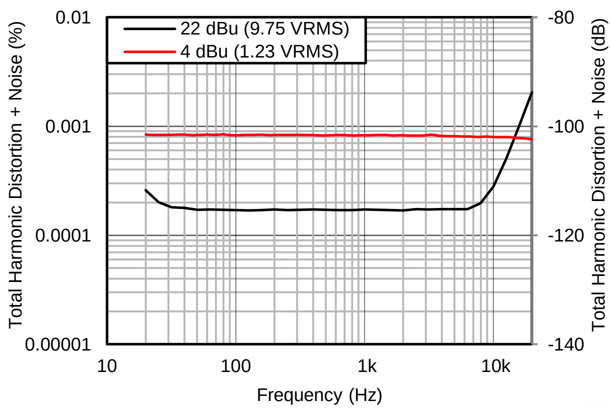


Figure 52. Frequency Response



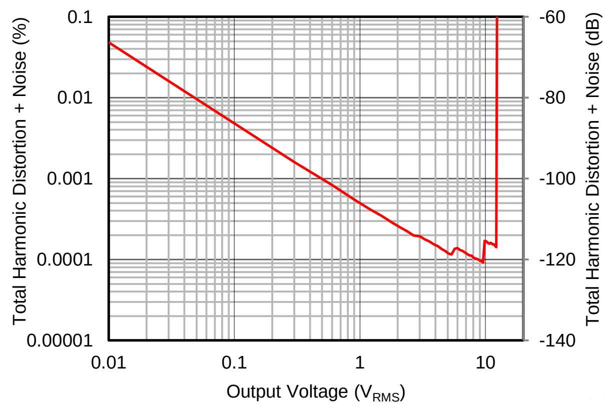
1-V_{RMS} Common-Mode Signal

Figure 53. Common-Mode Rejection Ratio vs Frequency



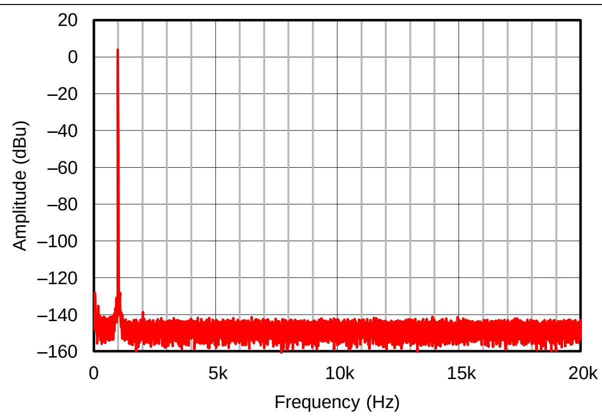
90-kHz Measurement Bandwidth

Figure 54. THD+N vs Frequency



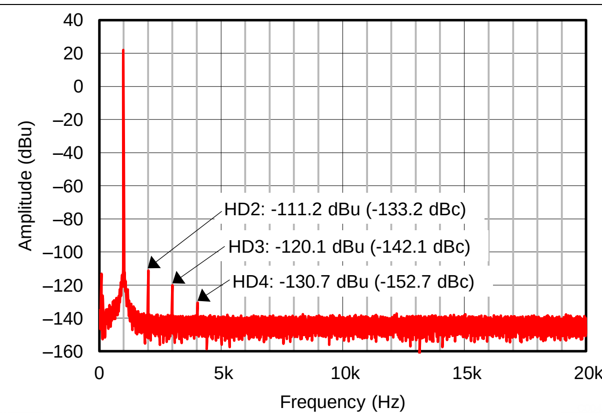
22-kHz Measurement Bandwidth

Figure 55. THD+N vs Amplitude



4–dBu Output Amplitude

Figure 56. Output Spectrum



22–dBu Output Amplitude

Figure 57. Output Spectrum

Typical Applications (continued)

8.2.2 Differential Line Receiver for Single-Supply Applications

The INA1650 can simply operate in single-supply applications by connecting the COM and REF pins to the output of the internal supply divider.

($V_{MID(OUT)}$). Adding a 1-µF capacitor to the $V_{MID(IN)}$ pin to filters noise from the power supply and the internal voltage divider.

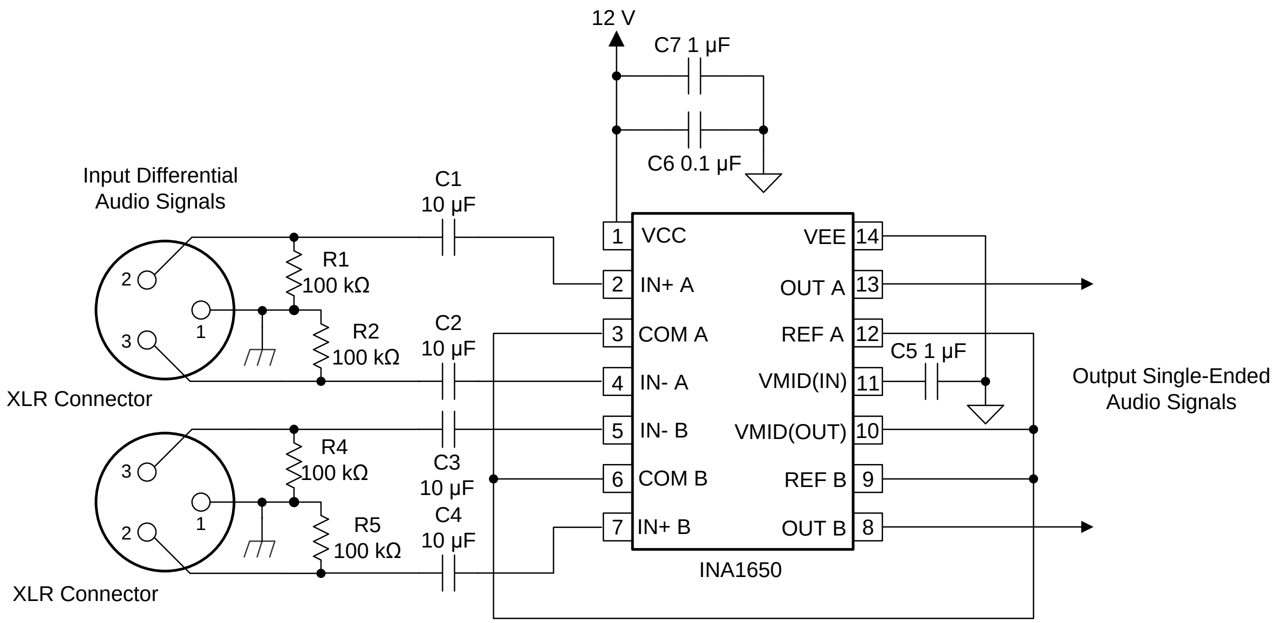


Figure 58. Differential Line Receiver for Single-Supply Applications

Typical Applications (continued)

8.2.3 Floating Single-Ended Input Line Receiver for Ground Loop Noise Reduction

Ground loops commonly form in audio systems where the equipment is interconnected with coaxial cables, which introduces significant common-mode noise. If the sheath of the coaxial cable is connected to the equipment chassis and safety ground, a ground loop forms, which includes the main electrical wiring and the audio signal path. The INA165x can break these ground loops by floating the sheath of the coaxial cable through resistors (R3 and R4 in Figure 59) so ground noise appears at the inputs of the INA165x as a common-mode signal. Capacitors C8 and C9 provide a high-frequency pathway to ground for radio frequency interference (RFI). A transient voltage suppressor (TVS) connected between the coaxial sheath and the chassis ground is shown in Figure 59. This TVS protects the inputs of the INA165x in the event of an electrostatic discharge to the signal input.

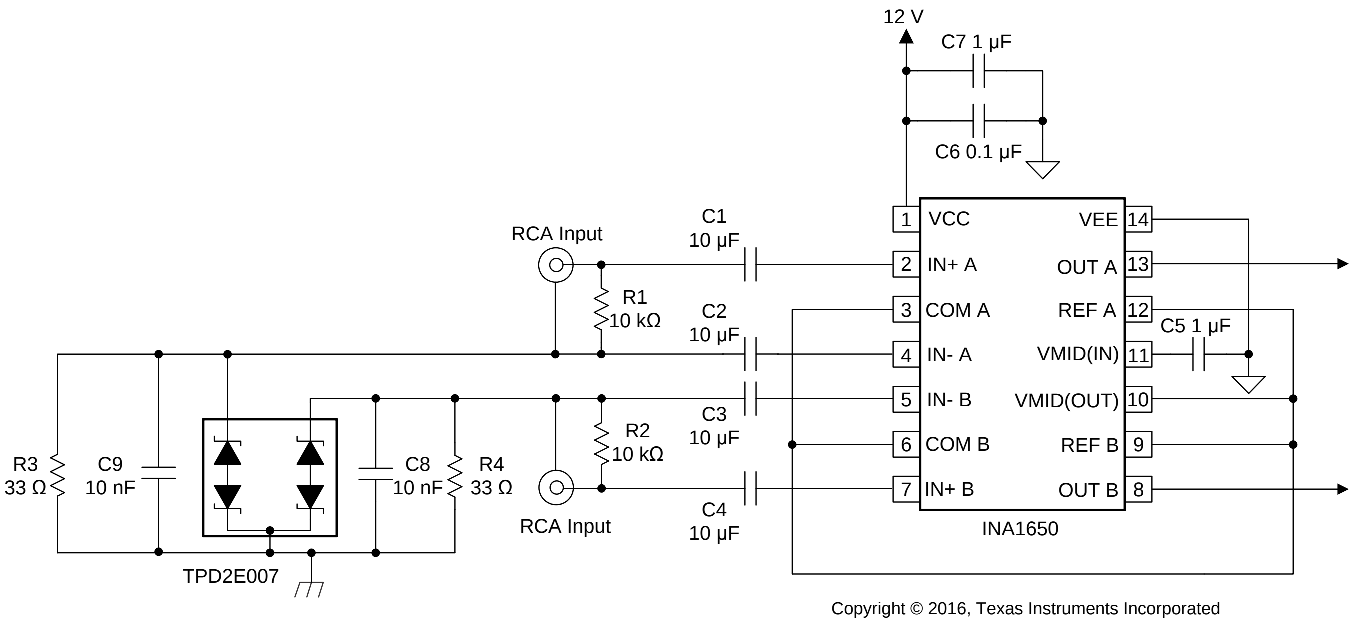


Figure 59. Ground Loop Isolation in Single-Ended Systems

Typical Applications (continued)

8.2.4 Floating Single-Ended Input Line Receiver With Differential Outputs

The application in Figure 59 can be further extended to include differential outputs, which are necessary for audio ADCs and many Class-D amplifier devices. Figure 60 shows the addition of an OPA1688 audio operational amplifier to the outputs of the INA1650 that convert the single-ended outputs to differential outputs.

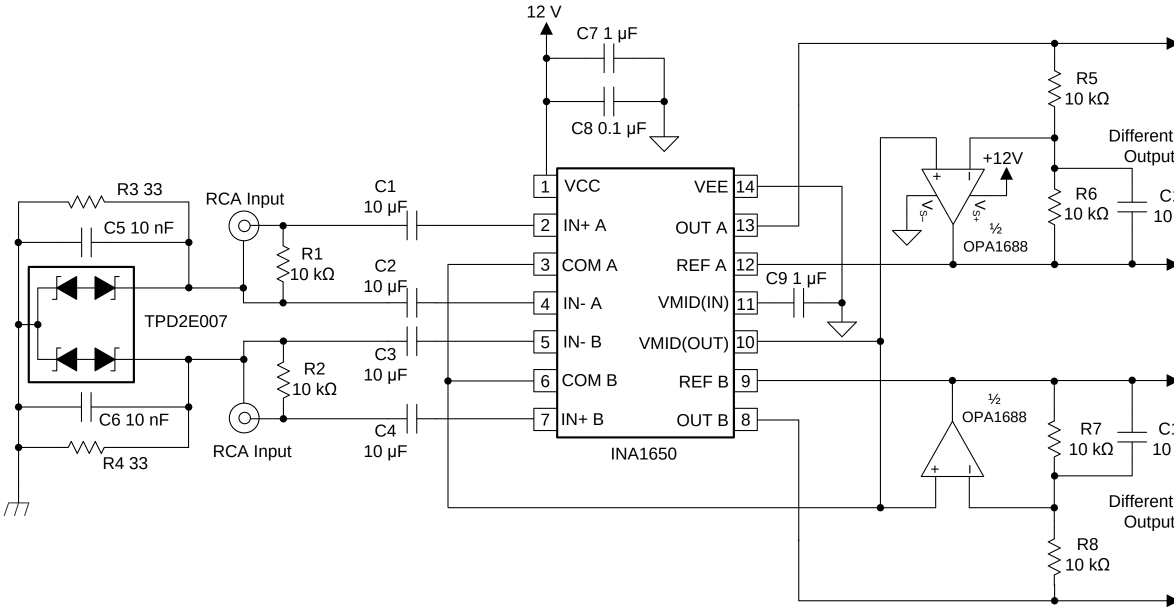


Figure 60. Single-Ended Line-Receiver Circuit With Differential Outputs

8.2.5 TRS Audio Interface in Single-Supply Applications

The INA1650 can be used for auxiliary audio inputs which may use a tip-ring-sleeve (TRS) connector where both audio channels share a common ground connection. Figure 61 shows the INA1650 configured as a line receiver for a TRS interface to remove common-mode noise on the sleeve connection.

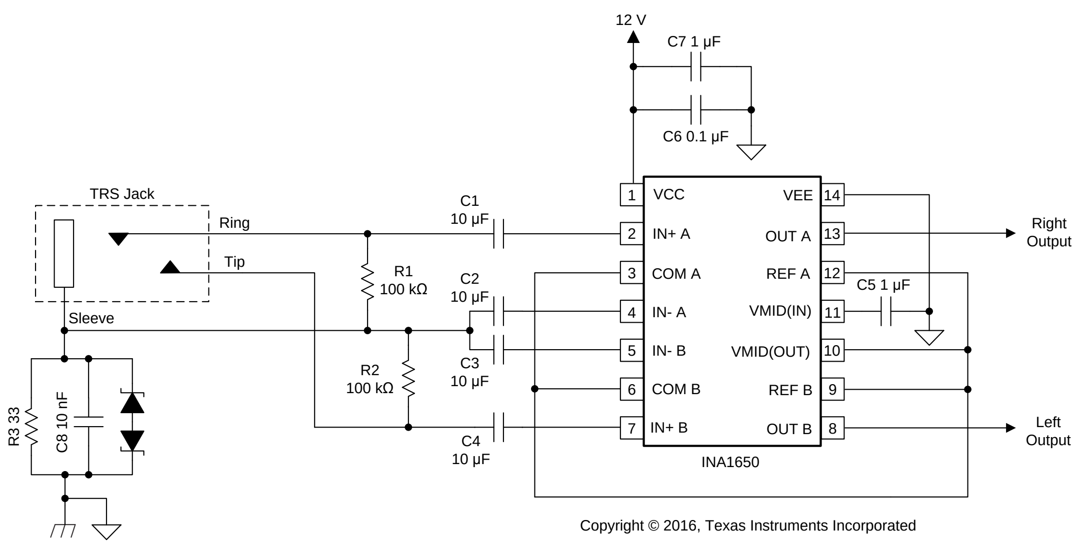


Figure 61. TRS Audio Interface in Single-Supply Applications

Typical Applications (continued)

8.2.6 Differential Line Driver With Single-Ended Input

The INA1650 can be employed in line-driver applications (Figure 62) where the precision matched internal resistor networks are useful in converting a single-ended signal to a balanced signal. Resistors R1 and R4 (shown in Figure 62) isolate the large cable capacitance from the outputs of the INA1650 to maintain stability. TI recommends AC-coupling capacitors C1 and C2 since the DC voltages of the connected equipment may be unknown. Resistors R2 and R3 dissipate any charge collected on the capacitors due to connecting equipment with a DC voltage present.

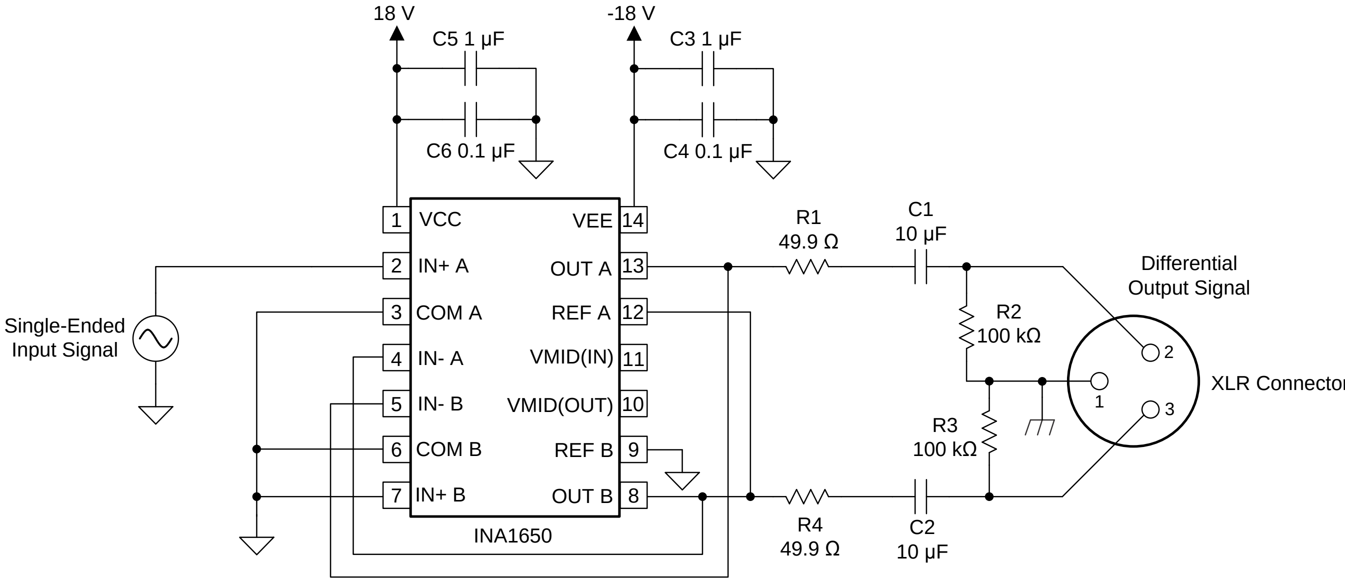


Figure 62. INA1650 Used as a Balanced Audio Line Driver

9 Power Supply Recommendations

The INA165x operates from ±2.25-V to ±18-V supplies while maintaining excellent performance. However, some applications do not require equal positive and negative output voltage swing. With the INA165x, power-supply voltages do not need to be equal. For example, the positive supply can be set to 25 V with the negative supply at –5 V.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Connect low-ESR, 1.0-µF and 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. Connecting bypass capacitors only from V+ to ground is acceptable in single-supply applications. Noise can propagate into analog circuitry through the power pins of this device. The bypass capacitors reduce the coupled noise by providing low-impedance pathways to ground.
- Connect the device REF pins to a low-impedance, low-noise, system reference point (such as an analog ground or the VMID(OUT) pin) with the shortest trace possible.
- Place the external components as close to the device as possible, as shown in Figure 63 and Figure 64.
- Use ground pours and planes to shield input signal traces and minimize additional noise introduced into the signal path.
- Keep the length of input traces equal and as short as possible. Route the input traces as a differential pair with as minimal spacing between them as possible.

10.2 Layout Examples

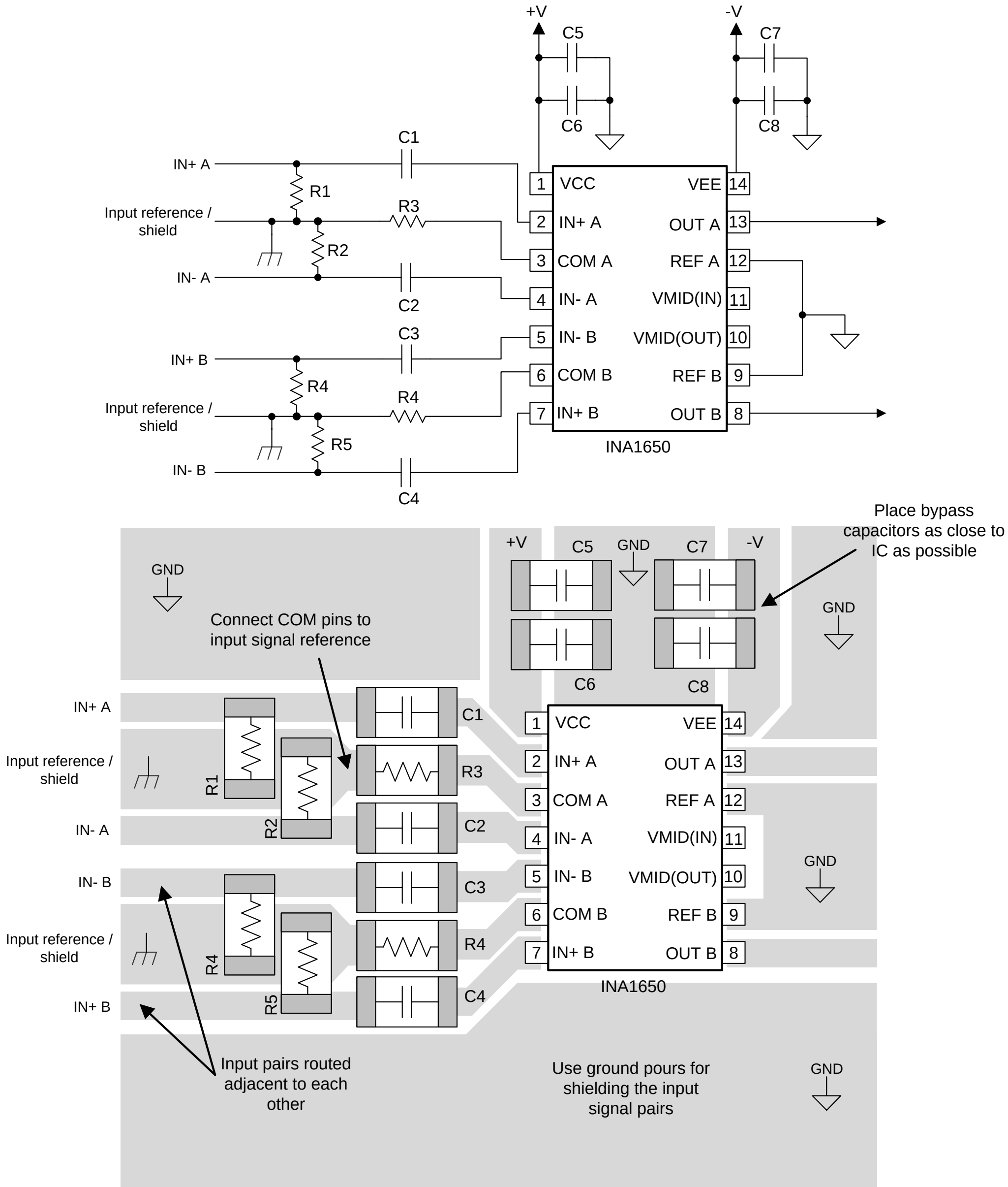


Figure 63. Layout Example for a Dual-Supply Line Receiver

Layout Examples (continued)

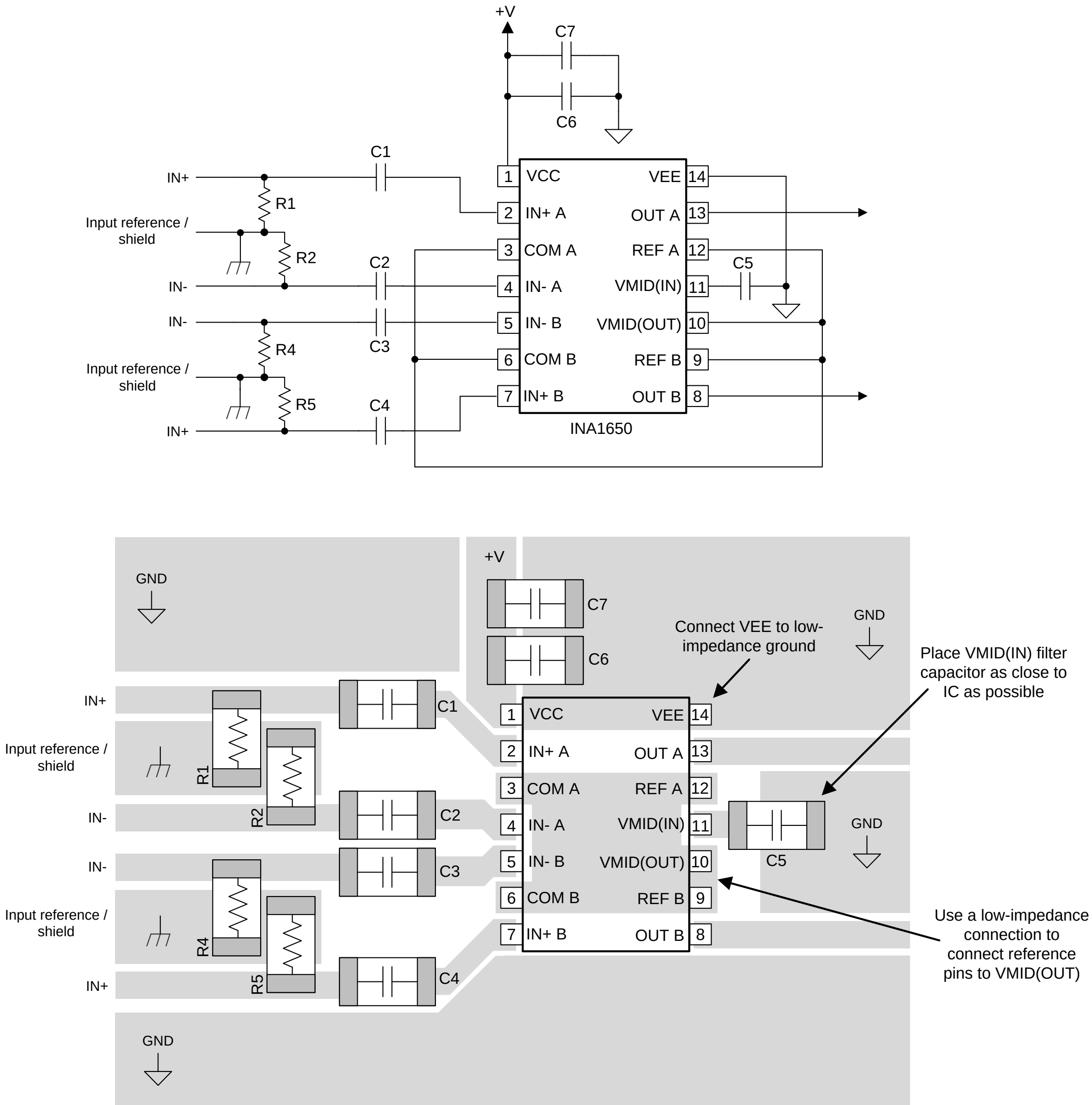


Figure 64. Layout Example for a Single-Supply Line Receiver

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the WEBENCH® Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 TI Precision Designs

TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Circuit Board Layout Techniques

11.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA1650	Click here	Click here	Click here	Click here	Click here
INA1651	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

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TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA1650IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IN1650C	Samples
INA1650IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IN1650C	Samples
INA1651IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA1651	Samples
INA1651IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA1651	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

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TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA1650, INA1651 :

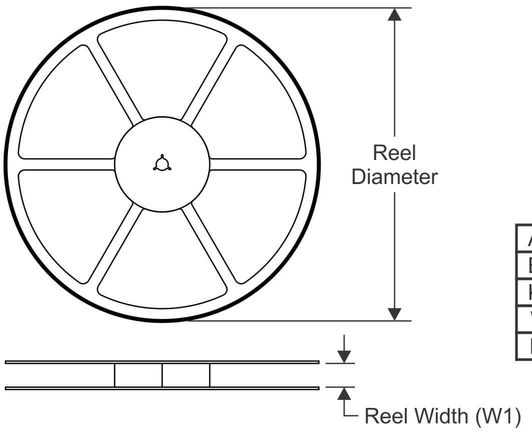
- Automotive: INA1650-Q1, INA1651-Q1

NOTE: Qualified Version Definitions:

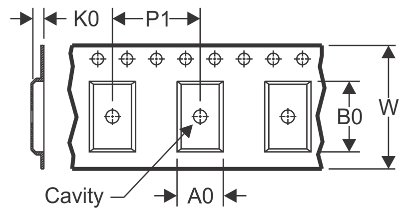
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

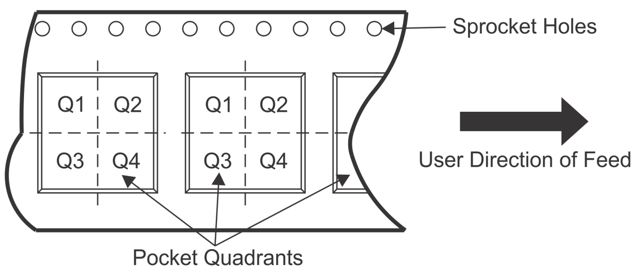


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

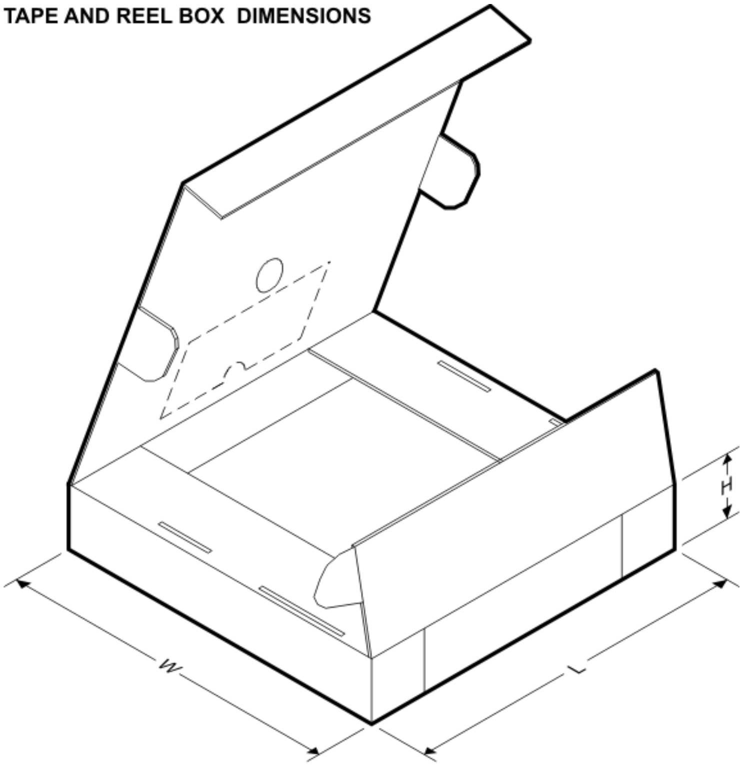
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA1650IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA1651IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

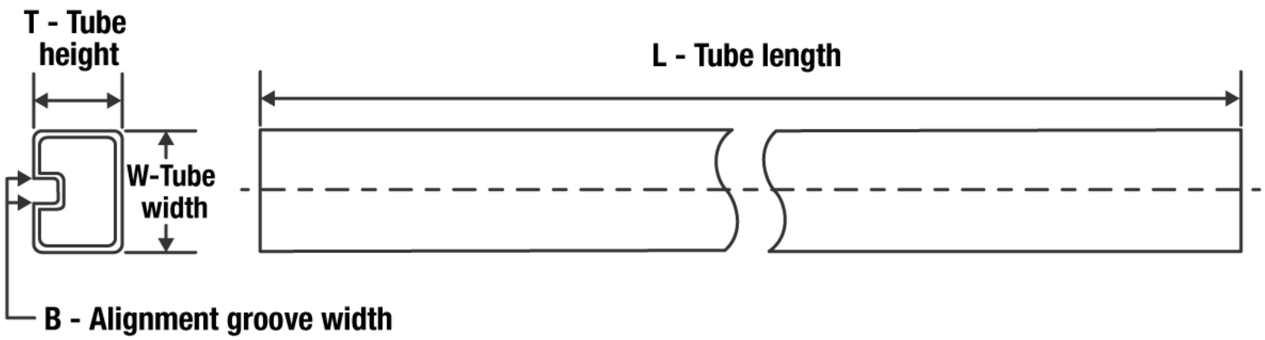
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA1650IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
INA1651IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

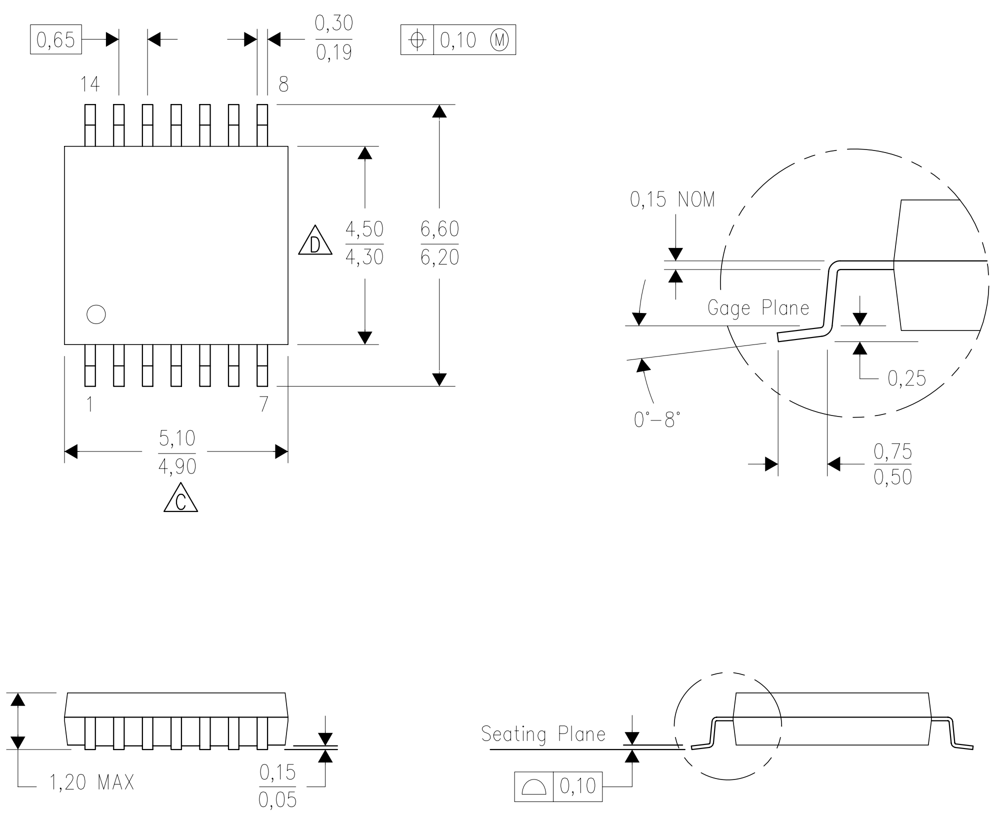
TUBE



*All dimensions are nominal

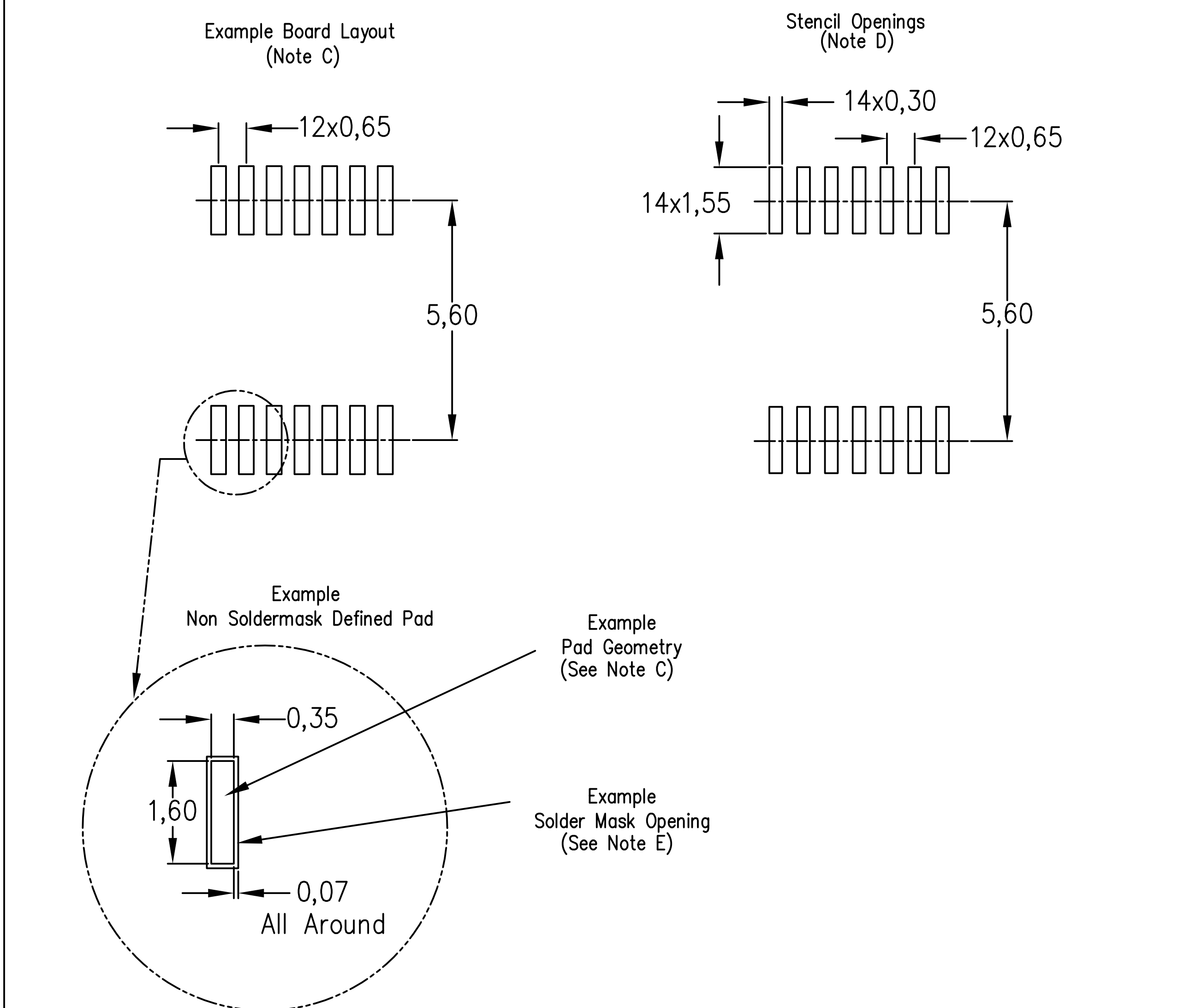
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA1650IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
INA1651IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4211284–2/G 08/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.