HV2801/HV2901

32-Channel Low-Charge-Injection High-Voltage Analog Switches

Features

- 32-Channel High-Voltage Analog Switch
- Integrated Bleed Resistors on the Outputs for HV2901
- CMOS Logic Circuitry for Low Power
- 3.3V or 5V CMOS Input Logic Level
- 2:1 Multiplexer/Demultiplexer
- 20 MHz Data Shift Clock Frequency
- 10 µA Low-Quiescent Power Dissipation
- Low Parasitic Capacitance
- DC to 50 MHz Analog Signal Frequency
- –60 dB Typical Off-Isolation at 5 MHz
- Excellent Noise Immunity
- Cascadable Serial Data Register with Latches
- Flexible Operating Supply Voltages

Applications

- Medical Ultrasound Imaging
- Non-Destructive Testing Metal Flaw Detection
- Piezoelectric Transducer Drivers
- Inkjet Printer Heads
- Optical MEMS Modules

General Description

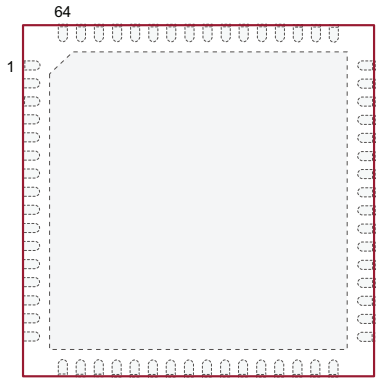
The HV2801 and HV2901 are 32-channel low-charge-injection high-voltage analog switch integrated circuits (ICs) intended for applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging, piezoelectric transducer drivers and printers. The HV2901 has integrated bleed resistors to eliminate voltage built up on capacitive loads such as piezoelectric transducers.

Input data is shifted into a 32-bit Shift register that can then be retained in a 32-bit latch. To reduce any possible clock feed-through noise, the latch enable ($\overline{LE}$) should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. These devices combine high-voltage bilateral DMOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

The HV2801 and HV2901 are suitable for various combinations of high-voltage supplies, e.g., V_{PP}/V_{NN}: +40V/–160V, +100V/–100V and +160V/–40V.

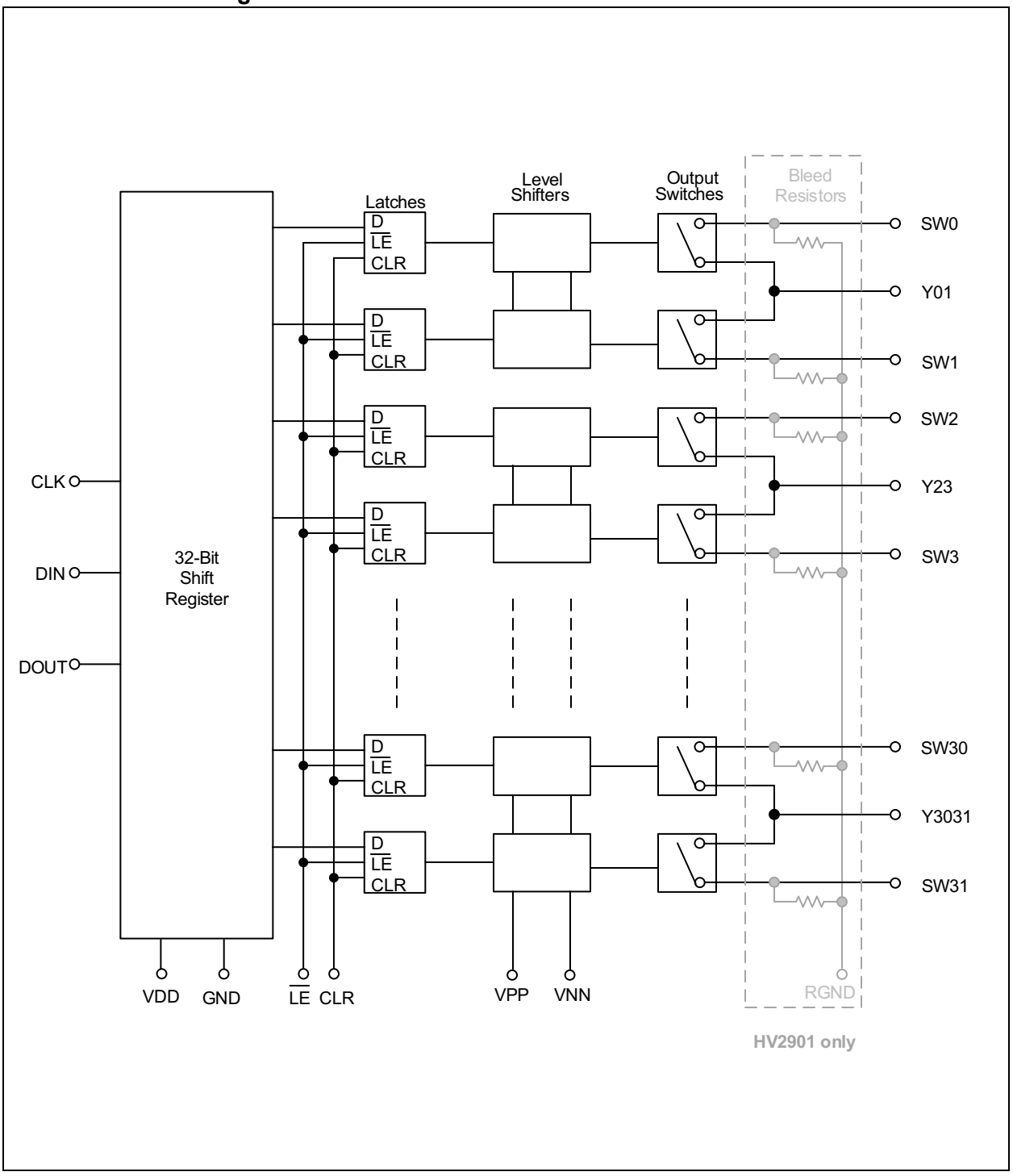
Package Type

64-lead QFN
(Top view)



See Table 2-1 for pin information.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Logic Power Supply Voltage, V_{DD} ..... –0.5V to +6.5V
Differential Supply Voltage, V_{PP}–V_{NN} 220V
High-Voltage Positive Supply, V_{PP} ..... –0.5V to V_{NN}+200V
High-Voltage Negative Supply, V_{NN} ..... +0.5V to –200V
Logic Input Voltage ..... –0.5V to V_{DD}+0.3V
Analog Signal Range, V_{SIG} ..... V_{NN} to V_{PP}
Peak Analog Signal Current/Channel 3A
Storage Temperature, T_S ..... –65°C to 150°C
Power Dissipation:
64-lead QFN 1.5W

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Power Supply Voltage	V_{DD}	3	—	5.5	V	**Note 1**, **Note 3**
High-Voltage Positive Supply	V_{PP}	40	—	V_{NN}+200	V	**Note 1**, **Note 3**
High-Voltage Negative Supply	V_{NN}	–160	—	–40	V	**Note 1**, **Note 3**
High-Level Input Voltage	V_{IH}	0.9 V_{DD}	—	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.1 V_{DD}	V	
Analog Signal Voltage Peak-to-Peak	V_{SIG}	V_{NN}+10V	—	V_{PP}–10V	V	**Note 2**

Note 1: Power-up/down sequence is arbitrary except GND must be powered up first and powered down last.
2: V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power-up/down transition.
3: Rise and fall times of power supplies V_{DD}, V_{PP} and V_{NN} should not be less than 1 millisecond.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all values are over operating conditions.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
Small Signal Switch On-Resistance	R_{ONS}	—	30	—	26	38	—	48	Ω	I_{SIG} = 5 mA	V_{PP} = +40V, V_{NN} = –160V
		—	25	—	22	27	—	32	Ω	I_{SIG} = 200 mA	
		—	25	—	22	27	—	30	Ω	I_{SIG} = 5 mA	V_{PP} = +100V, V_{NN} = –100V
		—	18	—	18	24	—	27	Ω	I_{SIG} = 200 mA	
		—	23	—	20	25	—	30	Ω	I_{SIG} = 5 mA	V_{PP} = +160V, V_{NN} = –40V
		—	22	—	16	25	—	27	Ω	I_{SIG} = 200 mA	
Small Signal Switch On-Resistance Matching	ΔR_{ONS}	—	20	—	5	20	—	20	%	I_{SIG} = 5 mA, V_{PP} = +100V, V_{NN} = –100V	
Large Signal Switch On-Resistance	R_{ONL}	—	—	—	15	—	—	—	Ω	V_{SIG} = V_{PP}–10V, I_{SIG} = 1A	
Output Bleed Resistor (For HV2901 only)	R_{INT}	—	—	20	35	50	—	—	kΩ	Output Switch to R_{GND}, I_{RINT} = 0.5 mA	
Switch-Off Leakage per Switch	I_{SOL}	—	5	—	1	10	—	15	µA	V_{SIG} = V_{PP}–10V, V_{NN} +10V (See **Section 3.1, Test Circuits**.)	
DC Offset Switch Off	V_{OS}	—	300	—	100	300	—	300	mV	R_{LOAD} = 100 kΩ (For HV2801), No load (For HV2901) (See **Section 3.1, Test Circuits**.)	
DC Offset Switch On		—	500	—	100	500	—	500	mV		
Quiescent V_{PP} Supply Current	I_{PPQ}	—	—	—	10	50	—	—	µA	All switches off	
Quiescent V_{NN} Supply Current	I_{NNQ}	—	—	—	–10	–50	—	—	µA		
Quiescent V_{PP} Supply Current	I_{PPQ}	—	—	—	10	50	—	—	µA	All switches on, I_{SW} = 5 mA	
Quiescent V_{NN} Supply Current	I_{NNQ}	—	—	—	–10	–50	—	—	µA		
Switch Output Peak Current	I_{SW}	—	3	—	3	2	—	2	A	V_{SIG} duty cycle < 0.1%	
Output Switching Frequency	f_{SW}	—	—	—	—	50	—	—	kHz	Duty cycle = 50%	
Average V_{PP} Supply Current	I_{PP}	—	16	—	—	20	—	22	mA	V_{PP} = +40V, V_{NN} = –160V	All output switches are turning ON and OFF at 50 kHz with no load
		—	14	—	—	14	—	14	mA	V_{PP} = +100V, V_{NN} = –100V	
		—	14	—	—	14	—	14	mA	V_{PP} = +160V, V_{NN} = –40V	
Average V_{NN} Supply Current	I_{NN}	—	16	—	—	20	—	22	mA	V_{PP} = +40V, V_{NN} = –160V	All output switches are turning ON and OFF at 50 kHz with no load
		—	14	—	—	14	—	14	mA	V_{PP} = +100V, V_{NN} = –100V	
		—	14	—	—	14	—	14	mA	V_{PP} = +160V, V_{NN} = –40V	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all values are over operating conditions.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Average V_{DD} Supply Current	I_{DD}	—	8	—	—	8	—	8	mA	f_{CLK} = 5 MHz, V_{DD} = 5V
Quiescent V_{DD} Supply Current	I_{DDQ}	—	10	—	—	10	—	10	µA	All logic inputs are static.
Data Out Source Current	I_{SOR}	0.45	—	0.45	0.7	—	0.4	—	mA	$V_{OUT} = V_{DD}–0.7V$
Data Out Sink Current	I_{SINK}	0.45	—	0.45	0.7	—	0.4	—	mA	V_{OUT} = 0.7V
Logic Input Capacitance	C_{IN}	—	10	—	—	10	—	10	pF	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all values are over operating conditions.
V_{DD} = 5V, $t_r = t_f \leq 5$ ns, 50% duty cycle and C_{LOAD} = 20 pF.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Set-Up Time Before $\overline{LE}$ Rises	t_{SD}	25	—	25	—	—	25	—	ns	
Time Width of $\overline{LE}$	t_{WLE}	56	—	—	56	—	56	—	ns	V_{DD} = 3V
		12	—	—	12	—	12	—	ns	V_{DD} = 5V
Clock Delay Time to Data Out	t_{DO}	8	40	8	19	40	8	40	ns	V_{DD} = 3V
		8	30	8	15	30	8	30	ns	V_{DD} = 5V
Time Width of CLR	t_{WCLR}	55	—	55	—	—	55	—	ns	
Set-Up Time Data to Clock	t_{SU}	21	—	21	—	—	21	—	ns	V_{DD} = 3V
		7	—	7	—	—	7	—	ns	V_{DD} = 5V
Hold Time Data from Clock	t_H	5	—	5	—	—	5	—	ns	V_{DD} = 3V
		7	—	7	—	—	7	—	ns	V_{DD} = 5V
Clock Frequency	f_{CLK}	—	8	—	—	8	—	8	MHz	V_{DD} = 3V
		—	20	—	—	20	—	20	MHz	V_{DD} = 5V
Clock Rise and Fall times	t_r, t_f	—	50	—	—	50	—	50	ns	
Turn-On Time	t_{ON}	—	5	—	—	5	—	5	µs	$V_{SIG} = V_{PP}–10V$, R_{LOAD} = 10 kΩ (See **Section 3.1, Test Circuits**.)
Turn-Off Time	t_{OFF}	—	5	—	—	5	—	5	µs	
Maximun V_{SIG} Slew Rate	dv/dt	—	20	—	—	20	—	20	V/ns	V_{PP} = +40V, V_{NN} = –160V
		—	20	—	—	20	—	20	V/ns	V_{PP} = +100V, V_{NN} = –100V
		—	20	—	—	20	—	20	V/ns	V_{PP} = +160V, V_{NN} = –40V

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all values are over operating conditions.
V_{DD} = 5V, $t_r = t_f \leq 5$ ns, 50% duty cycle and C_{LOAD} = 20 pF.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Off Isolation	K_O	–30	—	–30	–33	—	–30	—	dB	f = 5 MHz, 1 kΩ//15 pF load (See **Section 3.1, Test Circuits**.)
		–58	—	–58	–60	—	–58	—	dB	f = 5 MHz, 50Ω load (See **Section 3.1, Test Circuits**.)
Switch Crosstalk	K_{CR}	–60	—	–60	–70	—	–60	—	dB	f = 5 MHz, 50Ω load (See **Section 3.1, Test Circuits**.)
Output Switch Isolation Diode Current	I_{ID}	—	300	—	—	300	—	300	mA	300 ns pulse width, 2% duty cycle (See **Section 3.1, Test Circuits**.)
Off Capacitance SW to GND	$C_{SG(OFF)}$	—	14	—	9	14	—	14	pF	V_{SIG} = 0V, f = 1 MHz both SW OFF
Off Capacitance Y to GND		—	28	—	18	28	—	28	pF	
On Capacitance SW to GND	$C_{SG(ON)}$	—	33	—	23	33	—	33	pF	V_{SIG} = 0V, f = 1 MHz one SW ON, one SW OFF
On Capacitance Y to GND		—	33	—	23	33	—	33	pF	
Output Voltage Spike SW	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +40V, V_{NN} = –160V, R_{LOAD} = 50Ω (See **Section 3.1, Test Circuits**.)
	$-V_{SPK}$	—	—	—	—	–150	—	—	mV	
	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +100V, V_{NN} = –100V, R_{LOAD} = 50Ω (See **Section 3.1, Test Circuits**.)
	$-V_{SPK}$	—	—	—	—	–150	—	—	mV	
	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +160V, V_{NN} = –40V, R_{LOAD} = 50Ω (See **Section 3.1, Test Circuits**.)
	$-V_{SPK}$	—	—	—	—	–150	—	—	mV	

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

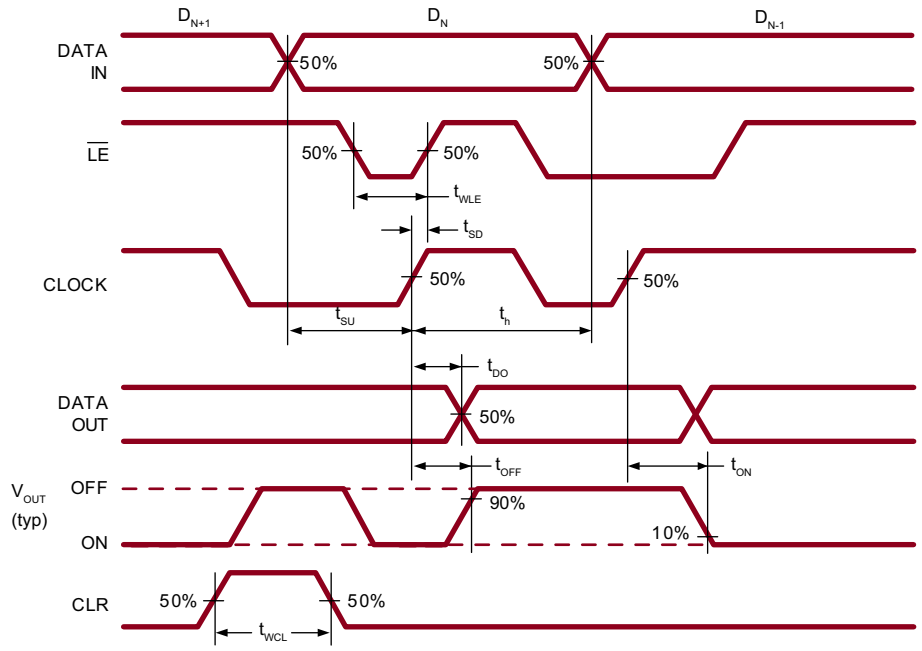
Electrical Specifications: Unless otherwise specified, all values are over operating conditions.
V_{DD} = 5V, $t_r = t_f \leq 5$ ns, 50% duty cycle and C_{LOAD} = 20 pF.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Output Voltage Spike Y	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +40V, V_{NN} = –160V, R_{LOAD} = 50Ω (See **Section 3.1, Test Circuits**.)
	$-V_{SPK}$	—	—	—	—	–150	—	—	mV	
	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +100V, V_{NN} = –100V, R_{LOAD} = 50Ω (See **Section 3.1, Test Circuits**.)
	$-V_{SPK}$	—	—	—	—	–150	—	—	mV	
	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +160V, V_{NN} = –40V, R_{LOAD} = 50Ω (See **Section 3.1, Test Circuits**.)
	$-V_{SPK}$	—	—	—	—	–150	—	—	mV	
Charge Injection (Per Switch)	QC	—	—	—	820	—	—	—	pC	V_{PP} = +40V, V_{NN} = –160V (See **Section 3.1, Test Circuits**.)
		—	—	—	600	—	—	—	pC	V_{PP} = +100V, V_{NN} = –100V (See **Section 3.1, Test Circuits**.)
		—	—	—	350	—	—	—	pC	V_{PP} = +160V, V_{NN} = –40V (See **Section 3.1, Test Circuits**.)

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	0	—	70	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
64-lead QFN	θ_{JA}	—	21	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The description of pins in HV2801 and HV2901 are listed on Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	HV2801 Pin Name	HV2901 Pin Name	Description
1	SW30	SW30	Analog Switch 30 Terminal
2	Y3031	Y3031	Analog Switch 30 and 31 Common Terminal
3	SW31	SW31	Analog Switch 31 Terminal
4	NC	NC	No connection
5	CLR	CLR	Clear logic input
6	NC	NC	No connection
7	$\overline{LE}$	$\overline{LE}$	Latch-enable logic input, low active
8	CLK	CLK	Clock logic input for Shift register
9	VDD	VDD	Logic supply voltage
10	DIN	DIN	Data in logic input
11	GND	GND	Ground
12	DOUT	DOUT	Data out logic output
13	NC	NC	No connection
14	SW0	SW0	Analog Switch 0 Terminal
15	Y01	Y01	Analog Switch 0 and 1 Common Terminal
16	SW1	SW1	Analog Switch 1 Terminal
17	SW2	SW2	Analog Switch 2 Terminal
18	Y23	Y23	Analog Switch 2 and 3 Common Terminal
19	SW3	SW3	Analog Switch 3 Terminal
20	SW4	SW4	Analog Switch 4 Terminal
21	Y45	Y45	Analog Switch 4 and 5 Common Terminal
22	SW5	SW5	Analog Switch 5 Terminal
23	SW6	SW6	Analog Switch 6 Terminal
24	Y67	Y67	Analog Switch 6 and 7 Common Terminal
25	SW7	SW7	Analog Switch 7 Terminal
26	SW8	SW8	Analog Switch 8 Terminal
27	Y89	Y89	Analog Switch 8 and 9 Common Terminal
28	SW9	SW9	Analog Switch 9 Terminal
29	SW10	SW10	Analog Switch 10 Terminal
30	Y1011	Y1011	Analog Switch 10 and 11 Common Terminal
31	SW11	SW11	Analog Switch 11 Terminal
32	SW12	SW12	Analog Switch 12 Terminal
33	Y1213	Y1213	Analog Switch 12 and 13 Common Terminal
34	SW13	SW13	Analog Switch 13 Terminal
35	VPP	VPP	Positive supply voltage
36	NC	—	No connection
	—	RGND	Ground for bleed resistor

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	HV2801 Pin Name	HV2901 Pin Name	Description
37	VNN	VNN	Negative voltage supply
38	SW14	SW14	Analog Switch 14 Terminal
39	Y1415	Y1415	Analog Switch 14 and 15 Common Terminal
40	SW15	SW15	Analog Switch 15 Terminal
41	SW16	SW16	Analog Switch 16 Terminal
42	Y1617	Y1617	Analog Switch 16 and 17 Common Terminal
43	SW17	SW17	Analog Switch 17 Terminal
44	VNN	VNN	Negative voltage supply
45	NC	—	No connection
	—	RGND	Ground for bleed resistor
46	VPP	VPP	Positive supply voltage
47	SW18	SW18	Analog Switch 18 Terminal
48	Y1819	Y1819	Analog Switch 18 and 19 Common Terminal
49	SW19	SW19	Analog Switch 19 Terminal
50	SW20	SW20	Analog Switch 20 Terminal
51	Y2021	Y2021	Analog Switch 20 and 21 Common Terminal
52	SW21	SW21	Analog Switch 21 Terminal
53	SW22	SW22	Analog Switch 22 Terminal
54	Y2223	Y2223	Analog Switch 22 and 23 Common Terminal
55	SW23	SW23	Analog Switch 23 Terminal
56	SW24	SW24	Analog Switch 24 Terminal
57	Y2425	Y2425	Analog Switch 24 and 25 Common Terminal
58	SW25	SW25	Analog Switch 25 Terminal
59	SW26	SW26	Analog Switch 26 Terminal
60	Y2627	Y2627	Analog Switch 26 and 27 Common Terminal
61	SW27	SW27	Analog Switch 27 Terminal
62	SW28	SW28	Analog Switch 28 Terminal
63	Y2829	Y2829	Analog Switch 28 and 29 Common Terminal
64	SW29	SW29	Analog Switch 29 Terminal
VSUB (Thermal Pad)			The central thermal pad on the bottom of package must be connected to VNN externally.

3.0 FUNCTIONAL DESCRIPTION

3.1 Test Circuits

Figure 3-1 to Figure 3-9 show the test circuits for HV2801/HV2901.

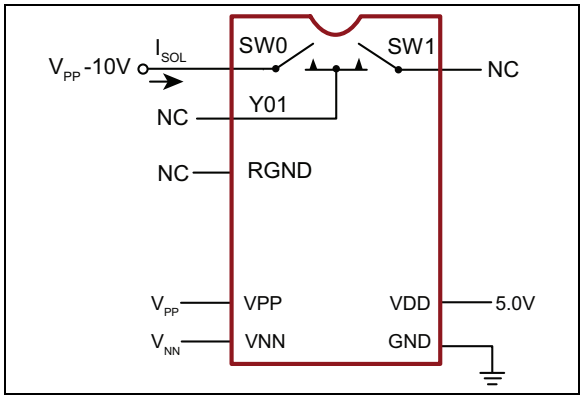


FIGURE 3-1: *Switch Off Leakage.*

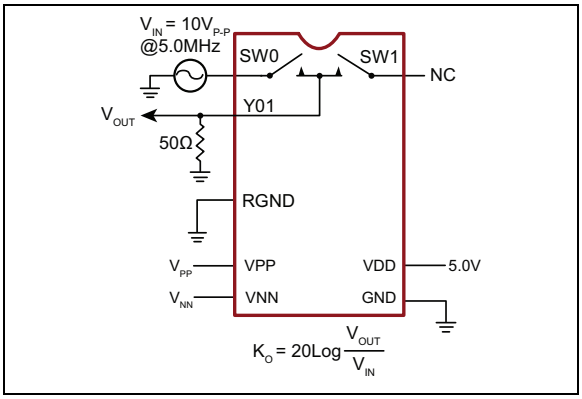


FIGURE 3-4: *Off Isolation.*

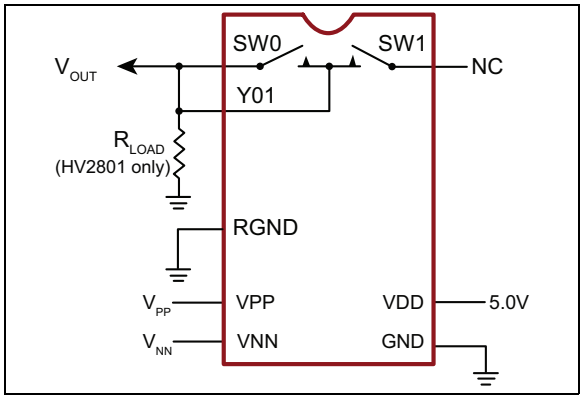


FIGURE 3-2: Switch DC Offset.

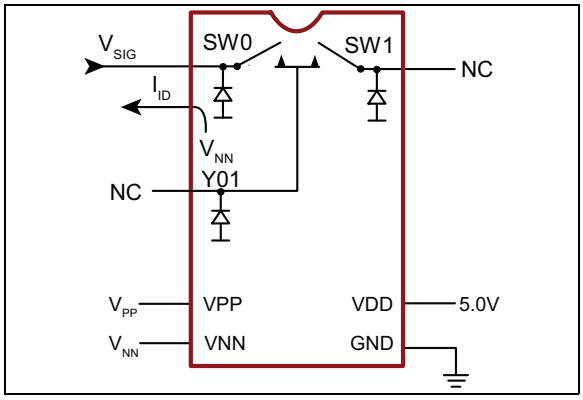


FIGURE 3-5: *Output Switch Isolation Diode Current.*

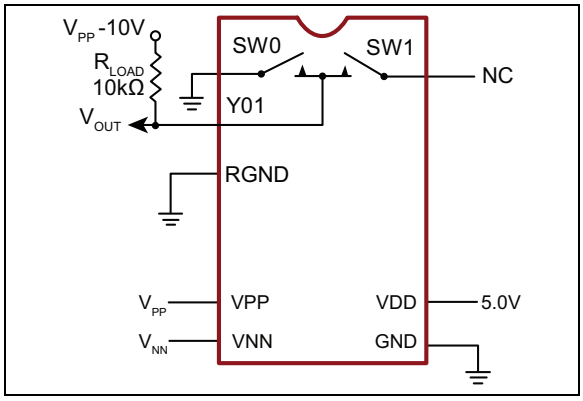


FIGURE 3-3: *T_{ON}/T_{OFF} Test Circuit.*

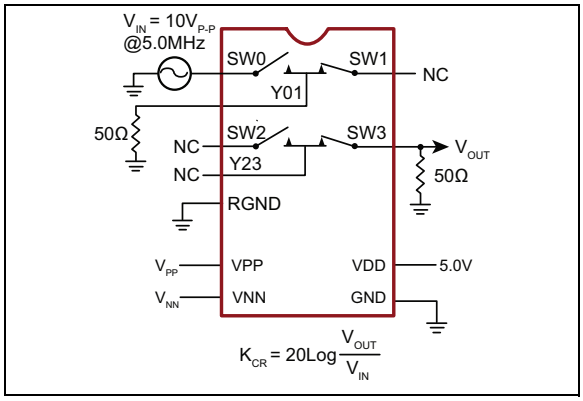


FIGURE 3-6: *Switch Crosstalk.*

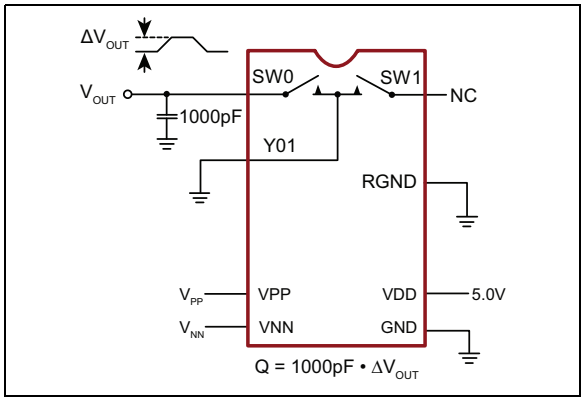


FIGURE 3-7: *Charge Injection.*

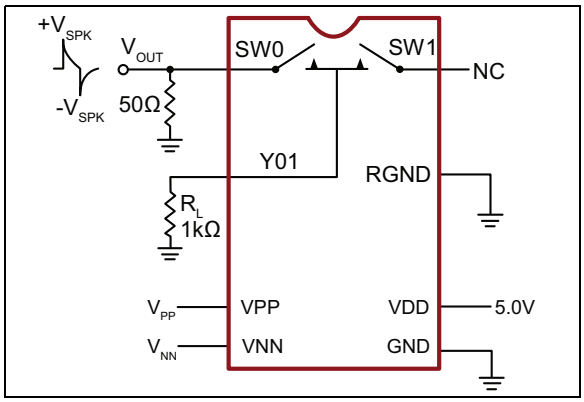


FIGURE 3-8: *Output Voltage Spike SW.*

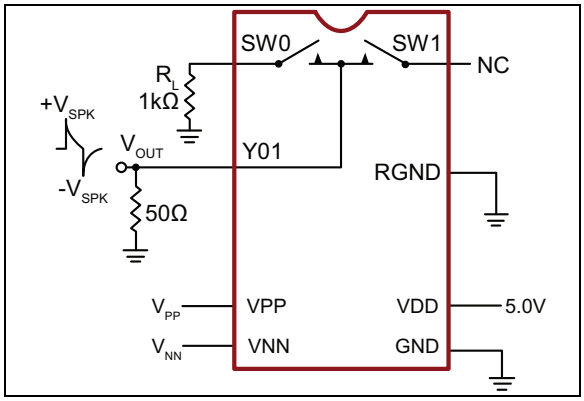


FIGURE 3-9: *Output Voltage Spike Y.*

TABLE 3-1: TRUTH FUNCTION TABLE

D0	D1	...	D15	D16	...	D31	$\overline{LE}$	CLR	SW0	SW1	...	SW15	SW16	...	SW31
L							L	L	OFF						
H							L	L	ON						
	L						L	L		OFF					
	H						L	L		ON					
							L	L							
							L	L							
			L				L	L				OFF			
			H				L	L				ON			
		...		L	...		L	L			...		OFF	...	
				H			L	L					ON		
							L	L							
							L	L							
							L	L							
							L	L							
						L	L	L							OFF
						H	L	L							ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Note 1: The 32 switches operate independently.

2: Serial data is clocked in on the L to H transition of the CLK.

3: All 32 switches go to a state retaining their Latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the Shift registers' data flow through the latch.

4: D_{OUT} is high when data in the Register 31 is high.

5: Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.

6: The CLR clear input overrides all other inputs.

4.0 PACKAGE MARKING INFORMATION

4.1 Package Marking Information

64-lead QFN

Example

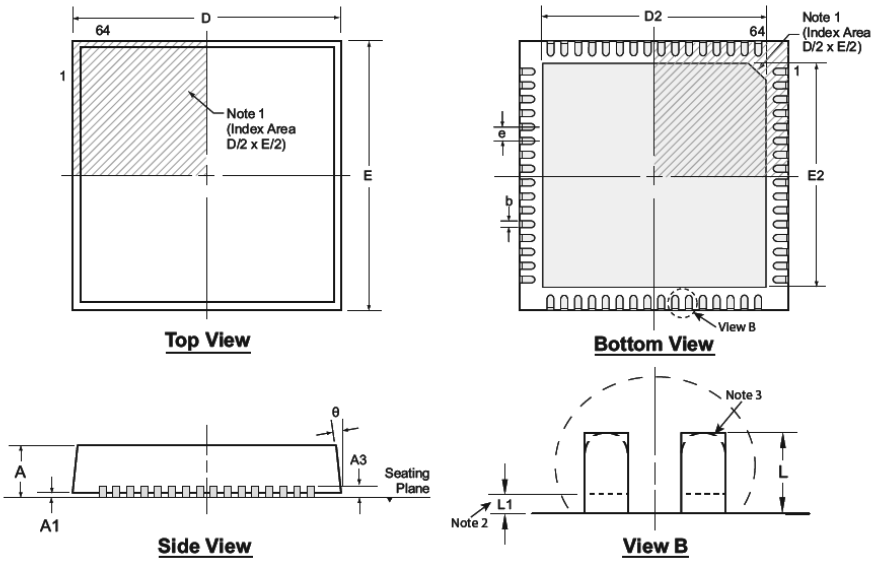
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

64-Lead QFN Package Outline (K6)

9.00x9.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	8.85*	6.00	8.85*	6.00	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	9.00	7.70*	9.00	7.70*		0.40	-	-
	MAX	1.00	0.05		0.30	9.15*	7.80†	9.15*	7.80†		0.50	0.15	14°

JEDEC Registration MO-220, Variation VMMD-4, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (July 2019)

- Converted and merged Supertex Doc#s DSFP-HV2801 and DSFP-HV2901 to Microchip DS20005840A
- Removed the “HVCMOS® Technology for high performance” from the Features and General Description sections
- Changed the package marking format
- Made minor changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Devices:	HV2801	=	32-Channel Low-Charge-Injection High-Voltage Analog Switch
	HV2901	=	32-Channel Low-Charge-Injection High-Voltage Analog Switch with Bleed Resistors
Package:	K6	=	64-lead QFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	260/Tray for a K6 Package

Examples:

a) HV2801K6-G: 32-Channel Low-Charge-Injection High-Voltage Analog Switch, 64-lead QFN, 260/Tray

b) HV2901K6-G: 32-Channel Low-Charge-Injection High-Voltage Analog Switch with Bleed Resistors, 64-lead QFN, 260/Tray

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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ISBN: 978-1-5224-4757-3

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