DALLAS JUI / XI/

DS2151Q T1 Single-Chip Transceiver

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FEATURES

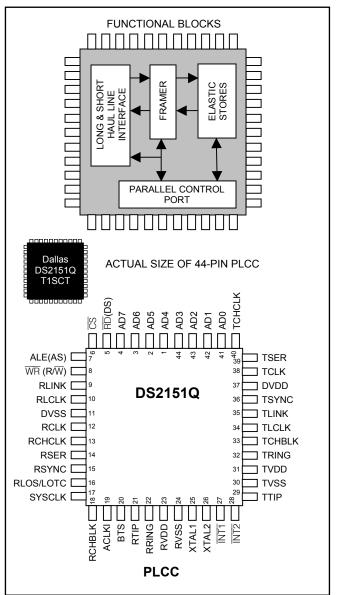
- Complete DS1/ISDN-PRI Transceiver Functionality
- Line Interface Can Handle Both Long- and Short-Haul Trunks
- 32-Bit or 128-Bit Jitter Attenuator
- Generates DSX-1 and CSU Line Build-Outs
- Frames to D4, ESF, and SLC-96^R Formats
- Dual On-Board Two-Frame Elastic Store Slip Buffers that Connect to Backplanes Up to 8.192MHz
- 8-Bit Parallel Control Port That can be Used on Either Multiplexed or Nonmultiplexed Buses
- Extracts and Inserts Robbed-Bit Signaling
- Detects and Generates Yellow and Blue Alarms
- Programmable Output Clocks for Fractional T1
- Fully Independent Transmit and Receive Functionality
- On-Board FDL Support Circuitry
- Generates and Detects CSU Loop Codes
- Contains ANSI One's Density Monitor and Enforcer
- Large Path and Line Error Counters Including BPV, CV, CRC6, and Framing Bit Errors
- Pin Compatible with DS2153Q E1 Single-Chip Transceiver
- 5V Supply; Low-Power CMOS

ORDERING INFORMATION

PART	TEMP	PIN-
IANI	RANGE	PACKAGE
DS2151Q	0° C to $+70^{\circ}$ C	44 PLCC
DS2151Q+	0° C to $+70^{\circ}$ C	44 PLCC
DS2151QN	-40°C to +85°C	44 PLCC
DS2151QN+	-40°C to +85°C	44 PLCC

+Denotes lead-free/RoHS-compliant package.

PIN CONFIGURATION



Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: <u>www.maxim-ic.com/errata</u>.

TABLE OF CONTENTS

1 DE1	AILED DESCRIPTION	.4
1.1	INTRODUCTION	.4
2 PIN	DESCRIPTION	.6
2.1	DS2151Q REGISTER MAP	.8
	NTROL REGISTERS	
	LOCAL LOOPBACK	
	REMOTE LOOPBACK	
	Payload Loopback	-
4.4	FRAMER LOOPBACK	15
4.5	LOOP CODE GENERATION1	8
	PULSE DENSITY ENFORCER1	
	POWER-UP SEQUENCE1	
	TUS AND INFORMATION REGISTERS1	
5.1	LOOP UP/DOWN CODE DETECTION	23
6 ERF	ROR COUNT REGISTERS	27
6.1	LINE CODE VIOLATION COUNT REGISTER (LCVCR)	27
	PATH CODE VIOLATION COUNT REGISTER (PCVCR)2	
6.3	MULTIFRAMES OUT OF SYNC COUNT REGISTER (MOSCR)2	29
7 FDL	/FS EXTRACTION AND INSERTION	30
7.1	RECEIVE SECTION	30
7.2	TRANSMIT SECTION	31
8 SIG	NALING OPERATION	32
9 TRA	ANSMIT TRANSPARENCY AND IDLE REGISTERS	34
	LOCK BLOCKING REGISTERS	
	_ASTIC STORES OPERATION	
11.1	RECEIVE SIDE	
11.1	TRANSMIT SIDE	
11.3	MINIMUM DELAY SYNCHRONOUS SYSCLK MODE	
	ECEIVE MARK REGISTERS	
	NE INTERFACE FUNCTIONS	
13.1	RECEIVE CLOCK AND DATA RECOVERY	
13.1	TRANSMIT WAVESHAPING AND LINE DRIVING	
13.3	JITTER ATTENUATOR	
	MING DIAGRAMS	
	C CHARACTERISTICS	
	C CHARACTERISTICS	
17 P/	ACKAGE INFORMATION	
17.1	44-PIN PLCC (56-G4003-001)6	30

LIST OF FIGURES

Figure 1-1. DS2151Q Block Diagram	5
Figure 13-1. External Analog Connections	
Figure 13-2. Jitter Tolerance	43
Figure 13-3. Transmit Waveform Template	
Figure 13-4. Jitter Attenuation	
Figure 14-1. Receive Side D4 Timing	
Figure 14-2. Receive Side ESF Timing	
Figure 14-3. Receive Side Boundary Timing with Elastic Store(s) Disabled	47
Figure 14-4. 1.544MHz Boundary Timing with Elastic Store(s) Enabled	47
Figure 14-5. 2.048MHz Boundary Timing with Elastic Store(s) Enabled	48
Figure 14-6. Transmit Side D4 Timing	48
Figure 14-7. Transmit Side ESF Timing	49
Figure 14-8. Transmit Side Boundary Timing with Elastic Store(s) Disabled	50
Figure 14-9. Transmit Data Flow	51
Figure 16-1. Intel Bus Read AC Timing	
Figure 16-2. Intel Bus Write AC Timing	
Figure 16-3. Motorola Bus AC Timing	
Figure 16-4. Receive Side AC Timing	
Figure 16-5. Transmit Side AC Timing	

LIST OF TABLES

Table 4-1. Output Pin Test Modes	13
Table 5-1. Receive T1 Level Indication	21
Table 5-2. Alarm Set and Clear Criteria	23
Table 6-1. Line Code Violation Counting Arrangements	27
Table 6-2. Path Code Violation Counting Arrangements	28
Table 6-3. Multiframes Out of Sync Counting Arrangements	29
Table 13-1. Source of RCLK Upon RCL.	40
Table 13-2. LBO Select in LICR	41
Table 13-3. Transformer Specifications	41
Table 13-4. Crystal Selection Guidelines	42
Table 15-1. Recommended DC Characteristics	
Table 15-2. Capacitance	52
Table 15-3. DC Characteristics	52
Table 16-1. AC Characteristics—Parallel Port	
Table 16-2. AC Characteristics—Receive Side	56
Table 16-3. AC Characteristics—Transmit Side	58

1 DETAILED DESCRIPTION

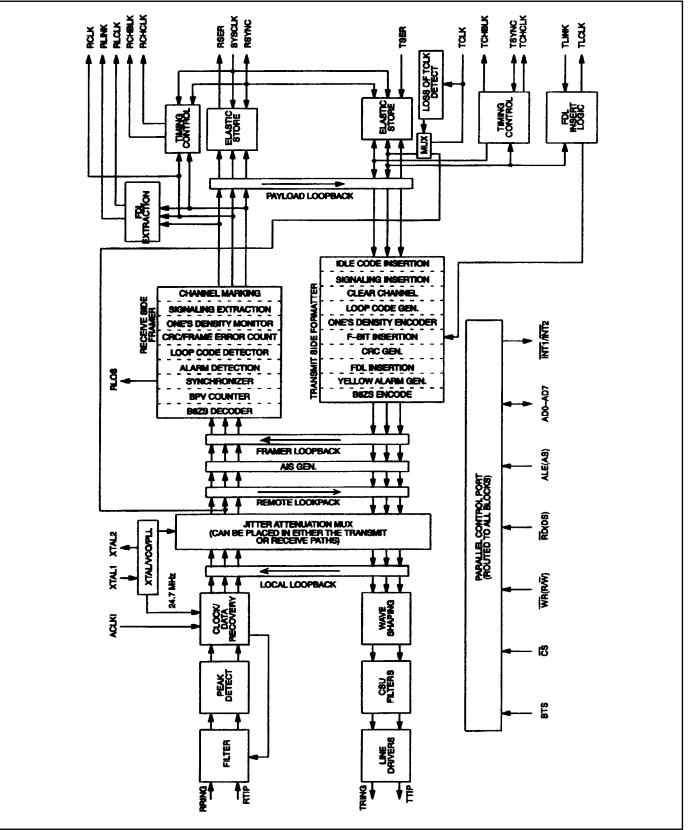
The DS2151Q T1 single-chip transceiver (SCT) contains all the necessary functions for connection to T1 lines whether they be DS-1 long haul or DSX-1 short haul. The clock recovery circuitry automatically adjusts to T1 lines from 0 feet to over 6000 feet in length. The device can generate both DSX-1 line build-outs as well as CSU build-outs of -7.5dB, -15dB, and -22.5dB. The on-board jitter attenuator (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting robbed-bit signaling data and FDL data. The device contains a set of 64 8-bit internal registers that the user can access to control the operation of the unit. Quick access via the parallel control port allows a single micro to handle many T1 lines. The device fully meets all of the latest T1 specifications including ANSI T1.403-199X, AT&T TR 62411 (12-90), and ITU G.703, G.704, G.706, G.823, and I.431.

1.1 Introduction

The analog AMI waveform off of the T1 line is transformer coupled into the RRING and RTIP pins of the DS2151Q. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive side framer where the digital serial stream is analyzed to locate the framing pattern. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered T1 data stream and an asynchronous backplane clock which is provided at the SYSCLK input.

The transmit side of the DS2151Q is totally independent from the receive side in both the clock requirements and characteristics. Data can be either provided directly to the transmit formatter or via an elastic store. The transmit formatter will provide the necessary data overhead for T1 transmission. Once the data stream has been prepared for transmission, it is sent via the jitter attenuation mux to the waveshaping and line driver functions. The DS2151Q will drive the T1 line from the TTIP and TRING pins via a coupling transformer.

Figure 1-1. DS2151Q Block Diagram



2 PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1-4,	AD4–AD7,		
41-44	AD0-AD3	I/O	Address/Data Bus. An 8-bit multiplexed address/data bus.
5	$\overline{\text{RD}}(\text{DS})$	Ι	Active-Low Read Input (Data Strobe)
6	\overline{CS}	Ι	Active-Low Chip Select. Must be low to read or write the port.
7	ALE(AS)	Ι	Address Latch Enable (Address Strobe). A positive going edge serves to demultiplex the bus.
8	$\overline{WR}(R/\overline{W})$	Ι	Active-Low Write Input (Read/Write)
9	RLINK	О	Receive Link Data. Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame. See Section <u>14</u> for timing details.
10	RLCLK	0	Receive Link Clock. 4kHz or 2kHz (ZBTSI) demand clock for the RLINK output. See Section <u>14</u> for timing details.
11	DVSS		Digital Signal Ground. 0.0V. Should be tied to local ground plane.
12	RCLK	0	Receive Clock. Recovered 1.544MHz clock.
13	RCHCLK	О	Receive Channel Clock . 192kHz clock that pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data, locating Robbed-Bit signaling bits, and for blocking clocks in DDS applications. See Section <u>14</u> for timing details.
14	RSER	0	Receive Serial Data. Received NRZ serial data, updated on rising edges of RCLK or SYSCLK.
15	RSYNC	I/O	Receive Sync. An extracted pulse, one RCLK wide, is output at this pin, which identifies either frame (RCR2.4 = 0) or multiframe boundaries (RCR2.4 = 1). If set to output frame boundaries, then via RCR2.5, RSYNC can also be set to output double-wide pulses on signaling frames. If the elastic store is enabled via the CCR1.2, then this pin can be enabled to be an input via RCR2.3 at which a frame boundary pulse is applied. See Section <u>14</u> for timing details.
16	RLOS/LOT C	Ο	Receive Loss of Sync/Loss of Transmit Clock. A dual function output. If CCR3.5 = 0, will toggle high when the synchronizer is searching for the T1 frame and multiframe; if CCR3.5 = 1, will toggle high if the TCLK pin has not toggled for 5μ s.
17	SYSCLK	Ι	System Clock. 1.544MHz or 2.048MHz clock. Only used when the elastic store functions are enabled via either CCR1.7 or CCR1.2. Should be tied low in applications that do not use the elastic store. If tied high for more than 100μ s, will force all output pins (including the parallel port) to tristate.
18	RCHBLK	Ο	Receive Channel Block. A user-programmable output that can be forced high or low during any of the 24 T1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384kbps service, 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Section <u>14</u> for timing details.
19	ACLKI	Ι	Alternate Clock Input. Upon a receive carrier loss, the clock applied at this pin (normally 1.544MHz) will be routed to the RCLK pin. If no clock is routed to this pin, then it should be tied to DVSS via a $1k\Omega$ resistor.

PIN	NAME	TYPE	FUNCTION
20	BTS	Ι	Bus Type Select. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{\text{RD}}(\text{DS})$, ALE(AS), and $\overline{\text{WR}}(\text{R}/\overline{\text{W}})$ pins. If BTS = 1, then these pins assume the function listed in parentheses.
21, 22	RTIP, RRING		Receive Tip and Ring. Analog inputs for clock recovery circuitry; connects to a 1:1 transformer (see Section 13 for details).
23	RVDD		Receive Analog Positive Supply . 5.0V. Should be tied to DVDD and TVDD pins.
24	RVSS		Receive Signal Ground. 0V. Should be tied to local ground plane.
25, 26	XTAL1, XTAL2		Crystal Connections. A pullable 6.176MHz crystal must be applied to these pins. See Section <u>13</u> for crystal specifications.
27	INT1	0	Receive Alarm Interrupt 1. Flags host controller during alarm conditions defined in Status Register 1. Active low, open drain output.
28	ĪNT2	0	Receive Alarm Interrupt 2. Flags host controller during conditions defined in Status Register 2. Active low, open drain output.
29	TTIP		Transmit Tip. Analog line driver output; connects to a step-up transformer (see Section 13 for details).
30	TVSS		Transmit Signal Ground. 0V. Should be tied to local ground plane.
31	TVDD		Transmit Analog Positive Supply. 5.0V. Should be tied to DVDD and RVDD pins.
32	TRING		Transmit Ring . Analog line driver outputs; connects to a step-up transformer (see Section 13 for details).
33	TCHBLK	0	Transmit Channel Block . A user-programmable output that can be forced high or low during any of the 24 T1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384kbps service, 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Section <u>14</u> for timing details.
34	TLCLK	0	Transmit Link Clock. 4kHz or 2kHz (ZBTSI) demand clock for the TLINK input. See Section <u>14</u> for timing details.
35	TLINK	Ι	Transmit Link Data. If enabled via TCR1.2, this pin will be sampled during the F-bit time on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs bit position (D4) or the Z-bit position (ZBTSI). See Section 14 for timing details.
36	TSYNC	I/O	Transmit Sync. A pulse at this pin will establish either frame or multiframe boundaries for the DS2151Q. Via TCR2.2, the DS2151Q can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double-wide pulses at signaling frames. See Section <u>14</u> for timing details.
37	DVDD		Digital Positive Supply. 5.0V. Should be tied to RVDD and TVDD pins.
38	TCLK	Ι	Transmit Clock. 1.544MHz primary clock.
39	TSER	Ι	Transmit Serial Data. Transmit NRZ serial data, sampled on the falling edge of TCLK.
40	TCHCLK	0	Transmit Channel Clock. 192kHz clock that pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section <u>14</u> for timing details.

2.1 DS2151Q Register Map

ADDRESS	R/W	REGISTER NAME	ADDRESS	R/W	REGISTER NAME
20	R/W	Status Register 1	30	R/W	Common Control Register 3
21		Status Register 2	31	R/W	Receive Information Register 2
22	R/W	Receive Information Register 1	32	R/W	Transmit Channel Blocking Register 1
23	R	Line Code Violation Count Register 1	33	R/W	Transmit Channel Blocking Register 2
24	R	Line Code Violation Count Register 2	34	R/W	Transmit Channel Blocking Register 3
25	R	Path Code Violation Count Register 1 (Note 1)	35	R/W	Transmit Control Register 1
26	R	Path Code Violation Count Register 2	36	R/W	Transmit Control Register 2
27	R	Multiframe Out of Sync Count Register 2	37	R/W	Common Control Register 1
28	R	Receive FDL Register	38	R/W	Common Control Register 2
29	R/W	Receive FDL Match Register 1	39	R/W	Transmit Transparency Register 1
2A	R/W	Receive FDL Match Register 2	3A	R/W	Transmit Transparency Register 2
2B	R/W	Receive Control Register 1	3B	R/W	Transmit Transparency Register 3
2C	R/W	Receive Control Register 2	3C	R/W	Transmit Idle Register 1
2D	R/W	Receive Mark Register 1	3D	R/W	Transmit Idle Register 2
2E	R/W	Receive Mark Register 2	3E	R/W	Transmit Idle Register 3
2F	R/W	Receive Mark Register 3	3F	R/W	Transmit Idle Definition Register
60	R	Receive Signaling Register 1	70	R/W	Transmit Signaling Register 1
61	R	Receive Signaling Register 2	71	R/W	Transmit Signaling Register 2
62	R	Receive Signaling Register 3	72	R/W	Transmit Signaling Register 3
63	R	Receive Signaling Register 4	73	R/W	Transmit Signaling Register 4
64	R	Receive Signaling Register 5	74	R/W	Transmit Signaling Register 5
65		Receive Signaling Register 6	75	R/W	Transmit Signaling Register 6
66	R	Receive Signaling Register 7	76	R/W	Transmit Signaling Register 7
67		Receive Signaling Register 8	77	R/W	Transmit Signaling Register 8
68		Receive Signaling Register 9	78	R/W	Transmit Signaling Register 9
69	R	Receive Signaling Register 10	79	R/W	Transmit Signaling Register 10
6A	R	Receive Signaling Register 11	7A	R/W	Transmit Signaling Register 11
6B	R	Receive Signaling Register 12	7B	R/W	Transmit Signaling Register 12
6C	R/W	Receive Channel Blocking Register 1	7C	R/W	Line Interface Control Register
6D	R/W	Receive Channel Blocking Register 2	7D	R/W	Test Register (Note 2)
6E	R/W	Receive Channel Blocking Register 3	7E	R/W	Transmit FDL Register
6F	R/W	Interrupt Mask Register 2	7F	R/W	Interrupt Mask Register 1

Note 1: Address 25 also contains Multiframe Out of Sync Count Register 1. *Note 2:* The Test Register is used only by the factory; this register must be cleared (set to all 0s) on power-up initialization to insure proper operation.

3 PARALLEL PORT

The DS2151Q is controlled via a multiplexed bidirectional address/data bus by an external microcontroller or microprocessor. The DS2151Q can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parentheses (). See the timing diagrams in Section <u>14</u> for more details. The multiplexed bus on the DS2151Q saves pins because the address information and data information share the same signal paths. The addresses are presented to the pins in the first portion of the bus cycle and data will be transferred on the pins during second portion of the bus cycle. Addresses must be valid prior to the falling edge of ALE (AS), at which time the DS2151Q latches the address from the AD0 to AD7 pins. Valid write data must be present and held stable during the later portion of the DS or WR pulses. In a read cycle, the DS2151Q outputs a byte of data during the latter portion of the DS or RD pulses. The read cycle is terminated and the bus returns to a high impedance state as RD transitions high in Intel timing or as DS transitions low in Motorola timing. The DS2151Q can also be easily connected to nonmultiplexed buses. Refer to the separate application note for a detailed discussion of this topic.

4 CONTROL REGISTERS

The operation of the DS2151Q is configured via a set of eight registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS2151Q has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), a Line Interface Control Register (LICR), and three Common Control Registers (CCR1, CCR2, and CCR3). Seven of the eight registers are described below. The LICR is described in Section <u>13</u>.

(MSB)				· ·		,	(LSB)
LCVCRF	ARC	OOF1	OOF2	SYNCC	SYNCT	SYNCE	RESYNC
	SYMBOL PO LCVCRF R		Line Code V	D DESCRIPT Violation Cou ount excessive cessive 0s	Int Register	Function Se	elect.
ARC]	RCR1.6	•	c Criteria. on OOF or RC on OOF only	CL event		
OOF1]	RCR1.5		me Select 1. e bits in error e bits in error			
OOF2]	RCR1.4	Out Of France $0 = \text{follow R}$ 1 = 2/6 frame				
SYNCC]	RCR1.3	1 = cross conIn ESF Fram0 = search for	ng Mode or Ft pattern, t uple Ft and Fs	s pattern		
SYNCT]	RCR1.2	Sync Time . 0 = qualify 1 1 = qualify 2				
SYNCE]	RCR1.1	Sync Enable 0 = auto resy 1 = auto resy	nc enabled			
RESYNC	;]	RCR1.0	of the receiv	en toggled fr ve side framer ubsequent res	is initiated.		

RCR1: RECEIVE CONTROL REGISTER 1 (Address = 2B Hex)

MSB)				-			(LSB)
RCS	RZBTSI	RSDW	RSM	RSIO	RD4YM	FSBE	MOSCRF
Y MBOL RCS		SITION CR2.7	NAME AND Receive Code 0 = idle code 1 = digital mi	e Select. (7F Hex)	T ION (1E/0B/0B/1E	/9E/8B/8B/	⁄9E Hex)
RZBTSI	R	CR2.6	Receive Side 0 = ZBTSI di 1 = ZBTSI er	sabled	ble.		
RSDW	R	2CR2.5	1 = do pulse do	lse double-w double-wide	ide in signalin in signaling fr R2.4 = 1 or wh	ames (Note	
RSM	R	2CR2.4		de (see the ti	ming in Section the timing in S	· · ·	
RSIO RCR2.3		RSYNC I/O Select. 0 = RSYNC is an output 1 = RSYNC is an input (only valid if elastic store enabl (Note: this bit must be set to 0 when CCR1.2 = 0.)				nabled)	
RD4YM RCR2.2		Receive Side 0 = 0s in bit 2 1 = a 1 in the	of all chann				
FSBE RCR2.1		PCVCR Fs Bit Error Report Enable. 0 = do not report bit errors in Fs bit position; only Ft bit position 1 = report bit errors in Fs bit position as well as Ft bit po					
MOSCRF	R	2CR2.0	0 = count error	ors in the frar	Count Regist ning bit positi ultiframes out	on	n Select.

RCR2: RECEIVE CONTROL REGISTER 2 (Address = 2C Hex)

(MSB)	_			\		- /	(LSB)
LOTCMC	TFPT	ТСРТ	RBSE	GB7S	TLINK	TBL	TYEL
SYMBO LOTCM(DSITION FCR1.7	NAME AND DESCRIPTION Loss Of Transmit Clock Mux Control. Determines we the transmit side formatter should switch to the ever RCLK if the TCLK input should fail to transition (Figure 0 = do not switch to RCLK if TCLK stops 1 = switch to RCLK if TCLK stops				
TFPT	-	TCR1.6	0 = Ft or FPS	bits sourced	Through . (Se internally l at TSER dur		, ,
ТСРТ		TCR1.5	0 = source C	RC6 bits inter	ough. (See no rnally TSER during		
RBSE		ГCR1.4	0 = no signal 1 = signaling	ing is inserted is inserted in	able. (See no d in any chanr n all channels on a channel l	nel (the TTR reg	
GB7S	GB7S TCR1.3 Global Bit 7 Stuffing. (See not 0 = allow the TTR registers containing all 0s are to be Bit 7 1 = force Bit 7 stuffing in all 0 the TTR registers are programm		isters to dete Bit 7 stuffed all 0 byte cha	ermine which			
TLINK		TCR1.2		DL or Fs bits	below.) from TFDL re from the TLN		
TBL		TCR1.1	0 = transmit	data normally	ee note below	,	IEG
TYEL		TCR1.0	Transmit Ye 0 = do not transmit Ye 1 = transmit Ye	ansmit yellow	(See note bel alarm	ow.)	

TCR1: TRANSMIT CONTROL REGISTER 1 (Address = 35 Hex)

Note: For a detailed description of how the bits in TCR1 affect the transmit side formatter of the DS2151Q, see Figure 14-9.

MSB)	TRATA		TOPWY		TOTO		(LSB)
EST1	TEST0	TZBTSI	TSDW	TSM	TSIO	TD4YM	B7ZS
SYMBOI TEST1		D SITION TCR2.7	NAME AND Test Mode B			Table 4-1.	
TEST0		TCR2.6	Test Mode B	sit 0 for Outp	out Pins. See	<u>Table 4-1</u> .	
TZBTSI		TCR2.5	Transmit Sid 0 = ZBTSI di 1 = ZBTSI er	sabled	able.		
TSDW		TCR2.4	TSYNC Dou TCR2.3 = 1 o 0 = do not pu 1 = do pulse o	or when TCR	2.2 = 0.) ide in signali	-	to 0 whe
TSM TCR2.3		TSYNC Mode Select. 0 = frame mode (see the timing in Section <u>14</u>) 1 = multiframe mode (see the timing in Section <u>14</u>)					
TSIO		TCR2.2	TSYNC I/O 0 = TSYNC i 1 = TSYNC i	s an input			
TD4YM TCR2.1		Transmit Sid 0 = 0s in bit 2 1 = 1 in the S	2 of all chann	els	ect.		
B7ZS	У	XTCR2.0	Bit 7 Zero S 0 = No stuffin 1 = Bit 7 forc	ng occurs		ıll Os	

TCR2: TRANSMIT CONTROL REGISTER 2 (Address = 36 Hex)

Table 4-1. Output Pin Test Modes

TEST1	TEST0	EFFECT ON OUTPUT PINS
0	0	Operate normally
0	1	Force all output pins tri-state (including all I/O pins and parallel port pins)
1	0	Force all output pins low (including all I/O pins except parallel port pins)
1	1	Force all output pins high (including all I/O pins except parallel port pins)

MSB)		-		1		-	(LSE
TESE	LLB	RSAO	RLB	SCLKM	RESE	PLB	FLE
SYMBOL TESE		DSITION CCR1.7	Transmit E 0 = elastic st	D DESCRIPT lastic Store En core is bypassed core is enabled	nable.		
LLB	(CCR1.6	Local Loop 0 = loopback 1 = loopback	k disabled			
RSAO	(CCR1.5	0 = allow ro	naling All 1s. bbed signaling robbed signali			
RLB	(CCR1.4	Remote Loo 0 = loopback 1 = loopback	k disabled			
SCLKM	(CCR1.3		lode Select. LK is 1.544MI LK is 2.048MI			
RESE	(CCR1.2	0 = elastic st	stic Store Ena core is bypassed core is enabled			
PLB	(CCR1.1	Payload Lo $0 = loopbacl$ $1 = loopbacl$	c disabled			
FLB	(CCR1.0	Framer Loo 0 = loopback 1 = loopback	k disabled			

CCR1: COMMON CONTROL REGISTER 1 (Address = 37 Hex)

4.1 Local Loopback

When CCR1.6 is set to a 1, the DS2151Q will be forced into Local Loopback (LLB). In this loopback, data will continue to be transmitted as normal through the transmit side of the SCT. Data being received at RTIP and RRING will be replaced with the data being transmitted. Data in this loopback will pass through the jitter attenuator and the jitter attenuator should be programmed to be in the transmit path. LLB is primarily used in debug and test applications. See Figure 1-1 for more details.

4.2 Remote Loopback

When CCR1.4 is set to a 1, the DS2151Q will be forced into Remote Loopback (RLB). In this loopback, data recovered off the T1 line from the RTIP and RRING pins will be transmitted back onto the T1 line (with any BPVs that might have occurred intact) via the TTIP and TRING pins. Data will continue to pass through the receive side of the DS2151Q as it would normally and the data at the TSER input will be ignored. Data in this loopback will pass through the jitter attenuator. RLB is used to place the DS2151Q into "line" loopback, which is a requirement of both ANSI T1.403 and AT&T TR62411. See Figure 1-1 for more details.

4.3 Payload Loopback

When CCR1.1 is set to a 1, the DS2151Q will be forced into Payload Loopback (PLB). Normally, this loopback is only enabled when ESF framing is being performed. In a PLB situation, the DS2151Q will loop the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, they are reinserted by the DS2151Q. When PLB is enabled, the following will occur:

- 1) Data will be transmitted from the TTIP and TRING pins synchronous with RCLK instead of TCLK.
- 2) All the receive side signals will continue to operate normally.
- 3) The TCHCLK and TCHBLK signals are forced low.
- 4) Data at the TSER pin is ignored.
- 5) The TLCLK signal will become synchronous with RCLK instead of TCLK.

4.4 Framer Loopback

When CCR1.0 is set to a 1, the DS2151Q will enter a Framer Loopback (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS2151Q will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

- 1) Unless the RLB is active, an unframed all 1s code will be transmitted at TTIP and TRING.
- 2) Data off the T1 line at RTIP and RRING will be ignored.
- 3) The RCLK output will be replaced with the TCLK input.

(MSB)				•			(LSB)
TFM	TB8ZS	TSLC96	TFDL	RFM	RB8ZS	RSLC96	RFDL
SYMBOI TFM		SITION CCR2.7	NAME AND Transmit Fr 0 = D4 framin 1 = ESF fram	ame Mode S ng mode			
TB8ZS	C	CCR2.6	Transmit B8 0 = B8ZS dis 1 = B8ZS ena	abled			
TSLC96	C	CCR2.5	Transmit SL 0 = SLC-96/F 1 = SLC-96/F	s bit Loading	g disabled	ble.	
TFDL	C	CCR2.4	Transmit FD 0 = 0 stuffer of 1 = 0 stuffer of	disabled	Enable.		
RFM	C	CCR2.3	Receive Fran 0 = D4 framin 1 = ESF fram	ng mode	ect.		
RB8ZS	C	CCR2.2	Receive B8Z 0 = B8ZS dis 1 = B8ZS ena	abled			
RSLC96	C	CCR2.1	Receive SLC 0 = SLC-96 d 1 = SLC-96 e	lisabled			
RFDL	C	CCR2.0	Receive FDL 0 = 0 destuffe 1 = 0 destuffe	er disabled	Enable.		

CCR2: COMMON CONTROL REGISTER 2 (Address = 38 Hex)

(MSB)			RECIOTER				(LSB)	
ESMDM	ESR	P16F	RSMS	PDE	TLD	TLU	LIRST	
SYMBO ESMDN		DSITION CCR3.7	NAME AND Elastic Stor details. 0=elastic stor 1=elastic stor	e Minimum	Delay Mod full two-fram		ion <u>11</u> for	
ESR	(CCR3.6		tores to a kr s been applie	own depth. S ed and is stab	Should be to	ggled after	
P16F CC		CCR3.5	Function of Pin 16. 0 = Receive Loss of Sync (RLOS). 1 = Loss of Transmit Clock (LOTC).					
RSMS	(CCR3.4	conversions f 0 = RSYNC 1 = RSYNC for this bit to	rom D4 to E5 will output a will output a have any aff pulses (RCR2	pulse at every pulse at every ect, the RSYN 2.4 = 1 and	multiframe y other multi NC must be s RCR2.3 =	frame note: et to output 0) and the	
PDE	(CCR3.3	Pulse Densit 0 = disable training 1 = enable training 1	ansmit pulse				
TLD	(CCR3.2	Transmit Loop Down Code (001). 0 = transmit data normally 1 = replace normal transmitted data with Loop Down code					
TLU	(CCR3.1	Transmit Lo $0 = \text{transmit } \mathbf{c}$ 1 = replace not	lata normally	` '	n Loop Up co	de	
LIRST	(CCR3.0	initiate an ir recovery state	nternal reset e machine an on power-up	etting this bit that affects d jitter attenus o. Must be cle	the slicer, A ator. Normall	AGC, clock by this bit is	

CCR3: COMMON CONTROL REGISTER 3 (Address = 30 Hex)

4.5 Loop Code Generation

When either the CCR3.1 or CCR3.2 bits are set to 1, the DS2151Q will replace the normal transmitted payload with either the Loop Up or Loop Down code, respectively. The DS2151Q will overwrite the repeating loop code pattern with the framing bits. The SCT will continue to transmit the loop codes as long as either bit is set. It is an illegal state to have both CCR3.1 and CCR3.2 set to 1 at the same time.

4.6 Pulse Density Enforcer

The SCT always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403-199X:

- no more than 15 consecutive 0s
- at least N 1s in each and every time window of 8 x (N +1) bits where N = 1 through 23

Violations for the transmit and receive data streams are reported in the RIR2.0 and RIR2.1 bits respectively.

When the CCR3.3 is set to 1, the DS2151Q will force the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, the CCR3.3 bit should be set to 0, since B8ZS encoded data streams cannot violate the pulse density requirements.

4.7 Power-Up Sequence

On power-up, after the supplies are stable, the DS2151Q should be configured for operation by writing to all of the internal registers (this includes setting the Test Register to 00Hex) since the contents of the internal registers cannot be predicted on power-up. Next, the LIRST bit should be toggled from 0 to 1 to reset the line interface (it will take the DS2151Q about 40ms to recover from the LIRST being toggled). Finally, after the SYSCLK input is stable, the ESR bit should be toggled from a 0 to a 1 (this step can be skipped if the elastic stores are disabled).

5 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS2151Q: Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register 1 (RIR1), and Receive Information Register 2 (RIR2). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a 1. All of the bits in these registers operate in a latched fashion. This means that if an event occurs and a bit is set to a 1 in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm(s) is still present.

The user will always precede a read of these registers with a write. The byte written to the register will inform the DS2151Q which bits the user wishes to read and have cleared. The user will write a byte to one of these four registers, with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information on. When a 1 is written to a bit location, the read register will be updated with current value and the previous value will be cleared. When a 0 is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically ANDed with the mask byte that was just written and this value should be written back into the same register to ensure that the bit does indeed clear. This second write is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. The write-read-write scheme is unique to the four status registers and it allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2151Q with higher-order software languages.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the INT1 and INT2 pins, respectively. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively.

(MSB)				·			(LSB)	
COFA	8ZD	16ZD	RESF	RESE	SEFE	B8ZS	FBE	
SYMBC COFA		DSITION RIR1.7	NAME AND DESCRIPTION Change of Frame Alignment. Set when the last resyr resulted in a change of frame or multiframe alignment.					
8ZD	8ZD RIR1.6 Eight 0 Detect. Set when a string of eight consecutive been received at RPOS and RNEG.					ve 0s have		
16ZD		RIR1.5	Sixteen 0 Detect. Set when a string of 16 consecutive 0s habeen received at RPOS and RNEG.					
RESF		RIR1.4	Receive Elastic Store Full. Set when the receive elastic store buffer fills and a frame is deleted.					
RESE		RIR1.3	Receive Elastic Store Empty. Set when the receive estore buffer empties and a frame is repeated.					
SEFE		RIR1.2	•	Frored Fram (Ft or FPS) ar	0		out of 6	
B8ZS		RIR1.1	detected at R	word Detect POS and RNI eted or not via	EG independe			
FBE		RIR1.0	Frame Bit I bit is receive	E rror. Set wh d in error.	nen a Ft (D4)	or FPS (ES	F) framing	

RIR1: RECEIVE INFORMATION REGISTER 1 (Address = 22 Hex)

(MSB)						,	(LSB)			
RL1	RL0	TESF	TESE	TSLIP	JALT	RPDV	TPDV			
SYMBC RL1		SITION RIR2.7	NAME AND Receive Leve							
RL0	1	RIR2.6	Receive Leve	Receive Level Bit 0. See <u>Table 5-1</u> .						
TESF]	RIR2.5	Transmit El store buffer fi			en the transr	nit elastic			
TESE]	RIR2.4	Transmit Elastic Store Empty. Set when the transmit elastic store buffer empties and a frame is repeated.							
TSLIP]	RIR2.3	Transmit E transmit elast		-					
JALT	1	RIR2.2	Jitter Attent FIFO reaches jitter attenuat	to within 4 b	oits of its limi	•				
RPDV	. I	RIR2.1	Receive Puls stream does r density.	•						
TPDV	1	RIR2.0	Transmit Pu stream does r density.	•						

RIR2: RECEIVE INFORMATION REGISTER 2 (Address = 31 Hex)

Table 5-1. Receive T1 Level Indication

RL1	RL0	TYPICAL LEVEL RECEIVED (dB)
0	0	+2 to -7.5
0	1	-7.5 to -15
1	0	-15 to -22.5
1	1	Less than -22.5

SR1: STATUS REGISTER 1 (Address = 20 Hex)

(MSB)		- (/			(LSB)	
LUP	LDN	LOTC	RSLIP	RBL	RYEL	RCL	RLOS	
SYMBO LUP	L PC	DSITION SR1.7			I. Set when t	the repeating	00001	
LDN		SR1.6	Loop Down Code Detected . Set when the repeating loop down code is being received.					
LOTC		SR1.5	Loss of Transmit Clock . Set when the TCLK pin has transitioned for one channel time (or 5.2μ s). Will force pin high if enabled via CCR1.6. Based on RCLK.					
RSLIP	RSLIP SR1.4 Receive Elastic Store Slip Occurrence . Set when elastic store has either repeated or deleted a frame.					he receive		
RBL		SR1.3	Receive Blu RTIP and RF			ue alarm is r	eceived at	
RYEL SR1.2			Receive Yellow Alarm . Set when a yellow alarm is received at RTIP and RRING.					
RCL SR1.1		Receive Carrier Loss . Set when 192 consecutive 0s have been detected at RTIP and RRING.						
RLOS		SR1.0	Receive Los to the receive	-	t when the de	vice is not syn	nchronized	

Table 5-2. Alarm Set and Clea	r Criteria
-------------------------------	------------

ALARM	SET CRITERIA	CLEAR CRITERIA
Blue Alarm (AIS) (see note below)	When over a 3ms window, five or	When over a 3ms window, six or
	less 0s are received	more 0s are received
Yellow Alarm	When bit 2 of 256 consecutive	When bit 2 of 256 consecutive
1. D4 bit 2 mode (RCR2.2=0)	channels is set to 0 for at least 254	channels is set to 0 for less than 254
	occurrences	occurrences
2. D4 12 th F-bit mode (RCR2.2=1;		
this mode is also referred to as	When the 12 th framing bit is set to	When the 12 th framing bit is set to 0
the "Japanese Yellow Alarm")	1 for two consecutive occurrences	for two consecutive occurrences
3. ESF Mode	When 16 consecutive patterns of	When 14 or less patterns of 00FF
	00FF hex appear in the FDL	hex out of 16 possible appear in the
		FDL
Red Alarm (RCL) (this alarm is	When 192 consecutive 0s are	When 14 or more 1s out of 112
also referred to as Loss of Signal)	received	possible bit positions are received
		starting with the first 1 received

Note: The definition of Blue Alarm (or Alarm Indication Signal) is an unframed all-ones signal. Blue alarm detectors should be able to operate properly in the presence of a 10-3 error rate and they should not falsely trigger on a framed all-ones signal. The blue alarm criteria in the DS2151Q has been set to achieve this performance. It is recommended that the RBL bit be qualified with the RLOS status bit in detecting a blue alarm.

5.1 Loop Up/Down Code Detection

Bits SR1.7 and SR1.6 will indicate when either the standard Loop Up or Loop Down codes are being received by the DS2151Q. When a Loop Up code has been received for 5 seconds, the CPE is expected to loop the recovered data (without correcting BPVs) back to the source. The Loop Down code indicates that the loopback should be discontinued. See the AT&T publication TR 62411 for more details. The DS2151Q will detect the Loop Up/Down codes in both framed and unframed circumstances with bit error rates as high as 10**-2. The loop code detector has a nominal integration period of 48ms. Hence, after about 48ms of receiving either code, the proper status bit will be set to a 1. After this initial indication, it is recommended that the software poll the DS2151Q every 100ms to 500ms until 5 seconds have elapsed to insure that the code is continuously present. Once 5 seconds have passed, the DS2151Q should be taken into or out of loopback via the Remote Loopback (RLB) bit in CCR1.

(MSB)		· ·		,			(LSB)		
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	-		
SYMBO RMF	L PO	DSITION SR2.7	NAME AND Receive Mul			ıltiframe bour	ndaries.		
TMF		SR2.6	Transmit M	Transmit Multiframe. Set on transmit multiframe boundaries.					
SEC		SR2.5		be set in incre		s of 1 second ms, 999ms, ar			
RFDL		SR2.4	Receive FDL Buffer Full . Set when the receive FDL buffer (RFDL) fills to capacity (8 bits).						
TFDL		SR2.3	Transmit Fl buffer (TFDI		Empty. Set w	when the tran	smit FDL		
RMTCH	I	SR2.2	Receive FD matches eithe			Set when the	he RFDL		
RAF		SR2.1	Receive FD received in th		t when eight	t consecutive	ones are		
_		SR2.0	Not Assigned	d. Should be s	set to 0 when	written.			

SR2: STATUS REGISTER 2 (Address = 21 Hex)

MSB)							(LSB)
LUP	LDN	LOTC	SLIP	RBL	RYEL	RCL	RLOS
SYMBOI LUP		DSITION IMR1.7	Loop Up Co 0 = interrupt	NAME AND DESCRIPTION Loop Up Code Detected. 0 = interrupt masked 1 = interrupt enabled			
LDN		IMR1.6	Loop Down 0 = interrupt 1 = interrupt	masked	ed.		
LOTC		IMR1.5	Loss of Tran 0 = interrupt 1 = interrupt	masked			
SLIP		IMR1.4	Elastic Store 0 = interrupt 1 = interrupt	masked	rence.		
RBL		IMR1.3	Receive Blue 0 = interrupt 1 = interrupt	masked			
RYEL		IMR1.2	Receive Yell 0 = interrupt 1 = interrupt	masked			
RCL		IMR1.1	Receive Car 0 = interrupt 1 = interrupt	masked			
RLOS		IMR1.0	Receive Loss $0 = $ interrupt $1 = $ interrupt	masked			

IMR1: INTERRUPT MASK REGISTER 1 (Address = 7F Hex)

(MSB)							(LSB)
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	
SYMB RMI		POSITION IMR2.7	Receive $0 = inte$	AND DESC e Multiframe rrupt masked rrupt enabled			
TMI	7	IMR2.6	0 = inte	n it Multifran rrupt masked rrupt enabled			
SEC		IMR2.5	0 = inte	cond Timer. rrupt masked rrupt enabled			
RFD	L	IMR2.4	0 = inte	e FDL Buffer rrupt masked rrupt enabled			
TFD	L	IMR2.3	0 = inte	n it FDL Buff rrupt masked rrupt enabled			
RMTC	CH	IMR2.2	0 = inte	e FDL Match rrupt masked rrupt enabled			
RAI	7	IMR2.1	0 = inte	e FDL Abort rrupt masked rrupt enabled			
—		IMR2.0	Not As	signed. Shoul	ld be set to 0 w	hen written t	0.

IMR2: INTERRUPT MASK REGISTER 2 (Address = 6F Hex)

6 ERROR COUNT REGISTERS

There are a set of three counters in the DS2151Q that record bipolar violations, excessive 0s, errors in the CRC6 codewords, framing bit errors, and number of multiframes that the device is out of receive synchronization. Each of these three counters are automatically updated on one second boundaries as determined by the one second timer in Status Register 2 (SR2.5). Hence, these registers contain performance data from the previous second. The user can use the interrupt from the 1-second timer to determine when to read these registers. The user has a full second to read the counters before the data is lost. All three counters will saturate at their respective maximum counts and they will not rollover (note: only the Line Code Violation Count Register has the potential to overflow).

6.1 Line Code Violation Count Register (LCVCR)

Line Code Violation Count Register 1 (LCVCR1) is the most significant word and LCVCR2 is the least significant word of a 16-bit counter that records code violations (CVs). CVs are defined as Bipolar Violations (BPVs) or excessive 0s. See <u>Table 6-1</u> for details of exactly what the LCVCRs count. If the B8ZS mode is set for the receive side via CCR2.2, then B8ZS codewords are not counted. This counter is always enabled; it is not disabled during receive loss of synchronization (RLOS = 1) conditions.

LCVCR1: LINE CODE VIOLATION COUNT REGISTER 1 (Address = 23 Hex) LCVCR2: LINE CODE VIOLATION COUNT REGISTER 2 (Address = 24 Hex)

(MSB)							(LSB)	_
LCV15	LCV14	LCV13	LCV12	LCV11	LCV10	LCV9	LCV8	LCVCR1
LCV7	LCV6	LCV5	LCV4	LCV3	LCV2	LCV1	LCV0	LCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
LCV15	LCVCR1.7	MSB of the 16-bit code violation count
LCV0	LCVCR2.0	LSB of the 16-bit code violation count

Table 6-1. Line Code Violation (Counting Arrangements
----------------------------------	-----------------------

COUNT EXCESSIVE 0S? (RCR1.7)	B8ZS ENABLED? (CCR2.2)	WHAT IS COUNTED IN THE LCVCRs		
No	No	BPVs		
Yes	No	BPVs + 16 consecutive 0s		
No	Yes	BPVs (B8ZS codewords not counted)		
Yes	Yes	BPVs + 8 consecutive 0s		

6.2 Path Code Violation Count Register (PCVCR)

When the receive side of the DS2151Q is set to operate in the ESF framing mode (CCR2.3 = 1), PCVCR will automatically be set as a 12-bit counter that will record errors in the CRC6 codewords. When set to operate in the D4 framing mode (CCR2.3 = 0), PCVCR will automatically count errors in the Ft framing bit position. Via the RCR2.1 bit, the DS2151Q can be programmed to also report errors in the Fs framing bit position. The PCVCR will be disabled during receive loss of synchronization (RLOS = 1) conditions. See <u>Table 6-2</u> for a detailed description of exactly what errors the PCVCR counts.

PCVCR1: PATH VIOLATION COUNT REGISTER 1 (Address = 25 Hex) PCVCR2: PATH VIOLATION COUNT REGISTER 2 (Address = 26 Hex) (MSB)

(MISD)							(LSD)	
(Note 1)	(Note 1)	(Note 1)	(Note 1)	CRC/FB11	CRC/FB10	CRC/FB9	CRC/FB8	PCVCR1
CRC/FB7	CRC/FB6	CRC/FB5	CRC/FB4	CRC/FB3	CRC/FB2	CRC/FB1	CRC/FB0	PCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC/FB11	PCVCR1.3	MSB of the 12-Bit CRC6 Error or Frame Bit Error
		Count (Note 2)

CRC/FB0 PCVCR2.0 LSB of the 12-Bit CRC6 Error or Frame Bit Error Count (Note 2)

Note 1: The upper nibble of the counter at address 25 is used by the Multiframes Out of Sync Count Register. **Note 2:** PCVCR counts either errors in CRC codewords (in the ESF framing mode; CCR2.3 = 1) or errors in the framing bit position (in the D4 framing mode; CCR2.3 = 0).

Table 6-2. Path Code Violation Counting Arrangements

FRAMING MODE (CCR2.3)	COUNT FS ERRORS? (RCR2.1)	WHAT IS COUNTED IN THE PCVCRs
D4	No	Errors in the Ft pattern
D4	Yes	Errors in both the Ft and Fs patterns
ESF	Don't Care	Errors in the CRC6 codewords

6.3 Multiframes Out of Sync Count Register (MOSCR)

Normally the MOSCR is used to count the number of multiframes that the receive synchronizer is out of sync (RCR2.0 = 1). This number is useful in ESF applications needing to measure the parameters Loss Of Frame Count (LOFC) and ESF Error Events as described in AT&T publication TR54016. When the MOSCR is operated in this mode, it is not disabled during receive loss of synchronization (RLOS = 1) conditions. The MOSCR has alternate operating mode whereby it will count either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When the MOSCR is operated in this mode, it is disabled during receive loss of synchronization (RLOS = 1) conditions. See Table 6-3 for a detailed description of what the MOSCR is capable of counting.

MOSCR1: MULTIFRAMES OUT OF SYNC COUNT REGISTER 1 (Address = 25 Hex)

MOSCR2: MULTIFRAMES OUT OF SYNC COUNT REGISTER 2 (Address = 27 Hex)

(MSB)							(LSB)	
MOS/FB11	MOS/FB10	MOS/FB9	MOS/FB8	(Note 1)	(Note 1)	(Note 1)	(Note 1)	MOSCR1
MOS/FB7	MOS/FB6	MOS/FB5	MOS/FB4	MOS/FB3	MOS/FB2	MOS/FB1	MOS/FB0	MOSCR2
SYMBOLPOSITIONMOS/FB11MOSCR1.7			1.7 M	AME AND SB of the rror Count (12-Bit Mu		Out of Syn	ic or F-Bit
MOS/FB0		MOSCR		SB of the 12 ount (Note 2		frames Out	of Sync or	F-Bit Error

Note 1: The lower nibble of the counter at address 25 is used by the Path Code Violation Count Register. **Note 2:** MOSCR counts either errors in framing bit position (RCR2.0 = 0) or the number of multiframes out of sync (RCR2.0 = 1).

Table 6-3. Multiframes Out of Sync Counting Arrangements

FRAMING MODECOUNT MOS OR F-BIT(CCR2.3)ERRORS? (RCR2.0)		WHAT IS COUNTED IN THE MOSCRs	
D4	MOS	Number of multiframes out of sync	
D4	F-Bit	Errors in the Ft pattern	
ESF	MOS	Number of multiframes out of sync	
ESF	F-Bit	Errors in the FPS pattern	

7 FDL/FS EXTRACTION AND INSERTION

The DS2151Q can extract/insert data from/into the Facility Data Link (FDL) in the ESF framing mode and from/into Fs bit position in the D4 framing mode. Since SLC-96 utilizes the Fs bit position, this capability can also be used in SLC-96 applications. The operation of the receive and transmit sections will be discussed separately.

7.1 Receive Section

In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the Receive FDL register (RFDL). Since the RFDL is 8 bits in length, it will fill up every 2ms (8 times 250µs). The DS2151Q will signal an external microcontroller that the buffer has filled via the SR2.4 bit. If enabled via IMR2.4, the INT2 pin will toggle low indicating that the buffer has filled and needs to be read. The user has 2ms to read this data before it is lost. If the byte in the RFDL matches either of the bytes programmed into the RFDLM1 or RFDLM2 registers, then the SR2.2 bit will be set to a 1 and the INT2 pin will be toggled low if enabled via IMR2.2. This feature allows an external microcontroller to ignore the FDL or Fs pattern until an important event occurs.

The DS2151Q also contains a 0 destuffer that is controlled via the CCR2.0 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (0111110) or an abort signal (1111111). If enabled via CCR2.0, the DS2151Q will automatically look for five 1s in a row, followed by a 0. If it finds such a pattern, it will automatically remove the 0. If the 0 destuffer sees six or more 1s in a row followed by a 0, the 0 is not removed. The CCR2.0 bit should always be set to a 1 when the DS2151Q is extracting the FDL. More on how to use the DS2151Q in FDL and SLC-96 applications is covered in a separate application note. Also, contact the factory for C code software that implements both ANSI T1.403 and AT&T TR54016.

RFDL: RECEIVE FDL REGISTER (Address = 28 Hex)

				•		,		
_	(MSB)							(LSB)
	RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0
-	i							
	SYMBOL		POSITION	NAME	AND DESC	RIPTION		
	RFDL7		RFDL.7	MSB o	f the Received	d FDL Code		
RFDL0		RFDL.0	LSB of	the Received	FDL Code			

The Receive FDL Register (RFDL) reports the incoming Facility Data Link (FDL) or the incoming Fs bits. The LSB is received first.

RFDLM2: RECEIVE FDL MATCH REGISTER 2 (Address = 2A Hex) (MSB) (LSB) RFDL7 RFDL5 RFDL2 RFDL0 RFDL6 RFDL4 RFDL3 RFDL1 SYMBOL POSITION NAME AND DESCRIPTION MSB of the FDL Match Code RFDL7 RFDL.7 **RFDL0** RFDL 0 LSB of the FDL Match Code

RFDLM1: RECEIVE FDL MATCH REGISTER 1 (Address = 29 Hex)

When the byte in the Receive FDL Register matches either of the two Receive FDL Match Registers (RFDLM1/RFDLM2), SR2.2 will be set to a 1 and the $\overline{INT2}$ will go active if enabled via IMR2.2.

7.2 Transmit Section

The transmit section will shift out into the T1 data stream, either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the Transmit FDL register (TFDL). When a new value is written to the TFDL, it will be multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full 8 bits have been shifted out, the DS2151Q will signal the host microcontroller that the buffer is empty and that more data is needed by setting the SR2.3 bit to a 1. The INT2 will also toggle low if enabled via IMR2.3. The user has 2ms to update the TFDL with a new value. If the TFDL is not updated, the old value in the TFDL will be transmitted once again.

The DS2151Q also contains a 0 stuffer that is controlled via the CCR2.4 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.4, the DS2151Q will automatically look for five 1s in a row. If it finds such a pattern, it will automatically insert a 0 after the five 1s. The CCR2.4 bit should always be set to a 1 when the DS2151Q is inserting the FDL. More on how to use the DS2151Q in FDL and SLC-96 applications is covered in a separate application note.

	$\mathbf{H} \mathbf{D} \mathbf{E} \cdot \mathbf{H} \mathbf{A} \mathbf{H} \mathbf{S} \mathbf{H} \mathbf{H} \mathbf{H} \mathbf{D} \mathbf{E} \cdot \mathbf{H} \mathbf{E} \mathbf{S} \mathbf{S} = \mathbf{H} \mathbf{E} \cdot \mathbf{H} \mathbf{E} \mathbf{S} \mathbf{S}$									
	(MSB)			-		-		(LSB)		
	TFDL7	TFDL6	TFDL5	TFDL4	TFDL3	TFDL2	TFDL1	TFDL0		
	SYMBOL		POSITION			DIDTION				
			TFDL 7							
	TFDL7		TTDL./	MSD 0			intica			
TFDL0		TFDL.0	LSB of	the FDL code to be transmitted						
11220										

TEDI · TRANSMIT EDI REGISTER (Address = 7E Hex)

The Transmit FDL Register (TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream in ESF mode. The LSB is transmitted first. In D4 operation the TFDL can be the source of the Fs pattern. In this case a 1ch is written to the TFDL register.

8 SIGNALING OPERATION

The Robbed-Bit signaling bits embedded in the T1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS2151Q. There is a set of 12 registers for the receive side (RS1 to RS12) and 12 registers on the transmit side (TS1 to TS12). The signaling registers are detailed below. The CCR1.5 bit is used to control the robbed signaling bits as they appear at RSER. If CCR1.5 is set to 0, then the robbed signaling bits will appear at RSER in their proper position as they are received. If CCR1.5 is set to a 1, then the robbed signaling bit positions will be forced to a 1 at RSER.

(MSB)							(LSB)	
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	RS1 (60)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	RS2 (61)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	RS3 (62)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	RS4 (63)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	RS5 (64)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	RS6 (65)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	RS7 (66)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	RS8 (67)
A/C(24)	A/C(23)	A/C(22)	A/C(1)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	RS9 (68)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	RS10 (69)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	RS11 (6A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	RS12 (6B)

RS1 TO RS12: RECEIVE SIGNALING REGISTERS (Address = 60 to 6B Hex)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	RS12.7	Signaling Bit D in Channel 24
A(1)	RS1.0	Signaling Bit A in Channel 1

Each Receive Signaling Register (RS1 to RS12) reports the incoming Robbed-Bit signaling from eight DS0 channels. In the ESF framing mode, there can be up to 4 signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only 2 framing bits per channel (A and B). In the D4 framing mode, the DS2151Q will replace the C and D signaling bit positions with the A and B signaling bits from the previous multiframe. Hence, whether the DS2151Q is operated in either framing mode, the user needs only to retrieve the signaling bits every 3ms. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The Receive Signaling Registers are frozen and not updated during a loss of sync condition (SR1.0 = 1). They will contain the most recent signaling information before the "OOF" occurred.

(MSB) (LSB) A(8) A(7) A(6) A(5) A(4) A(3) A(2) A(1) TS1 (70) A(16) A(15) A(14) A(13) A(12) A(11) A(10) A(9) TS2 (71) A(24) A(23) A(22) A(21) A(20) A(19) A(18) TS3 (72) A(17) B(8) B(7) B(6) B(5) B(4) B(3) B(2) B(1) TS4 (73) B(16) B(13) B(12) B(11) B(10) B(9) TS5 (74) B(15) B(14) B(24) B(23) B(22) B(21) B(20) B(19) B(18) B(17) TS6 (75) A/C(8)A/C(2)TS7 (76) A/C(7)A/C(6)A/C(5)A/C(4)A/C(3)A/C(1)TS8 (77) A/C(16) A/C(15) A/C(14) A/C(13) A/C(12) A/C(11) A/C(10) A/C(9) A/C(24) A/C(22) A/C(19) A/C(23) A/C(1)A/C(20) A/C(18) A/C(17)TS9 (78) B/D(8) B/D(4)B/D(3) B/D(1)TS10(79) B/D(7)B/D(6)B/D(5)B/D(2)B/D(16) TS11 (7A) B/D(15)B/D(14)B/D(13)B/D(12)B/D(11)B/D(10)B/D(9)B/D(24)B/D(23) B/D(22) B/D(21) B/D(20) B/D(19) B/D(18) B/D(17) TS12 (7B)

TS1 TO TS12: TRANSMIT SIGNALING F	REGISTERS (Address = 70 to 7B Hex)
(MSR)	(LSB)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	TS12.7	Signaling Bit D in Channel 24

A(1) TS1.0 Signaling Bit A in Channel 1

Each Transmit Signaling Register (TS1 to TS12) contains the Robbed-Bit signaling for eight DS0 channels that will be inserted into the outgoing stream if enabled to do so via TCR1.4. In the ESF framing mode, there can be up to 4 signaling bits per channel (A, B, C, and D). On multiframe boundaries, the DS2151Q will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe Interrupt in Status Register 2 (SR2.6) to know when to update the signaling bits. In the ESF framing mode, the interrupt will come every 3ms and the user has a full 3ms to update the TSRs. In the D4 framing mode, there are only 2 framing bits per channel (A and B). However in the D4 framing mode, the DS2151Q uses the C and D bit positions as the A and B bit positions for the next multiframe. The DS2151Q will load the values in the TSRs into the outgoing shift register every other D4 multiframe.

TRANSMIT TRANSPARENCY AND IDLE REGISTERS 9

There is a set of seven registers in the DS21510 that can be used to custom tailor the data that is to be transmitted onto the T1 line, on a channel-by-channel basis. Each of the 24 T1 channels can be either forced to be transparent or to have a user defined idle code inserted into them. Each of these special registers is defined below.

TTR1/TTR2/TTR3: TRANSMIT TRANSPARENCY REGISTERS (Address = 39) to 3B Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1 (39)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2 (3A)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3 (3B)
		•		•				•

SYMBOL CH24	POSITION TTR3.7	NAME AND DESCRIPTION Transmit Transparency Registers. 0 = this DS0 channel is not transparent
CH1	TTR1.0	1 = this DS0 channel is transparent

Each of the bit positions in the Transmit Transparency Registers (TTR1/TTR2/TTR3) represents a DS0 channel in the outgoing frame. When these bits are set to a 1, the corresponding channel is transparent (or clear). If a DS0 is programmed to be clear, no Robbed-Bit signaling will be inserted nor will the channel have Bit 7 stuffing performed. However, in the D4 framing mode, Bit 2 will be overwritten by a 0 when a Yellow Alarm is transmitted. Also the user has the option to prevent the TTR registers from determining which channels are to have Bit 7 stuffing performed. If the TCR2.0 and TCR1.3 bits are set to 1, then all 24 T1 channels will have Bit 7 stuffing performed on them regardless of how the TTR registers are programmed. In this manner, the TTR registers are only affecting which channels are to have Robbed-Bit signaling inserted into them. See Figure 14-9 for more details.

1101/1102/1103. 100011022 10001200 (Address = 30 to 32 1000								
(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (3C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (3D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (3E)
	SYMBOL POSITION CH24 TIR3.7		NAME AND DESCRIPTION Transmit Idle Registers. 0 = do not insert the Idle Code into this DS0 channel					
C	CH1	TI	R1.0	1 = inser	t the Idle C	ode into th	is channel	

TIR1/TIR2/TIR3' TRANSMIT IDLE REGISTERS (Address = 3C to 3E Hex)

•	TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address = 3F Hex)							
	(MSB)							(LSB)
	TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0
	SYME Tide	-	POSITION TIDR.7		E AND DES of the Idle C			
	TIDI	R0	TIDR.0	LSB o	of the Idle Co	de		

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3) represents a DS0 channel in the outgoing frame. When these bits are set to a 1, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). Robbed-Bit signaling and Bit 7 stuffing will occur over the programmed Idle Code unless the DS0 channel is made transparent by the Transmit Transparency Registers.

10 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3) control the RCHBLK and TCHBLK pins, respectively. The RCHBLK and TCHCLK pins are user-programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in Fractional T1 or ISDN-PRI applications. When the appropriate bits are set to a 1, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing diagrams in Section <u>14</u> for an example.

((Address	s = 6C to	6E Hex)						
	(MSB)							(LSB)	
	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (6C)
	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (6D)
	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (6E)
		1 BOL 124	POSITION RCBR3.7		NAME AND DESCRIPTION Receive Channel Blocking Registers 0 = force the RCHBLK pin to remain low during this channel time				luring this
	Cl	H1	RCB	R1.0	1 = force t	he RCHBL	K pin high	during this	s channel time

RCBR1/RCBR2/RCBR3: RECEIVE CHANNEL BLOCKING REGISTERS

TCBR1/TCBR2/TCBR3: TRANSMIT CHANNEL BLOCKING REGISTERS (Address = 32 to 34 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (32)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (33)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (34)

SYMBOL CH24	POSITION TCBR3.7	NAME AND DESCRIPTION Transmit Channel Blocking Registers. 0 = force the TCHBLK pin to remain low during this channel time
CH1	TCBR1.0	1 = force the TCHBLK pin high during this channel time

11 ELASTIC STORES OPERATION

The DS2151Q has two on-board two-frame (386 bits) elastic stores. These elastic stores have two main purposes. First, they can be used to rate-convert the T1 data stream to 2.048Mbps (or a multiple of 2.048Mbps), which is the E1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the T1 data stream and an asynchronous (i.e., not frequency locked) backplane clock. Both elastic stores contain full controlled slip capability, which is necessary for this second purpose. The receive side elastic store can be enabled via CCR1.2 and the transmit side elastic store is enabled via CCR1.7. The elastic stores can be forced to a known depth via the Elastic Store Reset bit (CCR3.6).

11.1 Receive Side

If the receive side elastic store is enabled (CCR1.2 = 1), then the user must provide either a 1.544MHz (CCR1.3 = 0) or 2.048MHz (CCR1.3 = 1) clock at the SYSCLK pin. The user has the option of either providing a frame sync at the RSYNC pin (RCR2.3 = 1) or having the RSYNC pin provide a pulse on frame boundaries (RCR2.3 = 0). If the user wishes to obtain pulses at the frame boundary, then RCR2.4 must be set to 0 and if the user wishes to have pulses occur at the multiframe boundary, then RCR2.4 must be set to 1. If the user selects to apply a 2.048 MHz clock to the SYSCLK pin, then the data output at RSER will be forced to all 1s every fourth channel and the F-bit will be deleted. Hence, channels 1, 5, 9, 13, 17, 21, 25, and 29 (time slots 0, 4, 8, 12, 16, 20, 24, and 28) will be forced to a 1.

Also, in 2.048MHz applications, the RCHBLK output will be forced high during the same channels as the RSER pin. See Section <u>16</u> for more details. This is useful in T1 to CEPT (E1) conversion applications. If the 386-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (193 bits) will be repeated at RSER and the SR1.4 and RIR1.3 bits will be set to a 1. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR1.4 bits will be set to a 1.

11.2 Transmit Side

The transmit side elastic store can only be used if the receive side elastic store is enabled. The operation of the transmit elastic store is very similar to the receive side; both have controlled slip operation and both can operate with either a 1.544MHz or a 2.048MHz SYSCLK. When the transmit elastic store is enabled, both the SYSCLK and RSYNC signals are shared by both the elastic stores. Hence, they will have the same backplane PCM frame and data structure. Controlled slips in the transmit elastic store are reported in the RIR2.5 bit and the direction of the slip is reported in the RIR2.3 and RIR2.4 bits.

11.3 Minimum Delay Synchronous SYSCLK Mode

In applications where the DS2151Q is connected to backplanes that are frequency-locked to the recovered T1 clock (i.e., the RCLK output), the full two-frame depth of the onboard elastic stores is really not needed. In fact, in some delay-sensitive applications the normal two-frame depth may be excessive. If the CCR3.7 bit is set to 1, then the receive elastic store (and also the transmit elastic store if it is enabled) will be forced to a maximum depth of 32 bits instead of the normal 386 bits. In this mode, the SYSCLK must be frequency-locked to RCLK and all of the slip contention logic in the DS2151Q is disabled (since slips cannot occur). Also, since the buffer depth is no longer two frames deep, the DS2151Q must be set up to source either a frame or multiframe pulse at the RSYNC pin. On power-up after the SYSCLK has locked to the RCLK signal, the Elastic Store Reset bit (CCR3.6) should be toggled from a 0 to a 1 to ensure proper operation.

12 RECEIVE MARK REGISTERS

The DS2151Q can replace the incoming data on a channel-by-channel basis with either an idle code (7F hex) or the digital milliwatt code, which is an 8-byte repeating pattern that represents a 1kHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). The RCR2.7 bit will determine which code is used. Each bit in the RMRs, represents a particular channel. If a bit is set to a 1, then the receive data in that channel will be replaced with one of the two codes. If a bit is set to 0, no replacement occurs.

RMR1/RMR2/RMR3: RECEIVE MARK REGISTERS (Address=2D to 2F Hex)

(MSB)						-	(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1 (2D)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2 (2E)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3 (2F)
	MBOL XH24		TION R3.7	Receive C		RIPTION ocking Regi eceive data		with this
	CH1	RM	R1.0	with either		de or the di		his channel att code

13 LINE INTERFACE FUNCTIONS

The line interface function in the DS2151Q contains three sections: the receiver, which handles clock and data recovery; the transmitter, which waveshapes and drives the T1 line; and the jitter attenuator. Each of these three sections is controlled by the Line Interface Control Register (LICR), which is described below.

LICR: LII (MSB)		RFACE C	ONTRO	OL REGIS	TER (Add	ress = 7	C Hex) (LSB)	
LB2	LB1	LB0	EGL	JAS	JABDS	DJA	TPD	LICR
	1 BOL B2	POSIT Licf		Line Build	D DESCRI -Out Select Table 13-2.		s the transm	itter build
LI	81	LICF	R.6		-Out Select Table 13-2.	Bit 1. Sets	s the transm	iitter build
LI	80	LICF	R.5		-Out Select <u>Table 13-2</u> .	Bit 0. Sets	s the transm	itter build
EC	GL	LICF	8.4	Receive Eq 0 = -36dB 1 = -30dB	lualizer Gaii	n Limit.		
JA	AS	LICF	8.3	0 = place th	nuator Selec le jitter attenu le jitter attenu	uator on the		
JAE	BDS	LICF	8.2	0 = 128 bits	nuator Buffe s (use for delay	-		,
D.	JA	LICF	R .1	0 = jitter att	ter Attenuat enuator enab tenuator disal	oled		
TI	Ъ	LICF	R.0	0 = normal	Power Down transmitter o down the tra pins	peration	d tri-states tl	ne TTIP

13.1 Receive Clock and Data Recovery

The DS2151Q contains a digital clock recovery system. See Figure 1-1 and Figure 13-1 for more details. The DS2151Q couples to the receive T1 twisted pair via a 1:1 transformer. See Table 13-3 for transformer details. The DS2151Q automatically adjusts to the T1 signal being received at the RTIP and RRING pins and can handle T1 lines from 0 feet to over 6000 feet in length. The crystal attached at the XTAL1 and XTAL2 pins is multiplied by 4 via an internal PLL and fed to the clock recovery system. The clock recovery system uses both edges of the clock from the PLL circuit to form a 32 times oversampler which is used to recover the clock and data. This oversampling technique offers outstanding jitter tolerance (see Figure 13-2). The EGL bit in the Line Interface Control Register is used to limit the sensitivity of the receiver in the DS2151Q. For most CPE applications, a receiver sensitivity of -30dB is wholly sufficient and hence the EGL bit should be set to 1. In some applications, more sensitivity than -30dB may be required and the DS2151Q will allow the receiver to go as low as -36dB if the EGL bit is set to 0, the DS2151Q will be more susceptible to crosstalk and its jitter tolerance will suffer.

Normally, the clock that is output at the RCLK pin is the recovered clock from the T1 AMI waveform presented at the RTIP and RRING inputs. When no AMI signal is present at RTIP and RRING, a Receive Carrier Loss (RCL) condition will occur and the RCLK can be sourced from either the ACLKI pin or from the crystal attached to the XTAL1 and XTAL2 pins. The DS2151Q will sense the ACLKI pin to determine if a clock is present. If no clock is applied to the ACLKI pin, then it should be tied to RVSS to prevent the device from falsely sensing a clock. See <u>Table 13-1</u>. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLK output can exhibit short high cycles of the clock. This is due to the highly oversampled digital clock recovery circuitry. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to being close to 50% duty cycle. See the receive AC timing characteristics in Section <u>16</u> for more details.

ACLKI PRESENT?	RECEIVE SIDE JITTER ATTENUATOR	TRANSMIT SIDE JITTER ATTENUATOR
Yes	ACLKI via the jitter attenuator	ACLKI
No	Centered crystal	TCLK via the jitter attenuator

Table 13-1. Source of RCLK Upon RCL

13.2 Transmit Waveshaping and Line Driving

The DS2151Q uses a set of laser-trimmed delay lines along with a precision Digital-to-Analog Converter (DAC) to create the waveforms that are transmitted onto the T1 line. The waveforms created by the DS2151Q meet the latest ANSI, AT&T, and CCITT specifications. See Figure 13-3. The user will select which waveform is to be generated by properly programming the L0 to L2 bits in the Line Interface Control Register (LICR).

L2	L1	LO	LINE BUILD-OUT	APPLICATION
0	0	0	0 to 133 feet/0dB	DSX-1/CSU
0	0	1	133 to 266 feet	DSX-1
0	1	0	266 to 399 feet	DSX-1
0	1	1	399 to 533 feet	DSX-1
1	0	0	533 to 655 feet	DSX-1
1	0	1	-7.5dB	CSU
1	1	0	-15dB	CSU
1	1	1	-22.5dB	CSU

Table 13-2. LBO Select in LICR

Due to the nature of the design of the transmitter in the DS2151Q, very little jitter (less than $0.005UI_{P-P}$ broadband from 10Hz to 100kHz) is added to the jitter present on TCLK. Also, the waveforms that they create are independent of the duty cycle of TCLK. The transmitter in the DS2151Q couples to the T1 transmit twisted pair via a 1:1.15 or 1:1.36 step-up transformer as shown in Figure 13-1. For the devices to create the proper waveforms, the transformer used must meet the specifications listed in Table 13-3.

 Table 13-3. Transformer Specifications

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio	1:1 (receive) and 1:1.15 or 1:1.36 (transmit) ±5%
Primary Inductance	600μH minimum
Leakage Inductance	1.0μH maximum
Intertwining Capacitance	40pF maximum
DC Resistance	1.2Ω maximum

13.3 Jitter Attenuator

The DS2151Q contains an on-board jitter attenuator that can be set to a depth of either 32 or 128 bits via the JABDS bit in the Line Interface Control Register (LICR). The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay sensitive applications. The characteristics of the attenuation are shown in Figure 13-4. The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit in the LICR. Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA-bit in the LICR. In order for the jitter attenuator to operate properly, a crystal with the specifications listed in Table 13-4 below must be connected to the XTAL1 and XTAL2 pins. The jitter attenuator divides the clock provided by the 6.176MHz crystal at the XTAL1 and XTAL2 pins to create an output clock that contains very little jitter. On-board circuitry will pull the crystal (by switching in or out load capacitance) to keep it long-term averaged to the same frequency as the incoming T1 signal. If the incoming jitter exceeds either 120UI_{P-P} (buffer depth is 128 bits) or 28UI_{P-P} (buffer depth is 32 bits), then the DS2151Q will divide the attached crystal by either 3.5 or 4.5, it also sets the Jitter Attenuator Limit Trip (JALT) bit in the Receive Information Register 2 (RIR2.2).

PARAMETER	SPECIFICATION
Parallel Resonant Frequency	6.176MHz
Mode	Fundamental
Load Capacitance	18pF to 20pF (18.5pF nominal)
Tolerance	±50ppm
Pullability	$C_L = 10 \text{pF}$, delta frequency = +175 ppm to
	+250ppm
	$C_L = 45 \text{pF}$, delta frequency = -175 ppm to -250 ppm
Effective Series Resistance	40Ω maximum
Crystal Cut	AT

Figure 13-1. External Analog Connections

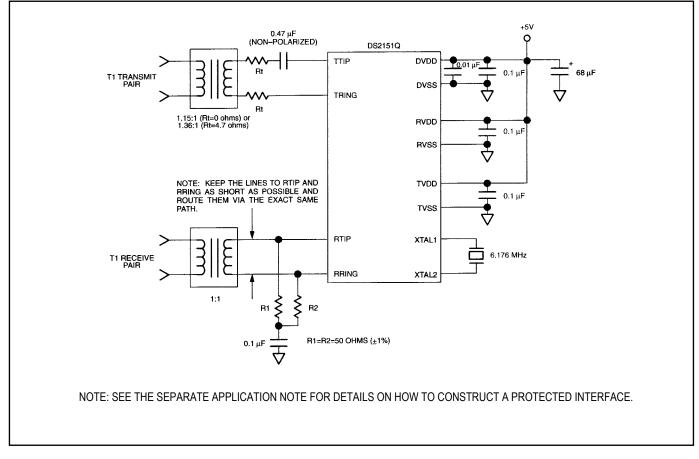
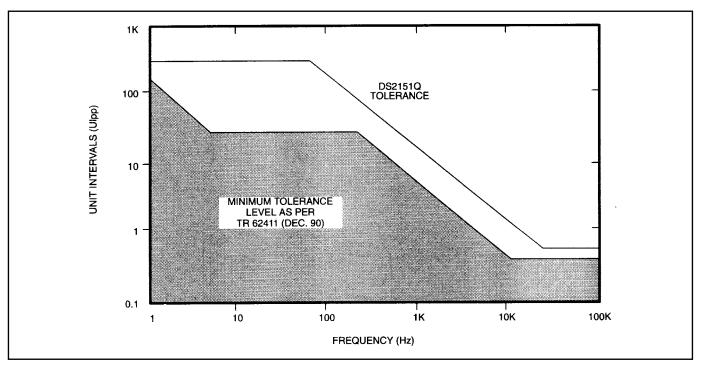


Figure 13-2. Jitter Tolerance



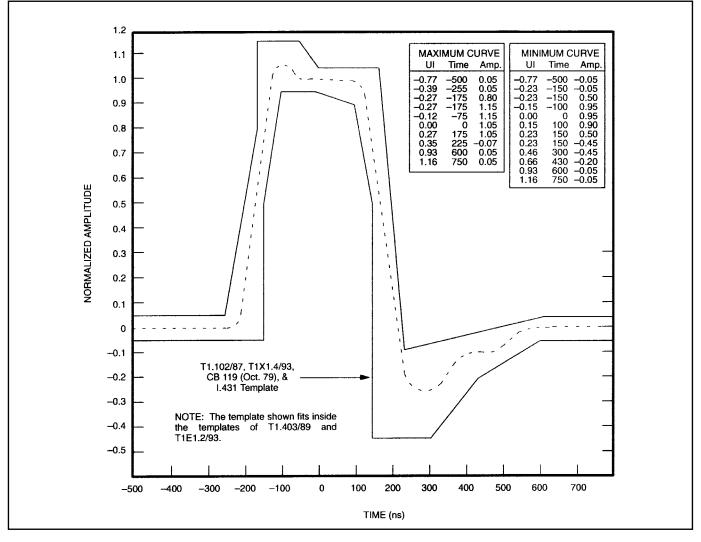
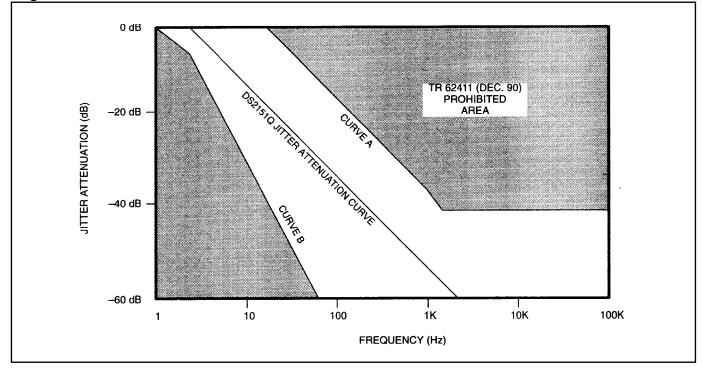


Figure 13-3. Transmit Waveform Template

Figure 13-4. Jitter Attenuation



14 TIMING DIAGRAMS



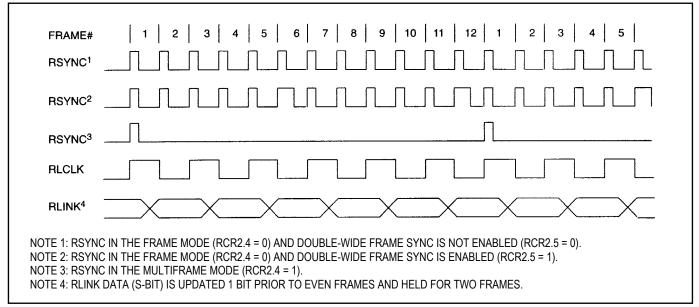
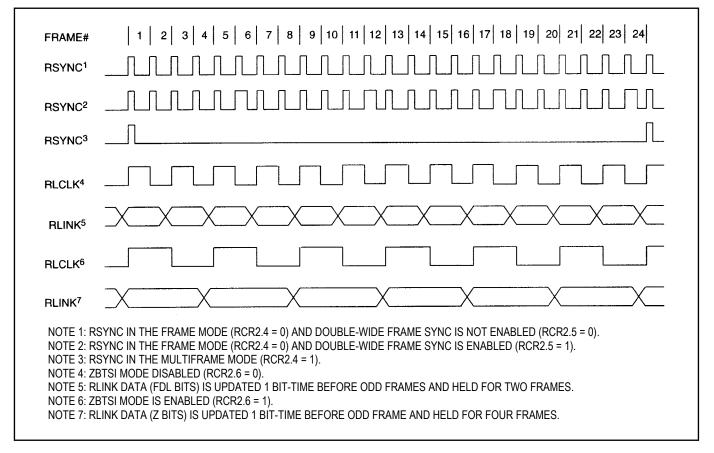


Figure 14-2. Receive Side ESF Timing



	INEL 23 C	CHANNEL 24 CH	ANNEL 1
RSYNC			
RCHCLK		· ·	
RCHBLK ¹			
RLCLK			
RLINK		X	

Figure 14-4. 1.544MHz Boundary Timing with Elastic Store(s) Enabled

RSYNC ¹	 		 ,
RSYNC ²	 	/ \	
RCHCLK	 		
RCHBLK ³			

RCHCLK	SYSCLKI L. CHANI TSER/ RSER1 X.X.	NEL 31 CH	ANNEL 32 CHANNEL 1
	RSYNC ²		
	RSYNC ³		
	RCHCLK		
	RCHBLK ⁴	<u></u>	

Figure 14-5. 2.048MHz Boundary Timing with Elastic Store(s) Enabled

Figure 14-6. Transmit Side D4 Timing

TSYNC ²					
TSYNC ³]		 		
TLCLK					
TLINK ⁴		+	 · · · · · · · · · · · · · · · · · · ·	 	

Figure 14-7. Transmit Side ESF Timing

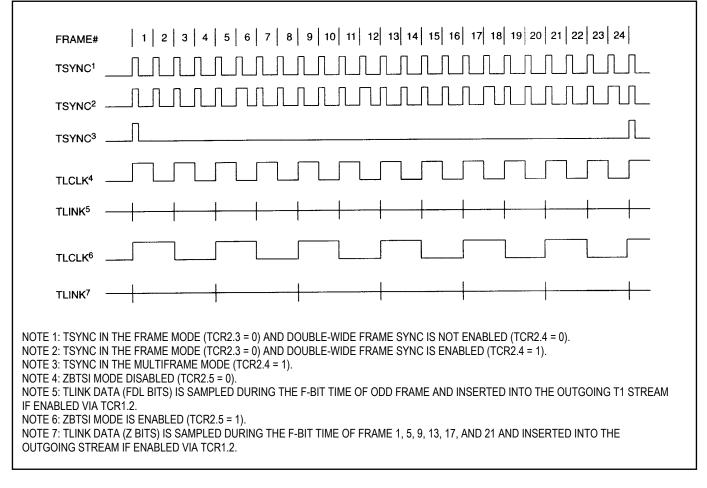
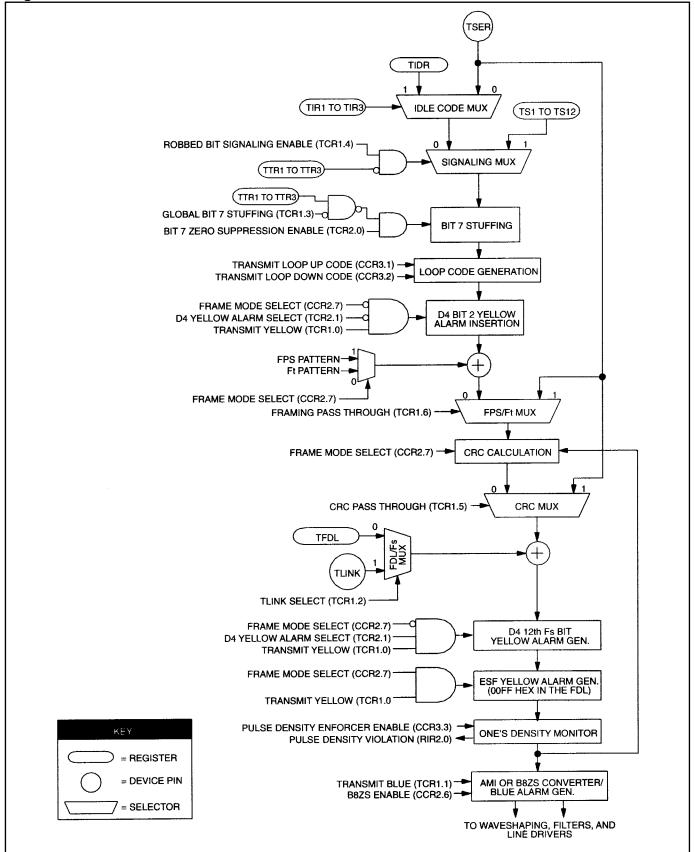


Figure 14-8. Transmit Side Boundary Timing with Elastic Store(s) Disabled
TCLK TLTL CHANNEL 1 TSER ¹ (LSB) F XMSB(XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
TSYNC ¹
TSYNC ²
TCHBLK ³
TLCLK
TLINK Don't Care
NOTE 1: TSYNC IS IN THE INPUT MODE (TCR2.2 = 0). NOTE 2: TSYNC IS IN THE OUTPUT MODE (TCR2.2 = 1). NOTE 3: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 1. NOTE 4: SEE Figure 14-4 AND Figure 14-5 FOR DETAILS ON TIMING WITH THE TRANSMIT SIDE ELASTIC STORE ENABLED.

Figure 14-9. Transmit Data Flow



15 DC CHARACTERISTICS ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-1.0V to $+7.0V$
Operating Temperature Range	
Commercial	$0^{\circ}C \text{ to } +70^{\circ}C$
Industrial	40°C to +85°C
Storage Temperature	55°C to +125°C
Soldering Temperature	

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Table 15-1. Recommended DC Characteristics

 $(T_A = 0^{\circ}C \text{ to } +70^{\circ}C \text{ for } DS2151Q, T_A = -40^{\circ}C \text{ to } +85^{\circ}C \text{ for } DS2151QN.)$

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Logic 1	V _{IH}	2.0		$V_{DD} + 0.3$	V	
Logic 0	V _{IL}	-0.3		+0.8	V	
Supply	V _{DD}	4.75		5.25	V	1

Table 15-2. Capacitance

 $(T_{A} = +25^{\circ}C)$

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Input Capacitance	C _{IN}		5		pF	
Output Capacitance	C _{OUT}		7		pF	

Table 15-3. DC Characteristics

 $(V_{DD} = 5V \pm 5\%, T_A = 0^{\circ}C \text{ to } +70^{\circ}C \text{ for } DS2151Q, T_A = -40^{\circ}C \text{ to } +85^{\circ}C \text{ for } DS2151QN.)$

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Supply Current at 5V	I _{DD}		65		mA	2
Input Leakage	I _{IL}	-1.0		+1.0	μΑ	3
Output Leakage	I _{LO}			1.0	μA	4
Output Current (2.4V)	I _{OH}	-1.0			mA	
Output Current (0.4V)	I _{OL}	+4.0			mA	

NOTES:

- 1) Applies to RVDD, TVDD, and DVDD.
- 2) TCLK = 1.544MHz.
- 3) $0V < V_{IN} < V_{DD}$.
- 4) Applies to $\overline{\text{INT1}}$ and $\overline{\text{INT1}}$ when tri-stated.

16 AC CHARACTERISTICS

Table 16-1. AC Characteristics—Parallel Port

 $(V_{DD} = 5V \pm 5\%, T_A = 0^{\circ}C \text{ to } +70^{\circ}C \text{ for } DS2151Q, T_A = -40^{\circ}C \text{ to } +85^{\circ}C \text{ for } DS2151QN.)$ (See Figure 16-1, Figure 16-2, and Figure 16-3.)

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Cycle Time	t _{CYC}	250			ns	
Pulse Width, DS Low or \overline{RD} High	PW_{EL}	150			ns	
Pulse Width, DS High or \overline{RD} Low	$\mathrm{PW}_{\mathrm{EH}}$	100			ns	
Input Rise/Fall Times	t_R, t_F			30	ns	
R/\overline{W} Hold Time	t _{RWH}	10			ns	
R/\overline{W} Setup Time before DS High	t _{RWS}	50			ns	
$\frac{\overline{CS} \text{ Setup Time before DS,}}{\overline{WR} \text{ or } \overline{RD} \text{ Active}}$	t _{CS}	20			ns	
$\overline{\mathrm{CS}}$ Hold Time	t _{CH}	0			ns	
Read Data Hold Time	t _{DHR}	10		50	ns	
Write Data Hold Time	t _{DHW}	0			ns	
Muxed Address Valid to AS or ALE Fall	t _{ASL}	20			ns	
Muxed Address Hold Time	t _{AHL}	10			ns	
Delay Time DS, \overline{WR} or \overline{RD} to AS or ALE Rise	t_{ASD}	25			ns	
Pulse Width AS or ALE High	PWASH	40			ns	
Delay Time, AS or ALE to DS, \overline{WR} or \overline{RD}	t _{ASED}	20			ns	
Output Data Delay Time from DS or \overline{RD}	t _{DDR}	20		100	ns	
Data Setup Time	t _{DSW}	80			ns	

Figure 16-1. Intel Bus Read AC Timing

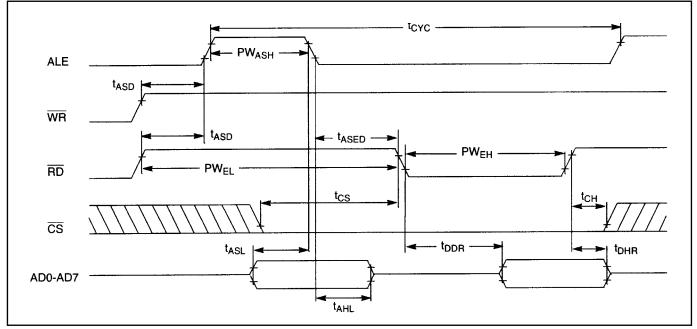


Figure 16-2. Intel Bus Write AC Timing

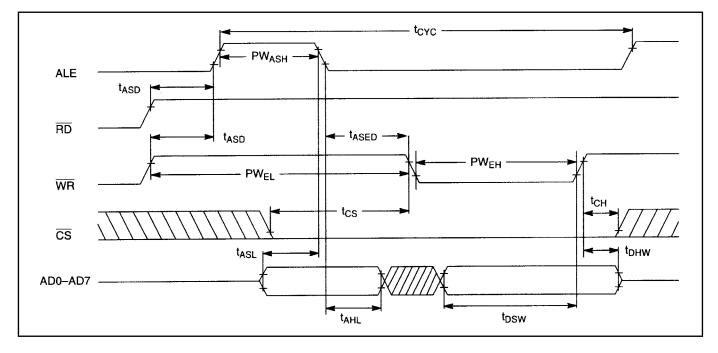


Figure 16-3. Motorola Bus AC Timing

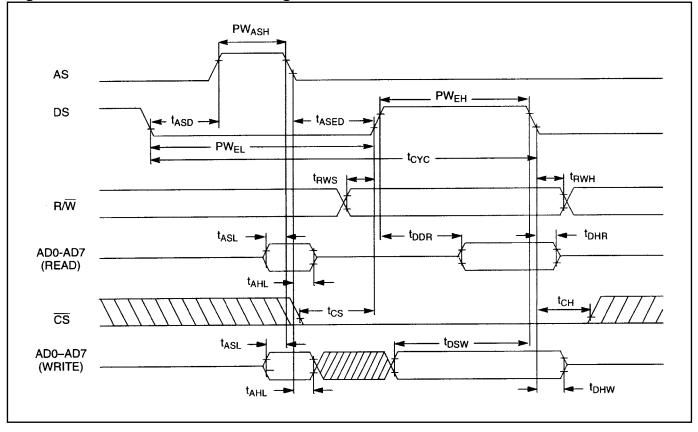


Table 16-2. AC Characteristics—Receive Side

 $(V_{DD} = 5V \pm 5\%, T_A = 0^{\circ}C \text{ to } +70^{\circ}C \text{ for } DS2151Q, T_A = -40^{\circ}C \text{ to } +85^{\circ}C \text{ for } DS2151QN.)$ (See Figure 16-4.)

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
ACLKI/RCLK Period	t _{CP}		648		ns	
RCLK Pulse Width	t _{CH}	230	324		ns	1
KCLK Fulse widdi	t _{CL}	230	324		ns	1
RCLK Pulse Width	t _{CH}	115			ns	2
	t _{CL}	115			ns	
SYSCLK Period	t _{SP}		648		ns	3
STSELKTENOG	t _{SP}		488		ns	4
SYSCLK Pulse Width	t _{SH}	75			ns	
	t _{SL}	75				
RSYNC Setup to SYSCLK Falling	t_{SU}	25		t _{SH} -5	ns	
RSYNC Pulse Width	t _{PW}	50			ns	
SYSCLK Rise/Fall Times	t _R , t _F			25	ns	
Delay RCLK or SYSCLK to RSER Valid	t _{DD}	10		80	ns	
Delay RCLK or SYSCLK to RCHCLK	t _{D1}	10		90	ns	
Delay RCLK or SYSCLK to RCHBLK	t _{D2}	10		90	ns	
Delay RCLK or SYSCLK to RSYNC	t _{D3}	10		80	ns	
Delay RCLK to RLCLK	t _{D4}	10		80	ns	
Delay RCLK to RLINK Valid	t _{D5}	10		110	ns	

NOTES:

1) Jitter attenuator enabled in the receive side path.

2) Jitter attenuator disabled or enabled in the transmit path.

3) SYSCLK = 1.544MHz.

4) SYSCLK = 2.048MHz.



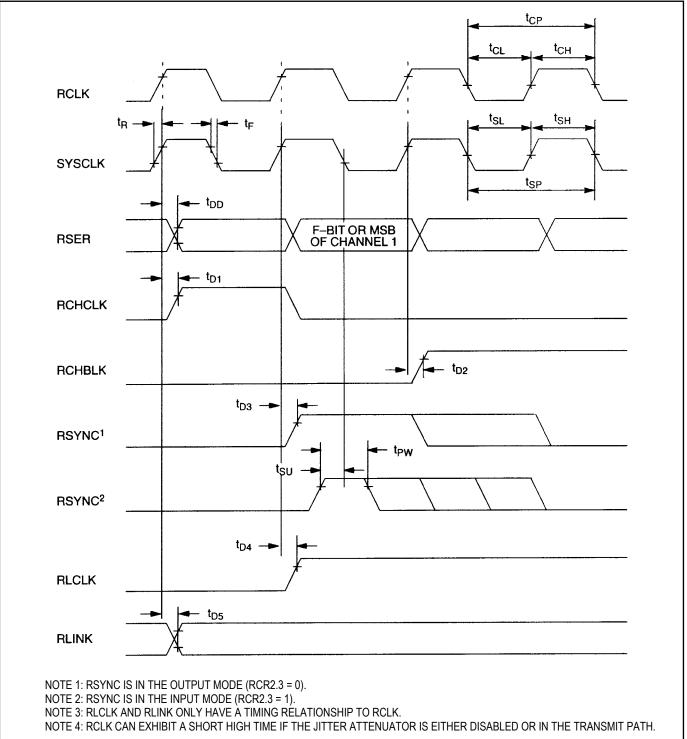


Table 16-3. AC Characteristics—Transmit Side

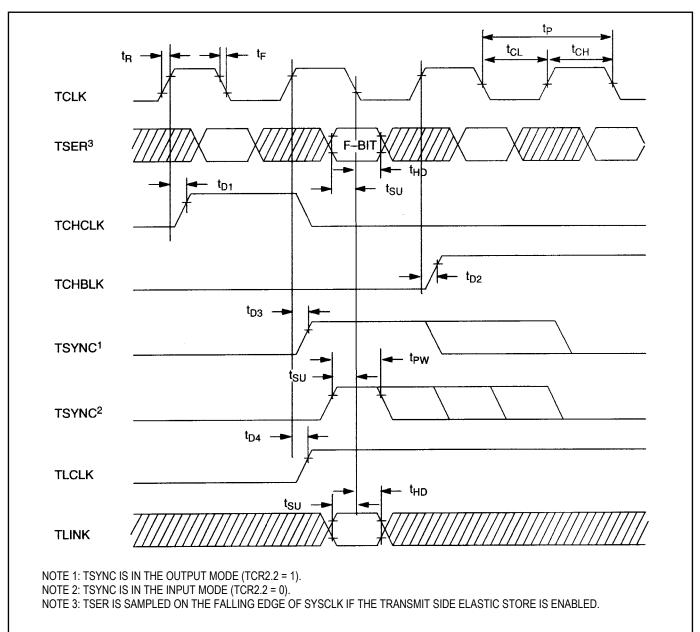
 $(V_{DD} = 5V \pm 5\%, T_A = 0^{\circ}C \text{ to } +70^{\circ}C \text{ for } DS2151Q, T_A = -40^{\circ}C \text{ to } +85^{\circ}C \text{ for } DS2151QN.)$ (See <u>Figure 16-5</u>.)

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
TCLK Period	t _P		648		ns	
TCLK Pulse Width	t _{CH}	75			ns	
ICLK Fulse widdi	t _{CL}	75			ns	
TSER and TLINK Set up to TCLK Falling	t_{SU}	25			ns	1
TSER and TLINK Hold from TCLK Falling	t _{HD}	25			ns	1
TSYNC Set up to TCLK Falling	t_{SU}	25		t _{CH} -5		
TSYNC Pulse Width	t _{PW}	50				
TCLK Rise/Fall Times	t_R, t_F			25	ns	
Delay TCLK to TCHCLK	t _{D1}	10		60	ns	
Delay TCLK to TCHBLK	t _{D2}	10		70	ns	
Delay TCLK to TSYNC	t _{D3}	10		60	ns	
Delay TCLK to TLCLK	t _{D4}	10		60	ns	

NOTES:

1) If the transmit side elastic store is enabled, then TSER is sampled on the falling edge of SYSCLK and the parameters t_{SU} and t_{HD} still apply.

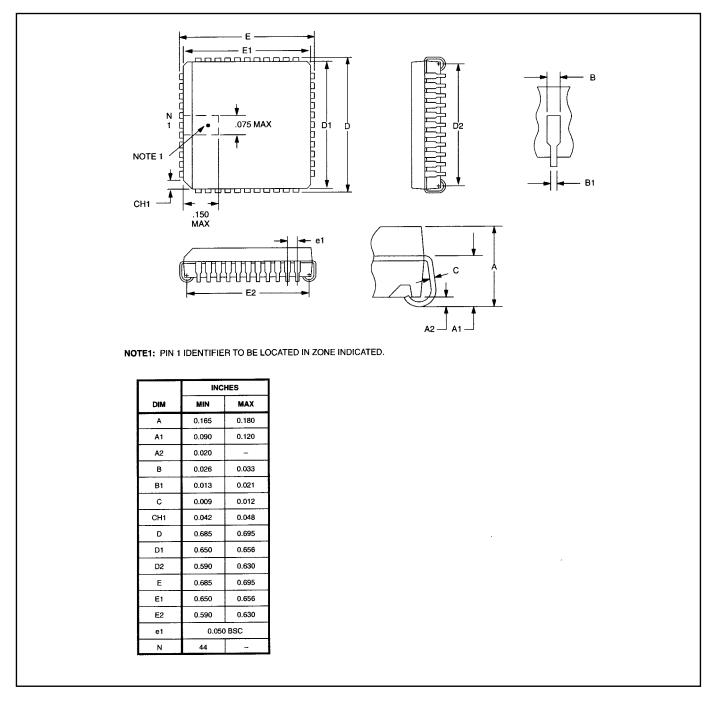




17 PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information.)

17.1 44-Pin PLCC (<u>56-G4003-001</u>)



60 of 60

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