FSL Logo

PRODUCT BULLETIN
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ISSUE DATE:	01-Jul-2016
NOTIFICATION:	17128
TITLE:	Kinetis KV4x Update RM, DS and Errata to Reflect Changes and Added KMS
EFFECTIVE DATE:	02-Jul-2016

DEVICE(S)

MPN
MKV42F128VLH16
MKV42F128VLL16
MKV42F256VLH16
MKV42F256VLL16
MKV42F64VLH16
MKV44F128VLH16
MKV44F128VLL16
MKV44F256VLH16
MKV44F256VLL16
MKV44F64VLH16
MKV46F128VLH16
MKV46F128VLL16
MKV46F256VLH16
MKV46F256VLL16

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AFFECTED CHANGE CATEGORIES

- DATASHEET
- ERRATA
- REFERENCE MANUAL

DESCRIPTION OF CHANGE

REFERENCE MANUAL
Kinetis KV4x: 168MHz Cortex-M4 up to 256KB Flash (100pin) at http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/kinetis-cortex-m-mcus/v-series-real-time-control-m0-plus-m4-m7/kinetis-kv4x-168-mhz-high-performance-motor-power-conversion-microcontrollers-mcus-based-on-arm-cortex-m4-core:KV4x?fpsp=1&tab=Documentation_Tab

Updates Include:

General changes throughout document

Added information about Kinetis Motor Suite (KMS)
Updated chapter Flash Memory Module (FTFA)
Added chapter for Kinetis Motor Suite Configuration

PORT changes

In Pin Control Register (PCRn), added additional details to Interrupt Configuration field (IRQC) description

Kinetis Flash Bootloader changes

In "Start-up Process" section, replaced "The flashloader initializes the .data and .bss sections" with "The flash loader's temporary working area in
RAM is initialized".

Crossbar switch module changes

General operation: Removed paragraph beginning with "A master is given control of the targeted slave..." and the following list, beginning with "A
higher priority master has...".
Fixed-priority operation: Removed the note referring to MGPCR from the "How the Crossbar Switch grants control of a slave

port to a master" table.
Initialization/application information: Changed wording of sentence about arbitration scheme.

AIPS module changes

Corrected misspellings in Memory map/register definition.

FTFA Changes

Add ACCERR check for sector size larger than segment size in Error Handling table for RD1XA and ERSXA commands
Modify FSEC[MEEN] register field description
Modify Flash Commands by Mode table entries for Read 1s All Blocks and Erase All Blocks commands
Add Read 1s All Execute-only Segments and Erase All Execute-only Segments commands; modify list of Margin Read Commands
Add reference to AN5112 in Flash Access Protection
Add ACCERR check for mode/security in Error Handling table for Verify Backdoor Access Key and Read 1s All Blocks commands
Change column heading from Byte to Offset Address in configuration field description table
Add suggestion to bit poll FSTAT[CCIF] for command completion in Generic flash command write sequence flowchart
Clarify that ACCERR and FPVIOL flags must be clear before ERSSUSP can be set in Suspending an Erase Flash Sector Operation
Remove erroneous reference to the flash configuration field in Suspending an Erase Flash Sector Operation
Specify minimum time of 4.3 msec between request to resume and suspend erase in Resuming an Erase Flash Sector Operation
Add list of specific commands impacted by Flash Access Protection
Clarify write-ability of ACCERR and FPVIOL while CCIF is set in FSTAT register description
In FTFA_FACSN[NUMSG], changed bit field value from 0x40 to

eDMA module changes

DMA_TCDn_CSR[ACTIVE]: Changed access from RW to RO.
ES : Removed bullet about uncorrectable TCD SRAM errors.
eDMA initialization : In bullet beginning with "Enable any hardware service requests..." replaced "ERQH and ERQL registers" with "ERQ register."

EWM changes

Substantial changes throughout the chapter which include:
Changed the term "service" to "refresh" throughout the chapter to better explain the EWM refresh mechanism.
Updated the block diagram.
Updated the table "EWM refresh mechanism"
Editorial changes

Chip-specific CMP changes

Added section CMP voltage references

PDB changes

In "Pulse-Out's" section, added a Pulse-Out generation diagram.
Updated LDOK with a slightly more clear description.
Added a note about SC[LDOK] to MOD, IDLY, PODLY, DACINTx, CHDLY0 and CHDLY1 registers.
Deleted "PDB signal description" section.

FlexCAN module changes

In CTRL2, removed the reserved fields at CTRL2 positions 0 and 1 with RW access and consolidated them with the reserved field at 2-10 with RO
access.
In the introduction section of Memory map/register definition, added text explaining that there is a separate message buffer memory map section,
and added a link to that section.

SPI module changes

In Section, Modified SPI Transfer Format (MTFE = 1, CPHA = 1), added note, "When using MTFE=1...POP operation."
In PCS0/SS—Peripheral Chip Select/Slave Select - Added note.
Deleted note from SOUT—Serial Output.
Clarified Memory Map/Register Definition introductory text by changing second sentence:
From: "Write access to the POPR and RXFRn also results in a transfer error."
To: "Any Write access to the POPR and RXFRn also results in a transfer error."
Updated PUSHR description.
In section, PCS0/SS—Peripheral Chip Select/Slave Select : Updated note.

I2C changes

Added a note for I2C_FLT[STOPF].

DATA SHEETS:

Kinetis KV4x: 168MHz Cortex-M4 up to 256KB Flash (100pin) at http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/kinetis-cortex-m-mcus/v-series-real-time-control-m0-plus-m4-m7/kinetis-kv4x-168-mhz-high-performance-motor-power-conversion-microcontrollers-mcus-based-on-arm-cortex-m4-core:KV4x?fpsp=1&tab=Documentation_Tab

Updates Include:

ENOB parameter value update

Changed Effective Number Of Bits (ENOB) value from 9.5 to 9.1

KMS information added

Changed occurrences of Freescale to NXP
In the features list, added a section for "Kinetis Motor Suite"
Added section Kinetis Motor Suite (KMS)

ERRATA:

Mask Set Errata for Mask 1N72K-Errata at http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/kinetis-cortex-m-mcus/v-series-real-time-control-m0-plus-m4-m7/kinetis-kv4x-168-mhz-high-performance-motor-power-conversion-microcontrollers-mcus-based-on-arm-cortex-m4-core:KV4x?fpsp=1&tab=Documentation_Tab

Errata Application Summary for KV4x MCU

Errata#	0N72K	1N72K	Errata title
e8210	Yes	No	ADC: ADC can't enter lp mode by setting ROSB when JTAG is active.
e9432	Yes	Yes	eFlexPWM: Fractional delay block may powerup with an output fo 1 instead of 0
e8341	Yes	Yes	FlexCAN: Entering Freeze Mode or Low Power Mode from Normal Mode can cause the FlexCAN module to stop operating
e10373	Yes	Yes	FTFA: Flas Access Control do not protect the flash from read access correctly
e10384	Yes	Yes	FTFA: For MCUs prior to work week 29 of 2016, FSEC[MEEN] = 10 disable Mass Erase only when the MCU us secured
e8162	Yes	No	I2C:IAAS and IICIF bits in the I2C Status Register are not set properly under certain condition after low power recovery
e9601	No	Yes	I2C: IICIFbit in the I2C Status Register isn't set properly under certain conditions after low power recovery
e9953	Yes	Yes	Possible incorrect readings on second ADC conversion when sampling two ADC channels and fist channel input voltage <VREFL or >VREFH
e9682	Yes	Yes	SPI: inconsistent loading of shift register data into the receive FIFO following an overflow event
e8209	Yes	No	SOC: High current in VLL3 and VLL2 Mode

Note - Workarounds available for all errata
e8210, e8209 e8162 is fixed removed.
e9953 explain possible incorrect readings on second ADC conversion when sampling two ADC channels and first channel input voltage < VREFL or > VREFH
e9432 explain Fractional delay block in eFlexPWM may power up with an output of 1 instead of 0
e10373 explain Flash Access Control do not protect the flash from read access correctly
e10384 explain FSEC[MEEN] = 10 disables Mass Erase only when the MCU is secured

REASON FOR CHANGE

Kinetis Motor Suite (KMS) is being introduced for KV4x MCUs.

Kinetis Motor Suite (KMS) is a bundled hardware and software solution aimed at enabling rapid configuration of motor drive systems and accelerating application development. KMS includes firmware targeting the Kinetis V (KV) series of microcontrollers (MCUs) and an intuitive PC-based graphical user interface. It supports field oriented velocity and position control of three phase permanent magnet and brushless DC motors.

Updates to the Reference Manual, Data Sheet and Errata reports were made to support the KMS introduction. Additional documentation errors were fixed and recently discovered errata have been added. Additional flash features were added to MCU's with Flash Access Controls features in order to provide increased protection the flash contents from accidental erasure.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

The flash operation is 100% backward compatible with existing use of the flash protection. The flash features added increases protection against accidental mass erasure of the flash contents. Errata number ERR010384 describe the basic features and implementation date. There are possible software implications to customers if the new features are to be used.

The errata describe existing conditions identified on current production devices.

Kinetis Motor Suite(KMS) features and enabled part numbers have been added to data sheet and reference manual documents.

NOTE:
THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a Support Case. Be aware that after you select this link to enter your request, you must choose the topic "Product Change Notification" once on the Salesforce page.

For sample inquiries - please go to www.nxp.com

QUALIFICATION STATUS: N/A

QUALIFICATION PLAN:

N/A

RELIABILITY DATA SUMMARY:

N/A

ELECTRICAL CHARACTERISTIC SUMMARY:

N/A

CHANGED PART IDENTIFICATION:

N/A

ATTACHMENT(S):
External attachment(s) FOR this notification can be viewed AT:
17128_KV4XP100M168DS_Rev3_Revision_History.pdf
17128_KV4XP100M168RM_Rev4_Release-Notes.pdf
17128_Errata__Kinetis_V_1N72K_02JUN16.pdf
