

NTB5411N, NTP5411N

Power MOSFET 80 Amps, 60 Volts N-Channel D²PAK, TO-220

Features

- Low $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- These are Pb-Free Devices

Applications

- LED Lighting and LED Backlight Drivers
- DC-DC Converters
- DC Motor Drivers
- Power Supplies Secondary Side Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	60	V	
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V	
Gate-to-Source Voltage – Nonrepetitive ($T_P < 10 \mu\text{s}$)	V_{GS}	± 30	V	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	I_D 80	A
		$T_C = 100^\circ\text{C}$	61	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D 166	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM} 185	A	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	75	A	
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50 V_{dc}, V_{GS} = 10 V_{dc}, I_{L(pk)} = 75 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$)	E_{AS}	280	mJ	
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	T_L	260	$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State (Note 1)	$R_{\theta JC}$	0.9	$^\circ\text{C}/\text{W}$
	$R_{\theta JA}$	43	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).

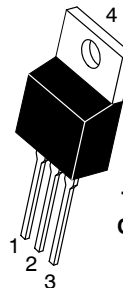
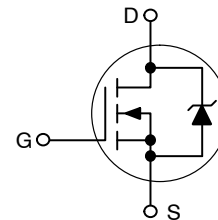


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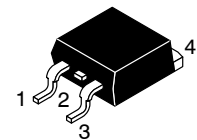
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$ (Note 1)
60 V	10 m Ω @ 10 V	80 A

N-Channel

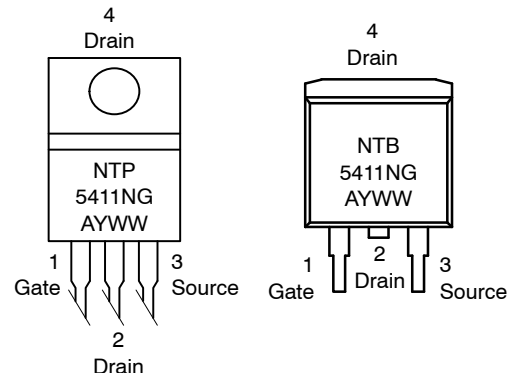


TO-220AB
CASE 221A
STYLE 5



D²PAK
CASE 418B
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



G = Pb-Free Device
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTB5411N, NTP5411N

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{DS} = 0 V, I _D = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			54.2		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V V _{DS} = 60 V	T _J = 25°C		10	μA
			T _J = 150°C		100	
Gate-Body Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 μA	2.0	3.2	4.0	V
Negative Threshold Temperature Coefficient	V _{GS(th)} /T _J			6.6		mV/°C
Drain-to-Source On Voltage	V _{DS(on)}	V _{GS} = 10 V, I _D = 80 A		0.71	0.92	V
		V _{GS} = 10 V, I _D = 40 A, 150°C		0.65		
Static Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 40 A		8.4	10	mΩ
Forward Transconductance	g _{FS}	V _{GS} = 15 V, I _D = 40 A		70		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		3365	4500	pF
Output Capacitance	C _{oss}			615		
Transfer Capacitance	C _{rss}			230		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 48 V, I _D = 80 A		92	130	nC
Threshold Gate Charge	Q _{G(TH)}			4.1		
Gate-to-Source Charge	Q _{GS}			19		
Gate-to-Drain Charge	Q _{GD}			43		

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 48 V, I _D = 80 A, R _G = 9.1 Ω		22		ns
Rise Time	t _r			122		
Turn-Off Delay Time	t _{d(off)}			116		
Fall Time	t _f			113		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V I _S = 37.5 A	T _J = 25°C		0.91	1.1	V _{dc}
			T _J = 150°C		0.8		
Reverse Recovery Time	t _{rr}	I _S = 37.5 A _{dc} , V _{GS} = 0 V _{dc} , di _S /dt = 100 A/μs		62		ns	
Charge Time	t _a			43			
Discharge Time	t _b			19			
Reverse Recovery Stored Charge	Q _{RR}			0.15			μC

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

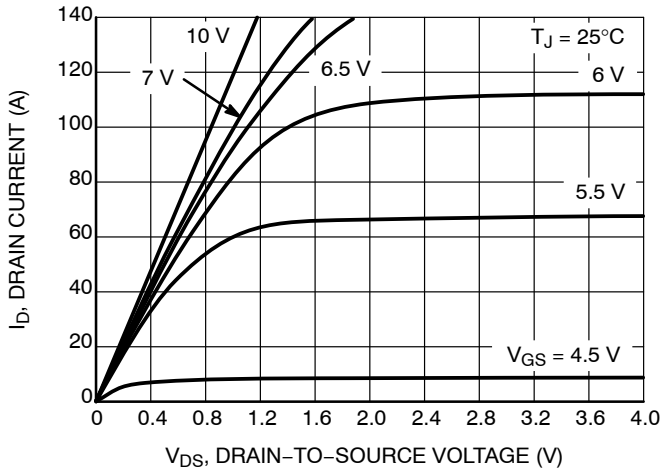


Figure 1. On-Region Characteristics

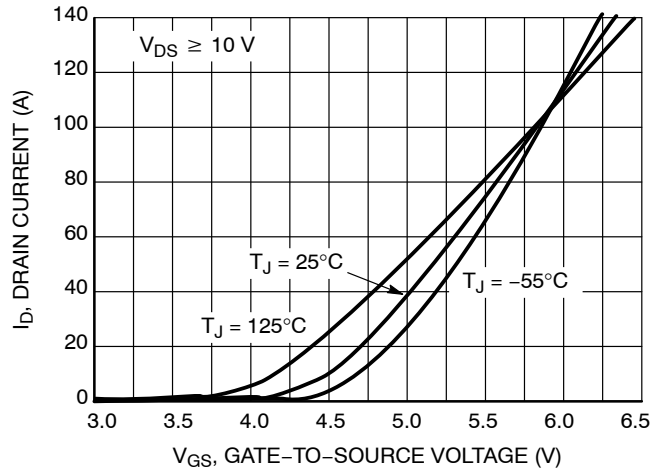


Figure 2. Transfer Characteristics

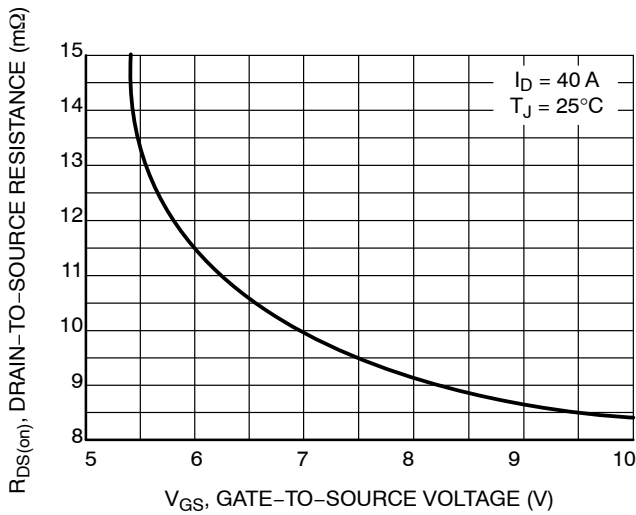


Figure 3. On-Resistance vs. Gate-to-Source Voltage

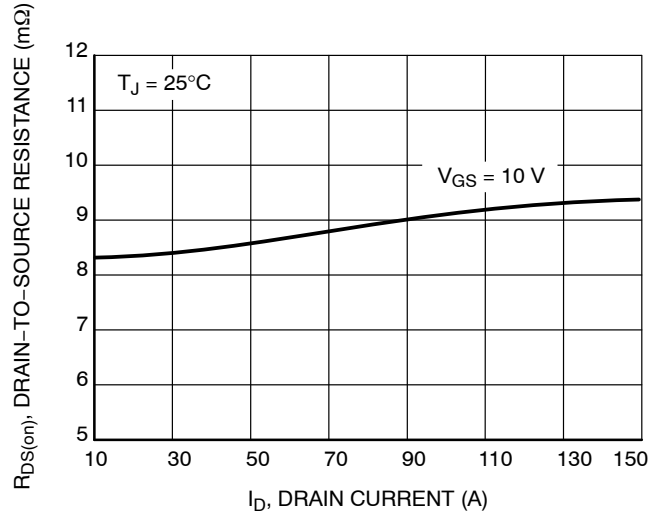


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

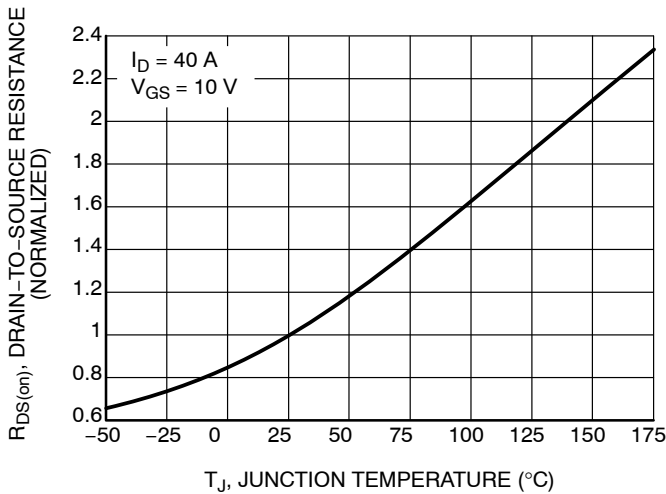


Figure 5. On-Resistance Variation with Temperature

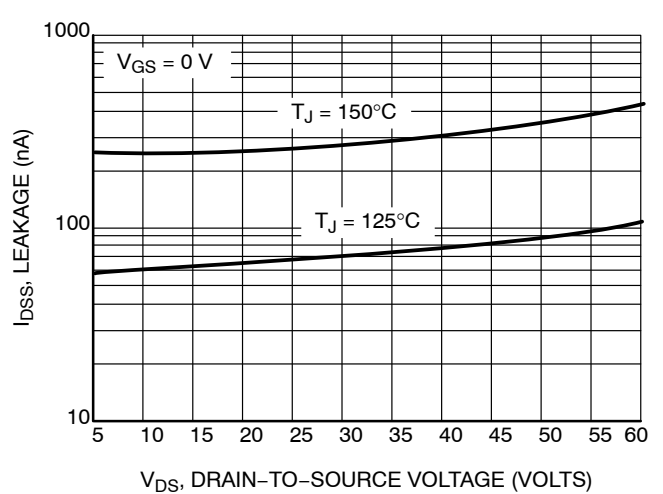


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL PERFORMANCE CURVES

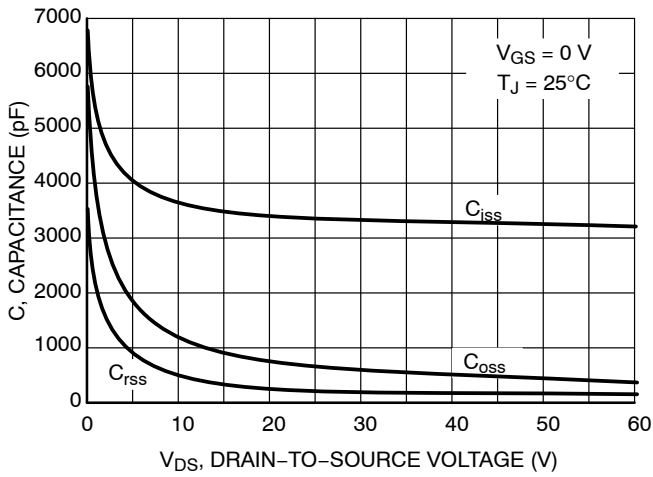


Figure 7. Capacitance Variation

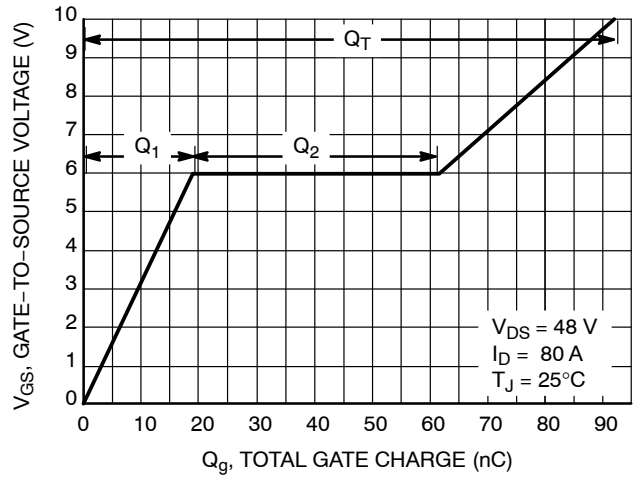


Figure 8. Gate-to-Source Voltage vs. Total Charge

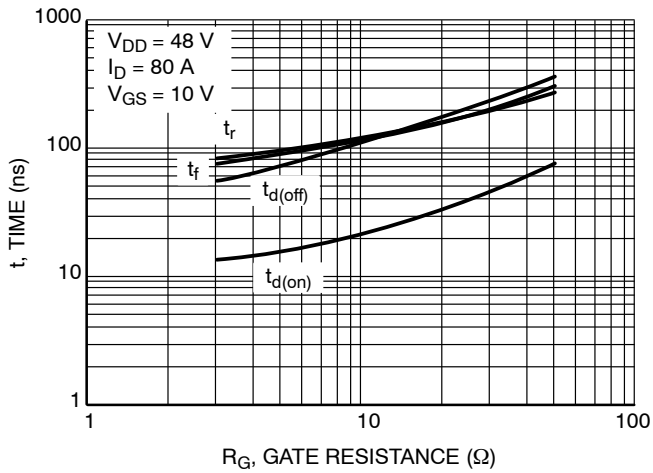


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

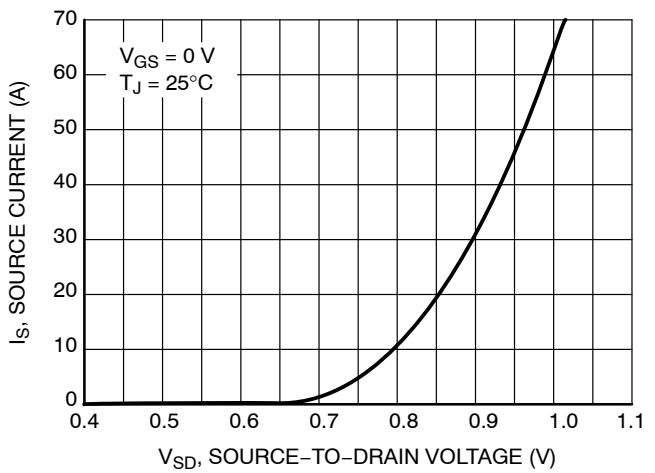


Figure 10. Diode Forward Voltage vs. Current

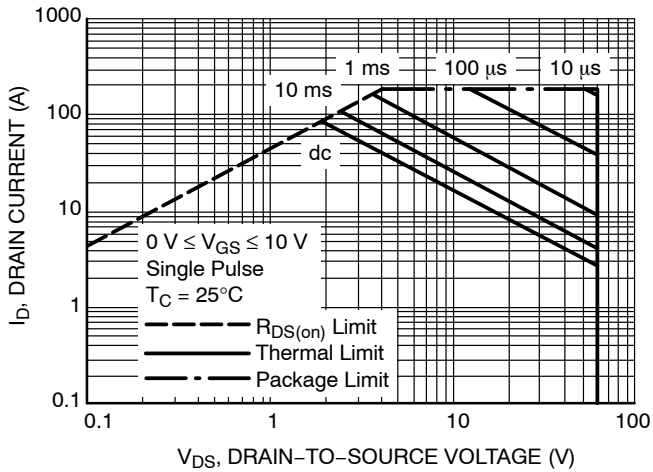


Figure 11. Maximum Rated Forward Biased Safe Operating Area

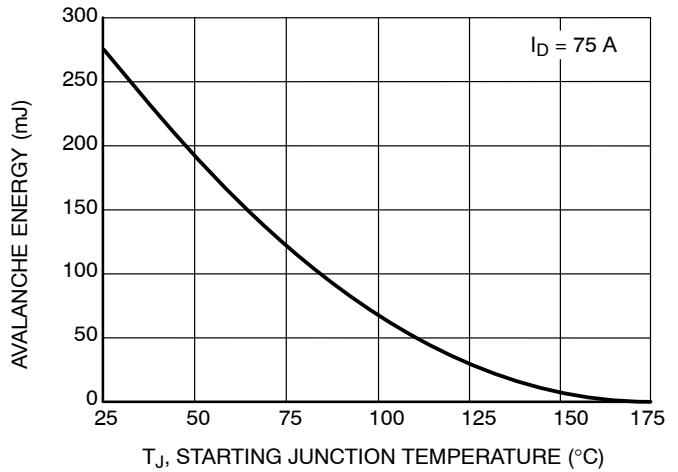


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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TYPICAL PERFORMANCE CURVES

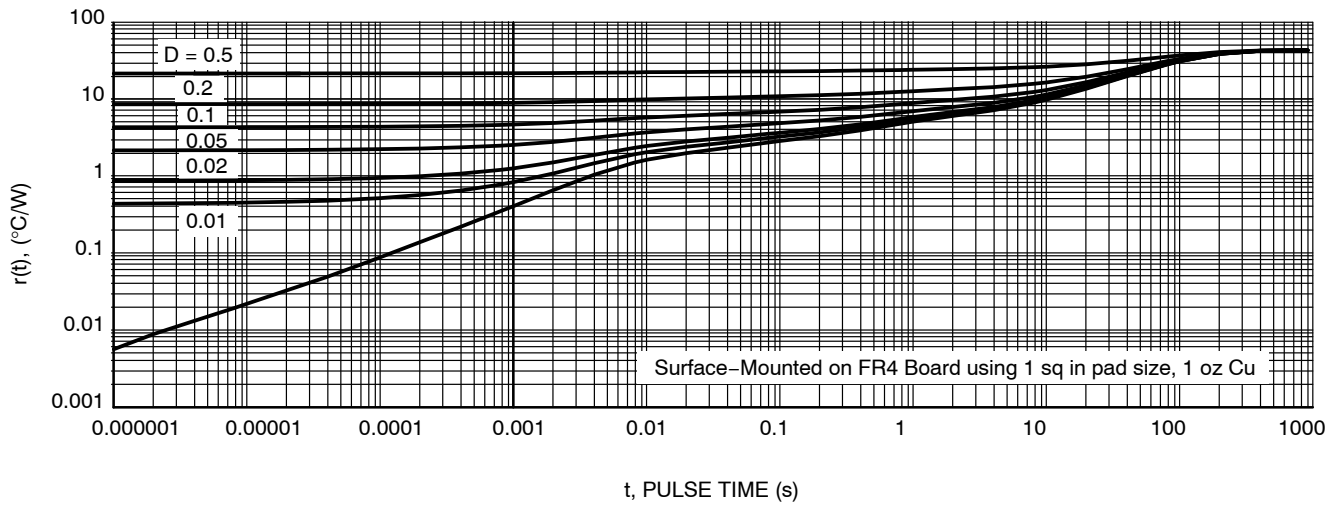


Figure 13. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping [†]
NTP5411NG	TO-220AB (Pb-Free)	50 Units / Rail
NTB5411NT4G	D ² PAK (Pb-Free)	800 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

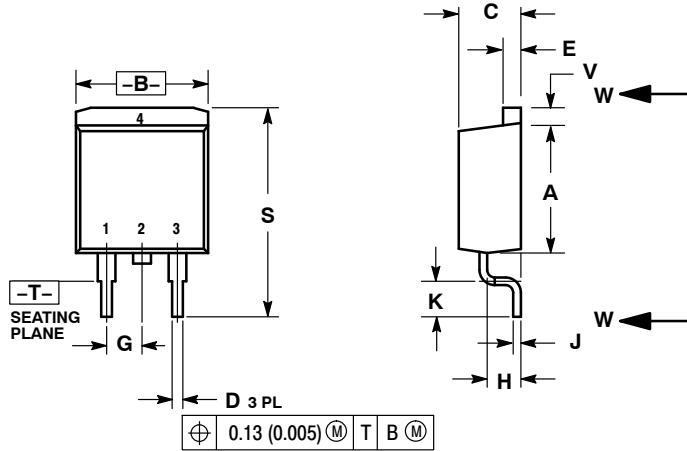
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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

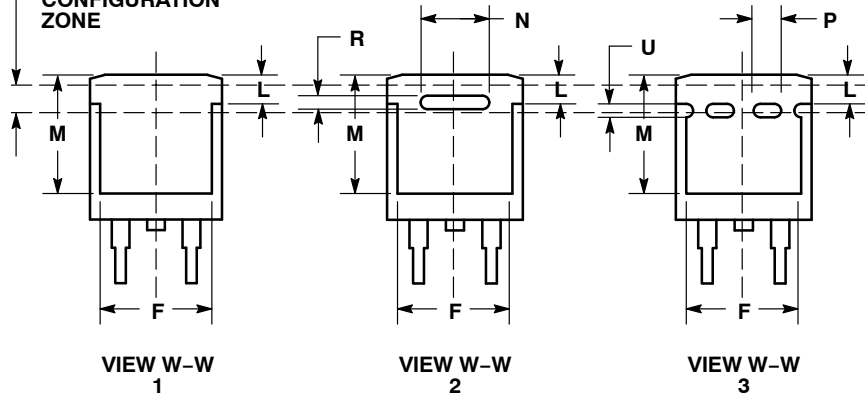


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE CONFIGURATION ZONE



- | | | | | | |
|--|---|---|--|---|--|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE | STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE |
|--|---|---|--|---|--|

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

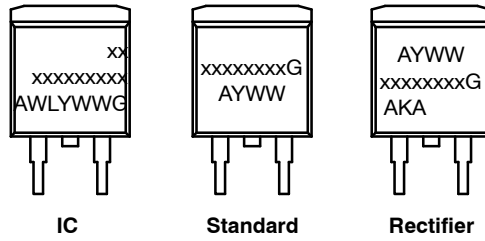
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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

**GENERIC
MARKING DIAGRAM***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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