LC03-6R2

ESD Protection Diode
Low Capacitance Surface Mount ESD Protection for High-Speed Data Interfaces

The LC03−6 surge protection is designed to protect equipment attached to high speed communication lines from ESD, EFT, and lighting.

Features

- SO−8 Package
- Peak Power − 2000 Watts 8 x 20 μS
- ITU K.20 I_{PP} = 40 A (5/310 μs)
- Bellcore 1089 (Intra−Building) 100 A (2/10 μs)
- ESD Rating:
  IEC 61000−4−2 (ESD) 15 kV (air) 8 kV (contact)
  IEC 61000−4−4 (EFT) 40 A (5/50 ns)
  IEC 61000−4−5 (lighting) 95 A (8/20 μs)
- UL Flammability Rating of 94 V−0
- Pb−Free Package is Available

Typical Applications

- High Speed Communication Line Protection

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Power Dissipation 8 x 20 μS @ T_A = 25°C (Note 1)	P_{pk}	2000	W
Peak Pulse Current (8 x 20 μS Waveform)	I_{PP}	100	A
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum 10 Seconds Duration	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Non−repetitive current pulse 8 x 20 μS exponential decay waveform

ON Semiconductor®

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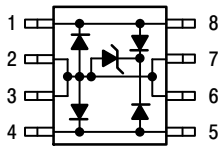
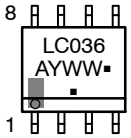
SO−8 LOW CAPACITANCE VOLTAGE SUPPRESSOR 2 kW PEAK POWER 6 VOLTS

PIN CONFIGURATION AND SCHEMATIC



SOIC−8
CASE 751
PLASTIC

MARKING DIAGRAM



LC036 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
LC03−6R2	SO−8	2500/Tape & Reel
LC03−6R2G	SO−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage @ I_t = 1.0 mA	V_{BR}	6.8	–	–	V
Reverse Leakage Current @ V_{RWN} = 5.0 V	I_R	N/A	–	20	μA
Maximum Clamping Voltage @ I_{PP} = 50 A, 8 x 20 μS	V_C	N/A	–	15	V
Maximum Clamping Voltage @ I_{PP} = 100 A, 8 x 20 μS	V_C	N/A	–	20	V
Between I/O Pins and Ground @ V_R = 0 V, 1.0 MHz	Capacitance	–	16	25	pF
Between I/O Pins @ V_R = 0 Volts, 1.0 MHz	Capacitance	–	8.0	12	pF

TYPICAL CHARACTERISTICS

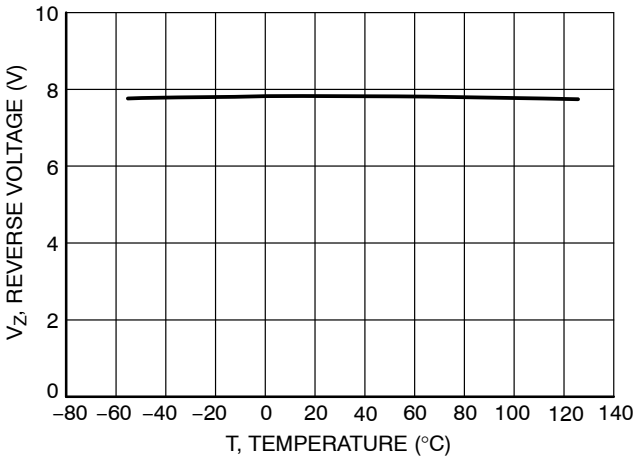


Figure 1. Reverse Voltage versus Temperature

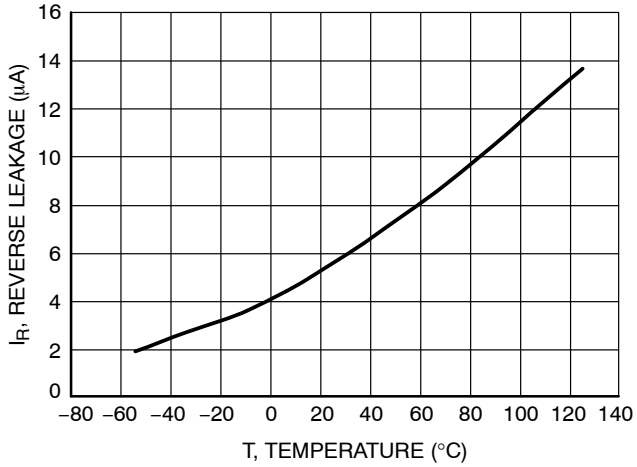


Figure 2. Reverse Leakage versus Temperature

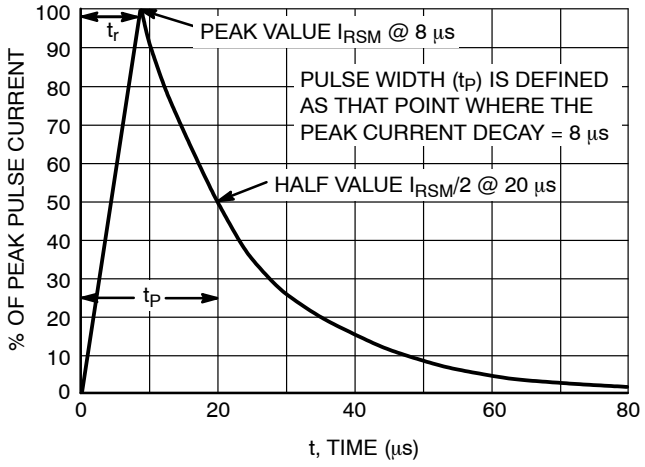


Figure 3. 8 x 20 μs Pulse Waveform

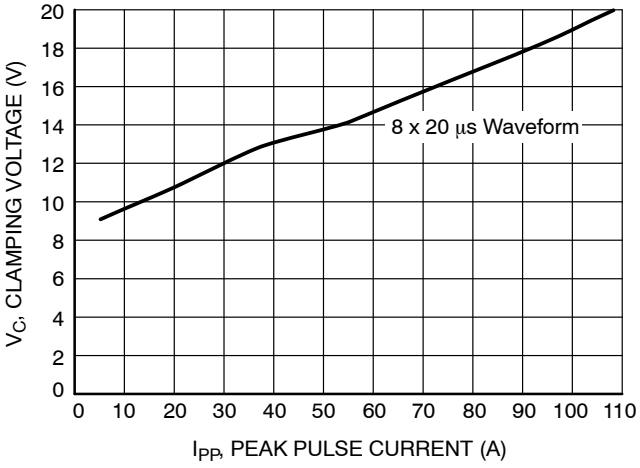


Figure 4. Clamping Voltage versus Peak Pulse Current

APPLICATIONS INFORMATION

The LC03−6 ON Semiconductor's device is a surge protection Diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to transient overvoltage conditions caused by lightning, electrostatic discharge (ESD), and electrical fast transients (EFT). Because of its relative low capacitance (<25 pf), it can be used in high speed I/O data lines such as USB 1.1 ports.

The integrated design of the LC03−6 device offers high surge rating, low capacitance steering diodes, and a surge protection diode integrated in a single package (SO−8). In addition, this device offers compliance to Bellcore 1089 requirements (intra−building).

LC03−6 Device's Configurations Options

Protection of Two High−speed I/O Data Lines

The LC03−6 device is able to protect two high speed data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. Depending in the application's requirements, the LC03−6 device can be configured for protection in either differential mode (Line−to−Line) or common mode (Line−to−ground). The Figure 5 shows the connection for Differential mode (Line−to−Line) and Common mode (Line−to−Ground) protection. The inputs and outputs of the I/O data lines are connected at terminals 1 to 8, and 4 to 5 while the terminals 2, 3, 6 and 7 are connected to ground; for better performance, it is recommended to minimize parasitic inductances by using ground planes and minimizing the PCB trace lengths for the ground return connections.

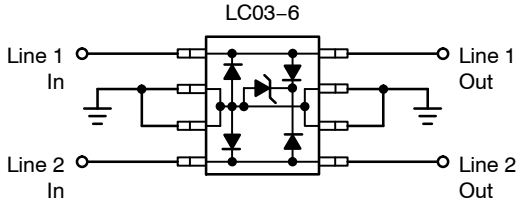


Figure 5. Configuration for Differential and Common Mode Protection

If differential protection is required by some particular applications, then the configuration for differential protection is made as shown in the Figure 6:

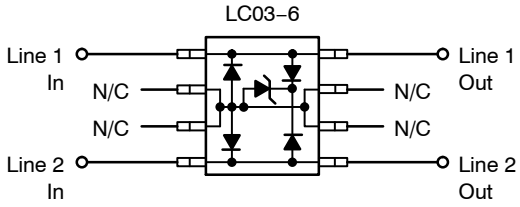


Figure 6. Configuration for Differential Protection (Line−to−Line)

T1/E1 Linecard Protection (Intra−Building)

The Figure 7 shows a typical schematic for a T1/E1 line card protection circuit. The LC03−6 device is connected between Tip and Ring on the transmit and receive line pairs. it provides protection to metallic and common mode lightning surges per Bellcore 1089 intra−building (For further information, see Bellcore 1089 standard). A metallic voltage is defined as a difference of potential between the T and R terminals of a telecommunications pair. Currents caused by lightning, in the absence of protector operation and with balanced terminal equipment and telecommunications loop, cause Tip and Ring conductors to attain the same potential hence do not produce metallic transients. Common mode surges are suppressed by the isolation of the transformer.

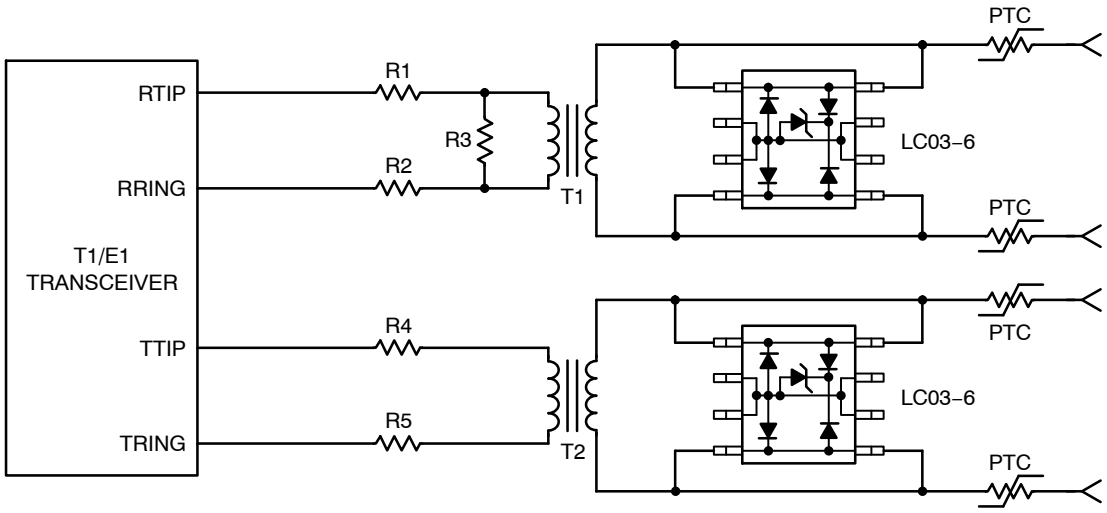


Figure 7. Typical T1 Line Card Protection

ESD Protection in USB 1.1 Port Applications

As we know, a USB port is composed of four lines. The lines D+ and D− are used for bi−directional data transmission, and the remaining two lines are reserved for bus voltage and ground. Since USB is a hot plugging and unplugging system, all its four lines have the risk to receive ESD conditions in the real field of the application.

Typical ESD protection techniques are commonly formed by the combination of different discrete semiconductor products which make this technique obsolete and non−efficient because the interconnections of the discrete devices increase the parasitic inductance effects during a transient condition which reduces significantly the performance of the ESD protection circuit. The LC03−6 device provides a unique surge protection Diode array designed to protect two I/O data lines (single USB port) against damage due to ESD conditions or transient voltage conditions. Because of its low capacitance, it can be used in high speed I/O data lines such as USB 1.1 components. In addition to its low capacitance characteristics, the LC03−6 device from ON Semiconductor complies with the most common industrial standards for ESD, EFT and surge protection: IEC61000−4−2, IEC61000−4−4, IEC61000−4−5.

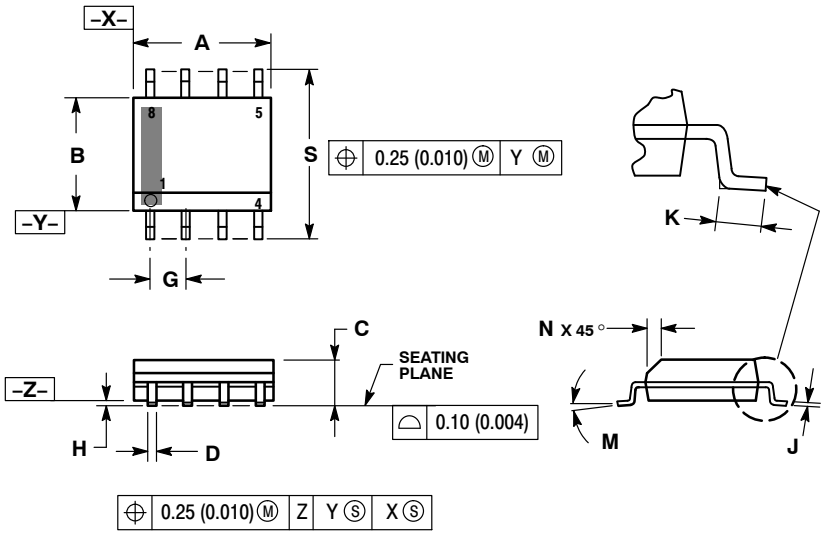
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

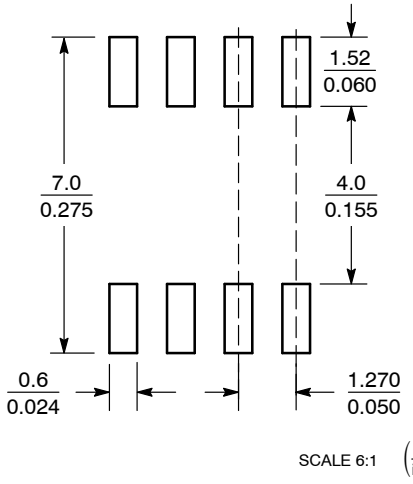
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

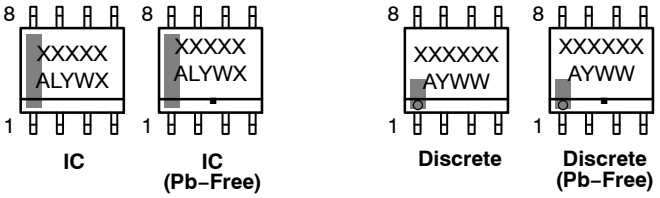
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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