Complete, 12-Bit, 45 MHz CCD Signal Processor

Data Sheet

ADDI7100

FEATURES

Pin-compatible upgrade for the AD9945
45 MHz correlated double sampler (CDS) with variable gain
6 dB to 42 dB, 10-bit variable gain amplifier (VGA)
Low noise optical black clamp circuit
Preblanking function
12-bit, 45 MHz ADC
No missing codes guaranteed
3-wire serial digital interface
3 V single-supply operation
Space-saving, 32-lead, 5 mm × 5 mm LFCSP

APPLICATIONS

Digital still cameras
Digital video camcorders
PC cameras
Portable CCD imaging devices
CCTV cameras

GENERAL DESCRIPTION

The ADDI7100 is a complete analog signal processor for charge-coupled device (CCD) applications. It features a 45 MHz, single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays. The signal chain for the ADDI7100 consists of a correlated double sampler (CDS), a digitally controlled variable gain amplifier (VGA), a black level clamp, and a 12-bit ADC.

The internal registers are programmed through a 3-wire serial digital interface. Programmable features include gain adjustment, black level adjustment, input clock polarity, and power-down modes. The ADDI7100 operates from a single 3 V power supply, typically dissipates 125 mW, and is packaged in a space-saving, 32-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM

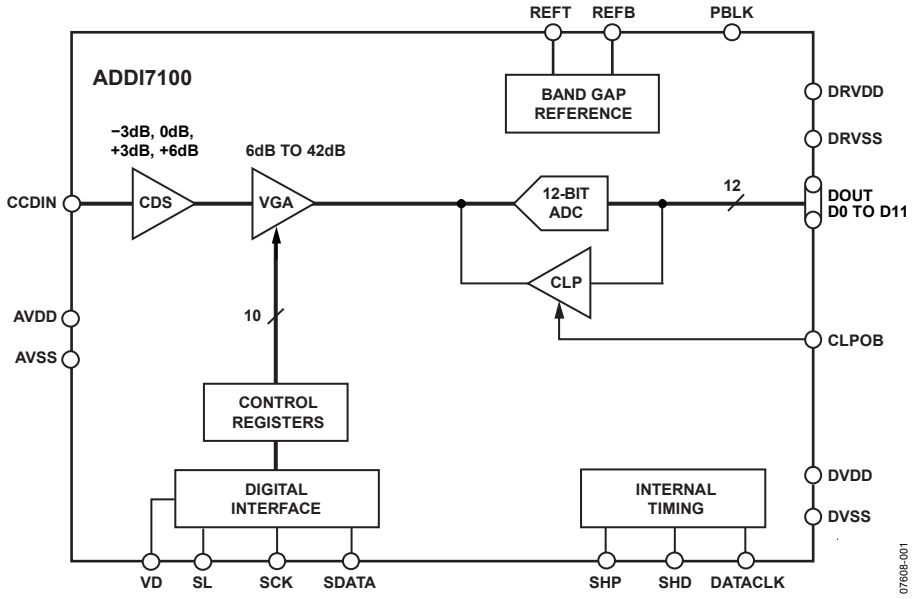

Figure 1.

Rev. E Document Feedback

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10/2008—Revision 0: Initial Version

SPECIFICATIONS

GENERAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD = 3 V, f_{SAMP} = 45 MHz, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	−25		+85	°C
Storage	−65		+150	°C
POWER SUPPLY VOLTAGE				
Analog, Digital, Digital Driver	2.7		3.6	V
POWER CONSUMPTION				
Normal Operation		125		mW
Full Standby Mode		1		mW
MAXIMUM CLOCK RATE	45			MHz

DIGITAL SPECIFICATIONS

DRVDD = DVDD = 2.7 V, C_L = 20 pF, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, I_{OH} = 2 mA	V_{OH}	2.2			V
Low Level Output Voltage, I_{OL} = 2 mA	V_{OL}			0.5	V

SYSTEM SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD = 3 V, f_{SAMP} = 45 MHz, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CDS	Input characteristics definition[1]				
Allowable CCD Reset Transient			0.5	1.2	V
CDS Gain Accuracy	VGA gain = 6 dB (Code 15, default value)				
−3 dB CDS Gain		−2.45	−2.95	−3.45	dB
0 dB CDS Gain	Default setting	5.40	5.90	6.40	dB
+3 dB CDS Gain		8.65	9.15	9.65	dB
+6 dB CDS Gain		11.10	11.60	12.10	dB
Maximum Input Range Before Saturation					
0 dB CDS Gain	Default setting		1.0		V p-p
−3 dB CDS Gain			1.4		V p-p
+6 dB CDS Gain			0.5		V p-p
Maximum CCD Black Pixel Amplitude	Positive offset definition[1]				
0 dB CDS Gain	Default setting	−100		+200	mV
+6 dB CDS Gain		−50		+100	mV
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution			1024		Steps
Gain Monotonicity			Guaranteed		
Gain Range					
Minimum Gain (VGA Code 15)	See Figure 13 for VGA curve		6.0		dB
Maximum Gain (VGA Code 1023)	See Variable Gain Amplifier (VGA) section for VGA gain equation		42.0		dB
BLACK LEVEL CLAMP MEASURED AT ADC OUTPUT					
Clamp Level Resolution			2048		Steps
Clamp Level	Measured at ADC output				
Minimum Clamp Level (Code 0)			0		LSB
Maximum Clamp Level (Code 1023)			511		LSB
ADC					
Resolution		12			Bits
Differential Nonlinearity (DNL)		−1.0	±0.5		LSB
No Missing Codes			Guaranteed		
Full-Scale Input Voltage			2.0		V
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)			2.0		V
Reference Bottom Voltage (REFB)			1.0		V
SYSTEM PERFORMANCE	Specifications include entire signal chain				
Gain Accuracy					
Low Gain (VGA Code 15)	6 dB total gain (default CDS, VGA)	5.4	5.9	6.4	dB
Maximum Gain (VGA Code 1023)		41.4	41.9	42.4	dB
Peak Nonlinearity, 1 V Input Signal	6 dB total gain (default CDS, VGA)		0.1		%
Total Output Noise	AC grounded input, 6 dB total gain		0.8		LSB rms
Power Supply Rejection (PSR)	Measured with step change on supply		45		dB

[1] Input signal characteristics are defined as shown in Figure 2.

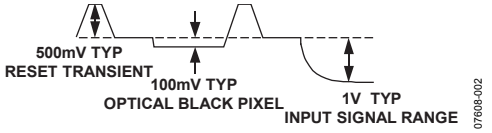


Figure 2.

TIMING SPECIFICATIONS

C_L = 20 pF, f_{SAMP} = 45 MHz, unless otherwise noted. See Figure 3, Figure 4, and Figure 16.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
SAMPLE CLOCKS					
DATACLK, SHP, SHD Clock Period	t_{CONV}	22			ns
DATACLK High/Low Pulse Width	t_{ADC}	9	11		ns
SHP Pulse Width	t_{SHP}		5.5		ns
SHD Pulse Width	t_{SHD}		5.5		ns
CLPOB Pulse Width[1]		2	20		Pixels
SHP Rising Edge to SHD Falling Edge	t_{S3}		5.5		ns
SHP Rising Edge to SHD Rising Edge	t_{S1}	9	11	$t_{CONV} - t_{S2}$	ns
SHD Rising Edge to SHP Rising Edge	t_{S2}	9	11	$t_{CONV} - t_{S1}$	ns
SHD Rising Edge to SHP Falling Edge	t_{S4}		5.5		ns
Internal Clock Delay	t_{ID}		4		ns
DATA OUTPUTS					
Output Delay	t_{OD}		15		ns
Pipeline Delay			15		Cycles
SERIAL INTERFACE					
Maximum SCK Frequency (Must Not Exceed Pixel Rate)	f_{SCLK}	40			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Rising Edge to SDATA Valid Hold	t_{DH}	10			ns

[1] Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp performance.

Timing Diagrams

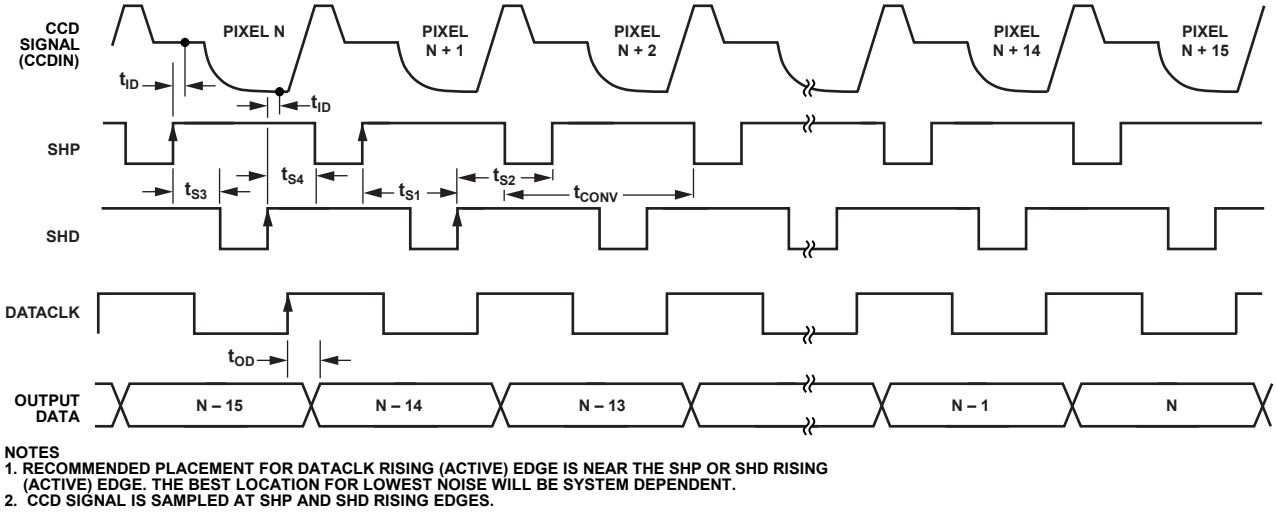
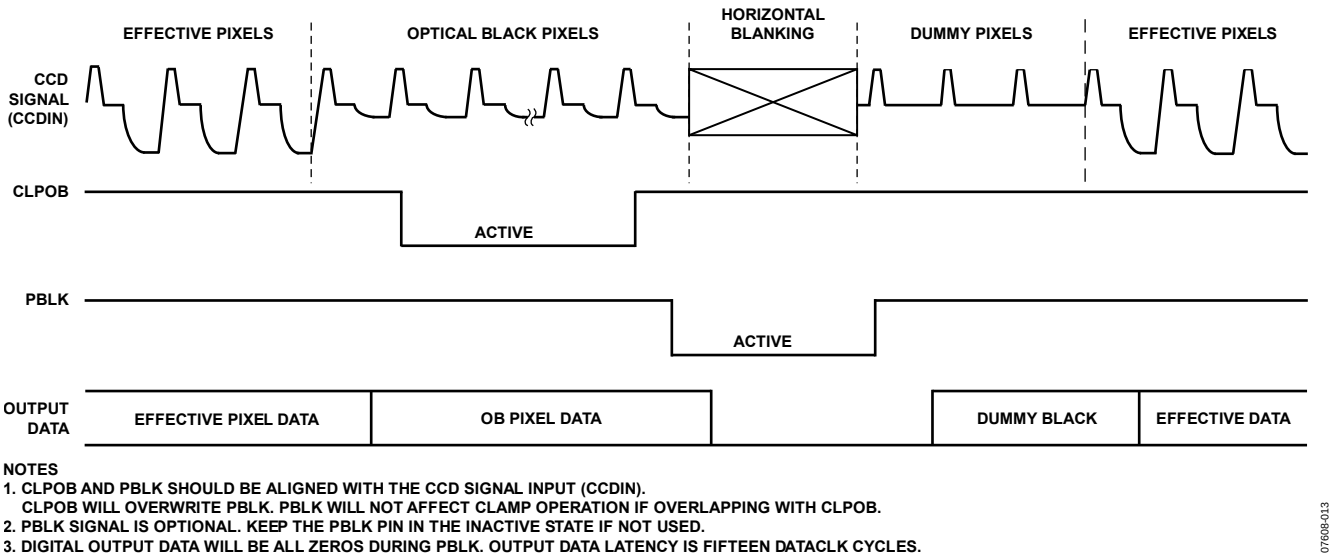


Figure 3. CCD Sampling Timing (Default Polarity Settings)



NOTES
1. CLPOB AND PBLK SHOULD BE ALIGNED WITH THE CCD SIGNAL INPUT (CCDIN). CLPOB WILL OVERWRITE PBLK. PBLK WILL NOT AFFECT CLAMP OPERATION IF OVERLAPPING WITH CLPOB.
2. PBLK SIGNAL IS OPTIONAL. KEEP THE PBLK PIN IN THE INACTIVE STATE IF NOT USED.
3. DIGITAL OUTPUT DATA WILL BE ALL ZEROS DURING PBLK. OUTPUT DATA LATENCY IS FIFTEEN DATACLK CYCLES.

Figure 4. Typical Clamp Timing (Default Polarity Settings)

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD to AVSS	−0.3 V to +3.9 V
DVDD to DVSS	−0.3 V to +3.9 V
DRVDD to DRVSS	−0.3 V to +3.9 V
Digital Outputs to DRVSS	−0.3 V to DRVDD + 0.3 V
SHP, SHD, DATACLK to DVSS	−0.3 V to DVDD + 0.3 V
CLPOB, PBLK to DVSS	−0.3 V to DVDD + 0.3 V
SCK, SL, SDATA to DVSS	−0.3 V to DVDD + 0.3 V
REFT, REFB, CCDIN to AVSS	−0.3 V to AVDD + 0.3 V
Junction Temperature	150°C
Lead Temperature (10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device with the exposed bottom pad soldered to the circuit board ground.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
32-Lead LFCSP	27.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

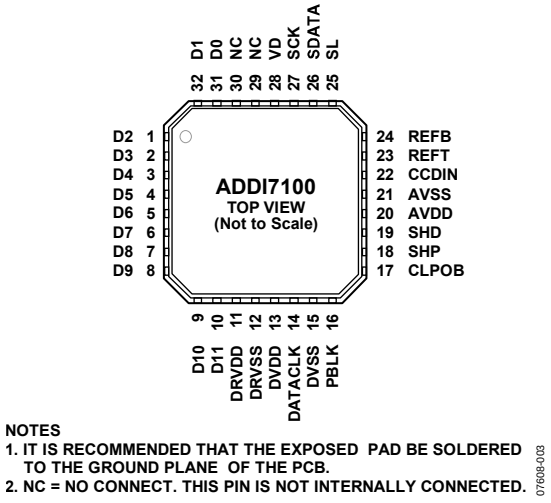


Figure 5. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1 to 10	D2 to D11	DO	Digital Data Outputs.
11	DRVDD	P	Digital Output Driver Supply.
12	DRVSS	P	Digital Output Driver Ground.
13	DVDD	P	Digital Supply.
14	DATACLK	DI	Digital Data Output Latch Clock.
15	DVSS	P	Digital Supply Ground.
16	PBLK	DI	Preblanking Clock Input.
17	CLPOB	DI	Black Level Clamp Clock Input.
18	SHP	DI	CDS Sampling Clock for CCD Reference Level.
19	SHD	DI	CDS Sampling Clock for CCD Data Level.
20	AVDD	P	Analog Supply.
21	AVSS	P	Analog Ground.
22	CCDIN	AI	Analog Input for CCD Signal.
23	REFT	AO	ADC Top Reference Voltage Decoupling.
24	REFB	AO	ADC Bottom Reference Voltage Decoupling.
25	SL	DI	Serial Digital Interface Load Pulse.
26	SDATA	DI	Serial Digital Interface Data Input.
27	SCK	DI	Serial Digital Interface Clock Input.
28	VD	DI	Vertical Sync Input. Controls the update time of VD-updated registers. If this pin is not needed, it should be tied to GND.
29, 30	NC	NC	No Connect. The pin is not internally connected.
31, 32	D0, D1	DO	Digital Data Output.
	EPAD		Exposed Pad. It is recommended that the exposed pad be soldered to the ground plane of the printed circuit board (PCB).

[1] AI = analog input, AO = analog output, DI = digital input, DO = digital output, P = power, and NC = no connect.

TYPICAL PERFORMANCE CHARACTERISTICS

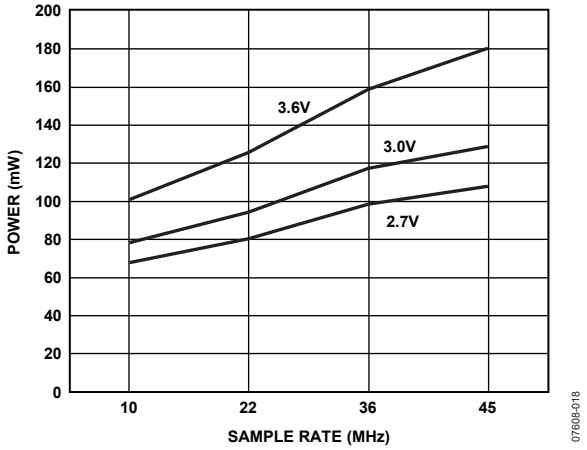


Figure 6. Power vs. Sample Rate

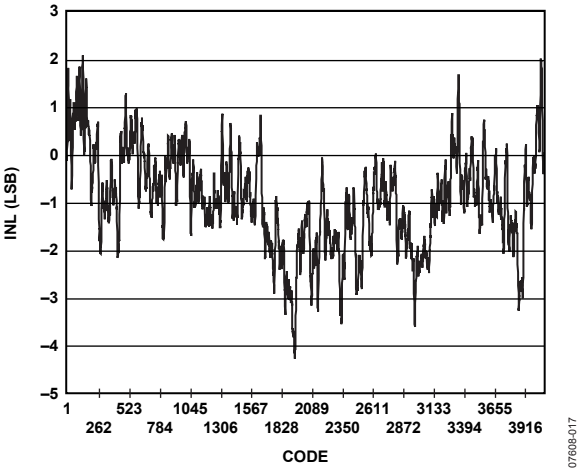


Figure 8. Typical INL Performance

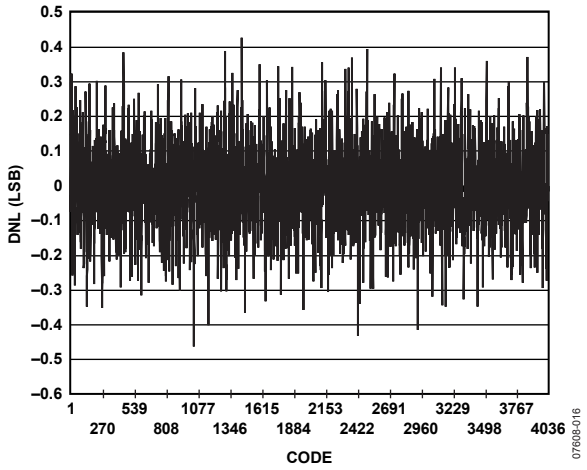


Figure 7. Typical DNL Performance

EQUIVALENT INPUT CIRCUITS

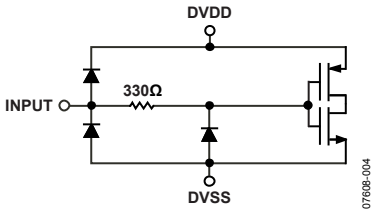


Figure 9. Digital Inputs
SHP, SHD, DATACLK, CLPOB, PBLK, SCK, SL, SDATA, and VD

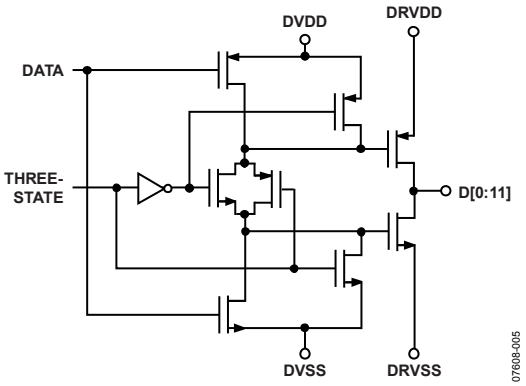


Figure 10. Data Outputs

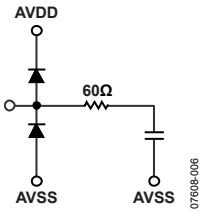


Figure 11. CCDIN (Pin 22)

TERMINOLOGY

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating conditions.

Peak Nonlinearity
Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the ADDI7100 from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level that is 1.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always gained appropriately to fill the full-scale range of the ADC.

Total Output Noise
The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSBs and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship

$$1 \text{ LSB} = (\textit{ADC Full Scale}/2^N \text{ codes})$$

where N is the bit resolution of the ADC. For example, 1 LSB of the ADDI7100 is 0.5 mV.

Power Supply Rejection (PSR)
PSR is measured with a step change applied to the supply pins. This represents a very high frequency disturbance on the power supply of the ADDI7100. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

Internal Delay for SHP/SHD
The internal delay (also called aperture delay) is the time delay that occurs from the time a sampling edge is applied to the ADDI7100 until the actual sample of the input signal is held. Both SHP and SHD sample the input signal during the transition from low to high; therefore, the internal delay is measured from the rising edge of each clock to the instant that the actual internal sample is taken.

CIRCUIT DESCRIPTION AND OPERATION

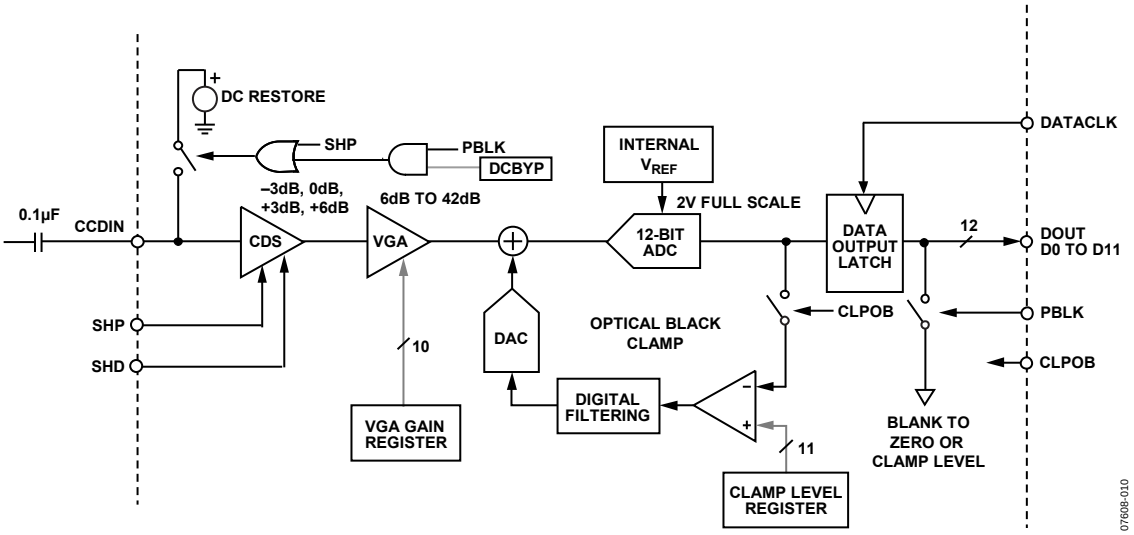


Figure 12. CCD Mode Block Diagram

The ADDI7100 signal processing chain is shown in Figure 12. Each processing step is essential for achieving a high quality image from the raw CCD pixel data.

DC RESTORE

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external 0.1 µF series coupling capacitor. This circuit restores the dc level of the CCD signal to approximately 1.5 V, which is compatible with the 3 V supply of the ADDI7100.

CORRELATED DOUBLE SAMPLER (CDS)

The CDS circuit samples each CCD pixel twice to extract video information and to reject low frequency noise. The timing shown in Figure 3 illustrates how the two CDS clocks, SHP and SHD, are used to sample the reference level and the data level, respectively, of the CCD signal. The CCD signal is sampled on the rising edges of SHP and SHD. Placement of these two clock signals is critical for achieving the best performance from the CCD. An internal SHP/SHD delay (t_{ID}) of 4 ns is caused by internal propagation delays.

OPTICAL BLACK CLAMP

The optical black clamp loop removes residual offsets in the signal chain and tracks low frequency variations in the CCD black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with the fixed black level reference selected by the user in the clamp level register (Address 0x04). The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a DAC. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during postprocessing, optical black clamping for the ADDI7100 can be disabled using Address 0x00, Bit 2. When the optical black clamp loop is disabled, the clamp level register can still be used to provide programmable offset adjustment.

Note that if the CLPOB is disabled, higher VGA gain settings reduce the dynamic range because the uncorrected offset in the signal path is amplified.

Horizontal timing is shown in Figure 4. Align the CLPOB pulse with the optical black pixels of the CCD. It is recommended that the CLPOB pulse be used during valid CCD dark pixels. It is recommended that the CLPOB pulse should be 20 pixels wide to minimize clamp noise. Shorter pulse widths can be used, but the ability of the loop to track low frequency variations in the black level is reduced.

ANALOG-TO-DIGITAL CONVERTER (ADC)

The ADDI7100 uses a high performance ADC architecture optimized for high speed and low power. Differential nonlinearity (DNL) performance is typically better than 0.5 LSB. The ADC uses a 2 V full-scale input range.

VARIABLE GAIN AMPLIFIER (VGA)

The VGA stage provides a gain range of 6 dB to 42 dB, programmable with 10-bit resolution through the serial digital interface. The minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. A plot of the VGA gain curve is shown in Figure 13.

$$VGA\ Gain\ (\text{dB}) = (VGA\ Code \times 0.0358\ \text{dB}) + 5.4\ \text{dB}$$

where *Code* is in the range of 0 to 1023.

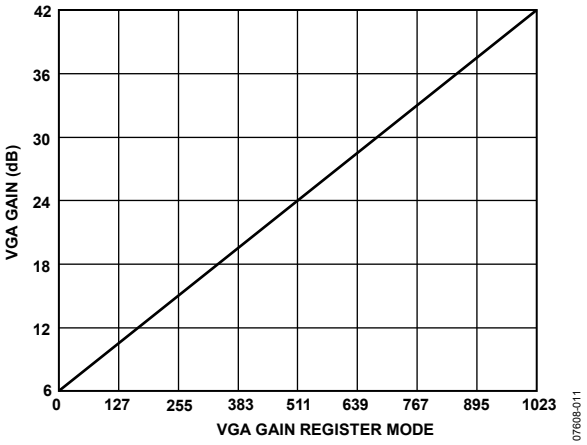


Figure 13. VGA Gain Curve

DIGITAL DATA OUTPUTS

By default, the digital output data is latched by the rising edge of the DATACLK input. Output data timing is shown in Figure 3. It is also possible to make the output data latch transparent, immediately validating the data outputs from the ADC. Setting the DOUTLATCH register (Address 0x01[5]) to 1 configures the latch as transparent. The data outputs can also be disabled by setting the DOUT_OFF register (Address 0x01[4]) to 1.

APPLICATIONS INFORMATION

The ADDI7100 is a complete analog front-end (AFE) product for digital still camera and camcorder applications. As shown in Figure 14, the CCD image (pixel) data is buffered and sent to the ADDI7100 analog input through a series input capacitor. The ADDI7100 performs the dc restoration, CDS sampling, gain adjustment, black level correction, and analog-to-digital conversion. The digital output data of the ADDI7100 is then processed by the image processing ASIC. The internal registers of the ADDI7100—used to control gain, offset level, and other functions—are programmed by the ASIC or by a microprocessor through a 3-wire serial digital interface. A system timing generator provides the clock signals for both the CCD and the AFE (see Figure 14).

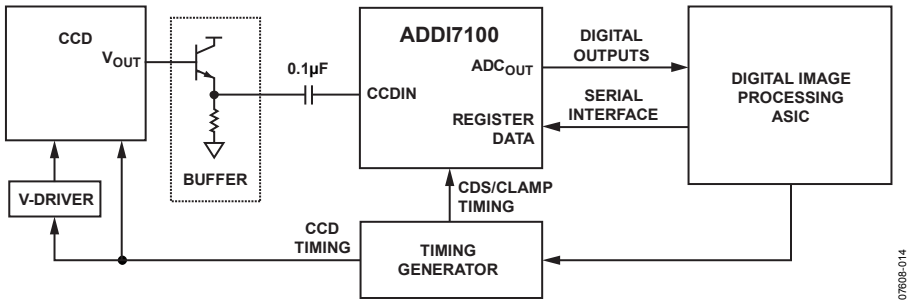


Figure 14. System Applications Diagram

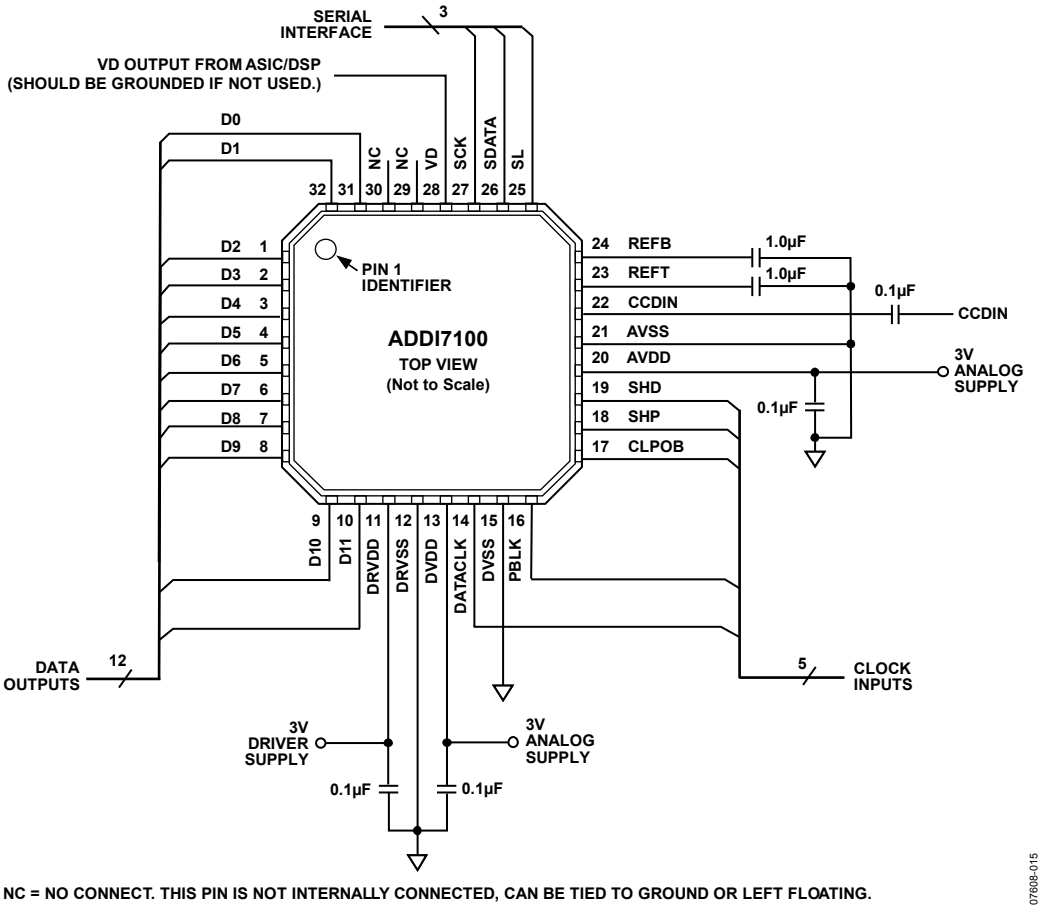


Figure 15. Recommended Circuit Configuration for CCD Mode

INITIAL POWER-ON SEQUENCE

After power-on, the ADDI7100 automatically resets all internal registers to default values. Settling of the internal voltage reference takes approximately 1 ms to complete. During this time, normal clock signals and serial write operations can take place, but valid output data do not occur until the reference is fully settled. When loading the desired register settings, the STARTUP register (Address 0x05[1:0]) must be set to 0x3.

GROUNDING AND DECOUPLING RECOMMENDATIONS

As shown in Figure 15, a single ground plane is recommended for the ADDI7100. This ground plane should be as continuous as possible to ensure that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. Place all decoupling capacitors as close as possible to the package pins.

A single clean power supply is recommended for the ADDI7100, but a separate digital driver supply can be used for DRVDD (Pin 11). Always decouple DRVDD to DRVSS (Pin 12), which should be connected to the analog ground plane. The advantages of using a separate digital driver supply include using a lower voltage (2.7 V) to match levels with a 2.7 V ASIC, and reducing digital power dissipation and potential noise coupling. If the digital outputs must drive a load larger than 20 pF, buffering is the recommended method to reduce digital code transition noise. Alternatively, placing series resistors close to the digital output pins may also help to reduce noise.

Note that the exposed pad on the bottom of the package should be soldered to the ground plane of the printed circuit board.

SERIAL INTERFACE TIMING

All ADDI7100 internal registers are accessed through a 3-wire serial interface. Each register consists of an 8-bit address and a 16-bit data-word. Both the address and the data-word are written starting with the LSB. To write to each register, a 24-bit operation is required, as shown in Figure 16. Although many data-words are fewer than 16 bits wide, all 16 bits must be written for each register. For example, if the data-word is only eight bits wide, the upper eight bits are don't care bits and must be filled with zeros during the serial write operation. If fewer than 16 data bits are written, the register is not updated with new data.

Figure 17 shows a more efficient way to write to the registers, using the ADDI7100 address autoincrement capability. Using this method, the lowest desired address is written first, followed by multiple 16-bit data-words. Each data-word is automatically written to the address of the next highest register. By eliminating the need to write each address, faster register loading is achieved. Continuous write operations can start with any register location.

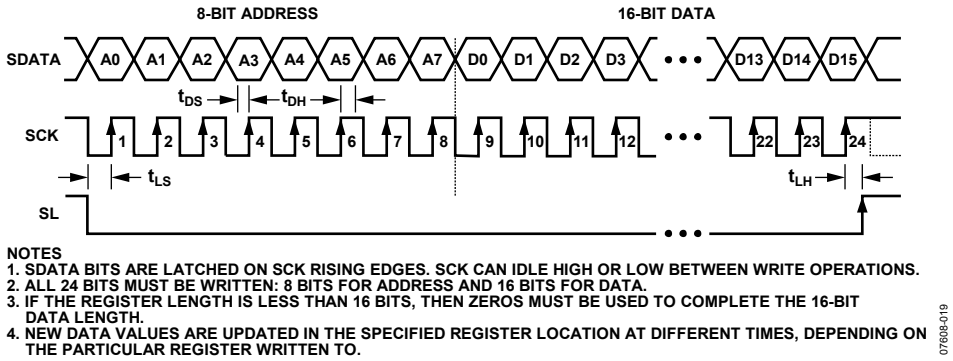


Figure 16. Serial Write Operation

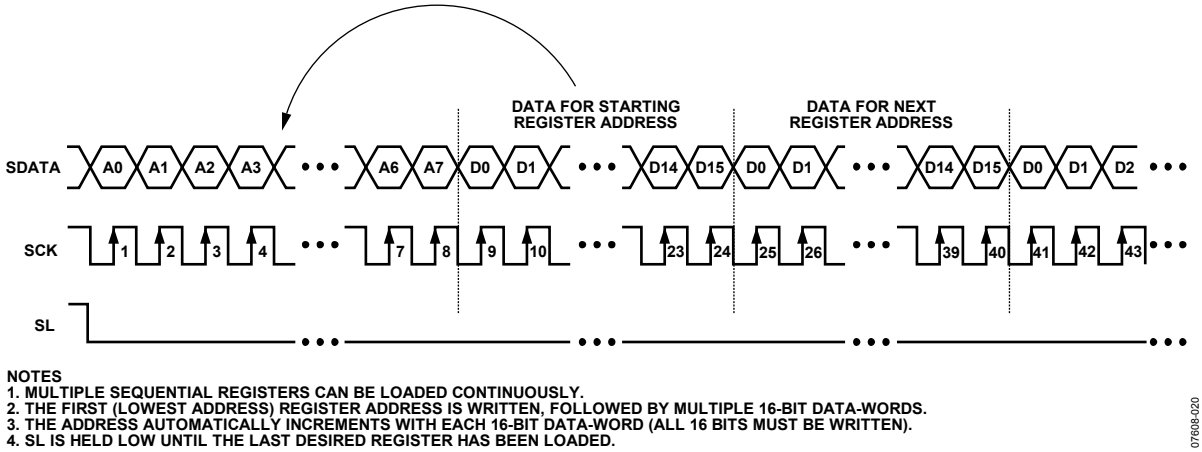


Figure 17. Continuous Serial Write Operation

COMPLETE REGISTER LISTING

Note that when an address contains fewer than 16 data bits, all remaining bits must be written as zeros.

Table 8. AFE

Address	Data Bits	Default Value	Update Type[1]	Name	Description
0x00	[1:0]	0	SCK	STANDBY	00: normal operation 01: reference standby 10: full standby 11: full standby
	[2]	0x1		CLAMP_EN	1: enable black clamp 0: disable black clamp
	[3]	0		FASTCLAMP	0: normal CLPOB settling 1: faster CLPOB settling
	[4]	0		FASTUPDATE	1: enable very fast clamping when CDS gain is changed 0: ignore CDS gain updates
	[5]	0		PBLK_LVL	0: blank to 0 1: blank to clamp level
	[6]	0		DCBYP	0: normal dc restore operation 1: dc restore disabled during PBLK active
	[8:7]	0x2		Test	Test use only; must be set to 2
	[10:9]	0x2		Test	Test use only; must be set to 2
0x01	[0]	0	SCK	SHPD_POL	0: rising edge sample 1: falling edge sample
	[1]	0		DATACLK_POL	0: rising edge triggered 1: falling edge triggered
	[2]	0		CLP_POL	0: active low 1: active high
	[3]	0		PBLK_POL	0: active low 1: active high
	[4]	0		DOUT_OFF	0: data outputs are driven 1: data outputs are disabled (high-Z)
	[5]	0		DOUTLATCH	0: retime data outputs with output latch (using DATACLK) 1: do not retime data outputs; output latch is transparent
	[6]	0		GRAY_EN	1: gray encode ADC outputs
0x02	[2:0]	0x1	SCK/VD	CDSGAIN	CDS gain setting: 0x0: −3 dB 0x1: 0 dB 0x2: +3 dB 0x3: +6 dB
0x03	[9:0]	0x0F	SCK/VD	VGAGAIN	VGA gain, 6 dB to 42 dB (0.0358 dB per step)
0x04	[10:0]	0x1EC	SCK/VD	CLAMPLEVEL	Optical black clamp level, 0 LSB to 511 LSB (0.25 LSB per step)
0x05	[1:0]	0	SCK	STARTUP	Must be set to 0x3 after power-up
	[3:2]	0		Test	Test use only; must be set to 0
0x06	[2:0]	0x6	SCK	Test	Test use only; must be set to 6
	[3]	0		Test	Test use only; must be set to 0
	[5:4]	0		Test	Test use only; must be set to 0
0x07	[0]	0	SCK	Test	Test use only; must be set to 0
0x08	[11:0]	0xFFF	SCK	Test	Test use only; must be set to 0xFFF
0x09	[11:0]	0xFFF	SCK	Test	Test use only; must be set to 0xFFF
0x0A	[0]	0	SCK	Test	Test use only; must be set to 0
0x0B	[0]	0	SCK	SW_RST	1: software reset; automatically resets to 0 after software reset
0x0C	[0]	0x1	SCK	OUTCONTROL	Data output control: 0: make all outputs dc inactive 1: enable data outputs

Address	Data Bits	Default Value	Update Type[1]	Name	Description
0x0D	[0]	0	SCK	VD_POL	0: falling edge triggered 1: rising edge triggered
0x0E	[6:0]	0	SCK	REG_UPDATE	Set the appropriate bits high to enable VD update of the selected registers: [0]: CDSGAIN (Register 0x02) [1]: VGAGAIN (Register 0x03) [2]: CLAMPLEVEL (Register 0x04) [3]: test use only; must be set to 0 [4]: test use only; must be set to 0 [5]: test use only; must be set to 0 [6]: test use only; must be set to 0
0xFF	[0]	0	SCK	Test	Test use only; do not access

[1] SCK = register is immediately updated when the 16th data bit (D15) is written. VD = register is updated at the VD falling edge.

OUTLINE DIMENSIONS

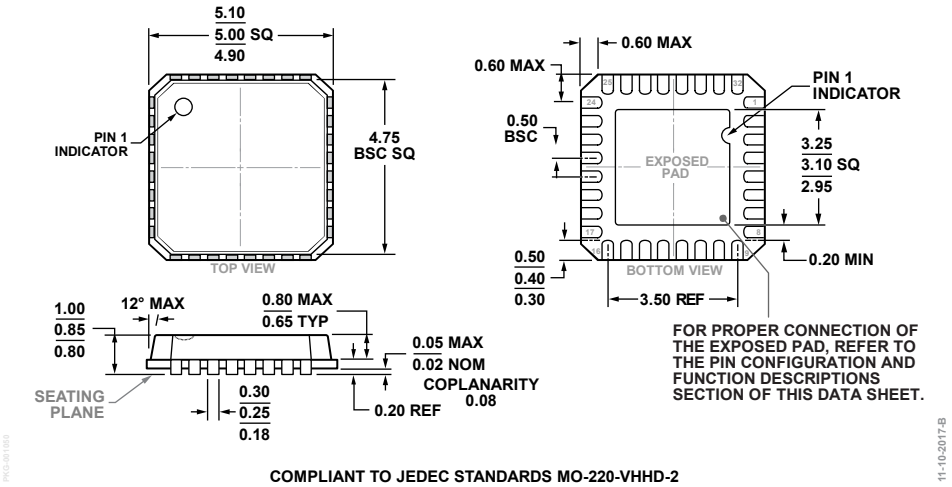


Figure 18. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.85 mm Package Height
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADDI7100BCPZ	−25°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-2
ADDI7100BCPZRL	−25°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-2

[1] Z = RoHS Compliant Part.

NOTES

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