AD9081/AD9082 System Development User Guide

SCOPE

This user guide provides information for systems engineers and software developers using the AD9081 and AD9082 family of software defined, direct RF sampling transceivers. This family of devices consists of high performance digital-to-analog converters (DAC) and analog-to-digital converters (ADC) with configurable digital datapaths in support of processing signals or RF bands of varying bandwidth. These devices also support various digital features that enhance or simplify system integration. Table 1 outlines the key differences between these devices, and the Common Features section outlines the common features shared among the devices. These devices are interchangeable unless otherwise stated in this user guide. For full specifications on the AD9081 and AD9082, refer to the AD9081 and AD9082 data sheets, which must be consulted in conjunction with this user guide to achieve successful product selection and design.

Table 1. Product Listing with Distinguishing Features

	Transmit (Tx)			Receive (Rx)			Special Digital Features				Device ID Register Values			
Device and Channel Configuration	No. of DAC Channels, Resolution	Max DAC Rate (GSPS)[1]	Max Tx Channel Bandwidth (GHz)	No. of ADC Channels	Max ADC Rate (GSPS)	Max Rx Channel Bandwidth (GHz)	Tx and Rx Bypass Operation	Rx to Tx Loopback	Fast Frequency Hopping (FFH)	Direct Digital Synthesis (DDS)	0x003	0x004	0x005	0x006
AD9081														
-4D4AC	4 – 16b	12	1.2	4	4	2	Yes	Yes	Yes	Yes	0Fh	81h	90h	A3h
-4D4AC	4 – 12b	12	1.6	4	4	2	Yes	Yes	Yes	Yes	0Fh	81h	90h	A3h
-4D4AB	4 – 16b	12	0.6	4	4	0.6	Yes	Yes	Yes	Yes	0Fh	81h	90h	B3h
AD9082														
-4D2AC	4 – 16b	12	1.2	2	6	3	Yes	Yes	Yes	Yes	0Fh	82h	90h	23h
-4D2AC	4 – 12b	12	2.4	2	6	3	Yes	Yes	Yes	Yes	0Fh	82h	90h	23h
-2D2AC	2 – 16b	12	2.4	2	6	3	Yes	Yes	Yes	Yes	0Fh	82h	90h	13h
AD9988														
-4D4AC	4 – 16b	12	1.2	4	4	1.6	No	No	No	No	0Fh	88h	99h	A3h
AD9986														
-4D2AC	4 – 16b	12	1.2	2	6	2.4	No	No	No	No	0Fh	86h	99h	23h
-4D2AC	2 – 16b	12	2.4	2	6	2.4	No	No	No	No	0Fh	86h	99h	23h
AD9207	N/A	N/A	N/A	2	6	3	Yes	N/A	Yes	N/A	03h	07h	92h	23h
AD9209	N/A	N/A	N/A	4	4	2	Yes	N/A	Yes	N/A	03h	09h	92h	A3h
AD9177	4 – 16b	12	1.2	N/A	N/A	N/A	Yes	Yes	Yes	Yes	04h	77h	91h	A3h

[1] Max DAC Rate assumes 16-bit resolution.

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SYSTEM OVERVIEW

The AD9081 is a highly integrated, RF mixed signal front-end (MxFE™) that features four 16-bit, 12 GSPS DAC cores and four 12-bit, 4 GSPS ADC cores, as shown in Figure 1. The AD9082 features four 16-bit, 12 GSPS DAC cores and two 12-bit, 6 GSPS ADC cores, as shown in Figure 2. Aside from the different ADC options, both devices are nearly identical in all other aspects (unless otherwise noted in this user guide). The devices include an optional on-chip clock multiplier for DAC and ADC sampling clock generation as well as broadband ADC and DAC cores with on-chip 100 Ω termination.

The transmit and receive digital datapaths are highly configurable and support a wide range of single band and multiband applications with varying RF bandwidth requirements. The transmit and receive datapaths consist of four main datapaths in support of wideband signals and eight channelizers in support of narrower band signals. For multiband applications with wide separation between RF bands, the channelizers can be used to process the individual RF bands to reduce the overall complex data rate needed to represent each narrower band. Both the main and channelizer datapath stages offer flexible interpolating and decimation factors to allow a manageable data interface rate aligned to the actual signal bandwidth requirements. The numerically controlled oscillator (NCO) of each stage can be independently tuned for maximum flexibility.

Additional digital features are listed in the Common Features section.

The serializer/deserializer (SERDES) interface supports eight lanes for transmit data and eight lanes for receive data. Both JESD204B and JESD204C protocols are supported as well as the ability to configure dual links. The JESD204B/C data link layer is highly flexible and allows optimization of the lane count (or rate) required to support a desired data throughput rate. Multichip synchronization and internal synchronization for deterministic latency and phase alignment are supported via an external alignment signal (SYSREF).

COMMON FEATURES

Analog Features

Common analog features for the devices include the following:

- Usable RF range up to 8 GHz
- ADC overvoltage protection
- DAC transmit gain control
- On-chip phased-locked loop (PLL) clock multiplier with output clock

Digital Features

Common digital features for the devices include the following:

- Transceiver and receiver digital upconverter (DUC) and digital downconverter (DDC)
- Highly configurable 196-tap programmable filter (PFILT) supporting four profiles
- Transceiver and receiver integer delay with receiver fractional delay
- Multichip synchronization
- Receiver signal monitoring and automatic gain control (AGC) assist features
- Transceiver gain control and power amplifier (PA) protection
- Power reduction options
- General purpose input/output (GPIO)

SERDES Interface

Common SERDES features for the devices include the following:

- JESD204B and JESD204C
- Eight transmit lanes and eight receive lanes
- Support for two links
- Support for up to 16 virtual converters
- Sample repeat option

SYSTEM OVERVIEW

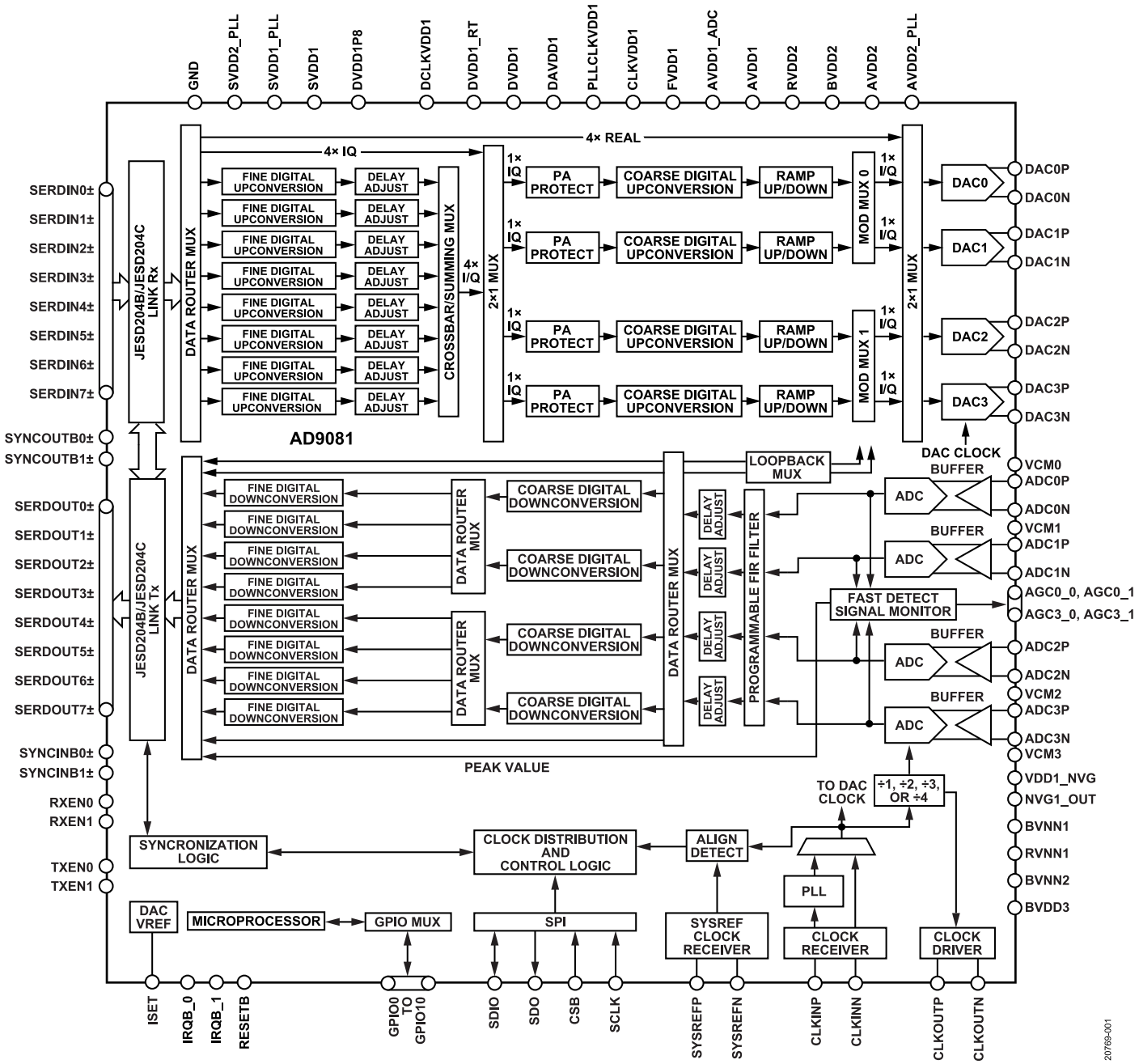

Figure 1. AD9081 Functional Block Diagram

SYSTEM OVERVIEW

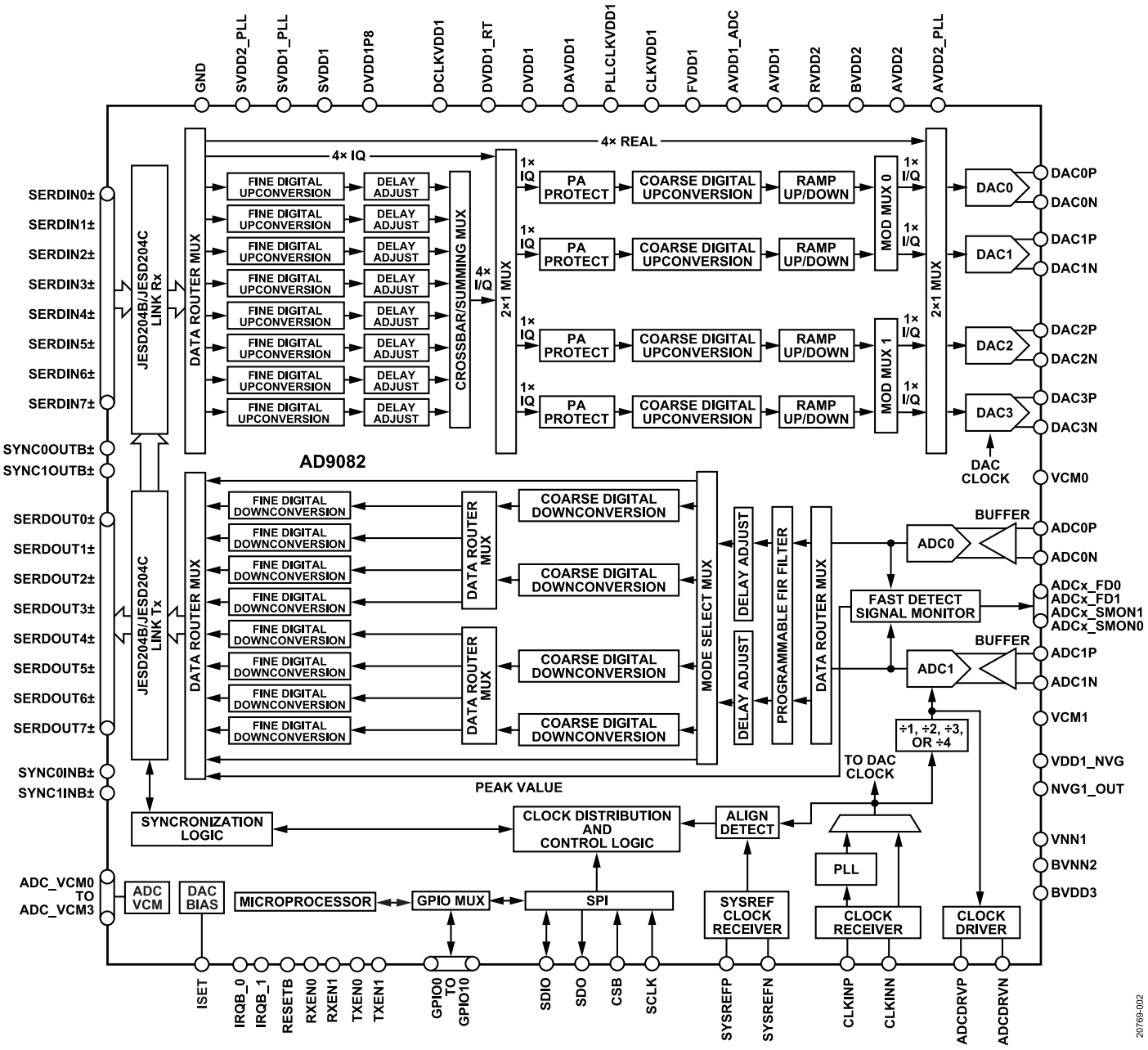

Figure 2. AD9082 Functional Block Diagram

SOFTWARE OVERVIEW

This section provides information about the application programming interface (API) software developed by Analog Devices, Inc., for the AD9xxx product family. This section outlines the overall architecture, folder structure, and methods for using the API software on any platform.

The device API C code drivers are provided as reference code that allows the user to quickly configure the product using high level function calls. The library acts as an abstraction layer between the application and the hardware. The API is developed in C99 to ensure agnostic processor and operating system integration. Customers can port this application layer code to their embedded systems by integrating their platform specific code base to the API hardware abstraction layer (HAL).

To request this software package, navigate to the software request form while signed in to your MyAnalog account. From under **Target Hardware**, select **High Speed Data Converters** and choose the desired API product package. You will receive an email notification once the software is provided to you.

SOFTWARE ARCHITECTURE

The device API library is a collection of APIs that provide a consistent interface for the AD9xxx product family. The APIs are designed such that there is a consistent interface to the devices.

The API library is a software layer that sits between the application and the device, as shown in Figure 3. The library is intended to serve the following purposes:

- To provide the application with a set of APIs that can be used to configure the device without the need for low level register access, which makes the application portable across different revisions of the hardware and across different hardware modules.
- To provide basic services to aid the application in controlling the components of the device module, such as NCO configuration and JESD204B/C link configuration.

The driver does not alter the device configuration or state of the device without assistance. The application must configure the device according to the required mode of operation and poll for status. The library acts only as an abstraction layer between the application and the hardware.

For example, the application is responsible for the following:

- Configuring the JESD interface
- Configuring the DDC and NCOs

The application must access the device only through the exported APIs. Accessing the device directly using serial peripheral interace (SPI) access is not recommended. If the application directly accesses the device hardware, the application must do so in a limited scope, such as for debug purposes. Note that this practice of direct access may affect the reliability of the API functions.

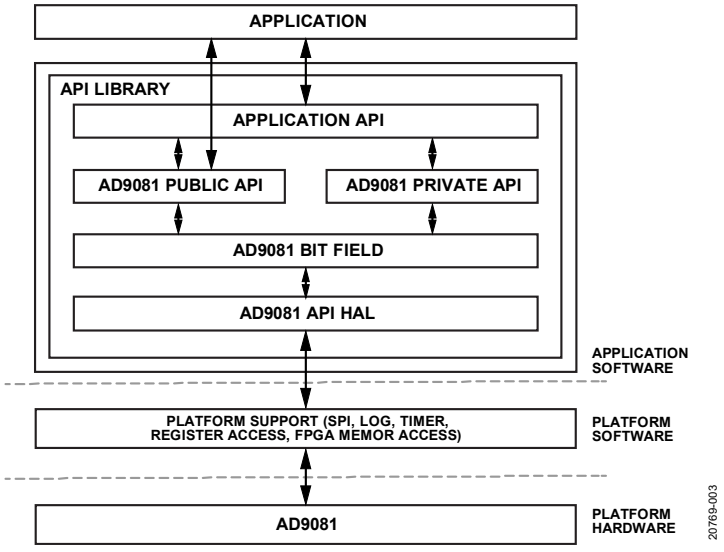

Figure 3. AD9081 API Architecture

SOFTWARE OVERVIEW

FOLDER STRUCTURE

The collective files of the device API library are structured as shown in Figure 4. Each branch in the directory hierarchy is explained in the /src/ad9081_api section through the /doc section. The library is supplied in source format. All source files are in standard C99 to simplify porting to any platform.

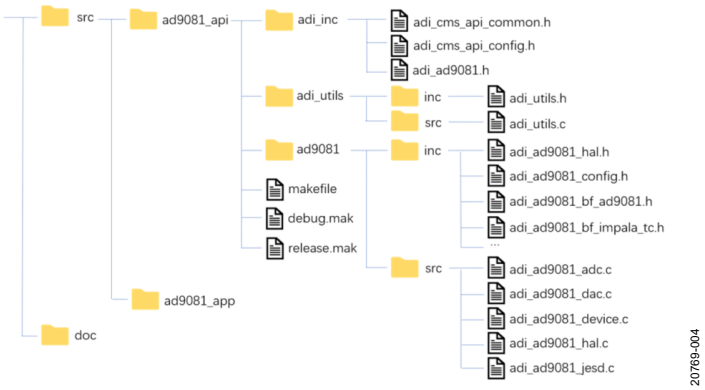

Figure 4. AD9081 Source Code Folder Structure

/src/ad9081_api

The device API root folder contains all source code and the example makefile for the API.

/src/ad9081_api/adi_inc

This folder contains all API public interface files. These files are the header files required by the client application for integration.

/src/ad9081_api/adi_utils

This folder contains the helper functions common to all Analog Devices APIs. These functions are internal private functions and are not designed for client application use.

/src/ad9081_api/ad9081

This folder includes the main API implementation code for the device APIs and any private header files used by the API. Analog Devices maintains this code as intellectual property and all changes are at the sole discretion of Analog Devices.

/src/ad9081_app

This folder contains simple source code examples of how to use the device API. The application targets the device evaluation board platform. Customers can use this example code as a guide to develop their own application based on individual user requirements.

/doc

This folder contains the documentation for the device APIs.

API INTEGRATION AND BUILD

This section provides an overview of the integration and building steps required when using Analog Devices API source code.

Because Analog Devices provides the full source code, the user can integrate and build the libraries per their application. However, users are required to integrate the API HAL with their platform specific code base. This action is readily accomplished because the API was developed in C99. The C99 standard was followed to ensure agnostic processor and operating system integration with the API code. See Figure 5 for the AD9xxx API integration flow.

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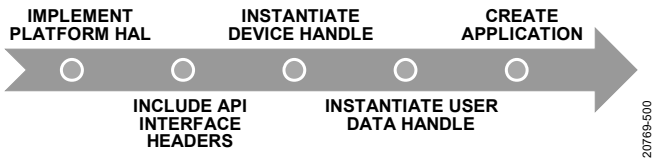

Figure 5. AD9xxx API Integration Flow

Integrating the AD9xxx API into an Application

There are five phases to integrating the AD9xxx API into an application as described in the Phase 1: Implement the HAL Functions section through Phase 5: Create the Application section.

Phase 1: Implement the HAL Functions

The API requires access to several platform specific hardware and system control functions, such as a system delay and sleep function, SPI bus controller functions, GPIO controller, and so on. The end user must provide and implement these functions per the AD9xxx requirements. The prototypes of these functions are defined in the **src/ad9xxx_api/adi_inc/adi_cms_api_common.h** header file and are explained in the HAL function pointer data types section of the general API architecture document.

Users develop their own HAL functions based on their hardware dependent platforms. Therefore, depending on their platform, users use different drivers for the peripherals, such as the SPI and GPIO. Users can use their own drivers for these peripherals, or users can use standard drivers if they use an operating system.

The AD9xxx API was developed such that developers can use any driver of their choosing for their platform requirements. However, there are a few platform dependent functions in the API HAL. Do not modify these layers because a specific function prototype was used for these functions. Instead, users must write their own platform functions based on these prototypes in the **adi_cms_api_common.h file** in the **src/AD9xxx_api/adi_inc** directory for specific platform requirements.

Per the AD9xxx API specification, the following HAL members are required, at the minimum, for proper operation of the AD9xxx APIs:

- hal_info.spi _xfer, pointer to the SPI data transfer function for each AD9xxx device
- hal_info.delay_us, pointer to the delay function for each AD9xxx device
- hal_info.log_write, pointer to the log write function for each AD9xxx device
- hal.info.reset_pin_ctrl, pointer to a function that implements reset pin control for each AD9xxx device

Phase 2: Include the AD9xxx API Interface Header Files

The **/src/ad9xxx_api/adi_inc/adi_AD9xxx.h** header file defines the interface to the AD9xxx API and must be included in the application.

Phase 3: Instantiate AD9xxx Device Handle

For each AD9xxx device, the application must instantiate a unique AD9xxx handler reference.

For a full description of the AD9xxx handler, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

For each handler instantiated by the application, all the required members of the device handler must be initialized prior to calling any APIs with that handler as a parameter.

Along with the HAL members, the SPI, GPIO, and other peripheral interfaces must also be initialized prior to using any API functions.

Example AD9xxx Device Instantiation on the ADS9 Platform

```
adi_AD9xxx_device_t AD9xxx_dev = {
.hal_info = {
.sdo = SPI_SDO,
.msb = SPI_MSB_FIRST,
.addr_inc = SPI_ADDR_INC_AUTO,
.log_write = ads9_log_write,
.delay_us = ads9_wait_us,
.spi_xfer = ads9_spi_xfer_AD9xxx,
```

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```
.reset_pin_ctrl = ads9_hw_rst_pin_ctrl_AD9xxx,
},
.serdes_info = {
.ser_settings = { /* AD9xxx jtx */
.lane_settings = {
{.swing_setting = AD9XXX_SER_SWING_850, .pre_emp_setting = AD9XXX_SER_PRE_EMP_0DB, .post_emp_setting = AD9XXX_SER_POST_EMP_0DB},
{.swing_setting = AD9XXX_SER_SWING_850, .pre_emp_setting = AD9XXX_SER_PRE_EMP_0DB, .post_emp_setting = AD9XXX_SER_POST_EMP_0DB},
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{.swing_setting = AD9XXX_SER_SWING_850, .pre_emp_setting = AD9XXX_SER_PRE_EMP_0DB, .post_emp_setting = AD9XXX_SER_POST_EMP_0DB},
},
.invert_mask = 0x00,
.lane_mapping = { { 6, 4, 3, 2, 1, 0, 7, 5 }, { 2, 0, 7, 7, 7, 7, 3, 1 } }, /* link0, link1 */
},
.des_settings = { /* AD9xxx jrx */
.boost_mask = 0xff,
.invert_mask = 0x00,
.ctle_filter = { 2, 2, 2, 2, 2, 2, 2, 2 },
.lane_mapping = { { 0, 1, 2, 3, 4, 5, 6, 7 }, { 4, 5, 6, 7, 0, 1, 2, 3 } }, /* link0, link1 */
}
}
};
```

Phase 4: Instantiate User Data Handle.

Another member of the device handler that must be instantiated properly is user_data. The user can implement a user defined data structure to hold all the peripheral specific configuration settings for the hardware platform that is connected to the AD9xxx. For the AD9xxx, there is a platform API for creating user data (that is, ads9_user_data_create_AD9xxx()).

Phase 5: Create the Application

Using the AD9xxx APIs provided in the **/src/AD9xxx_api/ adi_inc/adi_AD9xxx.h** header file, write the application code to initialize, configure, monitor, and log the AD9xxx device per your target application requirements.

An example application based on one of the Analog Devices platforms is provided with every product API as a reference. The example application is in the **/src/AD9xxx_app/app_ads9/ AD9xxx_app.c** folder. The application initializes the platform peripherals it is based on, initializes the device under test (DUT) and any other clocking chips on the evaluation board, and then configures the device for a use case.

This example application can be used to bring up the device in predefined use cases, or it can serve as a starting point for more complicated target applications.

API OVERVIEW BLOCK DIAGRAM

To set up the AD9xxx MxFE products, a variety of system high level API function calls facilitate the setup of the device in a variety of conditions. These function calls cover the configuration of all key feature blocks of the product and abstract the details of the required sequences to set up the chip properly and minimize the burden on the user to complete all steps manually.

Figure 6 shows the general overview of the system bring-up for the MxFE products. The blocks in green represent the stages of the hardware and system configuration outside of the AD9xxx that set up the environment around the product. These steps must be adapted based on the setup of the user and reference some of the example code and steps needed when using the Analog Devices evaluation platform (ADS9v2 field-programmable gate array (FPGA) board with the MxFE evaluation board). The blocks in blue reference the top system level API functions that are called as part of the example standalone application, which is included in the source code package in the src/AD9xxx_app folder. The example standalone application provides a set of preconfigured use cases that set up various conditions by calling these system high level APIs. For most use cases, the startup process is enough to get the MxFE configured properly for integration in any system.

This startup process consists of four basic functional groups of configurations: initialization and clocking, transmit datapath setup, receive datapath setup, and SERDES link establishment. Figure 6 shows the API function calls needed for each section.

For more details on the API function calls, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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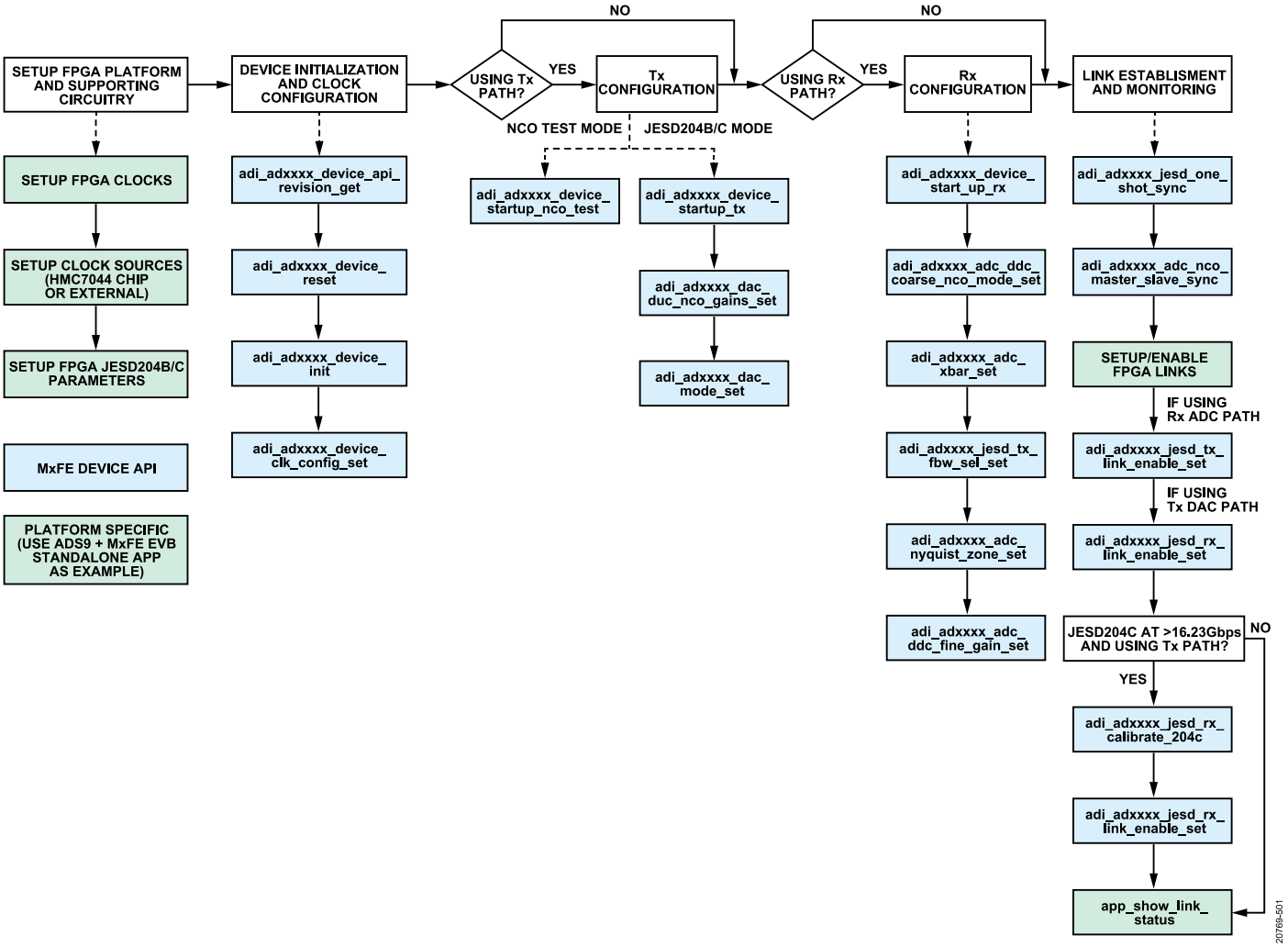

Figure 6. System High Level API Block Diagram

Although the setup flow shown in Figure 6 sets up the majority of the basic functional blocks in MxFE products, there are block level API function calls underneath each high level section. These block level API function calls can be called independently from some of the higher level API calls to tweak settings in various functional blocks of the chip.

Refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later, for each of the four basic functional groups and the input parameters available for user configuration. The source code for all API methods is provided in the API source code package and details how each block configuration is executed.

SERIAL PERIPHERAL INTERFACE

The device is configured using a flexible, synchronous serial communications port, shown in Figure 7, to allow a 3-wire or 4-wire simplified interface with industry standard microcontrollers and microprocessors. An active low input signal at the CSB pin starts and gates a communication cycle used to perform a write or read operation. This input signal must remain low throughout the communication cycle and must return high before returning low again to start a new communication cycle. The SCLK pin synchronizes data to and from the device and runs the internal state machines with all data input appearing on the bidirectional SDIO pin registered on the rising edge of SCLK. All data is driven out of the SDIO pin (or SDO pin for a 4-wire interface) occurring on the falling edge of SCLK during a read operation with the pin going into a high impedance state when the CSB pin returns high. To provide higher noise immunity, the SCLK input features a Schmitt trigger receiver. For timing specifications associated with the SPI port, refer to the device data sheet.

The SPI port is compatible with most synchronous transfer formats to allow a simplified write and read operation to all registers used to configure the device. Register 0x000 is used to configure the SPI, with Bits[7:4] being a mirror image of Bits[3:0]. Before configuring the device, set the self clearing bit, SOFTRESET (Bit 0), to perform a software reset. An LSB first transfer format is supported with the LSBFIRST bit (Bit 1). A multibyte transfer format with an incrementing address is supported with the ADDRINC bit (Bit 2). To enable a 4-wire interface using the SDO pin, set the SDOACTIVE bit (Bit 3) where the SDIO pin is a unidirectional input with the output appearing at the SDO pin.

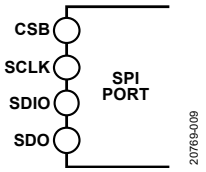

Figure 7. SPI Pins

The default communication cycle with MSB first consists of two phases, as shown in Figure 8. The first phase is the instruction cycle that consists of 16 SCLK cycles that define the operation type and the starting register address. The first bit of the 16-bit instruction word that appears at the SDIO input defines whether the upcoming data transfer is a read or write operation (R/$\overline{W}$). The remaining 15 bits (MSB to LSB format) specify the starting register address for the read or write data transfer operation. For multibyte transfers, the remaining register addresses are generated by the device based on the ADDRINC bit. If this bit is set high, multibyte SPI writes start with the specified address and increment by 1 for every eight bits sent. If the address increment bits are set to 0, the address decrements by 1 for every eight bits sent.

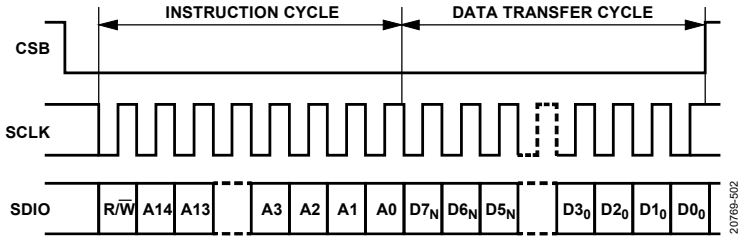

Figure 8. Serial Register Interface Timing, MSB First, Register 0x000, Bit 6 and Bit 1 = 0

The second phase of the communication cycle consists of eight SCLK cycles and is the actual transfer of a data byte between the device and the system controller. To transfer more than one byte (or N + 1 bytes) during the transfer cycle, 8×N SCLK additional cycles are required to ensure that the last byte is transferred. Each time one of the eight clock cycles completes, the internal address index updates such that the next eight data bits transfer to the next register address. Note that a multibyte transfer applies to all registers excluding the registers associated with the transmit and receive digital datapath NCO frequency or phase offset settings. These registers require an additional bit field to be written to such that all NCOs can update simultaneously, if desired, to maintain synchronization.

The SPI port can also support an LSB first data format, as shown in Figure 9, when the LSBFIRST bit is set. In this case, the instruction and data bits must be written from LSB to MSB with the R/$\overline{W}$ bit following the MSB (or A14) of the address word.

SERIAL PERIPHERAL INTERFACE

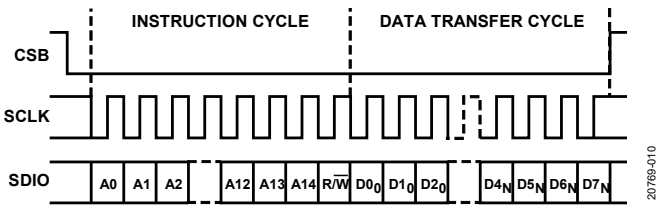

Figure 9. Serial Register Interface Timing, LSB First, Register 0x000, Bit 6 and Bit 1 = 1

For additional details, see the Analog Devices SPI standard.

SPI CONFIGURATION API

The API provides a HAL to allow users to configure the SPI per the end application requirements. Table 2 details the API functions related to reset, SPI configuration, and SPI read and write operations. For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 2. SPI and Reset API Functions

Function	Description
adi_adxxxx_device_init	Device initialization function. The SPI is configured per the user SPI settings defined by the HAL.
adi_adxxxx_device_reset	Device reset function to perform soft or hard reset.
adi_adxxxx_device_spi_register_set	SPI register set function to perform SPI reads per the user SPI operation defined by the HAL.
adi_adxxxx_device_spi_register_get	SPI register get function to perform SPI reads per the user SPI operation defined by the HAL.

SAMPLING CLOCK AND DISTRIBUTION OPTIONS

The DAC and ADC cores use sampling clocks that originate from either an external clock source or an on-chip clock multiplier that consists of an integer PLL circuit and voltage-controlled oscillator (VCO). Consider the internal clock multiplier for all applications where its phase noise meets the requirements of the target system, because use of the clock multiplier simplifies external clock distribution as well as multichip synchronization, if required. If the phase noise requirement cannot be met with the clock multiplier, supply an external clock equal to the desired DAC clock rate.

Figure 10 shows a block diagram of the internal clock multiplier with the clock distribution path that provides both DAC and ADC clocks, as well as a digital block that generates various internal system clocks. Table 3 lists the SPI registers associated with the clock and clock distribution. To access these registers, first set the SPI_EN_D2ACENTER bit field. A differential input clock signal is applied to the clock receiver input pins, CLKINP and CLKINN, to meet the amplitude and frequency requirements stated in the device data sheet. The PLL_BYPASS bit in Register 0x0094 determines if the sampling clock source originates from the external source or the PLL. If the external source is selected, the PLL circuitry automatically powers down if EN_PDPLL_ WHENBYPASS (Bit 4) in Register 0x0094 is set. In either case, the DAC clock is the primary clock and the ADC clock is derived from the DAC clock. The sampling clock passed onto the DAC core must be set to the desired DAC clock rate. The ADC clock is a divided version of the DAC clock with the divider circuit controlled by Register 0x0180. The divider setting of 1, 2, 3, or 4 is set by the ADCDIVN_DIVRATIO_SPI bits, and the ADCDIVN_PD bit provides a power-down option. The user can also export the internal ADC clock to other devices via a differential clock driver.

CLOCK MULTIPLIER

The clock multiplier uses an integer type PLL synthesizer to generate the internal DAC sampling clock. The relation between the DAC clock and the reference clock is as follows:

$$f_{DAC} = \left(f_{CLKIN} \times \frac{(M_{VCO} \times N_{VCO})}{R}\right) / D \quad (1)$$

where:

f_{DAC} is the desired DAC clock rate.

M_{VCO} is the VCO prescaler feedback divider ratio with a value of 5, 7, 8, or 11 (M = 8 is the nominal setting).

N_{VCO} is the VCO feedback divider ratio ranging from 2 to 50.

R is the reference clock divider ratio with a value of 1, 2, 3, or 4. Its value is set such that the phase frequency detector (PFD) frequency (f_{PFD}) operates within a range of 25 MHz to 750 MHz.

f_{CLKIN} is the input frequency of the differential signal appearing across CLKINP or CLKINN.

D is the VCO to DACCLK divider ratio with a value of 1, 2, 3, or 4.

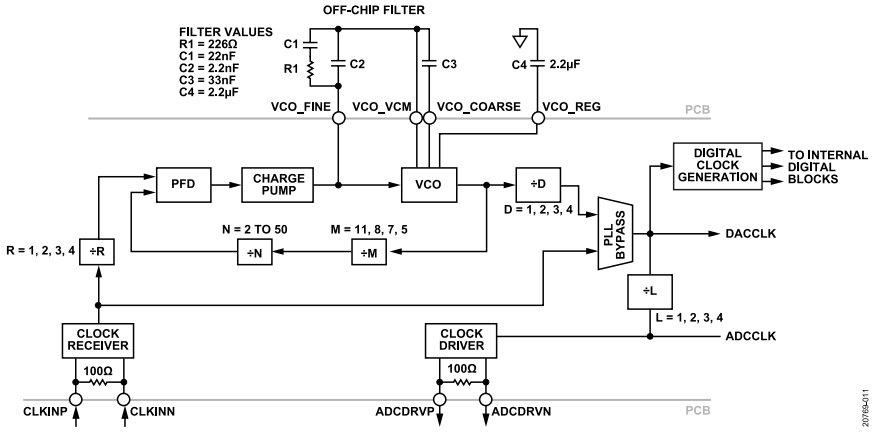

Figure 10. PLL and Clock Distribution Path Block Diagram

The PLL VCO is specified to operate over a frequency range of 5.8 GHz to 12 GHz. The VCO phase noise improves when operating with a lower VCO frequency. When f_{DAC} operation is as low as possible, but above 5.8 GHz, the VCO divider ratio must be at the minimum setting (D = 1), which results in the lowest valid VCO frequency, which is within the VCO specified range. Because the VCO divider does not include a reset capability, its output phase cannot be made deterministic via an external synchronization signal (such as SYSREF) when D > 1.

SAMPLING CLOCK AND DISTRIBUTION OPTIONS

Therefore, sample accurate deterministic latency accuracy or multichip synchronization (MCS) is not possible due to this phase ambiguity when using the clock multiplier PLL with D > 1.

When the PLL divider settings are configured, calibrate the VCO to ensure that a clock source remains stable over the fully specified device operating range. To initiate the VCO calibration, set the D_CAL_RESET bit (Register 0x00E2, Bit 1) high to reset the calibration engine, and then low to trigger the reset. The PLL_ LOCK_SLOW bit and/or the PLL_LOCK_FAST bit in Register 0x2008 can be read after the D_PLL_LOCK_CONTROL bit in Register 0x00EC is set to determine if the PLL has achieved a locked and stable state before proceeding further in the device initialization process.

Referring to Figure 10, the following external passive components are required when using the clock multiplier:

- The PLL loop fine filter that consists of R1, C1, and C2
- The PLL coarse loop filter that consists of C3 set to 33 nF, which does not impact phase noise.
- The VCO regulator bypass capacitor, C4, set to 2.2 µF.

Place these passive components on the back side of the printed circuit board (PCB) in close proximity to the device. If the clock multiplier is powered down, and a direct external clock is applied to the clock receiver input pins, these passive components are not needed. The VCO_COARSE, VCO_FINE, VCO_VCM, and VCO_VREG pins can be left unconnected.

The PLL loop filter and charge pump settings can be customized according to the PFD frequency, reference clock phase noise, and DAC output phase noise requirements. The charge pump output current can be set from 0 mA to 6.3 mA in the 6-bit D_CP_CURRENT bit field of Register 0x00E4, where the default setting is 1.9 mA, and a setting of 11 1111 corresponds to 6.3 mA.

The default charge pump setting with the values shown in Figure 10 results in a phase margin of approximately 80° if the PFD frequency (f_{PFD} = f_{CLKIN}/R) is set to 500 MHz. This setting also corresponds to a PLL loop bandwidth of 295 kHz when operating with a VCO output frequency of 9 GHz. Note that increasing the VCO output frequency to 12 GHz reduces the PLL loop bandwidth to 230 KHz. Doubling the charge pump level results in almost a doubling of the bandwidth that can improve jitter and phase noise performance.

General guidelines for optimizing phase noise performance include the following:

- Use the highest possible f_{PFD} to minimize the contribution of in band noise from the PLL and reference source. Figure 11 shows how the PLL phase noise varies as a function of the f_{PFD}, whereas the loop filter and charge pump values remain constant. Note that the trace corresponding to clock PLL disabled represents the extrapolated phase noise when the clock input is driven from an R&S SMA100B RF generator.
- Set the PLL filter bandwidth such that the PLL in band noise contribution intersects with the VCO open-loop noise contribution, which minimizes the overall combined contribution of both noise sources.

Together with the previous guidelines, general steps for configuring the clock multiplier PLL to obtain the required input reference clock frequency are as follows:

1. The DAC sample clock frequency is the starting point for configuring the clock multiplier PLL. Once this frequency is determined, the other settings can be established. This step is also necessary for ADC only versions. The ADC clock is derived from the internal clock that was used for the DACs.
2. Choose the VCO divider ratio (D), which is set using the PLL_DIVIDEFACTOR bit field. D can be 1, 2, 3, or 4. D must be chosen so that the VCO frequency (DAC sample clock frequency×D) is from 6000 MHz to 12000 MHz. The frequency of the DAC sample clock is (VCO frequency)/D.
3. Choose the ADC clock divide ratio (L), which is set using the ADCDIVN_DIVRATIO_SPI bit field. L can be 1, 2, 3 or 4. The ADC sample clock frequency is the DAC clock frequency/L. If the ADC clock is not needed, the ADC clock divider can be powered down.
4. The loop divider values M and N are then chosen so that M×N is from 10 to 550. M can be 5, 7, 8 or 11 and is set using the D_CONTROL_HS_FB_DIV bit field. N can be any integer from 2 through 50 and is set using the D_DIVIDE_CONTROL bit field. Start with M = 5 and vary N. If the desired characteristics cannot be met with M = 5, change the M value and vary N to find the desired configuration.
5. Choose the reference clock divider ratio (R) value to be 1, 2, 3, or 4. R is set using the D_REFIN_DIV bit field. After R is set, the frequency of the reference clock applied to the CLKINP and CLKINN pins is known.

The frequency of the applied reference clock is represented by the following equation:

$$f_{CLKIN} = \frac{f_{DAC} * D}{M_{VCO} * N_{VCO}} * R \quad (2)$$

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Note that the values contained in the bit fields are not necessarily the same as the value of the parameters they represent. For example, to set L = 1, ADCDIVN_DIVRATIO_SPI must be set to 00, not 01. See Table 3 for more information.

Table 3. PLL Clock Multiplier Registers

Address	Bits	Bit Name	Description
0x00D0	2	SPI_EN_D2ACENTER	Enable SPI access to bit fields associated with PLL.
0x0091	0	ACLK_POWERDOWN	Power down clock receiver.
0x0093	[1:0]	PLL_DIVIDEFACTOR	Programmable divide-by-D value.
0x0094	4	EN_PDPLL_WHENBYPASS	Enable power down of the PLL clock multiplier when the PLL is in bypass mode.
	0	PLL_BYPASS	Enable PLL bypass.
0x0180	4	ADCDIVN_PD	Power down ADC clock divider.
	[1:0]	ADCDIVN_DIVRATIO_SPI	ADC clock divider setting, VCO_L. Divide-by-1 = 00, divide-by-4 = 11.
0x0196	[4:0]	ADC_DRIVER_DATA_CTRL	ADC driver-output voltage swing level control.
0x0198	0	PD_ADC_DRIVER	Power down ADC driver.
0x00E2	1	D_CAL_RESET	VCO calibration.
0x00E3	[1:0]	D_REFIN_DIV	Programmable divide-by-R value.
0x00E4	[5:0]	D_CP_CURRENT	Charge pump current setting.
0x00E9	[5:0]	D_DIVIDE_CONTROL	Programmable divide-by-N_{VCO} value.
0x00EC	[5:4]	D_CONTROL_HS_FB_DIV	Programmable divide-by-M_{VCO} value.
	[2:1]	D_PLL_LOCK_CONTROL	00: no locks enabled. 01: fast lock enabled. 10: slow lock enabled. 11: fast lock, slow clock enabled.
0x2008	1	PLL_LOCK_FAST	High value indicates PLL lock.
	0	PLL_LOCK_SLOW	High value indicates PLL lock.

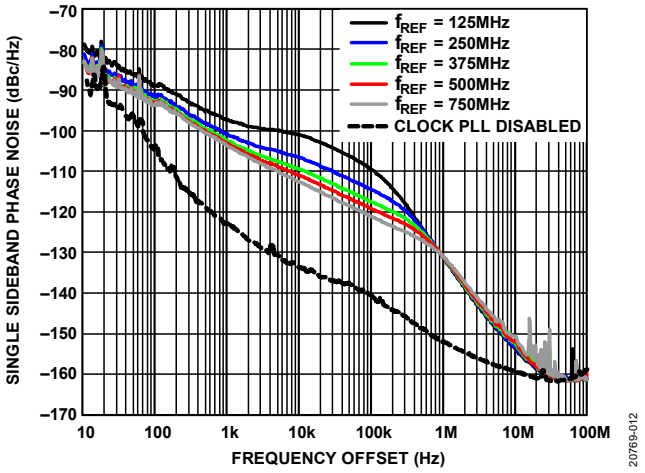

Figure 11. Single Sideband Phase Noise vs. Frequency Offset for Different PLL Reference Clock (f_{PFD}), Output Frequency (f_{OUT}) = 1.8 GHz, f_{DAC} = 12 GSPS, PLL Enabled with Exception of External 12 GHz Clock Input with Clock PLL Disabled

CLOCK RECEIVER INPUT

Figure 12 shows a simplified diagram of the clock receiver input that supports up to 12 GHz operation. The clock receiver input has a self biased input with a nominal common-mode voltage (V_{CM}) of 0.5 V and a differential impedance of 100 Ω across the input pins, CLKINP and CLKINN. To maintain the proper common-mode voltage bias, AC coupling of the external clock source to the clock receiver input is

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recommended. Limit the maximum differential input signal to 1.8 V peak-to-peak, which corresponds to a power level of approximately 6 dBm for a sine wave source. To disable the clock receiver, set the ACLK_ POWERDOWN bit in Register 0x0091.

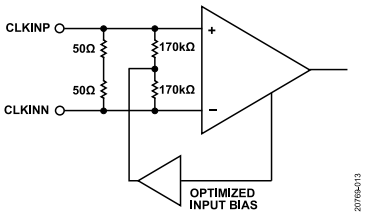

Figure 12. Clock Receiver Input Simplified Equivalent Circuit

The additive jitter and phase noise contribution from the clock receiver depends on the input slew rate and input voltage level. This additive jitter can limit the achievable noise floor performance of a DAC or ADC when operating under large signal conditions with high frequency content. To improve the phase noise performance, use a higher slew rate clock input signal.

Figure 13 shows the phase noise of the clock receiver path for different clock input sine wave drive levels at 12 GHz. The phase noise is measured with the DAC output reconstructing a 1.8 GHz full-scale output signal. The phase noise of the 12 GHz clock source (normalized to 1.8 GHz) is also provided to show the additive phase noise from the device. The plot shows that the drive level mostly impacts the high frequency offset phase noise (> 1 MHz) with drive levels above −3 dBm, resulting in the optimal wide offset performance.

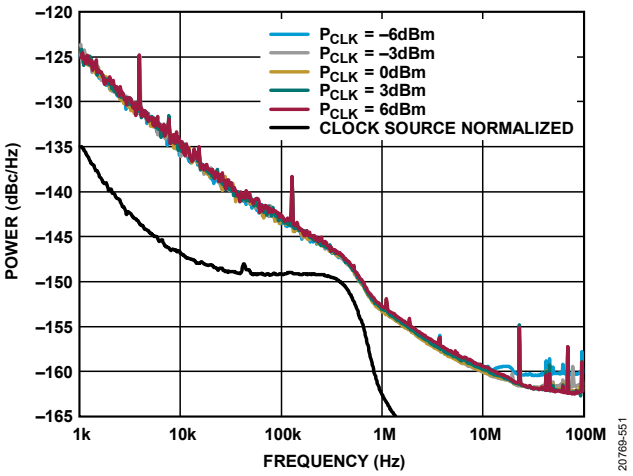

Figure 13. Single Sideband Phase Noise vs. Frequency Offset for Different Clock Input Power (P_{CLK}), f_{OUT} = 1.8 GHz, External 12 GHz Clock Input with Clock PLL Disabled

The quality of the clock source and the interface to the CLKINP pin and CLKINN pin directly impact AC performance. Ensure that the external clock path remains clean of any power supply or PCB coupling induced noise, and select the phase noise and spur characteristics of the clock source to meet the target application requirements.

High speed logic families that provide low voltage positive emitter coupled logic (LVPECL) or current mode logic (CML) output drivers are available on the HMC7044 and LTC6953 clock generation and distribution IC and are preferred because of the low jitter and high slew rates provided. Figure 14 shows an AC-coupled interface with an LVPECL driver. Note that, for a CML driver interface, the 240 Ω resistors must be removed, as shown in Figure 14.

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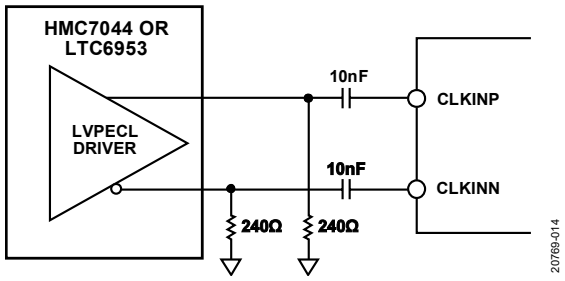

Figure 14. Differential LVPECL Sample Clock

Figure 15 shows the differential input return loss curve for the clock inputs up to 12 GHz with a reference impedance of 100 Ω. The S-parameters are available for download on the AD9081 or AD9082 product page. Consider an S-parameter evaluation using the component models with PCB extraction when optimizing the power transfer between the external clock driver and clock receiver input.

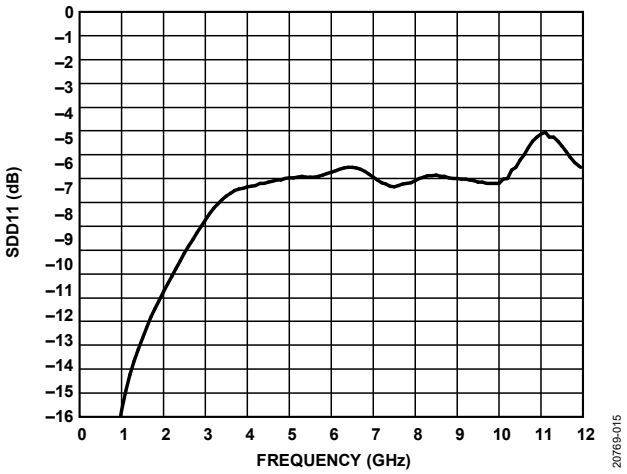

Figure 15. Clock Receiver Differential Input Return Loss

For high RF clock frequency generation beyond 4.5 GHz, a wideband synthesizer IC, such as the ADF5610 or ADF4372, can be used. The ADF5610 and ADF4372 have fundamental VCO modes extending up to 7.3 GHz and 8.0 GHz, respectively, with an internal clock doubler used to synthesize output frequency beyond the fundamental VCO limit. Figure 16 shows a recommended interface when the clock source is a single-ended signal, and a ceramic balun, such as the Mini-Circuits NCR2-113+, is used to convert the single-ended signal to a differential signal. Note that using the ADF5610 results in clock output multiplier spurs in the 30 dB range. Therefore, a band-pass filter may be necessary to attenuate these subharmonics.

Figure 17 shows a differential CML interface using the ADF4372, which is suitable for operation below an 8 GHz output.

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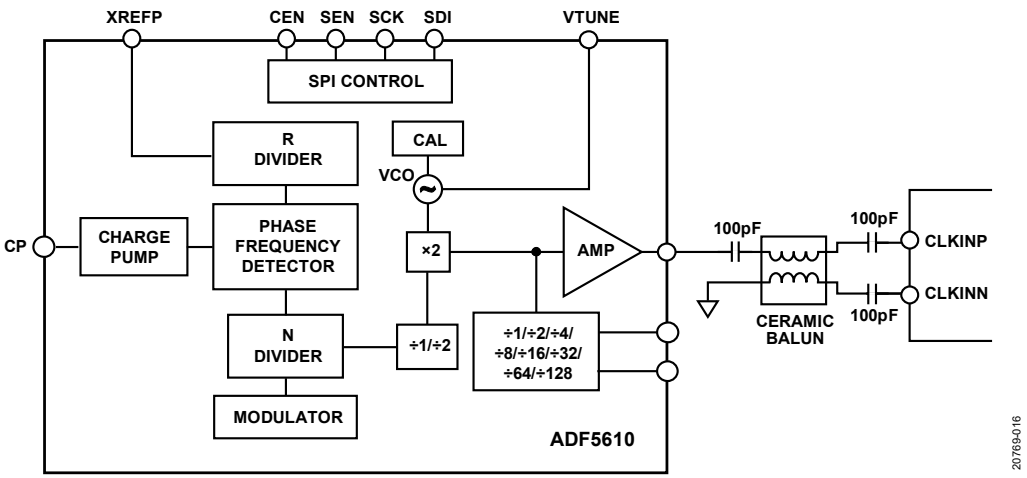

Figure 16. Balun Coupled Differential Clock

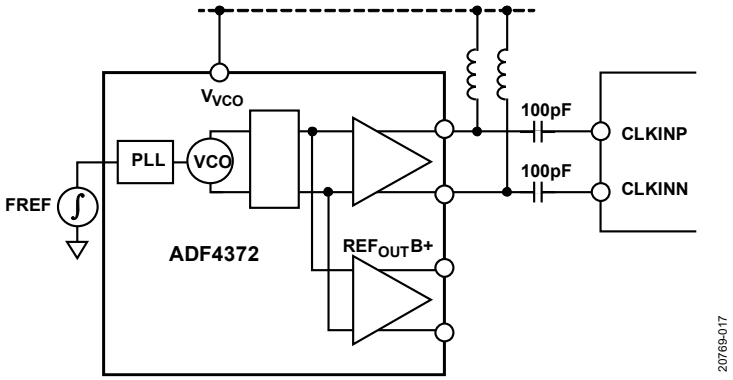

Figure 17. ADF4372 Differential CML Sample Clock

CLOCK OUTPUT DRIVER

An optional differential clock output driver with on-chip 100 Ω termination is available at the ADCDRVP pin and ADCDRVN pin to provide a clock equal to the ADC sample rate, as shown in Figure 10. To power down the output driver, set the PD_ADC_ DRIVER bit in Register 0x0198. The output provides a differential clock output with a nominal common-mode voltage of 0.5 V. The voltage swing level can be varied via the ADC_DRIVER_ DATA_CTRL bit in Register 0x0196 with the voltage swing set according to the following relationship:

Swing = 993 mV − *code*×99 mV

where the code can assume a value of 0 to 20 and an inversion of CLKOUT polarity occurring for codes 11 to 20. The driver output impedance remains relatively constant for different settings.

CLOCK CONFIGURATION APIS

Table 4 lists the API functions related to the configuration and control of the input clock receiver and the clock output driver as described in this section.

The adi_adxxxx_device_clk_config_set function is a high level function that configures the device appropriated per Analog Devices recommended setting, based on the DAC sampling frequency, ADC sampling frequency, and applied reference input of the desired use case clocking scheme. However, if the user wants to configure each block of the input clock receiver, on-chip PLL, and distribution dividers, the APIs are provided in Table 4.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

SAMPLING CLOCK AND DISTRIBUTION OPTIONS

Table 4. Input Clock Receiver and Output Driver Configuration and Control APIs

Function Call	Description
adi_adxxxx_device_clk_config_set	Function to set the input clock receiver per the desired reference clock and sampling clock requirements
adi_adxxxx_device_clk_pll_lock_status_get	Function to get the on-chip PLL status
adi_adxxxx_adc_clk_enable_set	Function to enable/power up the input clock receiver
adi_adxxxx_adc_clk_out_enable_set	Function to enable/power up the clock output driver

JESD204B/C INTERFACE FUNCTIONAL OVERVIEW AND COMMON REQUIREMENTS

The device employs serial interfaces that comply to the JESD204C standard for the ADC and DAC paths, including the JESD204B backward compatible option.

The main differences introduced in the JESD204C standard as employed on this device are the additional 64-bit/66-bit encoding scheme, the respective synchronization process (eliminating the need for the SYNCxOUTB± pins and SYNCxINB± pins), and the recommended operating link rates.

If the 8-bit/10-bit link layer option is selected, the link operation complies to both the JESD204B and JESD204C standards and the link lane rates can be between 1.5 Gbps and 15.5 Gbps. If the 64-bit/66-bit link layer option is selected, the link operation complies to the JESD204C standard, including the new synchronization process (SYNCxOUTB± pins and SYNCxINB± pins are not used), and the link lane rates can be between 6 Gbps and 24.75 Gbps. Table 5 shows the high level differences between using the 8-bit/10-bit and 64-bit/66-bit link layers.

This section of the user guide focuses on the common requirements for the ADC and DAC paths.

NEW FEATURES IN THE JESD204C STANDARD

The following subsections contain an overview of JESD204C specifications that are new or updated when compared to those in the JESD204B standard.

Terminology and Parameters

There are new terms and configuration parameters introduced in the JESD204C standard that are used to describe the functions associated with the 64-bit/66-bit link layer (see Table 6). These terms are detailed throughout the document in the context of the JESD204C transmitter and JESD204C receiver physical, link, and transport layers.

Table 5. Differences Between 8-Bit/10-Bit and 64-Bit/66-Bit Link Layer Operations

Function/Attribute	8-Bit/10-Bit Encoding	64-Bit/66-Bit Encoding
Payload Delivery Efficiency	80% encoding efficiency	96.97% encoding efficiency
SYNCxOUTB± and SYNCxINB± Signal	Yes, from JESD204B receiver to JESD204B transmitter	Not used, entirely feed forward
Link Initialization	Code group synchronization (CGS) + initial lane alignment sequence (ILAS)	Synchronization header alignment, extended multiblock alignment, and extended multiblock alignment achieved using embedded synchronization header stream
Scrambling	Optional (recommended)	Required
Error Monitoring	8-bit/10-bit disparity, not in table (NIT), and unexpected K-characters (UEKC) errors are detected	Cyclic redundancy check (CRC) checks per multiblock of data (2048 bits)
Deterministic Latency and Multichip Sync	Aligned to local multiframe clock (LMFC)	Aligned to a local extended multiblock clock (LEMC)
Lane Rate	1.5 Gbps ≤ lane rate ≤ 15.5 Gbps	6 Gbps ≤ lane rate ≤ 24.75 Gbps

JESD204B/C INTERFACE FUNCTIONAL OVERVIEW AND COMMON REQUIREMENTS

Table 6. New Terms and Parameters Defined in JESD204C

Term	Definition
Block	A structure starting with a 2-bit synchronization header containing 66 bits or 80 bits (*BkW*) total (always 66 bits for the device).
BkW	Block width, the number of bits in a block (always 66 bits for the device).
cmd	Command, as related to the command channel.
Command Channel	Data stream using extra bandwidth afforded from synchronization headers.
E	The number of multiblocks in an extended multiblock.
EMB_LOCK	A state that asserts extended multiblock alignment is achieved.
EoEMB	End of extended multiblock identifier bit (Bit 22 of the synchronization word).
EoMB	End of multiblock sequence (00001), decoded from the synchronization header stream.
Extended Multiblock	A set of data containing one or more multiblocks.
LEMC	Local extended multiblock clock.
Multiblock	A set of data containing 32 blocks.
PCS	Physical coding sublayer.
SH_LOCK	A state that asserts synchronization header alignment is achieved.
Synchronization Header (SH)	Two bits that guarantee a transition precede every block.
Synchronization Transition Bit	Decoded synchronization header (2b'10 = 0, 2b'01 = 1).
Synchronization Word	32 synchronization transition bits from a multiblock.

Physical Layer Updates

The JESD204C physical layer specification and the implementation on the device supports operation with the 8-bit/10-bit (JESD204B) and 64-bit/66-bit (JESD204C) link layers.

JESD204C introduces data interface classes and defines two categories of classes, Category B and Category C. There are three classes defined for each category. Table 7 lists the lane rates associated with each category. For Category C, there are three subclasses defined to minimize link power dissipation for a variety of channel types: C-S (short), C-M (medium) and C-R (reflective). Each class is a superset of the previous class. Table 8 lists the architectural differences between the classes. The device implements a class C-M interface on both the ADC and DAC paths, although the lane rate is limited to 1.5 Gbps on the low end (when employing 8-bit/10-bit encoding) and 24.75 Gbps on the high end (when employing 64-bit/66-bit encoding).

Table 7. Lane Data Rates for Data Interface Classes

Data Interface Class	Minimum Data Rate (Gbps)	Maximum Data Rate (Gbps)
B-3	0.3125	3.125
B-6	0.3125	6.375
B-12	6.375	12.5
Category C	6.375	32

Table 8. JESD204C 32 Gbps Interface Device Class Features

Class	Relative Power	Tx FFE[1] (dB)	Rx CTLE[2] (dB)	Rx DFE[3] (No. of Taps)
C-S	Low	9.5	6	0
C-M	Medium	9.5	9	3
C-R	High	9.5	12	14

[1] FFE is feedforward equalization.

[2] CTLE is continuous time linear equalizer.

[3] DFE is decision feedback equalizer.

Transport and Link Layer

The transport layer provides mapping between converter samples and octets. The 8-bit/10-bit and the 64-bit/66-bit link layers use the same octet format and there is no difference in the transport layer that depends on the encoding scheme.

The only difference between using the two encoding schemes is that the octets sent to the 64-bit/66-bit link layer must be scrambled. For the 8-bit/10-bit link layer, scrambling is optional.

JESD204B/C INTERFACE FUNCTIONAL OVERVIEW AND COMMON REQUIREMENTS

When using the 8-bit/10-bit link layer option of JESD204C, the device is fully compatible with the JESD204B specification and all that the specification implies. These implications include the use of K28 characters for CGS, ILAS, and character replacement as well as the SYNCxOUTB± pins and SYNCxINB± pins used to initiate synchronization and report errors from the receiver back to the transmitter.

When operating with 64-bit/66-bit encoding, the use of the SYNCxOUTB± pins and SYNCxINB± pins is eliminated and there is no compatibility with JESD204B. There is no encoding of the octets. The octets are packed into a 64-bit block of data. The entire block is then scrambled and has a 2-bit synchronization header appended. This format is shown in Figure 18, where D[0:7] represents the eight data octets, S[0:7] represents the scrambled octets, and SH is the 2-bit synchronization header.

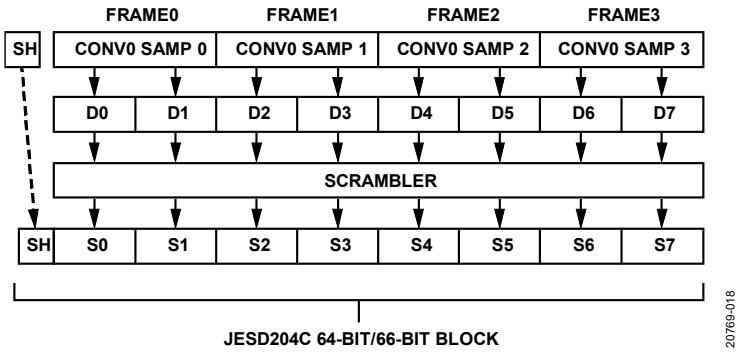

Figure 18. 64Bbit/66-Bit Block Format Example for LMFS = 1.1.2.1, N = N' = 16

The synchronization header is a 2-bit, unscrambled value at the beginning of each block. The header contents are interpreted to decode a single synchronization transition bit. The synchronization header bits must be either a 0 to 1 sequence to indicate a Logic 1 or a 1 to 0 sequence to indicate a Logic 0.

Table 9 shows the synchronization header and synchronization transition bit values.

Table 9. Synchronization Header Bit Values

Synchronization Header Bits[0:1]	Synchronization Transition Bit Value
00	Invalid
01	1
10	0
11	Invalid

Multiblocks (MB) and Extended Multiblocks (EMB)

There are 32 blocks in a JESD204C multiblock. The 32 synchronization transition bits in each multiblock make up a 32-bit synchronization word. The functions within the synchronization word are described in the Synchronization Word section. An extended multiblock is a container of E multiblocks and must contain an integer number of frames. When a multiblock does not contain an integer number of frames, E must be >1. Figure 19 shows the format of the multiblock and extended multiblock.

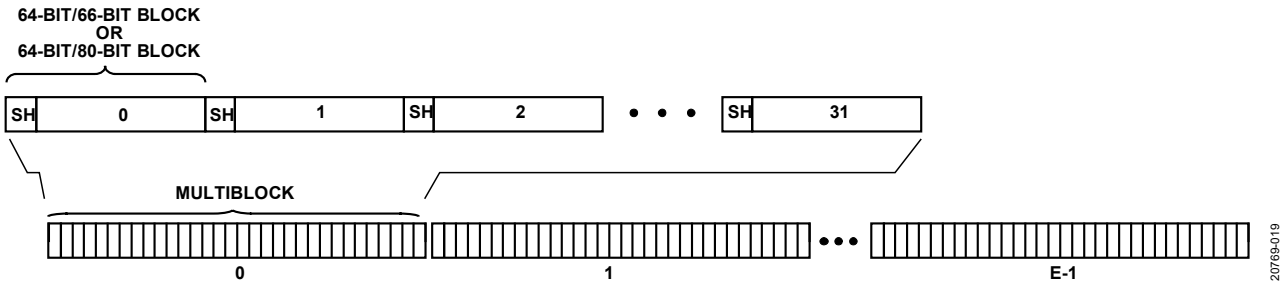

Figure 19. JESD204C Multiblock and Extended Multiblock Format

JESD204B/C INTERFACE FUNCTIONAL OVERVIEW AND COMMON REQUIREMENTS

The JESD204C standard supports a multiblock that is either 2112×(32×66) bits or 2560×(32×80) bits, depending on which 64-bit encoding scheme is used. A multiblock in the AD9081 and AD9082 is always 2112 (32×66) bits because 64-bit/ 80-bit encoding is not supported. For most implementations and configurations, an extended multiblock is one multiblock.

The E parameter is introduced in JESD204C and determines the number of multiblocks in the extended multiblock. The default value for E is 1. E must be > 1 for configurations where the number of octets in the frame (F) is not a power of two and is typically associated with modes where NP = 12.

This requirement ensures that the extended multiblock boundary coincides with a frame boundary.

The equation for E is given as the following:

$E = (K \times F)/256$

when 256 mod F != 0

E must be an integer and the number of frames in a multiframe (K) must be set appropriately.

LEMC is the local extended multiblock counter and is roughly equivalent to the LMFC in the 8-bit/10-bit link layer. The SYSREFN and SYSREFP input signal aligns all LEMCs in a system and the LEMC boundaries are used to determine synchronization and lane alignment.

Synchronization Word

The 32-bit synchronization word is constructed from each of the sample headers from the 32 blocks within the multiblock where Bit 0 is transmitted first. The synchronization word is used to enable lane synchronization, error detection, and deterministic latency.

There are seven bits (CMD, Bits[6:0]) that provide a command channel for the transmitter to communicate to the receiver. However, this command channel is not supported on the AD9081 and AD9082 and these bits are always zeros for the device.

Table 10 describes the different synchronization word fields and functions.

Table 10. Synchronization Word Fields and Functions

Synchronization Word Bit	Bit Name	Function
0	CRC11	Bits[11:9] of the 12-bit CRC check applicable to the previous multiblock.
1	CRC10	
2	CRC9	
3	1	Always 1.
4	CRC8	Bits[8:6] of the 12-bit CRC check applicable to the previous multiblock.
5	CRC7	
6	CRC6	
7	1	Always 1.
8	CRC5	Bits[5:3] of the 12-bit CRC check applicable to the previous multiblock.
9	CRC4	
10	CRC3	
11	1	Always 1.
12	CRC2	Bits[2:0] of the 12-bit CRC check applicable to the previous multiblock.
13	CRC1	
14	CRC0	
15	1	Always 1.
16	Cmd6	Bits[7:5] of the 7-bit command channel (not supported, always 0).
17	Cmd5	
18	Cmd4	
19	1	Always 1.
20	Cmd3	Bit 3 of the 7-bit command channel.
21	1	Always 1.
22	EoEMB	End of extended multiblock bit.
23	1	Always 1.

Table 10. Synchronization Word Fields and Functions (Continued)

Synchronization Word Bit	Bit Name	Function
24	Cmd2	Bits[2:0] of the 7-bit command channel.
25	Cmd1	
26	Cmd0	
27	0	End of multiblock pilot signal.
28	0	
29	0	
30	0	
31	1	

CRC-12 Encoder

The CRC-12 encoder in the JESD204C transmitter takes in the 2048 scrambled data bits of each multiblock and computes 12 parity bits. These parity bits are transmitted to the receiver during the subsequent multiblock.

The receiver computes 12 parity bits from each multiblock of data received. The 12 bits are compared to the bits that were received over the command channel. If the parity bits do not match, there is at least one error in the received data. See the 64-Bit/66-Bit Link Establishment Overview section for details.

8-BIT/10-BIT LINK ESTABLISHMENT OVERVIEW

When using the 8-bit/10-bit link layer, the link establishment process follows the protocol established in the original JESD204B/C standard (and subsequent versions). Using K28 characters and the SYNC~ signals, the link first establishes CGS, then frame synchronization (FS) and ILAS prior to transmitting sample data in the user data phase.

During the user data phase, character replacement (inserting K28.x characters) is used to monitor frame and multiframe alignment while an error checking circuit in the JESD204B/C receiver monitors incoming data for 8-bit/10-bit errors (running disparity, NIT, UEKC). Details are not provided because this protocol is well established. For more details, refer to the Analog Devices webcast on the JESD204B data link layer.

64-BIT/66-BIT LINK ESTABLISHMENT OVERVIEW

The link establishment process when using the 64-bit/66-bit link layer starts automatically when the link is powered on. The SYNC~ signal, or synchronization request, is not required. The process begins with synchronization header synchronizations, then progresses to extended multiblock synchronization, and then to extended multiblock alignment. Details on the 64-bit/66-bit link establishment process can be found in the 64-Bit/66-Bit Link Layer and Link Establishment section.

SERDES PLL AND CONFIGURATION

Because the JESD204B/C receiver and transmitter share the SERDES PLL, consider the following during PLL configuration:

- JESD204B/C receiver and transmitter modes must be selected such that the corresponding lane rates remain equal or that the lane rate of the JESD204B/C transmitter is a power of 2 divisor of the lane rate of the JESD204B/C receiver. In the latter case, the bit repeat option of the JESD204B/C transmitter (JTX_BR_LOG2_RATIO. Registers 0x0670 to Register 0x0677) must be enabled for every lane in use. (see the Configuring the JESD204B/C Transmitter Link section and JESD204B/C Transmitter Mode Tables section for details).
- If operating the transmit path only or both the transmit and receive paths, the initial SERDES PLL configuration steps are automatically performed according to the JESD204B/C configuration mode and total interpolation, which define the rate of the various clock domains internal to the device, as described in the JESD204B/C Transmitter Clock Relationships section. The specific register bits for these settings are JESD_MODE (Register 0x01FE, Bits[5:0]), COARSE_INTERP_SEL (Register 0x01FF, Bits[7:4]), and FINE_INTERP_SEL (Register 0x01FF, Bits[3:0]).
- If operating the receive path only, set the PLL reference clock period manually to perform the initial SERDES PLL configuration steps. To set the clock period, set the SDSPLLREFCLK_DIV_RATIO_SPI bit field to be enabled by the SDSPLLREFCLK_DIV_SPI_EN bit (Register 0x00CA, Bits[5:0] and Register 0x00CA, Bit 7, respectively).
- For receive path only operation, set the bit repeat function of the JESD204B/C transmitter according to the JTX_BR_ LOG2_RATIO register description when the lane rate is less than or equal to 8 Gbps.

When setting SDSPLLREFCLK_DIV_RATIO during PLL configuration, use the following guidelines:

JESD204B/C INTERFACE FUNCTIONAL OVERVIEW AND COMMON REQUIREMENTS

- If the JESD204B/C parameter F = power of 2, Register 0x00CA, Bits[5:0] = 4×(PCLK/f_{DAC}) – 1
- If the JESD204B/C parameter F ≠ power of 2, Register 0x00CA, Bits [5:0] = 4×(PCLK/(3×f_{DAC}) – 1

where:

PCLK = lane rate/40 for 8-bit/10-bit encoding

PCLK = lane rate/66 for 64-bit/66-bit encoding

Regardless of which paths are being operated, additional SERDES PLL settings are necessary to complete the configuration. The first set of register writes are to the PLL control bus (PLL_CBUS) register map and therefore, each register setting requires a sequence of register writes to the main register map. For Register 0x740, Register 0x741, and Register 0x72F of the main register map to provide access to the PLL_CBUS registers that are detailed in Table 12, perform the following steps:

- Write CBUS_ADDR_LCPLL (Register 0x740, Bits[7:0]) to the appropriate DESER_CBUS register address as described in Table 12.
- Write CBUS_WDATA_LCPLL (Register 0x741, Bits[7:0]) to the appropriate value as described in Table 12 based on the insertion loss of the PCB trace.
- For each deserializer lane requiring the value written to Register 0x407, set the appropriate bits in CBUS_ WSTROBE_LCPLL (Register 0x72F, Bits[7:0]) to 1.
- Write CBUS_WSTROBE_LCPLL (Register 0x72F, Bits[7:0]) back to 0x00 to reset the strobe.

The register PLL_CBUS writes described in Table 11 are supported in the device API as described in Table 13.

Table 11. LCPLL Registers and Settings

Register Map	Address	Bits	Setting
PLL_CBUS	0x8D	[7:0]	0x64
PLL_CBUS	0x8E	[7:0]	0xAC
PLL_CBUS	0x93	[7:0]	0x54
PLL_CBUS	0xB1	[7:0]	0x20
PLL_CBUS	0xB2	[7:0]	0x02
PLL_CBUS	0xB5	[7:0]	0x83
PLL_CBUS	0xB6	[7:0]	0x70
PLL_CBUS	0xD3	[7:0]	0x10
PLL_CBUS	0x8C	[7:0]	0x35

The second set of register writes are to the main register map and depend on whether the 8-bit/10-bit or the 64-bit/66-bit link layers are being used and at what lane rate the link is operating. These setting are specified in Table 12. After all requisite register writes are made, the last step in the SERDES PLL configuration process is to power up the PLL. To power up the PLL, set the PWRUP_LCPLL bit (Register 0x0721, Bit 0) to 1. These register writes are performed as part of the adi_adxxxx_jesd_rx_pll_startup function in the device API as described in Table 13.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Table 12. SERDES PLL Registers and Settings

		Register Setting per Lane Rate Range (Gbps)[1]							
		JESD204B				JESD204C			Reset
Address	Bits	1.0 to 2.0	2.0 to 4.0	4.0 to 8.0	8.0 to 15	6.0 to 8.0	8.0 to 16	>16	
0x0727	6	0	0	0	0	1	1	1	0
	[5:4]	1	1	1	1	1	1	0	2
	[2:0]	0	0	0	0	0	0	1	2
0x072D	1	0	0	0	0	0	0	0	0
0x072A	3	1	1	1	1	1	1	1	0
0x072B	[3:0]	2	1	0	8	0	8	8	8
0x0728									
F = 3×n	[7:0]	N/A	N/A	30	15	N/A	33	33	0
Else	[7:0]	40	20	10	5	22	11	11	0
0x0726	0	0	0	0	0	0	0	0	0

[1] N/A means not applicable.

SERDES PLL Configuration API

The configuration of the SERDES PLL as documented in this section are handled by the top level API functions, adi_adxxxx_ startup_tx and adi_adxxx_startup_rx. The APIs configure the recommended SERDES PLL configuration based on the receive and transmit mode information, and the JESD receive and transmit interface parameters are configured by the user application. In addition, it requires the clocking information to be set by the adi_adxxx_device_clk_config_set function. Table 13 lists the functions relating to the SERDES PLL configuration.

Note these functions return an error if the SERDES PLL fails to lock. The user can also explicitly check the status of the SERDES PLL by using the adi_adxxxx_jesd_pll_lock_status_get function.

Table 13. JESD204B/C SERDES PLL API Functions

Function Call	Description
adi_adxxxx_device_startup_tx	Function for full transmit path configuration
adi_adxxxx_device_startup_rx	Function for full receive path configuration
adi_adxxxx_device_clk_config_set	Function for device clock configuration
adi_adxxxx_jesd_pll_lock_status_get	Function to get status of SERDES PLL

SYSREF AND SUBCLASS 1 OPERATION

The device has a JESD204B/JESD204C Subclass 1 compatible SYSREF± input that provides flexible options for synchronizing the internal device blocks.

To synchronize the input clock divider, NCOs, DDCs, DUCs, signal monitor block, and JESD204B/C link, use the SYSREF± input. Subclass 1 operation using SYSREF± input aligns the LMFC/LEMC signals in both the transmitter and receiver in a JESD204B/JESD204C Subclass 1 system and results in deterministic latency from one power cycle to the next. Subclass 1 operation can also be used as a mechanism to achieve multichip synchronization. Figure 20 is a block diagram that illustrates the chip level SYSREF synchronization features and adjustments that can be used to achieve the most accurate synchronization possible.

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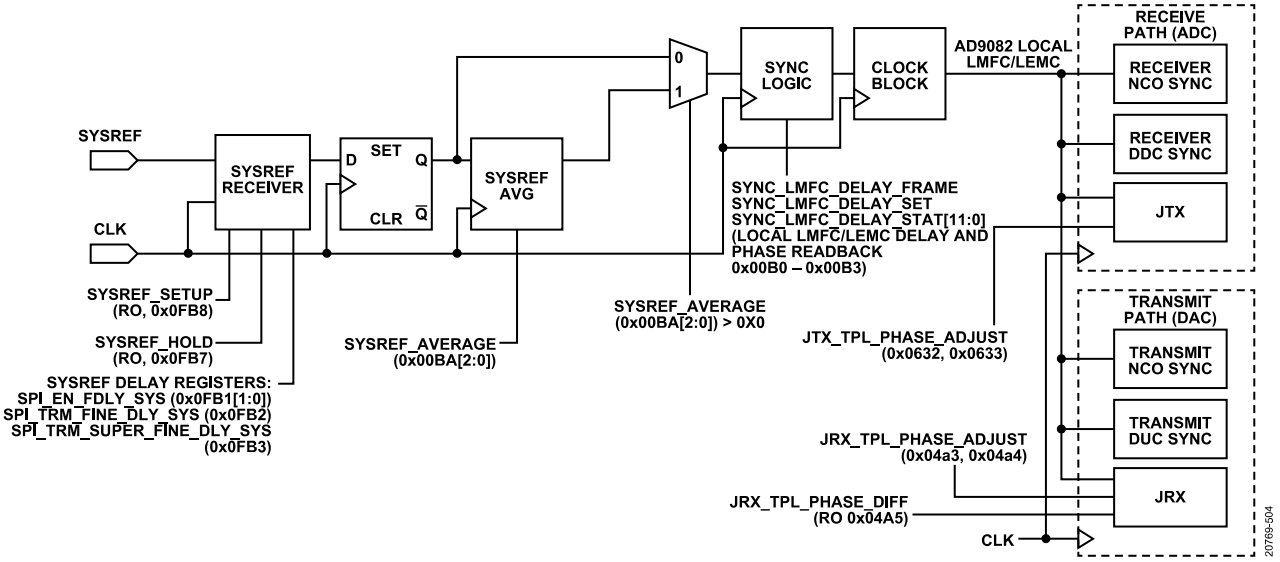

Figure 20. Chip Level Synchronization Block Diagram

SYSREF Receiver Input and Interface Options

The SYSREF receiver input shown in Figure 21 supports dc-coupled or ac-coupled interfaces to high speed differential output sources, such as LVPECL, CML, HSTL, and LVDS, as well as DC coupling to single-ended CMOS logic sources. For applications that require precise synchronization to an external trigger event or multichip synchronization, use clock generation ICs, such as the HMC7044 or LTC6952, with differential LVPECL or CML drivers. Use this method to achieve the lowest jitter performance between the generated clock reference and SYSREF output signals, as well as the fastest rise and fall time characteristics to ensure sample accurate timing accuracy.

Note that a dc-coupled LVPECL interface must include 150 Ω bias resistors to ground on each of the driver output pins.

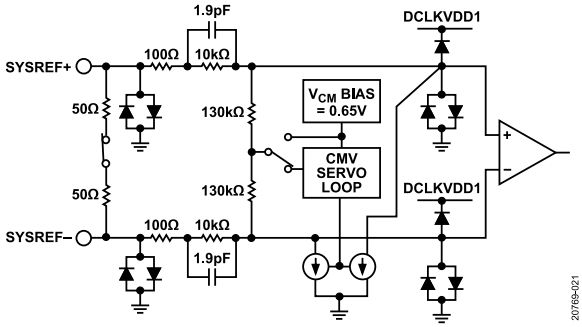

Figure 21. SYSREF± Receiver Block Diagram

Table 14 lists the SPI control fields and locations used to configure the SYSREF input receiver. Note that the SPI_EN_D2ACENTER bit must be set before configuring other bits in the table.

To configure the SYSREF input applications using Subclass 1 that only desire synchronization among the internal transmit and receive datapaths and the SERDES links within a single device can generate a phase coherent, synchronous SYSREF signal from the host processor. The pulse width of the SYSREF input signal must exceed four clock periods of the CLKIN input signal, such that the SYSREF input signal is registered by a rising edge of the CLKIN± input signal. Acceptable output drivers to generate this synchronous SYSREF input signal include an LVDS or a single-ended CMOS. Applications that prefer Subclass 0 synchronization (or have no synchronization requirements) can leave the SYSREF± pins open while powering down the internal receiver and synchronization circuitry by setting the SPI_SYSREF_EN bit to 0 and the SYSREF_PD bit to 1 to power down the SYSREF block. Note that, even in Subclass 0, some internal synchronization is still required using a one shot sync as described in this section. In Subclass 0 mode, the one shot sync pulse is provided internally instead of an external SYSREF signal based on the arbitrary phase of the LMFC/LEMC.

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The SYSREF_INPUTMODE bit is set according to the coupling method employed on the hardware with a 0 or 1 setting corresponding to DC coupling or AC coupling, respectively. The input voltage swing ranges either from 0.2 V p-p to 2 V p-p for a differential interface, or from 0.9 V p-p to 1.8 V p-p for a DC, single-ended, CMOS interface.

Table 14. SYSREF Input Receiver Control Registers

Register	Bits	Bit Name	Description	Reset	Access
0x00D0	2	SPI_EN_D2ACENTER	Enable access to control register ranges from 0x195 to 0x19F, and 0xF60-oxFBA. During normal operation, set this bit to zero to limit SPI clock corruption of the sample clock.	0x1	R/W
0x0198	1	SEL_ADC_CLK_DRIVER	Single-ended, common-mode voltage control 0: SysrefN normal mode 1: SysrefN common mode set by 10KΩ resistor to supply and shunt resistor to ground controlled by SYSREF_SINGLE_END_N.	0x0	R/W
0x019A	6	SYSREF_INPUTMODE	If SYSREF_SINGLE_END_MODE_SEL=0 0: disable internal 100ohm differential. 1: internal 100ohm differential. X: if sysref_single_end_mode_sel = 1.	0x0	R/W
	0	SYSREF_PD	Power down the SYSREF receiver and sync circuitry.	0x0	R/W
0x0FB0	3	SPI_SYSREF_EN	Enables sysref capture	0x0	R/W
0x0FB9	4	SYSREF_SINGLE_END _MODE_SEL	0: disconnect internal termination from ground 1: connect internal termination to ground (see Figure 22)	0x0	R/W
	0	SYSREF_DC_MODE_SEL	If not internally resistively biased (SYSREF_SINGLE_END_MODE_SEL = 0), 0: AC mode level shifter enabled-AC couple 1: DC mode level shifter enabled-DC couple	0x1	R/W
0x0FBA	7:4	SYSREF_SINGLE_END_N	SYSREF N Internal termination = 6.3kΩ to ground if sysref_single_end_mode_sel = 0	0x1	R/W
	3:0	SYSREF_SINGLE_END_P	SYSREF P Internal termination = 6.3kΩ to ground if sysref_single_end_mode_sel = 0	0x1	R/W

For AC-coupled differential interfaces, set the SYSREF_ INPUTMODE bit to 1 to enable the common-mode servo loop. This action forces the common-mode voltage (measured across the receiver amplifier input via the 130 kΩ resistors) to be equal to an internal common-mode reference voltage of approximately 0.65 V, which sets the allowable input common-mode level range from 0.6 V to 2.2 V. The servo loop controls a pair of common-mode current sources tied to each amplifier input with the current scaled to create symmetrical DC voltage drops across the pair of 10 kΩ series resistors. The upper limit of each current source is approximately 1.6 mA to allow an upper input common-mode range of 2.2 V. The sum of the two current sources creates a common-mode current of up to 3.2 mA that is sourced by the differential driver.

For AC-coupled differential interfaces, the common-mode servo loop must remain disabled with SYSREF_INPUTMODE = 1. In this case, the 130 kΩ resistors are connected to the 0.65 V reference voltage to provide the desired bias voltage for the receiver input. The SYSREF input signal applied to the external DC blocking capacitors must be near 50% of the duty cycle periodic signal (or burst long enough to charge capacitors to a steady state). Note that the pair of capacitors (C) combined with the internal differential termination resistor (R) create a high-pass filter with a cutoff frequency of $1/(\pi \times C \times R)$ with R being a nominal 100 Ω.

Select the value of C such that the cutoff frequency of the high-pass filter is less than ¼ of the periodic SYSREF input signal frequency. The edge rate must be fast enough to allow the SYSREF sampling clocks to properly sample the rising SYSREF edge before the next sample clock.

For a single-ended CMOS interface, disable the internal differential input resistive load. To disable the load, set the SYSREF_SINGLE_END_MODE_SEL bit. Use an external resistive divider to step down the output voltage swing if the CMOS driver can exceed a 1.8 V output, as shown in Figure 22, using the R1 and R2 resistors. For DC coupling pulsed SYSREF from clock drivers such as the LTC6952 and LTC6953, which have a common mode voltage mismatch with the device SYSREF input, use the configuration in Figure 23.

JESD204B/C INTERFACE FUNCTIONAL OVERVIEW AND COMMON REQUIREMENTS

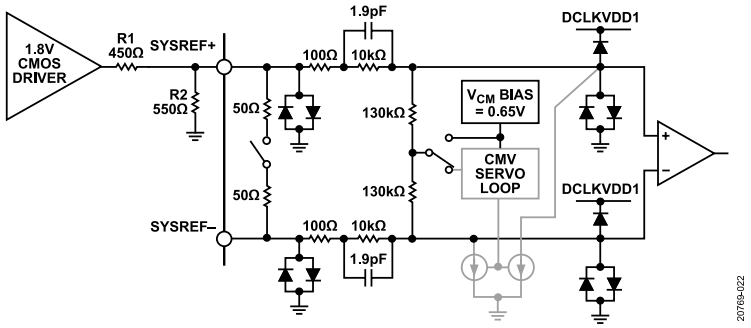

Figure 22. DC-Coupled CMOS Input

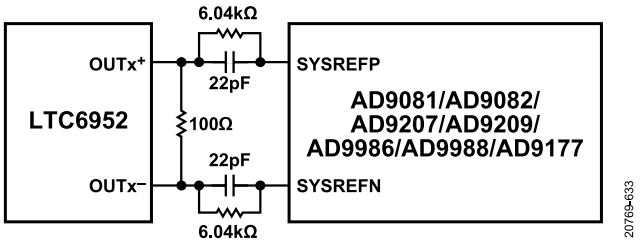

Figure 23. DC-Coupled Connection to LTC6952

Place the five components (100 Ω, 22 pF, and 6.04 kΩ) as close as possible to the AD9081/9082/9207/9209/9986/9988/9199 SYSREF inputs.

These component values are valid for driving pulsed SYSREF with the LTC6952 or LTC6953. Other SYSREF drivers with CML outputs can use a similar configuration, but the parallel RC values may need to change.

This configuration is not for continuous SYSREF applications. Continuous SYSREF mode requires AC coupling and can use the on-chip differential 100Ω termination within the device. For the configuration in Figure 23, use the settings in Table 15.

Table 15. Bitfield Settings for DC Coupling Pulsed SYSREF to LTC6952/3

Address	Bits	Bitfield Name	Settings	Description
0x0198	1	SEL_ADC_CLK_DRIVER	0	Single-ended, common-mode voltage control 0: SYSREFN normal mode
0x0FBA	3:0	SYSREF_SINGLE_END_P	0001	Sets 6.3kΩ internal termination on SYSREF P side to ground.
0x0FBA	7:4	SYSREF_SINGLE_END_N	1111	Sets 6.3kΩ internal termination on SYSREF N side to ground.
0x0FB9	4	SYSREF_SINGLE_END_MODE_SEL	1	
0x0FB9	0	SYSREF_DC_MODE_SEL	0	DC-coupled for connection to CML drivers, as shown in Figure 23.
0x019A	6	SYSREF_INPUTMODE	X	

SYSREF Modes

The device supports a single pulse or periodic SYSREF signal. The periodicity can be continuous, strobed, or gapped periodic. Note that only the next occurring SYSREF edge after enabling SYSREF_MODE_ONESHOT (Register 0x00B8, Bit 1 = 1) initiates the synchronization of the internal clocks, which remains true when providing a periodic SYSREF signal. See the SYSREF Setup/Sync Procedure section for details on the one shot sync procedure.

If providing a continuous SYSREF signal, ensure that the SYREF frequency is an integer submultiple of the LEMC (if in JESD204C mode) or the LMFC (if in JESD204B mode). If using the internal PLL as described in the Clock Multiplier section (PLL_BYPASS = 0), the SYSREF period must also be a common multiple of the input clock (CLKIN) period and the LMFC/LEMC period.

The LEMC frequency of the JESD204C receiver can be calculated using one of the following formulas:

$LEMC = Lane\ Rate/(E \times 2112)$

$LEMC = (DACCLK)/(S \times K \times Interp)$

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LEMC = (*M*×*NP*×*DACCLK*)/(2048×*L*×*E*×*Interp*)

where:

L, *M*, *NP*, and *E* are JESD204C parameters.

Interp is the total interpolation of the transmit data path.

To calculate the LEMC of the JESD204C transmitter, simply substitute ADCCLK for DACCLK and DCM for Interp. DCM is the total decimation of the receive datapath.

The LMFC frequency can be calculated using the following formula:

LMFC = (*DACCLK*)/(*S*×*K*×*Interp*)

where:

S and *K* are JESD204B parameters.

Interp is the total interpolation of the transmit data path.

To calculate the LMFC of the JESD204B transmitter, simply substitute ADCCLK for DACCLK and DCM for Interp.

If a delay is desired between enabling one shot mode and the synchronization, use the SYSREF_COUNT register (Address 0x00B4) to program the delay. This register sets the number of SYSREF edges to ignore before synchronizing. When one shot synchronization is complete, the SYSREF_MODE_ONESHOT bit self clears (Register 0x0B8, Bit 1 = 0). The ONESHOT_SYNC_ DONE bit (Register 0x00B8, Bit 4) goes high and the device enters SYSREF monitor mode automatically to monitor the phase of the incoming SYSREF signal.

SYSREF Monitor Mode

The device enters SYSREF monitor mode automatically when the one shot synchronization completes. To retrieve the 13-bit SYSREF_PHASE value, read Register 0x00B6, Bits[4:0] (SYSREF_ PHASE, Bits[12:8]) and Register 0x00B5 (SYSREF_PHASE, Bits[7:0]). This read verifies the phase relationship between the incoming SYSREF signal relative to the internal LMFC/LEMC boundaries. Note that the value read back after one shot sync completes reflects the phase of the most recent SYSREF leading edge occurring at the SYSREF± input pins prior to initiating the read back.

A readback of 0 indicates that SYSREF and LMFC/LEMC are aligned. A nonzero value such as 10, for example, indicates that the SYSREF rising edge is 10 cycles of the DAC clock later than the internal LMFC/ LEMC. Note that the SYSREF_PHASE registers are read only registers. These registers do, however, require a write strobe to trigger a value update. Write any value to these registers before reading them to get an accurate phase reading.

SYSREF Error Window

Alignment between the SYSREF and the LMFC/LEMC is monitored using the SYSREF_WITHIN_LMFC_ERRWINDOW bit (Register 0x00B7, Bit 7). The SYSREF_ERR_WINDOW bits (Register 0x00B7, Bits[6:0]) set how much SYSREF jitter or drift can be tolerated by the system.

Register 0x00B7 is set in units of DAC clocks. Figure 24 shows the relation between the SYSREF_ERROR_WINDOW setting, the DAC clock, and the SYSREF (averaged or sampled). As long as the SYSREF is aligned to the internal LMFC/LEMC reference to within the limits set in the SYSREF_ERR_WINDOW register, the SYSREF_WITHIN_LMFC_ERRWINDOW bit is set to 1. If the value is outside this limit, the value is 0.

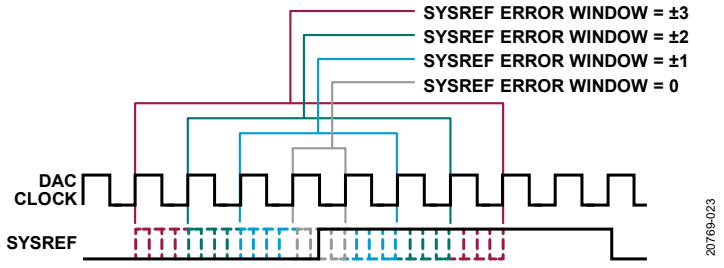

Figure 24. SYSREF_ERROR_WINDOW Setting Example

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Either the SYSREF_WITHIN_LMFC_ERRWINDOW bit can be polled by the system sl controller, or an interrupt can be enabled using the EN_SYSREF_IRQ bit (Register 0x0020, Bit 2). If the EN_SYSREF_IRQ bit = 1 and the monitored SYSREF (SYSREF jitter) is not within the limits set by the SYSREF_ERR_WINDOW bits, the IRQ_SYSREF_JITTER bit (Register 0x0026, Bit 2) latches and pulls the IRQB_x pin low (x = MUX_SYSREF_JITTER bit setting).

To clear the IRQ_SYSREF_JITTER bit, write a 1 to the bit when latched. To route the interrupt to the GPIOx pins, set the MUX_ SYSREF_JITTER bit (Register 0x002C, Bit 2) to 1 as well.

If the EN_SYSREF_IRQ bit is 0, the IRQ_SYSREF_JITTER bit shows the current status, similar to the function of the SYSREF_WITH-IN_LMFC_ERRWINDOW.

SYSREF Sampling Modes

The device incorporates two continuous SYSREF operating modes, single SYSREF mode and averaged SYSREF mode. The SYSREF_AVER-AGE bits (Register 0x00BA, Bits[2:0]) are used to select between these modes.

Single (Sampled) SYSREF Mode

The SYSREF_AVERAGE bits (Register 0x00BA, Bits[2:0]) set the SYSREF mode. By default, single sampled SYSREF mode is enabled (Register 0x00BA, Bits[2:0] = 0x0). In this mode, the SYSREF operates as a standard JESD204B/JESD204C Subclass 1 signal. Single and averaged SYSREF synchronization characteristics include the following:

- Synchronous sampling of a single SYSREF pulse.
- Meets setup and hold time requirements for reliable synchronization. These requirements are increasingly difficult to achieve as the sample rate increases.
- For single SYSREF mode, SYSREF± input jitter must be less than half of the difference between the CLK± input period and the SYSREF setup and hold time keep out window (KOW). KOW = hold time (t_{HOLD}) + setup time (t_{SETUP}).

Because setup and hold time requirements (with respect to the sample clock) must be met for single SYSREF mode to properly synchronize multiple devices, single SYSREF mode does not operate properly above the absolute maximum input clock rate. The KOW for the device is 142 ps as illustrated in Figure 25. Add the amount of SYREF jitter to the KOW to calculate the absolute maximum input clock frequency allowed for single sample SYSREF mode. Typically, this frequency is about 6 GHz.

Max CLKIN = 1/(KOW + SYSREF jitter)

For multichip synchronization with a high SYSREF jitter, use averaged SYSREF mode.

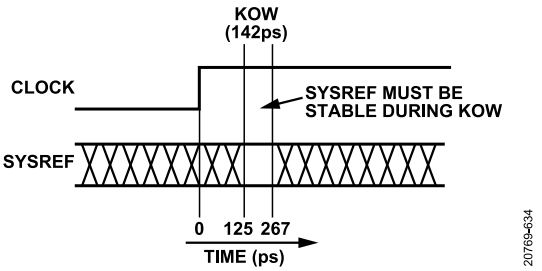

Figure 25. SYSREF Setup and Hold Time KOW

Averaged SYSREF Mode

In averaged SYSREF mode (Register 0x00BA, Bits[2:0] > 0x0), the averaging function determines the mean phase of the SYSREF. The SYSREF_AVERAGE register (Register 0x00BA, Bits[2:0]) sets the number of SYSREF occurrences that are averaged.

Figure 25 shows how the SYSREF averaging function insulates the synchronization logic from the effects of a miss sampled SYREF input signal. The number of averaged SYSREF occurrences that are averaged is 2^N, where N is the value in the SYSREF_ AVERAGE register. Averaged SYSREF mode works the same way as single SYSREF mode, except for the position of the SYSREF is considered to be the mean of several SYSREF phases. The following conditions must be met to employ SYSREF averaging mode, and are increasingly difficult to achieve as the sample rate increases:

- Synchronous sampling of the mean SYSREF phase.
- Mean SYSREF location must meet setup and hold time requirements for reliable synchronization.

Note that averaging SYSREF mode is only available for one shot synchronization mode and is not available for SYSREF monitor mode. When using averaging SYSREF mode for one shot synchronization, use the SYSREF_IRQ function or read the SYSREF_PHASE register to monitor SYSREF alignment to the LMFC/LEMC. See the bit descriptions for EN_SYSREF_IRQ (Register 0x0020, Bit 2), IRQ_SYSREF_JITTER (Register 0x0026, Bit 2), and MUX_SYSREF_JITTER (Register 0x002C, Bit 2) in Table 18 to set up the SYSREF_IRQ function. Set the SYSREF_ AVERAGE register back to 0 when the ONESHOT_SYNC_ DONE bit (Register 0x00B8, Bit 4) is set to 1 (synchronization is complete) for proper monitoring mode operation.

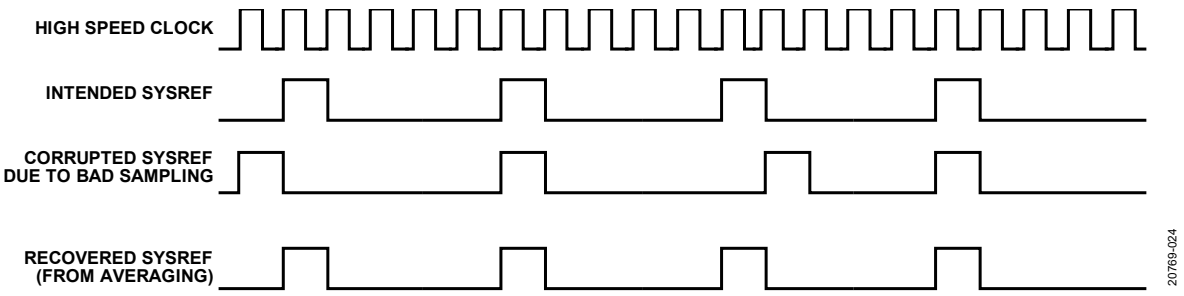

Figure 26. JESD204C Conceptual Illustration of Recovered SYSREF

SYSREF Setup and Hold Time Monitor

The device has a SYSREF_SETUP register and SYSREF_HOLD register (Registers 0x0FB7 and Register 0x0FB8, respectively) that can be used to check if a potential setup or hold time condition exists on the SYSREF± input. The effectiveness of this method to determine robust SYSREF capture may not be robust for input clocks above 4GHz. To validate the SYSREF signal is being captured reliably, the SYSREF_PHASE register can be read (see the SYSREF Monitor Mode section). Multiple readback values of 0 (clearing the readback value in-between readbacks) indicate a successful SYSREF capture.

The SYSREF_SETUP and SYSREF_HOLD registers act as pseudo thermometer indicators (16 bits) of the potential for a timing error. The edge detector circuit takes eight samples of the CLKIN± input before the SYSREF leading edge and eight samples after the SYSREF leading edge. The state of the CLKIN± input at each of these 16 samples is reported in the SYSREF_SETUP and SYSREF_HOLD registers, as shown in Figure 27 The SYSREF_SETUP register contains the sample values to the left of the SYSREF edge and SYSREF_HOLD contain the sample values to the right of the SYSREF edge. To determine the proximity to the clock edge, and therefore the risk of encountering a setup or hold time violation, calculate the absolute value of the difference between the number of 1s in the two registers. If this calculation results in 0, there is no risk of a timing violation. The further this value is away from 0, the higher the risk. The three cases shown in Figure 30 result in these risk assessment calculated values:

1. Abs(0-0) = 0 (no risk)
2. Abs(0-6) = 6 (high risk)
3. Abs(8-8) = 0 (no risk)

Note that the high risk example assumes the default value for SYSREF_EDGE_SEL (Register 0x0FB6, Bit 0) which is set to sample SYSREF with the rising edge of CLKIN. In this case, there is no risk if the SYSREF rising edge is near the falling edge of CLKIN (before = 1s and after = 0s, for example). If the risk assessment calculation indicates a potential SYSREF timing error, provide coarse phase adjustment of the SYSREF signal at the SYSREF source device. If finer adjustment of the SYSREF phase is needed, the SYSREF receiver circuit of the device has a delay circuit that can be used to fine tune the SYSREF timing. The SPI_EN_FDLY_SYS bits (Register 0x0FB1, Bits[1:0]) enable the delay and the SPI_TRM_FINE_DLY_SYS (Register 0x0FB2) and SPI_TRM_SUPER_FINE_DLY_SYS (Register 0x0FB3) registers set fine and superfine delays. These bits are described in Table 18. Depending on the frequency of CLKIN±, these register adjustments may not be enough to cover a full cycle of the CLKIN± input. Therefore, it is recommended to use adjustments at the SYSREF source device prior to using these registers for fine tuning.

JESD204B/C INTERFACE FUNCTIONAL OVERVIEW AND COMMON REQUIREMENTS

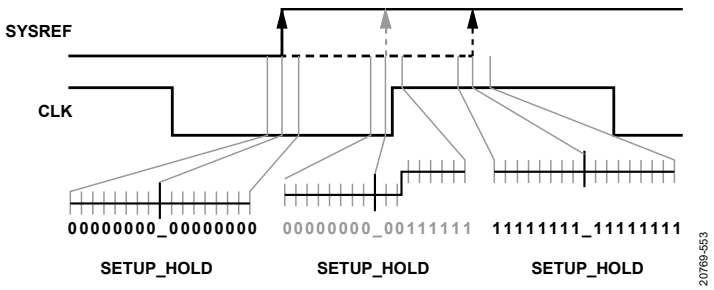

Figure 27. Conceptual Illustration of the SYSREF Edge Detector

SYSREF Setup/Sync Procedure

Using the SYSREF signal to synchronize the internal clocking structures of the device ensures clock accuracy to within a single DAC clock cycle as long as the setup and hold time requirements are met for each device in the JESD204B/C system. To apply SYSREF for clock synchronization, take the following steps:

1. Set up the system clocking, the system SERDES PLL, and the ADC, DAC, and SERDES modes and parameters (see the SERDES PLL and Configuration section and Configuring the JESD204B/C Receiver section).
2. Check for SYSREF setup and hold time errors and make appropriate adjustments using the procedure in the SYSREF Setup and Hold Time Monitor section.
3. Use the SPI bits described in or Table 14 to set up and enable the SYSREF receiver. See Table 18 for descriptions of these bits.
4. Use the SYSREF_COUNT and SYSREF_AVERAGE registers (see Table 18) to set up SYSREF pulse skipping, averaging, or both. The user can configure the chip to skip or average, or skip then average a certain number of SYSREF pulses. SYSREF skipping and averaging operations are valid for one shot sync mode. Monitor mode can only be used with sampled SYSREF mode.
   - "Oneshot sync" is recommended and is implemented in the adi_ad9xxx_jesd_oneshot_ sync() function that is part of the API release package referenced in this document. The API code is shown in Figure 28. Table 18 details the SPI bits referenced in the procedure.
5. Use the ROTATION_MODE register (see Table 18) to set up JESD204B/C receiver and transmitter datapath control during one shot synchronization. The user can configure the chip to do soft off the transmitter datapath and/or JESD204B/C receiver before clock synchronization, and soft on the datapaths after clock synchronization.
6. Use the SYSREF_ERR_WINDOW register (see Table 18) to set up SYSREF tolerant window. The user can set a certain error window, and the synchronization IRQ is asserted only when the external SYSREF signal is out of the window on the internal LMFC/LEMC (see Figure 24). Note that the error window is only available for SYSREF monitor mode.
7. Set up the transmit and receive least common multiple (LCM), if necessary, using the RX_TX_LMFC_LCM register (see Table 16).
   - It is possible that the device JESD204B/C receiver has an LMFC/LEMC period that is different from the device JESD204B/C transmitter LMFC/LEMC period. In this scenario, users need to calculate the LCM of the transmitter and receiver LMFC/LEMC to set up the roper SYSREF period. The SYSREF period must be the same or an integer multiple of the LCM. This LCM value must be set to let the synchronization logic know the relationship between the transmitter LMFC/LEMC and the receiver LMFC/LEMC. If the LMFC/LEMC period of the JESD204B/C receiver is an integer multiple of the JESD204B/C transmitter LMFC/LEMC period, set the RX_TX_LMFC_LCM register to 0. Table 16) shows examples on how to set the RX_TX_LMFC_LCM register appropriately for different JESD204B/C receiver to JESD204B/C transmitter LMFC/LEMC ratios.
8. Apply SYSREF pulses and keep the continuous pulses active until the ONESHOT_SYNC_DONE bit (Register 0x00B8, Bit 4) goes high, which indicates that the clock synchronization is complete.

JESD204B/C INTERFACE FUNCTIONAL OVERVIEW AND COMMON REQUIREMENTS

```
int32_t adi_txfe_jesd_oneshot_sync(adi_txfe_device_t *device, adi_cms_jesd_subclass_e subclass)
{
    int32_t err;
    uint8_t pd_fdacby4, sync_done;
    TXFE_NULL_POINTER_RETURN(device);
    TXFE_LOG_FUNC();

    err = adi_txfe_hal_bf_get(device, REG_CLK_CTRL1_ADDR, BF_PD_FDACBY4_CLK_INFO, &pd_fdacby4, 1); /* not paged */
    TXFE_ERROR_RETURN(err);
    err = adi_txfe_hal_bf_set(device, REG_CLK_CTRL1_ADDR, BF_PD_FDACBY4_CLK_INFO, 0); /* not paged */
    TXFE_ERROR_RETURN(err);
    err = adi_txfe_hal_bf_set(device, REG_ROTATION_MODE_ADDR, BF_ROTATION_MODE_INFO, 1); /* not paged */
    TXFE_ERROR_RETURN(err);

    err = adi_txfe_hal_bf_set(device, REG_SPI_ENABLE_DAC_ADDR, BF_SPI_EN_D2A0_INFO, 1);
    TXFE_ERROR_RETURN(err);
    err = adi_txfe_hal_bf_set(device, REG_SPI_ENABLE_DAC_ADDR, BF_SPI_EN_D2A1_INFO, 1);
    TXFE_ERROR_RETURN(err);
    err = adi_txfe_hal_bf_set(device, REG_SPI_ENABLE_DAC_ADDR, BF_SPI_EN_ANACENTER_INFO, 1);
    TXFE_ERROR_RETURN(err);

    if (device->dev_info.dev_rev == 3) { /* r2 */
        err = adi_txfe_hal_bf_set(device, REG_ACLK_CTRL_ADDR, BF_PD_TXDIGCLK_INFO, 1); /* not paged */
        TXFE_ERROR_RETURN(err);
        err = adi_txfe_hal_bf_set(device, REG_ADC_DIVIDER_CTRL_ADDR, BF_SPI_SWAP_ADC_SYNC_INFO, 0); /* not paged */
        TXFE_ERROR_RETURN(err);
    }

    err = adi_txfe_hal_bf_set(device, REG_SYSREF_MODE_ADDR, BF_SYSREF_MODE_ONESHOT_INFO, 0); /* not paged */
    TXFE_ERROR_RETURN(err);
    err = adi_txfe_hal_bf_set(device, REG_SYSREF_MODE_ADDR, BF_SYSREF_MODE_ONESHOT_INFO, 1); /* not paged */
    TXFE_ERROR_RETURN(err);
    if (err = adi_txfe_hal_bf_wait_to_clear(device, REG_SYSREF_MODE_ADDR, BF_SYSREF_MODE_ONESHOT_INFO), /* not paged */
        err != API_CMS_ERROR_OK) {
        TXFE_LOG_WARN("sysref_mode_oneshot bit never cleared.");
    }
    err = adi_txfe_hal_bf_get(device, REG_SYSREF_MODE_ADDR, BF_ONESHOT_SYNC_DONE_INFO, &sync_done, 1); /* not paged */
    TXFE_ERROR_RETURN(err);
    if (sync_done != 1) {
        TXFE_LOG_WARN("oneshot sync not finished.");
    }

    if (device->dev_info.dev_rev == 3) { /* r2 */
        err = adi_txfe_hal_bf_set(device, REG_ADC_DIVIDER_CTRL_ADDR, BF_SPI_SWAP_ADC_SYNC_INFO, 1); /* not paged */
        TXFE_ERROR_RETURN(err);
        err = adi_txfe_hal_bf_set(device, REG_ACLK_CTRL_ADDR, BF_PD_TXDIGCLK_INFO, 0); /* not paged */
        TXFE_ERROR_RETURN(err);
    }

    err = adi_txfe_hal_bf_set(device, REG_CLK_CTRL1_ADDR, BF_PD_FDACBY4_CLK_INFO, pd_fdacby4); /* not paged */
    TXFE_ERROR_RETURN(err);

    if (sync_done != 1)  {
        return API_CMS_ERROR_JESD_SYNC_NOT_DONE;
    }

    return API_CMS_ERROR_OK;
}
```

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Figure 28. One Shot Sync Procedure Function Code

Table 16. Example RX_TX_LMFC_LCM Settings

JESD204B/C Receiver LMFC/LEMC to JESD204B/C Transmitter LMFC/LEMC Period Ratio	RX_TX_LMFC_LCM Setting
3:2	5
2	0
1:2	1
2:5	9
5:3	14

SYSREF Phase Adjust

The user may need to adjust the local LMFC/LEMC on the device to gain phase alignment with other devices in the system. In this case, use the SYNC_LMFC_DELAY_SET_FRM register (Register 0x00B0) and SYNC_LMFC_DELAY_SET (Register 0x00B1) register. Note that this adjustment is not used to implement Subclass 1 deterministic latency. Those adjustments are discussed in the Device Latency section.

JESD204B/C INTERFACE FUNCTIONAL OVERVIEW AND COMMON REQUIREMENTS

SYSREF Configuration APIs

The API library provides functions to configure and control SYSREF operation and synchronization. Table 17 details the available functions. By default, the API initializes the device into one shot synchronization mode.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 17. SYSREF and Subclass 1 Related APIs

Function	Description
adi_adxxxx_jesd_sysref_input_mode_set	Function to set configuration of SYSREF interface to AC coupling or DC coupling
adi_ad9xxx_jesd_sysref_spi_enable_set	Function to enable SYSREF capture
adi_ad9xxx_jesd_oneshot_sync	Function to set SYSREF operation into one shot synchronization
adi_ad9xxx_jesd_sysref_enable_set	Function to enable/power up the SYSREF circuit, set rotation mode, enable one shot synchronization, and monitor for completion of clock rotation after SYSREF

Table 18. SYSREF Control Registers (DAC and ADC Paths)

Address	Bits	Bit Name	Description	Reset	Access
0x0020	2	EN_SYSREF_IRQ	Enables the IRQ pin and sets the function of the IRQ_SYSREF_JITTER bit. 0 = IRQ_SYSREF_JITTER shows the current status of the SYSREF jitter monitor, the threshold of which is set by the SYSREF_ERR_WINDOW bit field (Register 0x00B7). 1 = IRQ_SYSREF_JITTER latches a SYSREF jitter monitor error condition (becomes a sticky bit) if the error condition occurs and enables the IRQ pin.	0	R/W
0x0026	2	IRQ_SYSREF_JITTER	If EN_SYSREF_IRQ = 0, IRQ_SYSREF_JITTER shows the real time status of the SYREF jitter monitor. 0 = SYSREF is currently within the SYSREF jitter limits set by the SYSREF_ERR_WINDOW register (Register 0x00B7). 1 = SYSREF is currently outside the SYSREF jitter limits set by the SYSREF_ERR_WINDOW register (Register 0x00B7). If EN_SYSREF_IRQ = 1, IRQ_SYSREF_JITTER indicates if a SYSREF jitter monitor error condition has occurred (becomes a sticky bit) since the power-on reset or last clearing of the bit. 0 = SYSREF is within the SYSREF jitter limits set by the SYSREF_ERR_WINDOW register (Register 0x00B7) since the last clearing of the bit. 1 = SYSREF has gone outside the SYSREF jitter limit set by the SYSREF_ERR_WINDOW register (Register 0x00B7) and pulled the IRQB_x pin low (x = MUX_SYSREF_JITTER setting) to trigger an interrupt. Write any value to the IRQ_SYSREF_JITTER bit when latched to clear the register.	0	R
0x002C	2	MUX_SYSREF_JITTER	Select which IRQB_x pin (0 = IRQB_0, 1 = IRQB_1) outputs SYSREF_JITTER_IRQ information.	0x0	R/W
0x0091	3	PD_TXDIGCLK	Control bit needed as part of the one shot synchronization sequence along with SPI_SWAP_ADC_SYNC (Register 0x0180, Bit 7). See the SYSREF Setup/Sync Procedure section.	0x0	R/W
0x00B0	[4:0]	SYNC_LMFC_DELAY_SET_FRM	SYSREF to LMFC/LEMC Coarse Delay (in Frame Units).	0x0	R/W
0x00B1	[7:0]	SYNC_LMFC_DELAY_SET	SYSREF to LMFC/LEMC Fine Delay (in DAC Clock Units).	0x0	R/W
0x00B2	[7:0]	SYNC_LMFC_DELAY_STAT, Bits[7:0]	SYSREF to LMFC/LEMC Delay Status (in DAC Clock Units).	0x0	R
0x00B3	[3:0]	SYNC_LMFC_DELAY_STAT, Bits[11:8]	SYSREF to LMFC/LEMC Delay Status (in DAC Clock Units).	0x0	R
0x00B4	[7:0]	SYSREF_COUNT	Sets the number of rising SYSREF edges to ignore before synchronization (pulse counting mode).	0x0	R/W
0x00B5	[7:0]	SYSREF_PHASE, Bits[7:0]	Contains the phase offset between the monitored SYSREF and internal LMFC/LEMC in DAC clock units. Write any value to these registers to initiate a phase value update.	0x0	R
0x00B6	[4:0]	SYSREF_PHASE, Bits[12:8]		0x0	R
0x00B7	7	SYSREF_WITHIN_LMFC_ERRWINDOW	When this register = 1, the latest SYSREF is within the error window centered by LMFC. See Figure 24.	0x0	R/W

JESD204B/C INTERFACE FUNCTIONAL OVERVIEW AND COMMON REQUIREMENTS

Table 18. SYSREF Control Registers (DAC and ADC Paths) (Continued)

Address	Bits	Bit Name	Description	Reset	Access
	[6:0]	SYSREF_ERR_WINDOW	Sets the amount of jitter allowed on the SYSREF input. SYSREF jitter variations larger than this value trigger an interrupt (DAC clock units). See Figure 24.	0x0	R/W
0x00B8	5	INIT_SYNC_DONE	Initial Synchronization Done Flag (After Initial Power-Up).	0x0	R
	4	ONESHOT_SYNC_DONE	One Shot Synchronization Done Flag (After Enabling SYSREF and Following the Procedure in the SYSREF Setup/Sync Procedure Section.	0x0	R
	1	SYSREF_MODE_ONESHOT	One Shot Synchronization Rotation Mode Enable.	0x0	R/W
0x00B9	[1:0]	ROTATION_MODE	00: in Subclass 0, clock rotation occurs immediately. If in Subclass 1, rotate the clocks as soon as the SYSREF_MODE_ONESHOT bit (Register 0x00B8, Bit 1) is enabled and pulses arrive at the SYSREF input. 01 = device powers down the JESD204B/C? link before clock rotation and brings the link back up afterwards. 10 = device powers down the datapath (using soft on/off function) before the clock rotation and brings the datapath back up afterwards. 11 = device powers down the JESD204B/C link and the datapath (using soft on/off function) before the clock rotation and brings the datapath and link back up afterwards.	0x0	R/W
0x00BA	[2:0]	SYSREF_AVERAGE	Sets how many SYSREF pulses are averaged before one shot synchronization or monitoring. The number of SYSREF pulses to be averaged is calculated by 2^N. When set to 0, SYSREF is in sampled mode and no averaging is done. This bit field must be set before enabling one shot mode.	0x0	R/W
0x00BC	0	NCO_SYNC_MS_TRIG	Set to 1 to trigger main/subordinate NCO synchronization. NCO_SYNC_MS_TRIG is self clearing.	0x0	R/W
0x00BD	[3:0]	RX_TX_LMFC_LCM	If the JESD204B/C transmitter LMFC/LEMC period is an integer multiple of the JESD204B/C receiver LMFC/LEMC, set RX_TX_LMFC_LCM to 0. Otherwise, set RX_TX_LMFC_LCM to the value shown in Table 16. For example, if the receiver to transmitter LMFC/LEMC ratio = 3:2, set RX_TX_LMFC_LCM to 5. If the receiver to transmitter LMFC/LEMC ratio = 2, set RX_TX_LMFC_LCM to 1. If the receiver to transmitter LMFC/LEMC ratio = 5:3, set RX_TX_LMFC_LCM to 14.	0x0	R/W
0x00C5	5	AVRG_FLOW_EN	Set to 1 when using SYSREF averaging mode.	0x0	R/W
0x00D0	2	SPI_EN_D2ACENTER	Enable access to control is ranges 0x195 to 0x19F and 0xF60 to oxFBA. During normal operation, set this bit to 0 to limit SPI clock corruption of the sample clock.	0x1	R/W
0x0180	7	SPI_SWAP_ADC_SYNC	Control bit needed as part of the one shot synchronization sequence along with PD_TXDIGCLK (Register 0x0091, Bit 2). See the SYSREF Setup/Sync Procedure section.	0x0	R/W
0x019A	6	SYSREF_INPUTMODE	0 = dc-coupled. 1 = ac-coupled.	0x0	R/W
0x019E	0	SYSREF_SAMPLE_TYPE	Clock that samples SYSREF first. 0 = SYSREF is sampled by reference clock and then by the high speed clock. 1 = SYSREF is sampled directly by high speed clock.	0x0	R/W
0x0FB0	3	SPI_SYSREF_EN	Enables SYSREF capture.	0x0	R/W
0x0FB1	[1:0]	SPI_EN_FDLY_SYS	Enable fine and super fine delay on the SYSREF input. 00 = SYSREF delay is disabled. Bit 0 enables fine delay (adjustable via Register 0x0FB2) and Bit 1 enables super fine delay (adjustable via Register 0x0FB3). Note that there is a small phase step from SYSREF delay off to SYSREF delay on.	0x0	R/W
0x0FB2	[7:0]	SPI_TRM_FINE_DLY_SYS	Fine delay adjustment of the SYSREF input in 1.1 ps steps with a maximum adjustment range of 56 ps, applicable when Register 0x0FB1, Bit 0 = 1. Note that the maximum effective setting is 0x2F, where the 56 ps of adjustment range is realized. Values above this have no effect on the delay.	0x0	R/W
0x0FB3	[7:0]	SPI_TRM_SUPER_FINE_DLY_SYS	Super fine delay adjustment of the SYSREF input in ~16 fS steps, applicable when Register 0x0FB1, Bit 1 = 1. Maximum super fine delay is approximately 4 ps (255×16 fS).	0x0	R/W
0x0FB6	1	SYSREF_TRANSITION_SEL	SYSREF Transition Selection. 0 = SYSREF is valid on low to high transitions using the selected CLK edge. 1 = SYSREF is valid on high to low transitions using the selected CLK edge.	0	R/W

JESD204B/C INTERFACE FUNCTIONAL OVERVIEW AND COMMON REQUIREMENTS

Table 18. SYSREF Control Registers (DAC and ADC Paths) (Continued)

Address	Bits	Bit Name	Description	Reset	Access
	0	SYSREF_EDGE_SEL	SYSREF Capture Edge Selection. 0 = SYSREF captured on the rising edge of the CLK input. 1 = SYSREF captured on the falling edge of the CLK input.	0x0	R/W
0x0FB7	[7:0]	SYSREF_SETUP	Read only registers used together to determine if a potential setup or hold time violation exists (see the Averaged SYSREF Mode section).	0x0	R
0x0FB8	[7:0]	SYSREF_HOLD		0x0	R
0x0FB9	4	SYSREF_SINGLE_END_MODE_SEL	0 = not single-ended. 1 = 1.8 V single-ended input mode.	0	R/W
	0	SYSREF_DC_MODE_SEL	0 = AC-couple, 1 = DC-couple	1	R/W

RECEIVE INPUT AND DIGITAL DATAPATH

ADC ARCHITECTURE OVERVIEW

The ADC architectures used for the AD9081 4 GSPS ADCs and AD9082 6 GSPS ADCs are shown in Figure 29 and Figure 30, respectively, with the ADC full-scale voltage set to a nominal 1.475 V p-p. Both ADCs include a wideband buffer amplifier and use an interleave architecture. An interleave architecture consists of parallel sub ADCs with the sampling instances offset from each other to maintain uniform sampling of the input signal. Note that the sub ADCs are based on a pipeline architecture. For additional information on interleaving ADCs, see the *Interleaving ADCs: Unraveling the Mysteries* Analog Dialogue article.

The 4 GSPS ADC in the AD9081 consists of two sub ADCs operating at one half of the ADC sample rate with the sampling clocks adjusted to be near a 180° offset. Background interleaving calibrations in the AD9081 minimize the fixed interleaving spurs at fs/2 and fs/2 fin image spur for applications that cannot easily frequency plan those two interleaving spurs.

The 6 GSPS ADC in the AD9082 consist of four sub ADCs implemented in a 3 + 1 Analog Devices proprietary randomization architecture where the sub ADCs operate at an average of 1/3 the ADC sample rate and the sampling clocks are adjusted to be near a 120° offset. The additional sub ADC allows an amount of random rotation among the sub ADCs, which results in any residual gain, offset, and timing mismatches (that otherwise appears as interleaving tones modulated in amplitude and phase) appearing only as additive colored noise. Further background calibration is used to minimize the amount of this additive noise.

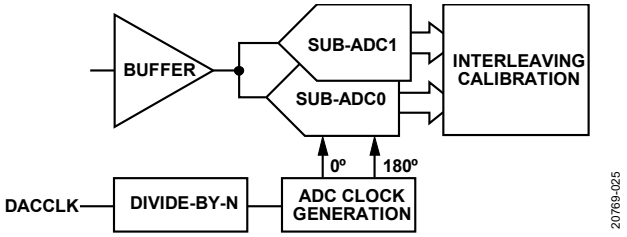

Figure 29. ADC Architecture of AD9081 4 GSPS ADC

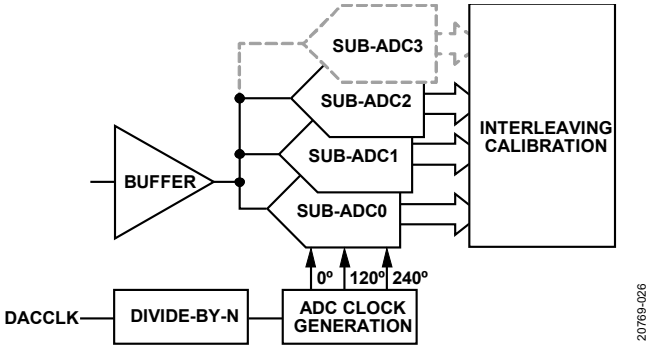

Figure 30. ADC Architecture of AD9082 6 GSPS ADC

Calibration and Specifying Nyquist Zone

Calibration is used to reduce residual spurious artifacts that are common among interleaving ADC architectures because of sub ADC timing, gain, and offsets mismatches. The ADCs are initially factory calibrated as well as recalibrated during the device initialization process. Background calibration is also employed to further improve and maintain the performance across device operating conditions. Note, the ADC calibration performed during device initialization as well as background calibration is not sensitive to whether an input signal is present and occurs in parallel with other initialization steps. Also, the calibration remains independent of the receive digital datapath or JESD204B/C mode settings.

One background calibration algorithm employed adjusts the interleaving timing mismatches and depends on the knowledge of the Nyquist zone being odd or even, which depends on the ADC input frequency (f_{IN}) and sample rate (f_{ADC}), as defined in the following equation and Figure 31:

$$Nyquist\ Zone = ROUNDDOWN \times (f_{IN}/(f_{ADC}/2)) + 1$$

RECEIVE INPUT AND DIGITAL DATAPATH

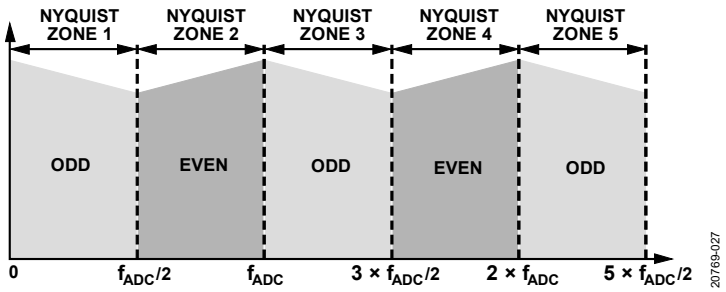

Figure 31. Relationship Between Nyquist Zone Number vs. Odd or Even

Most applications operate within one Nyquist zone and provide some degree of analog filtering to limit any aliasing from the adjacent Nyquist zones, which is typically recommended to be below −35 dBFS for optimum timing calibration. For optimal ADC performance, applications such as multiband receivers that sample input signals that either span odd and even Nyquist zones, or operate on signals falling within 100 MHz of a Nyquist boundary (including dc), must disable the background timing calibration. For signals falling within 50 Hz of a Nyquist boundary, gain calibration must be disabled as well. For such cases, the factory calibration can be used as is or a onetime timing calibration can be performed. To perform this calibration, apply a large signal level (with the peak level not exceeding −1 dBFS) in the valid frequency region and disable the calibration to essentially freeze the updated calibration values.

The AD9081, like the AD9082, is optimized to operate in a single Nyquist Zone and requires enough filtering around the Nyquist edges. Timing and/or gain calibration must be disabled when the input signal is very close to the Nyquist boundary. If the frequency is within 20 MHz of the Nyquist edge, including dc, disable the timing calibration. If the frequency falls within 50 Hz of the Nyquist edge, gain calibration can be disabled. Because the AD9081 is a two-way interleaved ADC, if the CW tone falls near N×fs/4 and 20 dB below full scale, calibration may converge slowly.

Table 19 lists the SPI registers associated with specifying the ADC Nyquist zone as well as enabling and disabling the timing, offset and gain background calibration. Note the following when modifying these registers:

- A transfer operation using Bit 0 of Register 0x2100 is required (by setting this self clearing bit to 1) after a write operation to any of the bit fields in Register 0x2110, Register 0x2116, or Register 0x2117.
- Register 0x2110 is used to specify the Nyquist zone of each ADC independently. Bit 0 must be set to 1 to modify any of the ADC default settings. Bits[4:1] are assigned to the individual ADCs with a setting of 1 or 0 pertaining to an even or odd Nyquist zone, respectively.
- Before disabling any of the calibrations, set Bit 0 of Register 0x2115 to 1. To disable the background calibrations pertaining to any of the ADCs, set the corresponding bit field to 0 followed by a transfer operation.

Table 19. SPI Registers for ADC Calibration

Register	Bits	Control Function
0x2100	0	Transfer bit
0x2110	[4:0]	Nyquist zone Enable background timing calibration ADC0 = Bit 1, ADC1 = Bit 2, ADC2 = Bit 3, ADC3 = Bit 4
0x2111	[3:0]	Invert ADC output data
0x2115	0	USER_ADC_CAL_ADJ
0x2116	[3:0]	Enable background timing calibration ADC0 = Bit 0, ADC1 = Bit 1, ADC2 = Bit 2, ADC3 = Bit 3
0x2117	[3:0]	Enable offset calibration ADC0 = Bit 0, ADC1 = Bit 1, ADC2 = Bit 2, ADC3 = Bit 3
	[7:4]	Enable background gain calibration ADC0 = Bit 4, ADC1 = Bit 5, ADC2 = Bit 6, ADC3 = Bit 7

Calibration and Nyquist Zone Configuration APIs

The adi_ad9081_adc_config and adi_ad9081_adc_nyquist_ zone_set functions specify the ADC Nyquist zone per the application requirements. These functions are contained in the **adi_adxxxx_adc.c** file.

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For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 20. Calibration and Nyquist Zone Configuration APIs

Function	Description
adi_adxxxx_adc_nyquist_zone_set	Function to set the Nyquist zone

ADC INPUT BUFFER

The differential input buffer shown in Figure 32 is used to isolate the interleaving sub ADC core from the external driver. The buffer mode of operation can be controlled using the SPI registers listed in Table 21. The buffer input resistance is set by a pair of 50 Ω resistors tied to the output of a common-mode amplifier, which provides a nominal differential input resistance of 100 Ω. Note that because the ADC full-scale nominal input span is 1.5 V p-p, the corresponding full-scale input power level for a sine wave input is 4.5 dBm. For applications sensitive to polarity inversion that may have inadvertently occurred between the buffer input and the driver interface (resulting in 180° phase mismatches between ADC inputs), data inversion at the designated ADC output(s) can be realized by setting the appropriate bits in Register 0x2111, Bits[3:0] to 1, where Bit 0 corresponds to ADC0.

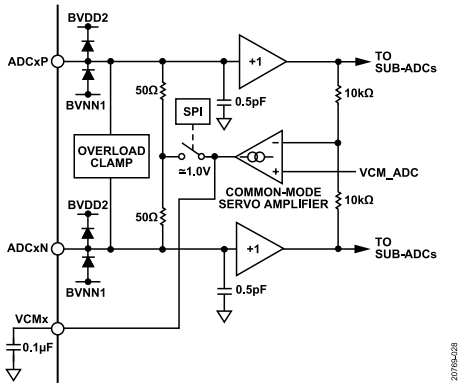

Figure 32. ADC Input Buffer

The buffer includes a common-mode servo loop that maintains the input at a nominal 1 V input common-mode voltage. A 0.1 µF capacitor is required at each VCMx output to ensure the stability of the common-mode feedback loop. In AC-coupled applications, the output of the common-mode amplifier is connected to each end of the 50 Ω input resistors via a switch, which closes the feedback loop internally. In DC-coupled applications where the external driver supports use in a servo loop, the switch is opened such that the external driver closes the servo loop externally with the buffer VCMx output connected to the external drive common-mode voltage input. Figure 33 and Figure 34 show examples of AC coupling and DC coupling applications where the internal switch is enabled or disabled, respectively. By default, the common-mode loop is configured in support of AC-coupled applications.

Note that a more sophisticated internal switch matrix is used to control the common-mode circuitry between ac-coupled and dc-coupled applications than what is shown in Figure 34. Table 22 lists the associated SPI registers required to configure the common-mode loop in support of AC or DC-coupled applications. Note that all ADC buffers are simultaneously configured for either AC or DC configuration. To reconfigure the loop, stop the ADC background calibration using CAL_FREEZE_GLOBAL before enabling the SPI enable paging bit fields, SPI_EN_REG8_ADC1 and SPI_EN_REG8_ADC0, which provide access to the remaining bit fields in Table 19. Table 22 lists the bit field settings for the quad 4 GSPS and dual 6 GSPS ADC product variants. Upon configuring these bit fields, re-enable CAL_FREEZE_GLOBAL.

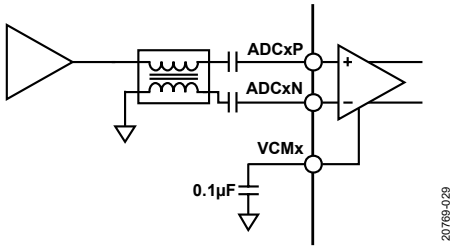

Figure 33. Example of AC-Coupled Input

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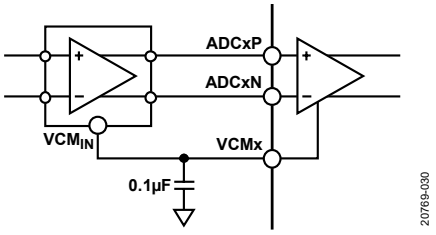

Figure 34. Example of DC-Coupled Input, Differential Driver with a VCMx Input Pin Per Driver Amplifier

Table 21. SPI Register for ADC Buffer

Address	Bits	Bit Name	Description
0x2112	0	CAL_FREEZE_GLOBAL	Set to 1 to freeze calibration for reconfiguration of common-mode loop. Set back to 0 upon completion.
0x00D1	1	SPI_EN_REG8_ADC1	Global enable of ADC1 and ADC0 analog register SPI access through the 8-bit SPI register.
	0	SPI_EN_REG8_ADC0	
0x1721	[7:6]	CMBUF_PD	Power down common-mode buffer.
0x1732	[3:0]	SPI_CMIN_INPUT_SEL	Select common-mode loop for TxFE or MxFE.
0x1733	[6:3]	SPI_CMIN_OUT_SEL	Select common-mode loop for TxFE or MxFE.
	[2:0]	SPI_CMIN_OUT_PULDWN	Pulls VCMx pin low when common-mode buffer disabled.

ADC Input Buffer API

The API supports the ADC input buffer with the adi_ad9xxx_adc_ core_analog_regs_enable_set and ad9081_adc_analog_input_buffer function, which is contained in the **adi_adxxxx_adc.c** file.

Table 22. AC Coupling vs. DC Coupling Bit Field Settings for the Common-Mode Loop

Bit Field Name		SPI_EN_REG_ADCx	CMBUF_PD	SPI_CMIN_IN_SEL	SPI_CMIN_ OUT_SEL	SPI_CMIN_ OUT_PULDWN
Bit Field Address		Register 0x00D1, Bits[1:0]	Register 0x1721, Bits[7:6]	Register 0x1732, Bits[3:0]	Register 0x1733, Bits[6:3]	Register 0x1733, Bits[2:0]
Mode						
Quad ADC, 4 GSPS	AC	3	3	14	14	4
	DC	3	3	14	4	7
Dual ADC, 6 GSPS	AC	3	2	0	0	3
	DC	3	2	0	4	7

Overload Protection

The buffer includes a fast response overload clamp with the threshold set to approximately 2 V, or 3 dB higher than the ADC full-scale input. The clamping network prevents overdrive transient or continuous overdrive conditions from damaging the internal circuitry within the buffer. When the input signal is within the ADC full-scale range, the clamp is off and has no effect on the input impedance of the buffer input. When the input signal exceeds the threshold, the clamp turns on within 500 ps and reduces the input impedance of the buffer to keep the peak voltage in the buffer within a safe limit. The reduced differential impedance across the buffer input forms a voltage divider with the source impedance of the external driver stage, which leads to a voltage reduction as the buffer impedance reduces. When the transient disappears, the recovery time depends on the amount of overrange, but is typically within a few ns upon the input signals envelope level re-entry into the full-scale input span of the ADC, 0 dBFS.

Figure 35 shows the recovery response to when the buffer input of the ADC is driven with a pulsed 1.5 GHz CW tone with overrange levels of 6 dBFS, 12 dBFS, and 17 dBFS. In terms of absolute power levels, this equates to levels of approximately 10.5 dBm, 16.5 dBm, and 21.5 dBm. Note that the recovery response is also inclusive of test setup limitations that includes an RF amplifier (Mini-Circuits ZRL-3500+) that is driven near its compression point for the 17 dBFS case (with approximately 3 dB loss between the amplifier and buffer input). The recovery time to within 2% of the full-scale input of the ADC is less than 5 ns, 10.5 ns, and 14 ns, inclusive of the test setup limitation.

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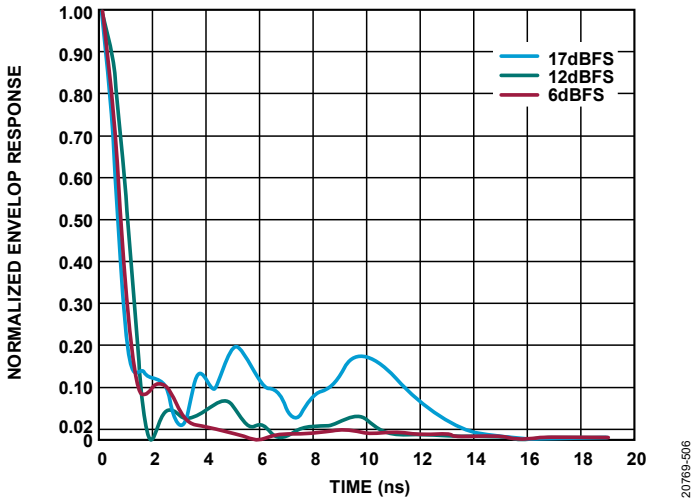

Figure 35. Normalized Envelope Response Shows the Buffers Recovery Time to Within 2% for Different Overrange Conditions Relative to the ADC's Full-Scale Input of 0 dBFS

ADC Input Driving Considerations

Optimum AC performance is achieved when driving the ADC input differentially with a signal that has excellent amplitude and phase balance over the frequency bands of interest to reduce even order distortion products. For DC coupling and/or AC performance up to 2 GHz, a differential ADC driver, such as the ADL5569, is acceptable to use. For applications that require higher linearity or input frequency, consider using a single-ended RF gain block followed by an RF balun that provides a differential input to the ADC.

In any case, the interface to the ADC is important to maintain the achievable performance and bandwidth. For this reason, both S parameter equivalent AC analysis models of the ADC input are available on each product web page. Included in the simulation package are balun models from Marki, Mini-Circuits, and Murata. Designers are encouraged to simulate with these models combined with models of the selected RF components and PCB layout models. Figure 36 and Figure 37 show the Smith charts representing the ADC input differential S parameter for the different devices. Some applications can use a differential matching network that also serves as a band limiting filter.

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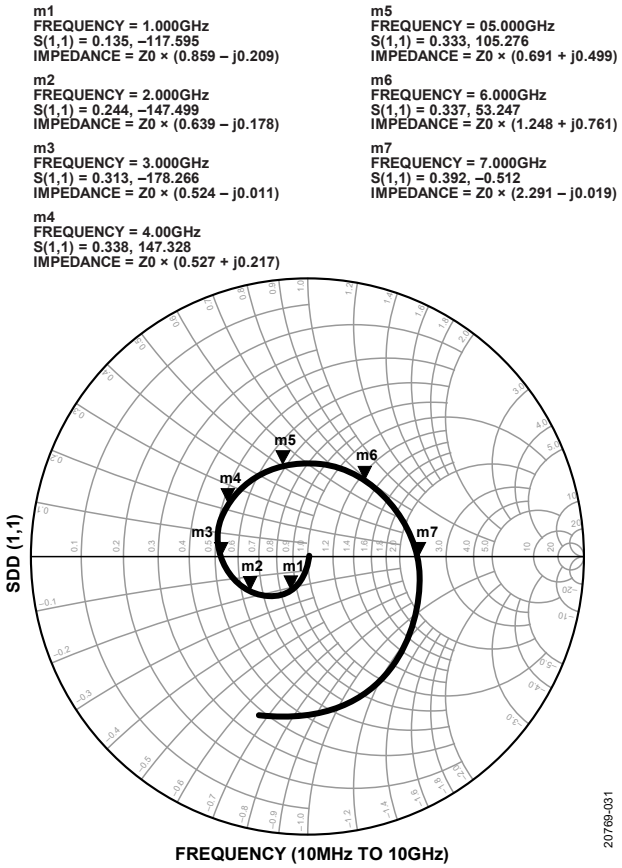

Figure 36. AD9081 ADC Buffer Input Differential Return Loss (SDD11)

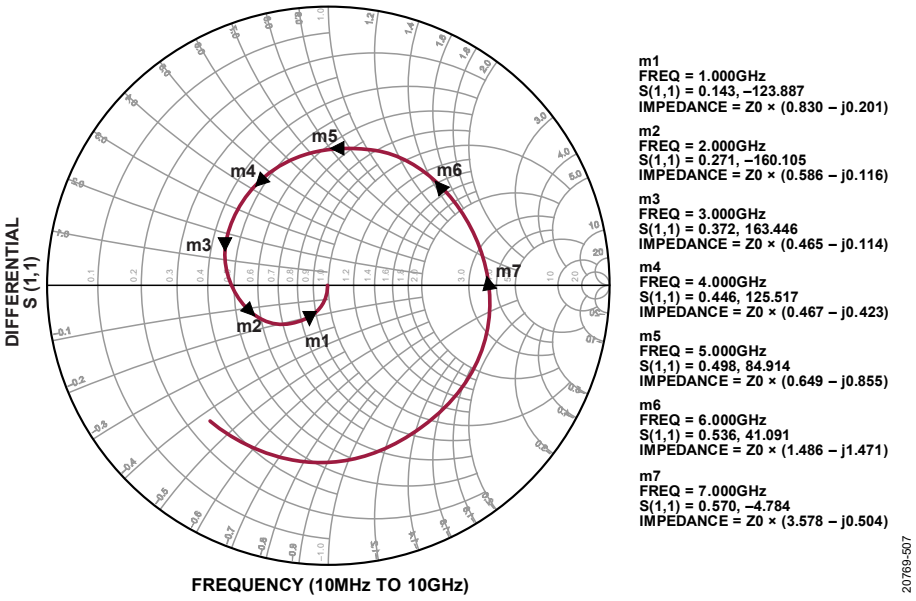

Figure 37. AD9082 ADC Buffer Input Differential Return Loss (SDD11)

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For AC characterization purposes, the Marki BALH-0009 balun is used because the balun maintains optimal balance over the widest frequency range. A lower cost, smaller size balun, such as the Mini-Circuits TCM1-83x, can be considered at the expense of degraded phase and amplitude balance in some frequency regions. Figure 39 compares the measured frequency response of the different baluns using the ADC0 input of the AD9082 on the FMCA-EBZ and FMCB-EBZ evaluation boards. Note that the de-embedded ADC −3dB bandwidth extends to 8 GHz when driven by an ideal 100 Ω source. Low temperature co-fired ceramic (LTCC) baluns, such as the Murata LTCC balun, LDB13G0BAADA042, which is also included in the simulation package, can also be considered.

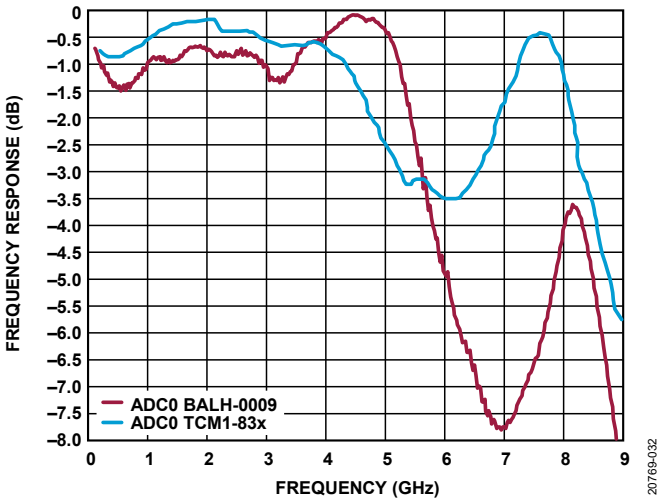

Figure 38. Measured Input Bandwidth of AD9082 ADC0 Input Comparing Use of Marki BALH-0009 Board and Mini-Circuits TCM1-83x on FMCA-EBZ and FMCB-EBZ Evaluation Boards, Respectively (No Matching Network)

RECEIVE DIGITAL DATAPATH OVERVIEW

All product variants share the same receive digital datapath regardless of whether the product variant consists of a dual 6 GSPS or quad 4 GSPS ADC core (with the noted exceptions highlighted in Table 1). The receive digital datapath shown in Figure 39 consists of a main datapath followed by a channelizer path. The main datapath consists of four coarse digital downconversion (CDDC) blocks and an optional fractional delay block (available for Main Data Path 0 or Main Data Path 3 only). Each CDDC block consists of a bypassable, digital quadrature downconverter with a 48-bit NCO followed by a decimation filter supporting factors of 2, 3, 4, and 6. The channelizer datapath consists of eight fine digital downconversion (FDDC) blocks that offer additional digital downconversion capacity with a decimation filter supporting factors of 2, 3, 4, 6, 8, 12, 16, and 24. A data router multiplexer is used to select the desired data outputs (at different stages of the receive datapath) that are aggregated for the JESD204B/C link.

The channelizer path provides additional digital downconversion stages and higher decimation factors. The additional downconversion stages enable multiband applications where two or more smaller RF bands can be downconverted separately and represented at the lowest possible sample rate to reduce the overall throughput and post digital signal processing requirements of the host processor. A dual 2×4 crossbar multiplexer allows up to four FDDC blocks to be mapped to the output of a CDDC block with the maximum complex data interface rate limited to 1500 MSPS.

The receive datapath offers considerable flexibility and the following auxiliary features to simplify system design:

- Support for two independent JESD204B/C transmitter links that each have different receive datapath configurations
- Fast detection and signal monitoring capability at the ADC output with high and low programable thresholds to facilitate external AGC implementations
- Optional programmable digital filter that allows the user to provide customized digital filtering and/or equalization directly to the wideband signal content represented at the ADC output(s).
- Programable integer delay per ADC output to compensate for any RF channel delay mismatch
- Fractional delay (one ADC only) for fine delay calibration of I/Q delay mismatch or for fine timing alignment in digital predistortion applications
- Bypassable upsampler to enable different sample rates among receive datapaths that share the same JESD204B/C link
- Optional 6 dB gain enhancement when downconverting a real signal as well as a complex to real (C2R) data conversion block

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- FFH with up to 16 preassigned hop frequencies.

A paging scheme is used to individually control common blocks. Table 23 shows the different paging registers for the common blocks. This approach allows maximum flexibility for individual registers pertaining to specific blocks to be configured or common settings to be shared among two or more datapath blocks configured simultaneously.

Table 23. Receive Paging Register Map Description

Address	Name	Register Description
0x0018	ADC_COARSE_PAGE	Receive main path and ADC paging
0x0019	FINE_DDC_PAGE	Channelizer paging
0x001A	JTX_PAGE	Support for two JESD204B/C transmitter links with separate data format and JESD204B/C transmitter crossbar settings
0x001E	PFILT_CTL_PAGE	PFILT paging bits
0x001F	PFILT_COEFF_PAGE	PFILT paging register for coefficients

Each block is described in order of appearance in Figure 39, from the ADC output to the input of the JESD204B/C block, with the exception of the fast detect and signal monitoring block (used for AGC assist) and the programmable PFILT block, which are covered in more detail in the DAC Outputs section.

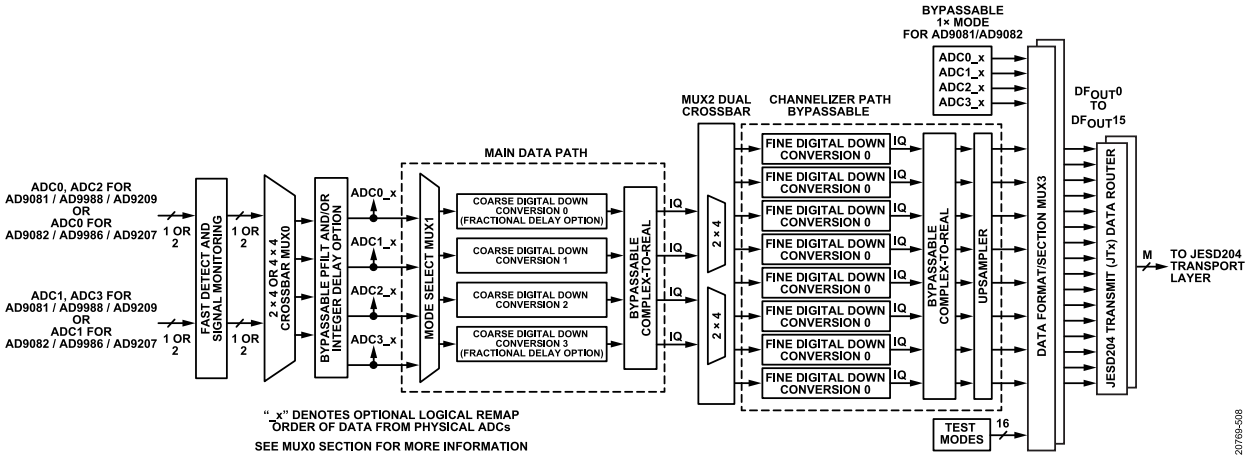

Figure 39. Complete Receive Digital Datapath

RECEIVE DATAPATH CONFIGURATION CONSIDERATIONS

Proper selection of the main datapath decimation factor (M_{RX}) and channelizer datapath decimation factor (NRX) for each receive datapath must be considered, as well as whether an additional JESD204B/C link is required when datapath requirements differ based on the usage case. An optimum configuration is one where all desired RF signal channels are supported while operating at the lowest possible data rate. Lowering the data rate into the host processor reduces any post digital filtering and the number of JESD204B/C lanes required to transfer the data.

The simplest case occurs when all receive datapaths can be configured with the same total decimation factor with matching values for M_{RX} and N_{RX} to require one JESD204B/C link with all output data rates from the receive datapaths matched. This scenario is often the case in single-band communication applications that consist of multiple antennas with the target RF bands common among all paths. A more complicated case can occur if an additional RF band needs to be supported with different bandwidth requirements, which requires a different decimation factor that supports the data rate of the added RF band. In this case, the output data rates from the receive datapaths may not match and require the use of either an additional JESD204B/C link or the upsampler shown in Figure 39 to match the lower rate receive datapaths to the highest rate datapath, such that one JESD204B link can still be used. Using the upsampler to match data rates requires that all data rates in the JESD204B/C link be related by any factor in the form of 2^N.

A more complicated case can arise in a communication application where one (or more) of the receive datapaths associated with an ADC must be quickly repurposed with a different configuration, which results in a different output data rate. An example of this scenario is a time division duplex application, where the ADCs used for the receiver can also be used to monitor the transmit power amplifier output as part of a digital predistortion loop where the bandwidths (output data rates) are often 3 to 5 times the bandwidth required for a receive operation. In this case,

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a separate link is required to support the wide band configuration and allow the JESD204B/C links to remain stable when switching between receive and transmit operations.

The receive digital datapath contains two separate stages of decimation following the complex downconversion NCO in the main and channelizer datapaths. The usable bandwidth after the decimation filters is 81.4% of the I/Q data output rate (f_{IQ_OUT}). The M_{RX} can be set to 1, 2, 3, 4, or 6 in the COARSE_DEC_SEL bit field (Register 0x0282, Bits[3:0]), and the N_{RX} can be set to 2, 3, 4, 6, 8, 12, 16, or 24 in the FINE_DEC_SEL bit field (Register 0x0283, Bits[2:0]). Each channelizer can also be bypassed in the FINE_BYPASS bit field in Register 0x0287 to set N_{RX} to 1. The following equations shows the total decimation factor as a function of $M_{RX} \times N_{RX}$ as well as the ADC rate, f_{ADC}, and f_{IQ_OUT} (with both values represented in either MSPS or GSPS):

Total Decimation = f_{ADC}/f_{IQ_OUT}

Total Decimation = $M_{RX} \times N_{RX}$

The upsampler requires knowledge of the total decimation factor for each receive datapath as well as the lowest decimation factor of all datapaths assigned to a JESD204B/C link. The total decimation factor for each receive datapath is set by the DDC_ OVERALL_DECIM bit field in Register 0x0284. Note that both crossbar Mux2 (using the COARSE_FINE_CB register, Register 0x0281) and the DDC_OVERALL_DECIM bit field must be programmed even in cases where the channelizer is bypassed using the FINE_BYPASS bit field.

The lowest total decimation factor value is specified in the CHIP_ DECIMATION_RATIO bit field in Register 0x0289. The JTX_ LINK0_PAGE and JTX_LINK1_PAGE bit fields specify to which link this value is assigned. Based on the CHIP_DECIMATION_ RATIO value, the upsampler matches the receive path with the lower data rate (or total higher decimation factor) to the path with the highest rate if the two paths relate by any factor of 2^N. The upsampler repeats the samples of the lower rate bands to match that of the higher band with the expectation that the host processor performs the opposite function by down sampling this data stream (without digital filtering) to retain the original data rate of that receive datapath.

Selecting the optimum M_{RX} and N_{RX} values for each receive datapath depends on the following factors and trade-offs:

- The f_{IQ_OUT} required to represent the signal bandwidth of interest. This data rate must exceed the bandwidth by at least a factor of 1.2288 to allow the signal to fall within the digital filters bandwidth. For instance, if the desired signal bandwidth was 100 MHz, the minimum f_{IQ_OUT} must be no less than 122.88 MSPS.
- The optimum f_{ADC} results in the desired RF band(s) of interest to meet the required spurious content because of ADC performance limitations that manifest as harmonics or digital induced image spurs. Ensure that these bands fall well within a Nyquist zone (see Figure 31), which requires some degree of frequency planning to determine a suitable range of operation within the maximum specified range. Large signal bandwidths (including multiband support) typically benefit from operating with higher ADC clock rates. In practice, a suitable ADC clock rate within 75% and 100% of the maximum ADC lock rate often exists.
- Recognition of whether the application requires multiband support, and if so, whether the spacing between RF bands (with consideration to the signal bandwidths) benefits from using the channelizer FDDC capability to create two or more separate receive datapaths. For instance, consider the dual band case that consists of one 75 MHz band at 1.7475 GHz and another 70 MHz band at 2.535 GHz. Both bands can be represented with an f_{IQ_OUT} of 92.16 MSPS if each band is assigned an individual channelizer path, which results in two separate receive datapaths. If a single receive datapath is used to process both bands simultaneously (occupying an edge to edge bandwidth of 860 MHz), the f_{IQ_OUT} must exceed 1057 MSPS, which is a 5.7 factor increase in data throughput rate that must be supported by the JESD204B/C link as well as host processor.
- Compare the ratio of the edge to edge bandwidth required to support all bands of interest to the sum of all RF band occupied bandwidths to determine whether to use channelizers. If this ratio exceeds 2, consider using the channelizers.
- Recognition that the maximum data rate from the main datapath is limited to 1500 MSPS places restrictions on the minimum value of M_{RX} when using the channelizers such that $M_{RX} > f_{ADC}/1500$ where f_{ADC} is specified in MHz. The usable bandwidth is limited to 1220 MHz because of the digital filter passband response. Multiband applications where the edge to edge bandwidth exceeds this limit require an additional coarse digital downconverter (CDDC) stage to process one of the outer bands.
- The total decimation factor for a given receive datapath depends on the fIQ_OUT and the fADC that meet the performance specifications of the application. In applications where the total decimation factor exceeds 4, different M_{RX} and N_{RX} combinations can be used while still satisfying the 1500 MSPS limit. In this case, it is preferred to select the combination that results in the highest M_{RX} because this selection leads to a lower f_{IQ_OUT} into the channelizer path and results in slightly lower power dissipation. However, if the performance is limited by spurious content from the decimation stage, other combinations can be considered
- To benefit from the upsampler ability to enable the use of one JESD204B/C link for receive datapaths with different f_{IQ_OUT} rates, keep all data rates related by a factor of 2^N.

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Receive Datapath Configuration API

The API library provides a function, adi_ad9081_device_startup_ rx, that configures the receive datapaths of the device from ADCs to a JESD interface, per Figure 39. The end application provides the API with the details of the desired receiver datapaths via the parameters to describe the desired decimation, NCOs, and sampled data output formats, as well as the desired downstream JESD interfaced. The API handles the configuration for the full datapath.

The adi_ad9081_device_startup_rx API depends on the ADC sampling clock information. Therefore, for proper operation, the adi_ad9081_device_clk_config_set function must be called prior to calling the adi_ad9081_device_startup_rx function.

For full details on adi_ad9081_device_clk_config_set and adi_ad9081_device_startup_rx , see the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Additional API functions are provided for configuration of the components of the receive datapath, such as the NCOs, DDCs, and crossbar muxes. Note calling these functions may override configurations set by adi_ad9081_device_startup_rx.

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 24. Receive Datapath Configuration API

Function	Description
adi_ad9081_device_startup_rx	Function to configure the receive datapaths

MUX0

Mux0 is a crossbar multiplexer that takes the form of either a 2×4 input to output crossbar for the AD9082 (with two ADCs), or a 4×4 input to output crossbar for the AD9081 (with four ADCs). Mux0 allows the mapping of any ADC physical output to any PFILT input. If the PFILT filter (and/or cyclical integer delay line) is bypassed, the Mux0 outputs become inputs following the Mux1 stage. These multiplexer outputs are referred to as logical ADC outputs with the suffix _x added to distinguish these outputs from the physical data output directly from the ADC. Figure 40 shows the input to output relationship for the 2×4 and 4×4 Mux0 crossbars use cases.

The logical ADC outputs can be mapped to any physical ADC data input. This mapping is controlled by Bits[1:0] of the PFILT_ CTL_PAGE register (Register 0x001E) and Bits[3:0] of the PFILT_DIN_SELECT mapping register (Register 0x0B12), where two 2-bit fields correspond to a pair of logical ADC outputs (ADC1_x and ADC0_x or ADC3_x and ADC2_x). Table 25 and Table 26 show the mapping settings for the 2×2 and 4×4 multiplexers. The value selected for each 2-bit field represents the ADC input to be mapped to that logical output with the value representative of the ADC output selected. Two or more logical ADCs can be mapped to the same physical ADC. Mapping the same logical numeric ADC to the physical counterpart is typically sufficient.

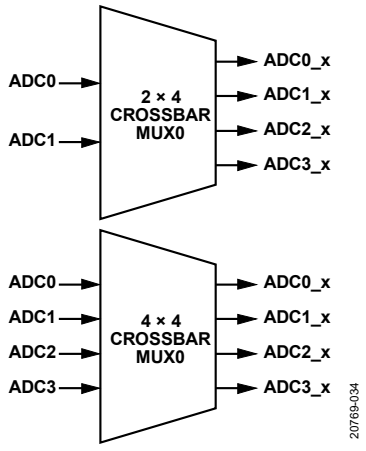

Figure 40. 2×4 and 4×4 Crossbar Mux0 for AD9082 and AD9081

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Table 25. 2×4 Crossbar Mux0 Mapping for AD9082, AD9986, AD9207

		PFILT_DIN_SELECT (Register 0x0B12)	
Logical ADC	PFILT_CTL_PAGE (Register 0x001E, Bits[1:0])	Bits[3:2]	Bits[1:0]
ADC0_x	01		00 = ADC0 10 = ADC1
ADC1_x	01	01 = ADC1 11 = ADC0	
ADC2_x	10		00 = ADC1 10 = ADC0
ADC3_x	10	01 = ADC0 11 = ADC1	

Table 26. 4×4 Crossbar Mux0 Mapping for AD9081, AD9988, AD9209

		PFILT_DIN_SELECT (Register 0x0B12)	
Logical ADC	PFILT_CTL_PAGE (0x001E[1:0])	Bits[3:2]	Bits[1:0]
ADC0_x	01		00 = ADC0 01 = ADC2 10 = ADC1 11 = ADC3
ADC1_x	01	00 = ADC2 01 = ADC1 10 = ADC3 11 = ADC0	
ADC2_x	10		00 = ADC1 01 = ADC3 10 = ADC0 11 = ADC2
ADC3_x	10	00 = ADC3 01 = ADC0 10 = ADC2 11 = ADC1	

MUX0 Configuration API

The API supports the configuration of Mux0 via the adi_ad9081_ adc_pfir_ctl_page_set and adi_ad9081_adc_pfir_din_select_set functions, both of which are contained in the **adi_adxxxx_adc.c** file.

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

BYPASSABLE INTEGER DELAY AND PFILT

The Mux0 block outputs can be directed to either the Mux1 block input or to an auxiliary digital signal processing (DSP) block. The auxiliary DSP block includes a programable finite impulse response filter (see the Programmable Filter (PFILT) section) followed by an integer delay block with either block outputs serving as possible inputs to the Mux1 block. The integer delay block shown in Figure 41 provides coarse mismatch timing delay compensation for each logical ADC with a timing resolution equal to the ADC sampling period or $1/f_{ADC}$. The integer delay block option consists of a 16-tap delay line with a 16:1 multiplexer to select which tap is used for the output.

RECEIVE INPUT AND DIGITAL DATAPATH

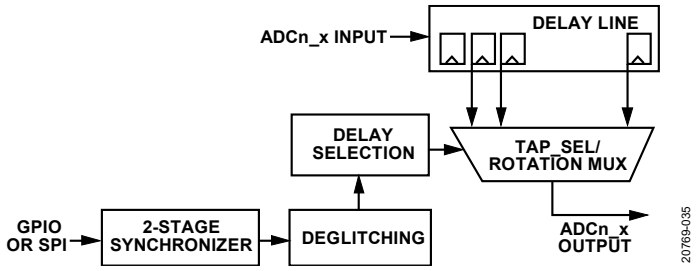

Figure 41. Optional Integer Delay Block Implementation

The ADC_COARSE_PAGE register (Register 0x0018) selects which integer delay block to program. The CDELAY_ENABLE register (Register 0x0B14) enables the block and the CSHIFT0 register (Register 0x0B01) sets a delay from −8 to +7 ADC sample periods. A CSHIFT0 register setting of 0x0 corresponds to a −8 sample shift. Three additional delay settings are available in the CSHIFT1, CSHIFT2, and CSHIFT3 registers (Register 0x0B02 to Register 0x0B04) for applications where four different profile settings are desired and accessible under GPIO or SPI control using the CD_CTRL register (Register 0x0B05). The CD_GPIO_EN bit of the CD_CTRL register enables GPIO control, and the CDSEL bit selects the delay setting when under SPI control. Refer to the GPIOx Pin Operation section for information on GPIO pin assignment.

Integer Delay and PFILT Configuration API

The API library provides functions to configure the auxiliary DSP block integer delay and PFILT block. These functions are listed in Table 27.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 27. Receive Datapath Configuration API

Function	Description
adi_ad9081_adc_cycle_delay_set	Function to set coarse DDC to route to auxiliary DSP and to configure the desired delay
adi_ad9081_adc_cycle_delay_enable_set	Function to enable or disable the delay block
adi_ad9081_adc_cycle_delay_selection_set	Selects the delay when under SPI control
adi_ad9081_adc_cycle_delay_enable_via_gpio_set	Enables GPIO control of the block

MUX1

Mux1 is a crossbar multiplexer that defines the connection between the logical ADCs and the CDDC in the main datapath, which can process real or complex data. As a result, this connection can support either real data from a single logical ADC or complex data from a pair of logical ADCs. Mux1 is controlled by the ADC_COARSE_CB register (Register 0x0280).

Table 29 shows how Register 0x0280, Bits[1:0] control the mapping for the AD9081 and AD9082. If complex data is selected, the user can swap the connection, such that I data becomes Q data (and vice versa), which results in a spectral inversion using the C_MXR_IQ_SFL (Register 0x0280) bit field, Bits[7:4].

Mux1 Configuration API

The API library fully supports the configuration of the receive main datapaths. The top level API function, adi_adxxxx_device_ startup_rx, configures the receive main datapath. In addition, the functions in Table 28 allow the user to manually configure each block of the receive main datapath, as described in Receive Datapath Configuration Considerations section. Table 28 details the supported APIs for the configuration of Mux1.

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

RECEIVE INPUT AND DIGITAL DATAPATH

Table 28. Mux1 Configuration APIs

Function	Description
adi_adxxxx_device_startup_rx	Function to configure full receive datapath including the main CDDC datapaths
adi_adxxxx_adc_adc2cddc_xbar_set	Function to mux data from ADC to main datapath CDDC
adi_adxxxx_adc_adc2cddc_xbar_set	Function to retrieve ADC from main datapath CDDC

Table 29. Mux1 Real or Complex Register Settings

Device	Real or Complex	Register 0x0280, Bits[1:0][1]	Default Mapping	Comments
AD9081	Real	0x0	ADC0_x to CDDC0, ADC1_x to CDDC1 ADC2_x toCDDC2, ADC3_x to CDDC3	Each logical ADC mapped to the corresponding CDDC
	Complex	0x1	ADC0_x and ADC1_x to CDDC0 and CDDC1 ADC2_x and ADC3_x to CDDC2 and CDDC3	ADC0_x and ADC1_x form a complex I/Q pair and are mapped to CDDC0 and CDDC1 ADC2_x and ADC3_x form a complex I/Q pair and are mapped to CDDC2 and CDDC3
AD9082	Real	0x2	ADC0_x to CDDC0 and CDDC2 ADC1_x to CDDC1 and CDDC3	ADC0 output is mapped to CDDC0 and CDDC2 ADC1 output is mapped to CDDC1 and CDDC3
	Complex	0x3	ADC0_x and ADC1_x to CDDC0, CDDC1, CDDC2, and CDDC3	ADC0_x and ADC1_x form a complex I/Q pair and are mapped to all CDDCs

[1] Bit 3 is set to 0 by default.

RECEIVE MAIN DIGITAL DATAPATH

The receive main datapath shown in Figure 42 consists of four identical CDDC blocks with the exception that a bypassable fractional delay block can also be used in conjunction with the CDDC0 and CDDC3 paths only. Each CDDC block consists of a quadrature digital downconversion stage for frequency translation of either a real or complex signal as well as a selectable decimation filter for data rate reduction and filtering. Optional gain compensation with C2R data translation is also included. The ADC_COARSE_PAGE register (Register 0x0018) configures each main datapath independently. To disable unused main datapaths, use the COARSE_DDC_EN register (Register 0x0285, Bits[3:0]).

Main Datapath CDDC

Frequency translation is accomplished with a complex NCO and a digital quadrature mixer, where a real or complex input spectrum is multiplied by the NCO complex exponential frequency ($e^{-j\omega ct}$) output, which centers the desired signal complex output spectrum around dc. Figure 43 and Figure 44 show examples of the frequency translation stage for real and complex inputs, respectively.

The frequency translation stage of each CDDC block can be controlled individually and supports four different IF modes based on the COARSE_MXR_IF bit field setting in Register 0x0282, Bits [7:6].

These IF modes include the following:

- Variable IF mode: The NCO and mixers for frequency translation to a lower IF and the NCO is digitally tunable. Set the COARSE_MXR_IF bits to 00 to enable this mode.
- $F_S/4$ IF mode: This mode is similar to variable IF mode, except that the NCO is tuned to exactly $f_{ADC}/4$ to allow the sample sequence to consist of only four phases having a repetitive +1, 0, −1, 0 sequence, which removes the need for digital multipliers in the mixing process and reduces digital power consumption. Applications where the desired signal bandwidth is situated near the center of a Nyquist zone can use this mode. Set the COARSE_MXR_IF bits to 10 to enable this mode.
- 0 Hz IF (ZIF) mode: The mixers are bypassed. Set the COARSE_MXR_IF bits to 01 to disable the NCO.
- Test mode (NCO only mode): The path from the ADC is disconnected, the input samples to the NCO are forced to 0.999 of positive full scale, and the NCO is enabled. Set the COARSE_MXR_IF bits to 11 to enable this mode. This mode is similar to the NCO only mode of the CDUC and FDUC blocks that are part of the transmit datapath. NCO only mode allows the NCOs to generate sinusoid samples as an output to downstream blocks, either for testing the response of the decimation filters or to loopback the samples into the transmit datapath as additional NCOs in a DDS application. The latter can be particularly useful when utilizing the AD9177 as a DDS.

RECEIVE INPUT AND DIGITAL DATAPATH

Main Datapath CDDC IF Mode Configuration API

The API supports the configuration of the IF modes via the adi_ad9081_adc_ddc_coarse_nco_mode_set function, which is contained in the **adi_adxxxx_adc.c** file.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

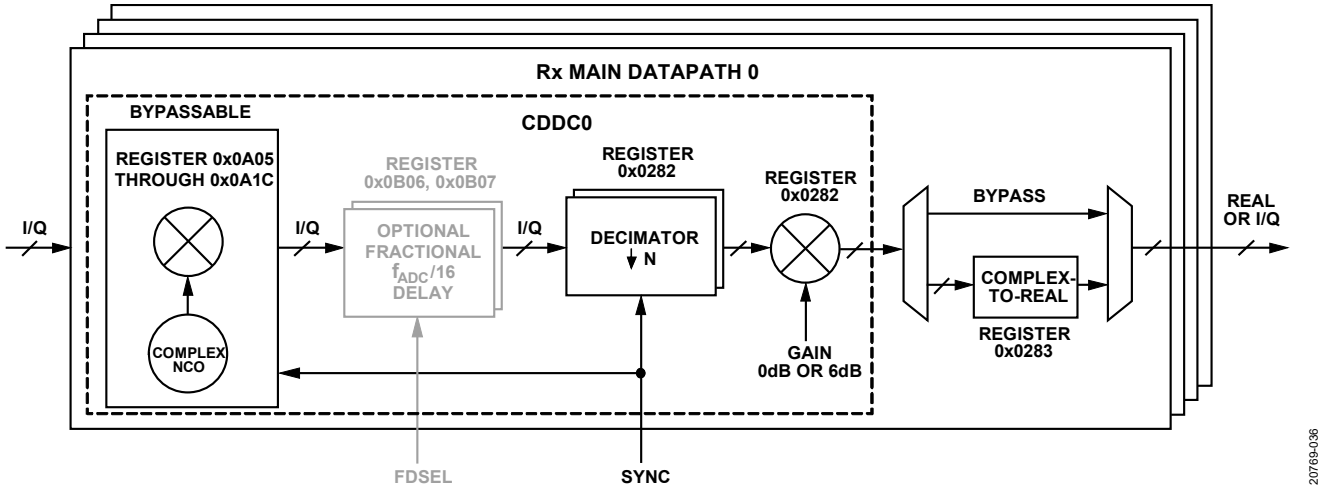

Figure 42. Main Receive Digital Datapath Block Diagram

RECEIVE INPUT AND DIGITAL DATAPATH

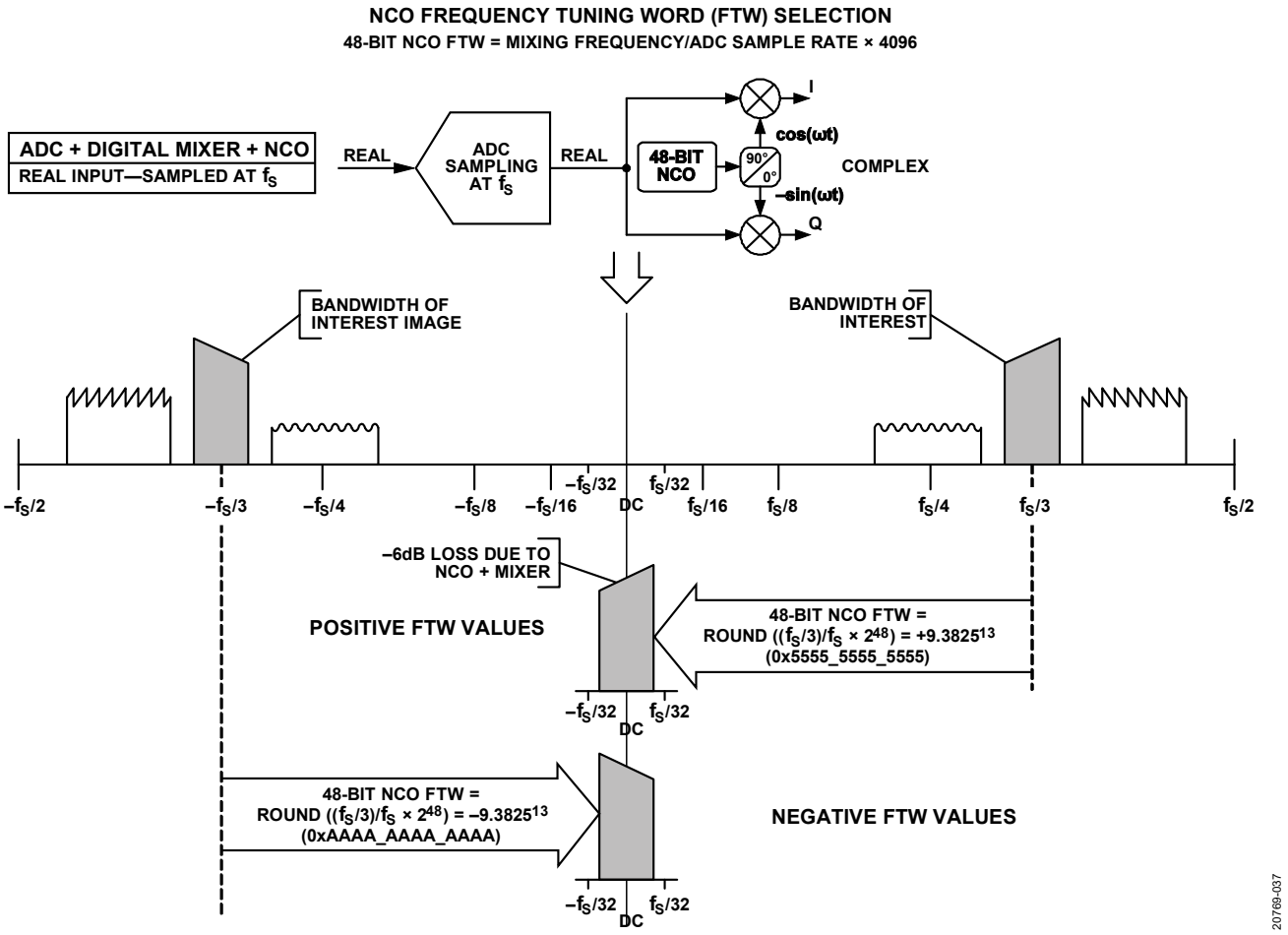

Figure 43. DDC NCO Frequency Tuning Word Selection, Real Inputs

RECEIVE INPUT AND DIGITAL DATAPATH

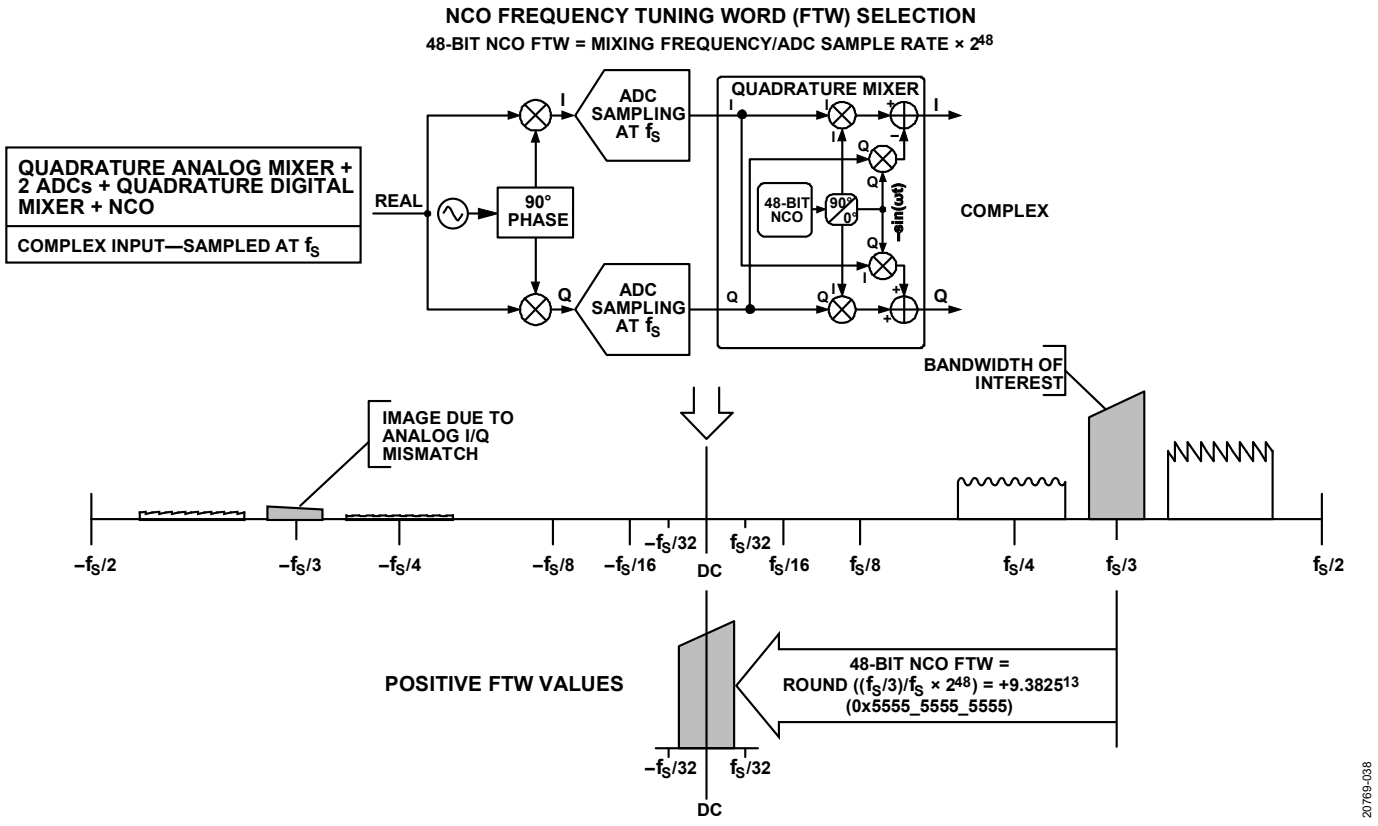

Figure 44. DDC NCO Frequency Tuning Word Selection, Complex Inputs

CDDC Variable IF NCO Operating Modes

The NCO can be configured for different modes of operation if variable IF mode is selected. Figure 45 shows a block diagram of a digital quadrature NCO and the other stages within the CDDC. The gray lines in Figure 45 represent the SPI control lines. The 48-bit complex NCO supports the following modes of operation:

- Dual modulus mode for higher frequency resolution where the modulus is set by the phase increment numerator (PIFA) and phase increment denominator (PIFB) words.
- Integer-N mode where 48-bit frequency and phase settings are set by the phase increment word (PIW) and phase offset word (POW). This mode also supports phase coherency when switching among up to 16 different frequency assignments where the phase is referenced to a single synchronization event at Time 0. See the Receive Main and Channelizer Path FFH NCO Mode section for more information.

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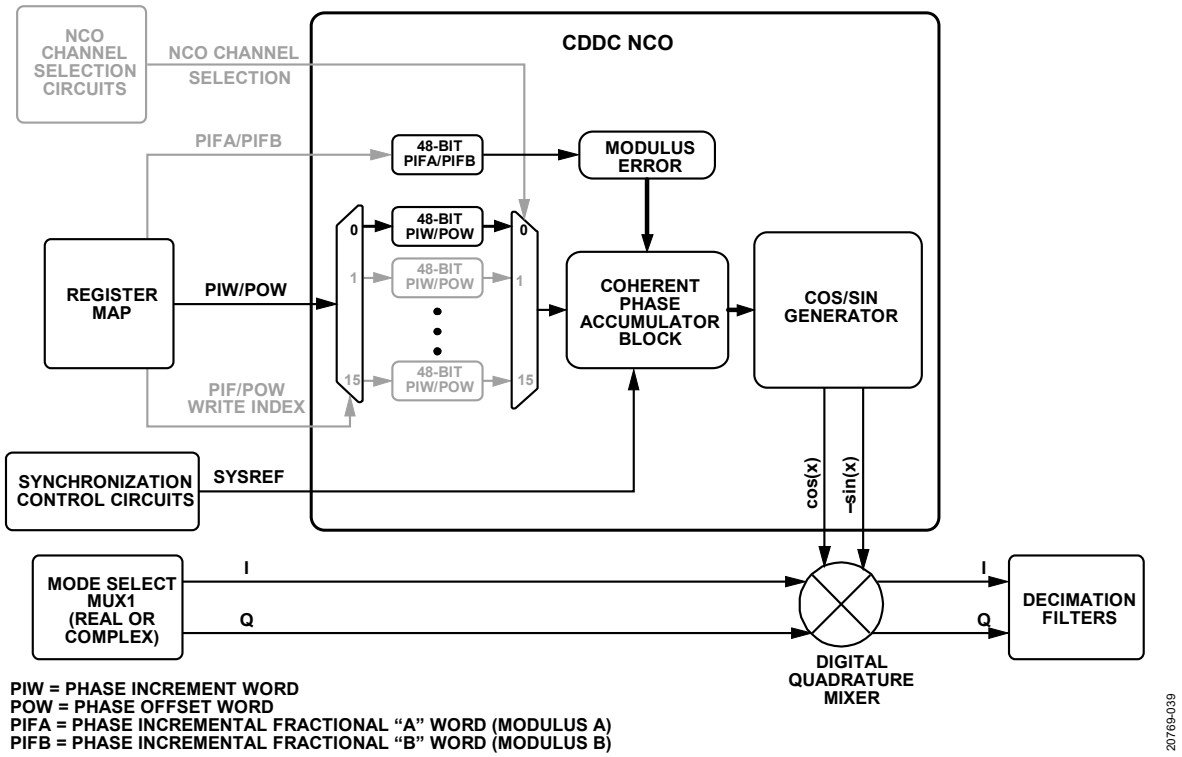

Figure 45. NCO Block Diagram with CDDC Stage

Table 30 shows the registers used to configure the NCO frequency and phase settings. Note the difference in terminology used to describe the NCO settings in comparison to the transmit path NCO, where the acronyms of PIW, POW, PIFA, and PIFB are used instead of frequency tuning word (FTW), PHASE_OFFSET, ACC_MODULUS, and ACC_DELTA. The NCO frequency value is determined by the following settings:

- A 48-bit, twos complement number entered in the PIW that represents the phase increment word, which is also known as the FTW.
- A 48-bit, unsigned number entered in the PIFA that represents the phase increment fractional numerator word.
- A 48-bit, unsigned number entered in the PIFB that represents the phase increment fractional denominator word.

Table 30. Main Datapath CDDC NCO Registers

Address	Register Name	Description
0x0A00	COARSE_DDC_SYNC_CTRL	Software and hardware synchronization options
0x0A03	COARSE_DDC_NCO_CTRL	Channel selection control (for FFH operation)
0x0A04	COARSE_DDC_PROFILE_CTRL	GPIO or SPI load
0x0A0A to 0x0A05	COARSE_DDC_PHASE_INC	48 bits of PIW
0x0A10 to 0x0A0B	COARSE_DDC_PHASE_OFFSET	48 bits of POW
0x0A16 to 0x0A11	COARSE_DDC_PHASE_INC_FRAC_A	48 bits of PIFA
0x0A1C to 0x0A17	COARSE_DDC_PHASE_INC_FRAC_B	48 bits of PIFB
0x0A1D	COARSE_DDC_TRANSFER_STATUS	DDC chip transfer status. Bit 0
0x0A1F	COARSE_DDC_TRANSFER_CTRL	DDC chip transfer. Bit 0

The NCO initial phase value is determined by a 48-bit, twos complement number entered in the POW that represents the phase offset. This value can create a known phase relationship between multiple chips or between individual DDC channels inside the chip.

To allow all NCOs to simultaneously update in the main receive datapath, a main/subordinate implementation is used to transfer the PIW, POW, PIFA, and PIFB settings. Transfer control can be either under software control (via SPI) or hardware control (via the GPIO pin). Hardware control allows different profile settings to be loaded quickly with more precise timing accuracy. For software control, set the self clearing Bit 0 of the COARSE_DDC_ TRANSFER_CTRL register to 1 to update all NCOs.

RECEIVE INPUT AND DIGITAL DATAPATH

The status of the transfer can be read back from Bit 0 of the COARSE_DDC_TRANSFER_STATUS register if confirmation of the transfer is desired.

Frequencies between $-f_{ADC}/2$ and $+f_{ADC}/2$ ($f_{ADC}/2$ is excluded) are represented using the following values:

- PIW = 0x8000_0000_0000 and PIFA = 0x0000_0000_0000 represent a frequency of $-f_{ADC}/2$.
- PIW = 0x0000_0000_0000 and PIFA = 0x0000_0000_0000 represent DC (frequency is 0 Hz).
- PIW = 0x7FFF_FFFF_FFFF and PIFA = 0x0000_0000_0000 represent a frequency of just below $+f_{ADC}/2$.

Each NCO contains a separate phase accumulator word (PAW). The initial reset value of each PAW is set to zero and incremented every clock cycle. The instantaneous phase of the NCO is calculated using the PAW, PIW, PIFA, PIFB, and POW. This architecture allows the PIW and POW registers to be updated at any time and still maintain deterministic phase results in the PAW of the NCO while in programmable dual modulus or integer-N mode. However, in the dual modulus mode, the user must carry out the following procedure to update the PIFA and/or the PIFB registers to ensure proper NCO operation:

- Write to the PIFA and PIFB registers for all DDCs.
- Either toggle the COARSE_DDC_SOFT_RESET bit in Register 0xA00 (Bit 4) or assert the SYSREFP/SYSREFN pin to synchronize the NCOs.

CDDC NCO Configuration APIs

The API library fully supports configuration of the receive main datapaths. The top level API adi_adxxxx_device_startup_rx configures the receive main datapath. In addition, the functions in Table 32 allow the user to manually configure each block of the receive main datapath as described in the Receive Main Digital Datapath section. Table 32 details the supported APIs for the configuration of Mux1.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 31. Main CDDC NCO Synchronization APIs

Function	Description
adi_adxxxx_device_startup_rx	Function to configure the full receive datapath including the main CDDC datapaths
adi_adxxxx_adc_ddc_coarse_nco_mode_set	Function to set main datapath CDDC NCO mode of operation as described in this section

CDDC NCO Synchronization Options

To simultaneously reset all main datapath NCO phase accumulators to the initial POW defined for each NCO via software (via SPI write operation) or hardware (via external SYSREF signal), set the COARSE_DDC_TRIG_NCO_ RESET_EN bit (Bit 7) in the COARSE_DDC_SYNC_CTRL register. When an asynchronous SPI generated signal is acceptable to synchronize all main datapath NCOs, consider the SPI software reset option. To reset the NCOs, set the COARSE_DDC_SOFT_ RESET bit (Bit 4) to 1 to hold the NCOs in a reset state, then set the same bit to 0 to release the NCOs.

For deterministic latency, multichip synchronization, or synchronization to an external event, an external SYSREF signal is required for proper synchronization of the NCOs (as well as internal digital clocks that include the LMFC). The COARSE_ DDC_SYNC_CTRL register is used to configure this method of NCO synchronization. Within this register, set the COARSE_ DDC_SYNC_EN bit (Bit 0) to 1 to use the external SYSREF signal, then set the COARSE_DDC_SYNC_NEXT bit (Bit 1) to 0 for continuous mode or 1 for next valid edge SYSREF mode.

The internal clocking relationship between the main datapath CDDCs cause a default phase offset between the coarse NCOs in CDDC0 and CDDC1 with respect to the coarse NCOs in CDDC2 and CDDC3. To negate this phase offset existing across DDCs and to get all NCOs aligned by reset, the following programming is recommended. Program the POW phase offset associated with the NCOs pertaining to CDDC0 and CDDC1 to a value that is 8×PIW higher than the POW value associated with NCOs pertaining to CDDC2 and CDDC3. Note that the default POW for all NCOs is 0°.

CDDC NCO Synchronization Options API

The API library supports the CDDC NCO synchronization functions listed in Table 32.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Table 32. CDDC NCO Synchronization APIs

Function	Description
adi_ad9081_adc_ddc_coarse_trig_nco_reset_enable_set	Function to reset the main datapath NCO phase accumulators
adi_ad9081_adc_ddc_coarse_reset_set	Function to hold and release the NCOs in reset state
adi_ad9081_adc_ddc_coarse_sync_enable_set	Function to enable use of SYSREF for CDDC NCO synchronization
adi_ad9081_adc_ddc_coarse_sync_next_set	Function to configure use of SYSREF for CDDC NCO synchronization
adi_ad9081_adc_ddc_coarse_nco_phase_offset_set	Function to configure CDDC NCO phase offset

NCO Setting Consideration for Homodyne Transmit-to-Receive Loopback Applications.

Applications such as digital predistortion, where the transmitted signal is observed by the receiver, require absolute phase stability, such that the recovered signal from a transmitted unmodulated CW carrier experiences no phase drift due to transmit and receive NCO settings that are slightly misaligned. Misalignment can occur if the ratio between the DAC and ADC sample rate is not considered when setting the NCO frequency settings in the transmit and receive datapaths. If the ADC sample rate is a factor of two (or four) less than the DAC rate, set the LSB (or lower two LSBs) of the receive NCO integer-N setting to 0 to allow the tuning resolutions relative to the DAC rate to remain matched.

NCO Dual Modulus Mode

This mode operates in a fractional-N mode and automatically enables when the PIFA is set to a nonzero value to provide a tuning accuracy resolution of >48 bits. An example of a rational frequency synthesis requirement that requires >48 bits of accuracy is a carrier frequency of 1/3 the sample rate. When a frequency accuracy of ≤48 bits is acceptable, integer-N mode is more suitable because this mode also supports phase coherent switching when changing NCO frequencies. For programmable dual modulus mode, set the PIFA to a nonzero value (not equal to 0x0000_0000_0000) and use the following equations (for more information on the programmable modulus feature, see the AN-953 Application Note, *Direct Digital Synthesis (DDS) with a Programmable Modulus*):

$$\frac{\mathrm{mod}(f_C, f_{ADC})}{f_{ADC}} = \frac{M}{N} = \frac{PIW + \frac{PIFA}{PIFB}}{2^{48}} \quad (1)$$

$$FTW = floor\left(2^{48}\frac{\mathrm{mod}(f_C,\ f_{ADC})}{f_{ADC}}\right) \quad (2)$$

$PIFA = \mathrm{mod}(2^{48} \times M, N)$ (3)

$PIFB = N$ (4)

where:

f_C is the desired carrier frequency.

M is the integer representing the rational numerator of the frequency ratio.

N is the integer representing the rational denominator of the frequency ratio.

Note that Equation 1 to Equation 4 apply to the aliasing of signals in the digital domain, that is, the aliasing introduced when digitizing analog signals. M, N, PIFA, and PIFB are integers reduced to the lowest terms.

For example, if the f_{ADC} is 3000 MSPS and f_C is 1001.5 MHz,

$$\frac{\mathrm{mod}(1001.5,\ 3000)}{3000} = \frac{M}{N} = \frac{2003}{6000} \quad (3)$$

$$PIW = floor\left(2^{48}\frac{\mathrm{mod}(1001.5,\ 3000)}{3000}\right) = 0\text{x}5576\_19\text{F}0\_\text{FB}38 \quad (4)$$

$PIFA = \mathrm{mod}(2^{48} \times 2003, 6000) = 0\text{x}0000\_0000\_0\text{F}80$

$PIFB = 0\text{x}0000\_0000\_1770$

To calculate the actual carrier frequency (f_{C_ACTUAL}) in this case, use the following equation:

RECEIVE INPUT AND DIGITAL DATAPATH

$$f_{C\_ACTUAL} = \frac{PIW + \frac{PIFA}{PIFB} \times f_{ADC}}{2^{48}} \quad (5)$$

In the case of this example, the f_{C_ACTUAL} is as follows:

$$f_{C\_ACTUAL} = \frac{0x5576\_19F0\_FB38 \times \frac{0x0000\_0000\_0F80}{0x0000\_0000\_1770}}{2^{48}} = 1001.5\text{MHz} \quad (6)$$

NCO Integer-N Mode

Integer-N mode is the default NCO setting and provides a 48-bit tuning resolution. This mode is automatically enabled when the NCO PIFA setting is set to all 0s. In this mode, calculate the NCO PIW with the following equation:

$$PIW = round(2^{48}\frac{\text{mod}(f_C, f_{ADC})}{f_{ADC}}) \quad (5)$$

Note that Equation 5 applies to the aliasing of signals in the digital domain, that is, the aliasing introduced when digitizing analog signals.

For example, if the f_{ADC} is 3000 MSPS and the f_C is 416.667 MHz,

$$PIW = round(2^{48}\frac{\text{mod}(416.667, 3000)}{3000}) = 0x2EC6\_C03A\_8E23 \quad (7)$$

To calculate the f_{C_ACTUAL} in this case, use the following equation:

$$f_{C\_ACTUAL} = \frac{PIW \times f_{ADC}}{2^{48}} \quad (8)$$

where the resulting f_{C_ACTUAL} value is as follows:

$f_{C\_ACTUAL} = \frac{416.667 \times 3000}{2^{48}}$ = 416.66699 MHz

CDDC Variable IF Dual Modulus Mode and Integer-N Mode APIs

The API library fully supports configuration of the receive main datapaths including NCO. The top level API function adi_adxxxx_device_start-up_rx configures the receive main CDDC. In addition, the API has functions that allow the user to manually configure CDDC NCOs as described in these sections. Table 33 lists the supported APIs for configuration of CDDC variable IF dual modulus mode and integer-N mode.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

The API also supports variable IF dual modulus (fractional-N) mode and the integer-N mode via the adi_ad9081_adc_ddc_ coarse_nco_ftw_set function, which is contained in the **adi_adxxxx_adc.c** file.

Transfer control and status are supported by the adi_ad9081_ adc_ddc_coarse_chip_xfer_set and adi_ad9081_adc_ddc_coarse_ chip_xfer_status_get functions, which are also contained in the **adi_adxxxx_adc.c** file.

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

RECEIVE INPUT AND DIGITAL DATAPATH

Table 33. Main Datapath Configuration APIs

Function	Description
adi_adxxxx_device_startup_rx	Function to configure the full receive datapath including the main CDDC datapaths
adi_ad9081_adc_ddc_coarse_nco_ftw_set	Function to set the main datapath CDDC NCO mode of operation as described in this section
adi_ad9081_adc_ddc_coarse_chip_xfer_set	Function to set the transfer control configuration
adi_ad9081_adc_ddc_coarse_chip_xfer_status_get	Function to get the transfer control configuration

Optional Fractional Delay for Receive Main Datapath 0 or Receive Main Datapath 3 Only

For the Receive Main Datapath 0 or Receive Main Datapath 3 only, a bypassable fractional delay block with a resolution of $1/(f_{ADC}/16)$ and tuning range of −8 steps to +7 steps relative to $1/(f_{ADC}/16)$ can be switched into the datapath between the NCO and decimator blocks. Fractional delay compensation is useful either for a direction conversion receiver to compensate for timing skew between the I and Q baseband input signals, or in digital predistortion applications where the timing alignment between the captured portion of a transmitted signal influences the level of nonlinearity compensation achieved by many algorithms.

The fractional delay block consists of 16 parallel FIR delay filters with the first filter imparting a −0.5 cycle shift. Each subsequent filter providing an additional 1/16 cycle shift results in a programable span of −0.5 cycles to +7/16 cycles with a cycle corresponding to $1/f_{ADC}$. A 16:1 multiplexer determines which filter output is selected, which is the reason for the delay.

Up to four different fractional delay settings can be stored and quickly loaded under GPIO or SPI control with each setting designated as FSHIFTx, where x = 0, 1, 2, or 3. The filters are specified to have <0.1 dB ripple and group delay accuracy of $<150/f_{ADC}$ over 80% of the filter bandwidth. Lastly, an inherent 5-cycle delay is incurred because of the implementation and is additive relative to the programable cyclic delay.

To enable the fractional delay block, take the following steps prior to enabling the internal digital datapath clocks:

- Set the FDELAY_IO_MUX_SEL bit in Register 0x0B18 (Bit 0) to 0 to select Receive Main Datapath 0 or set the bit to 1 to select Receive Main Datapath 3.
- Set the EQ_UPSAMP_CLK_SEL bit in Register 0x0B06 (Bit 5) to the corresponding JESD204B/C transmitter link (0 or 1) that the selected receive main datapath uses.
- Set the FD_EN bit in Register 0x0B06 (Bit 3) to 1 to enable the complete fractional delay block.

Take the following programming steps at any point in time to change the delay settings:

- Program the FSHIFTx delay settings in Register 0x0B07 through Register 0xB0A, Bits[3:0]. Note that only the FSHIFT0 delay must be programmed if fast switching between delay values is not required.
- When fast switching between fractional delay values is desired, set the FD_GPIO_EN bit in Register 0x0B06 (Bit 2) to 1 to select GPIO pin control. Note that the default bit value is 0, which corresponds to the FDSEL value in Register 0x0B06, Bits[1:0], and determines which preprogrammed FSHIFTx value is selected. See Table 125 for more information on GPIOx pin mapping.

The fast switching fractional delay feature often coexists with the programable finite impulse response (FIR) filter used to compensate for (or equalize) channel impairments in the RF receive path where the outputs of several power amplifiers are observed with a single receive observation path via time multiplexing. In such applications, the delay (and equalization) characteristics can vary between the outputs of the different power amplifiers, which makes having distinct settings associated with each power amplifier observation path advantageous. For this reason, the fractional delay block (like the PFILT block) can be loaded with four different settings within 15 ns via the two GPIO pins.

Main Datapath Decimation Stage

The cascaded decimation filter line up shown in Figure 46 provides a selectable decimation factor of 2, 3, 4, and 6, as well as a bypass option (or 1) based on the COARSE_DEC_SEL setting in Register 0x0282, Bits[3:0]. Table 34 shows the characteristics of each filter pair relative to the decimated f_{IQ_OUT}. The usable pass band is the frequency band over which the response maintains a pass-band ripple of less than ±0.001 dB with an alias (or image) rejection greater than 100 dB. Note that the pass band for a single filter when driven with a real input is half of the complex pass band. Table 35 shows the filter line up used to achieve the different decimation factors with the resulting I/Q output data rate and usable pass band assuming an ADC sample rate of 3000 MSPS.

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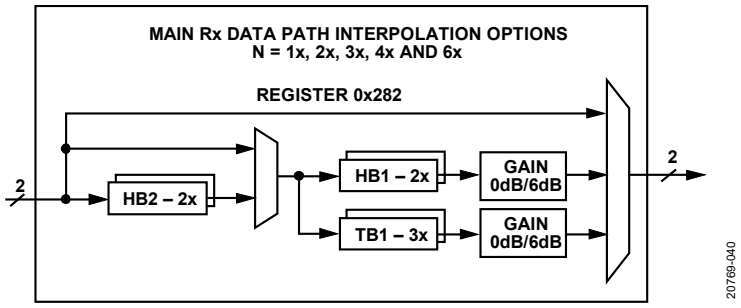

Figure 46. Main Datapath Decimation Filter Lineup

Table 34. Main Datapath Decimation Filter Characteristics

Filter Name	Decimation Ratio	Pass Band (% of f_{IQ_OUT})
HB2	2	40.7
HB1	2	81.4
TB1	3	81.4

Table 35. I/Q Output Data Rate and Usable Complex Pass Band vs. Decimation Ratio with f_{ADC} = 3000 MSPS and 6000 MSPS

		f_{ADC} = 3000 MSPS		f_{ADC} = 6000 MSPS	
DDC Ratio	Filter Use	f_{IQ_OUT} (MSPS)	Pass Band (MHz)	f_{IQ_OUT} (MSPS)	Pass Band (MHz)
2	HB1	1500	1221	3000	2442
3	TB1	1000	814	2000	1628
4	HB2 + HB1	750	610	1500	1221
6	HB2 + TB1	500	407	1000	814

Main Datapath Decimation API

The API library fully supports the configuration of the receive main datapaths including decimation blocks. The top level API function adi_adxxxx_device_startup_rx configures decimation per the use case described by its parameter. In addition, the API has functions that allows the user to manually configure CDDC decimation blocks as described in these sections. details the supported APIs for configuration of CDDC decimation modes.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 36. Main Datapath Configuration APIs

Function	Description
adi_adxxxx_device_startup_rx	Function to configure the full receive datapath, including the main CDDC datapaths
adi_ad9081_adc_ddc_coarse_dcm_set	Function to set the main datapath CDDC decimation

Bypassable 6 dB Gain Stage and Complex to Real Conversion

Each main datapath contains a bypassable, controlled gain stage and a C2R data translation block. These two features are controlled by the COARSE_GAIN and COARSE_C2R_EN bits (Bits[5:4]) in Register 0x0282.

The gain is selectable as either 0 dB or 6 dB and compensates for the 6 dB loss in the signal level incurred when downconverting a real input signal, because the undesired sideband image is typically filtered by the decimation filters (assuming it falls in the stop band region) that follow the mixing stage. Only enable this gain stage if the channelizer datapath is bypassed. If the channelizer datapath is also enabled, enable this similar functional block in this stage instead to prevent possible digital overflow because of excessive gain if 6 dB gain is applied in both stages.

The C2R block can only be enabled for decimation factors of 2 or 4 because of the implementation. The block reuses the last half-band filter in the filtering stage with an $f_S/4$ complex mixer to upconvert the signal. When the signal is upconverted, the Q output from the complex mixer is disregarded and the I output represents the real output.

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Main Datapath 6 dB Gain Stage and Complex-to-Real Conversion API

The API library fully supports configuration of the receive main datapaths, including decimation blocks. The top level API function adi_adxxxx_device_startup_rx configures the C2R conversion per the use case described by its parameters. In addition, the API has functions that allow the user to manually configure C2R conversion blocks as described in these sections. There is also an API function that allows the application to enable or disable the 6 dB gain. Table 37 details the supported APIs for the configuration of CDDC decimation modes.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 37. Main Datapath 6 dB Gain and Complex to Real Conversion Configuration APIs

Function	Description
adi_adxxxx_device_startup_rx	Function to configure the full receive datapath, including the main CDDC datapaths
adi_adxxxx_adc_ddc_coarse_gain_set	Function to set the main datapath CDDC decimation

Mux2

Mux2 is a dual 2×4 crossbar multiplexer, shown in Figure 47, that defines the mapping of complex data transferred between the four receive main path outputs and the eight channelizer inputs. This mapping has the CDDC0 and CDDC1 outputs assigned to the FDDC of Channelizer 0 to Channelizer 3, and the CDDC2 and CDDC3 are assigned to Channelizer 0 to Channelizer 4 (or FDDC4 to FDDC7). The COARSE_FINE_CB register (Register 0x0281) is used to configure this dual crossbar multiplexer.

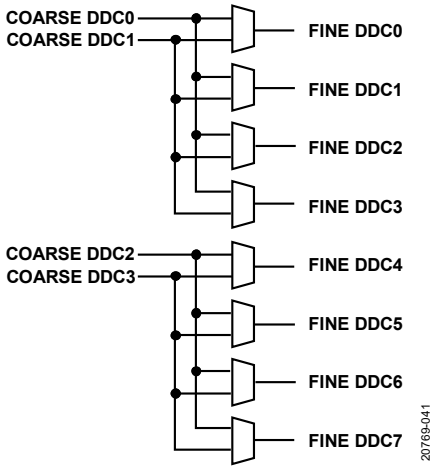

Figure 47. Dual 2×4 Crossbar Multiplexer

The receive channelizer datapath shown in Figure 48 consists of eight identical FDDCs followed by a C2R stage and optional upsampler stage. Each FDDC consists of a quadrature digital downconversion stage for frequency translation of only complex signals with a data rate no greater than 1500 MSPS with a selectable decimation filter for data rate reduction and filtering. Bypassable gain compensation, C2R data translation, and an optional upsampler are also included. The FINE_DDC_PAGE register (Register 0x0019) is used to configure each main channelizer path independently. To disable unused channelizer datapaths, use the FINE_DDC_EN bits (Register 0x0286, Bits[7:0]).

MUX2 APIs

The API library fully supports configuration of Mux2. The top level API function adi_adxxxx_device_startup_rx configures the C2R conversion per the use case described by its parameters. In addition, the API has functions that allow the user to manually configure Mux2 as described in this section. Table 38 details the supported APIs for the configuration of Mux2.

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Table 38. Mux2 APIs

Function	Description
adi_adxxxx_device_startup_rx	Function to configure the full receive datapath, including the main CDDC datapaths
adi_txfe_adc_xbar_set	Function to set Mux1 and Mux2 configuration
adi_txfe_adc_cddc2fddc_xbar_set	Function to set Mux2
adi_txfe_adc_xbar_get	Function to get Mux1 and Mux2 settings
adi_txfe_adc_xbar_find_cddc	Function to retrieve CDDC connected to FDDC

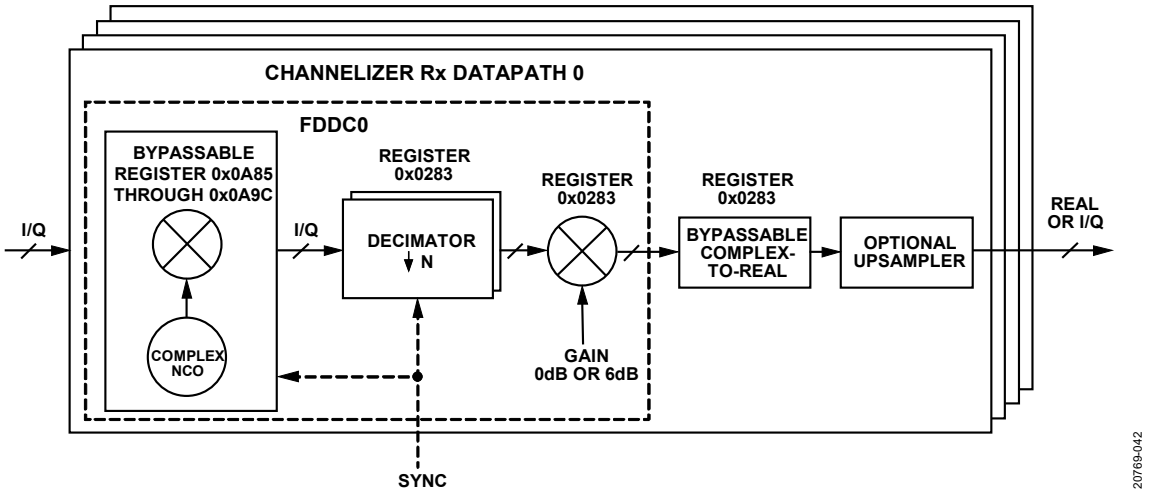

Figure 48. Channelizer Digital Datapath Block Diagram

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Receive Channelizer Fine Digital Downconverter

Frequency translation is accomplished with a complex NCO and a digital quadrature mixer where a real or complex input spectrum is multiplied by the $e^{-j\omega ct}$ output, which centers the desired signal complex output spectrum around dc. Like the main datapath CDDC, each FDDC frequency translation stage can be controlled individually and supports four different IF modes based on the FINE_MXR_IF bit field setting in Register 0x0283, Bits[7:6].

These IF modes and the corresponding FINE_MXR_IF bit settings include the following:

- Variable IF mode: Set the FINE_MXR_IF bits to 00 to enable this mode.
- $F_S/4$ IF mode: Set the FINE_MXR_IF bits to 10 to enable this mode.
- ZIF mode: Set the FINE_MXR_IF bits to 01 to enable this mode.
- Test mode: Set the FINE_MXR_IF bits to 11 to enable this mode.
- These FDDC NCO modes are equivalent to the modes described in the Main Datapath CDDC section for the CDDC NCO.

Receive Channelizer Digital Datapath API

The API library fully supports configuration of FDDC NCOs. The top level API function adi_adxxxx_device_startup_rx configures FDDC NCOs conversion per the use case described by its parameters. In addition, the API has functions that allow the user to manually configure FDDC NCO as described in this section. Table 39 provides an overview of these functions.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Table 39. FDDC NCO APIs

Function	Description
adi_adxxxx_device_startup_rx	Function to configure the full receive datapath, including the channelizer FDDC datapaths
adi_adxxxx_adc_ddc_fine_nco_enable_set	Function to enable or disable fine NCO in channelizer datapaths

FDDC Variable IF NCO Operating Modes

The NCO in the FDDC shown in Figure 49 is the same core design used for the CDDC, and the operation is the same except that a different set of registers are designated with the prefix FINE (as opposed to COARSE). Refer to the CDDC Variable IF NCO Operating Modes section for a more detailed version of the description that follows. Note that the data rate into the receive channelizer (f_{IQ_IN}) is equal to the data rate out of the receive main datapath (f_{IQ_OUT}), which is also equal to f_{ADC}/M_{RX}. For this reason, the tuning range for the NCO in the FDDC is specified to be between $-f_{IQ\_IN}/2$ and $+f_{IQ\_IN}/2$ with the equations used to determine the NCO setting values based on f_{IQ_IN}.

The 48-bit complex NCO supports integer-N and dual modulus, where PIW and POW words are used to define the frequency tuning and phase offset setting, and PIFA and PIFB are used for the modulus setting when operating in dual modulus mode. The registers used to define these settings as well as other relevant NCO settings used for control options are shown in Table 40. Note that a main/subordinate implementation is also used to update all receive channelizer NCOs simultaneously using SPI control by setting the self clearing Bit 0 to 1 in the FINE_DDC_TRANSFER_ CTRL register with the option to readback Bit 0 in the FINE_ DDC_TRANSFER_STATUS register to confirm the transfer.

Table 40. Channelizer Data Path FDDC NCO Registers

Address	Register Name	Description
0x0A80	FINE_DDC_SYNC_CTRL	Software and hardware synchronization options
0x0A83	FINE_DDC_NCO_CTRL	Channel selection control (for FFH operation)
0x0A84	FINE_DDC_PROFILE_CTRL	GPIO or SPI load
0x0A8A to 0x0A85	FINE_DDC_PHASE_INC	PIW
0x0A90 to 0x0A8B	FINE_DDC_PHASE_OFFSET	POW
0x0A96 to 0x0A91	FINE_DDC_PHASE_INC_FRAC_A	PIFA
0x0A9C to 0x0A97	FINE_DDC_PHASE_INC_FRAC_B	PIFB
0x0A9D	FINE_DDC_TRANSFER_STATUS	DDC chip transfer status bit (read only)
0x0A9F	FINE_DDC_TRANSFER_CTRL	DDC chip transfer bit

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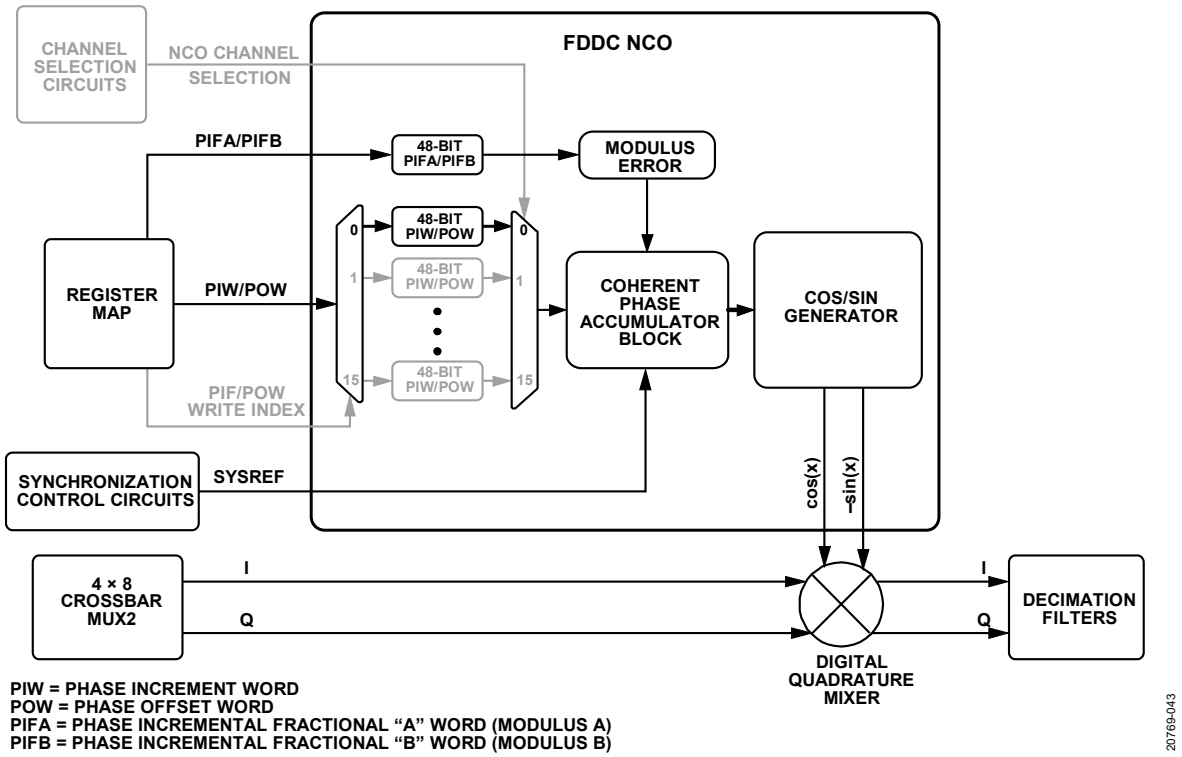

Figure 49. Fine NCO Block Diagram with FDDC Stage

NCO Synchronization Options for FDDC

The phase accumulators of all channelizer datapath NCOs can be reset simultaneously via the software (via SPIO) or via the hardware (via the external SYSREF signal). To reset the accumulators simultaneously, set the FINE_DDC_TRIG_NCO_ RESET_EN bit (Bit 7) in the FINE_DDC_SYNC_CTRL register. When an asynchronous SPI generated signal is acceptable to synchronize all main datapath NCOs, consider the SPI software reset option. To reset the NCOs, set the FINE_DDC_SOFT_ RESET bit (Bit 4) to 1 to hold the NCOs in a reset state, then set the same bit to 0 to release the NCOs.

For multichip synchronization or synchronization to an external event, an external SYSREF signal is required for proper NCO synchronization, as well as internal digital clocks that include the LMFC. To enable this method of NCO synchronization, first set the FINE_DDC_SYNC_EN bit to 1 to use the external SYSREF signal. Then set the FINE_DDC_SYNC_NEXT bit (Bit 1) either to 0 for continuous mode or 1 for next valid edge SYSREF mode.

NCO Synchronization Options for FDDC API

The API supports FDDC NCO synchronization via the APIs listed in Table 41.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 41. FDDC NCO Synchronization APIs

Function	Description
adi_txfe_adc_ddc_fine_reset_set	Function to reset the FDDC NCOs in the channelizer datapaths

NCO Dual Modulus Mode for FDDC

This mode of operation provides a tuning accuracy resolution of >48 bits by operating in a fractional-N mode and is automatically enabled when the PIFA is set to a nonzero value. For programable dual modulus mode, set the PIFA to a nonzero value (not equal to 0x0000_0000_0000)

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and satisfy the following four equations (for more information on the programable modulus feature, see the AN-953 Application Note, *Direct Digital Synthesis (DDS) with a Programmable Modulus*):

$$\frac{\mathrm{mod}(f_C, f_{IQ\_IN})}{f_{IQ\_IN}} = \frac{M}{N} = \frac{PIW + \frac{PIFA}{PIFB}}{2^{48}} \quad (6)$$

$$FTW = floor(2^{48}\frac{\mathrm{mod}(f_C, f_{IQ\_IN})}{f_{IQ\_IN}}) \quad (7)$$

$PIFA = \mathrm{mod}(2^{48} \times M, N)$ (8)

$PIFB = N$ (9)

NCO Integer-N Mode for FDDC

Integer-N mode is the default setting for the FDDC NCOs and is automatically applied when the NCO PIFA setting is set to all 0s. In this mode, calculate the NCO PIW with the following equation:

$$PIW = round(2^{48}\frac{\mathrm{mod}(f_C, f_{IQ\_IN})}{f_{IQ\_IN}}) \quad (10)$$

FDDC Variable IF Dual Modulus Mode and Integer-N Mode API

The API library fully supports configuration of FDDC NCOs. The top level API function adi_adxxxx_device_startup_rx configures FDDC NCOs conversion per the use case described by its parameters. In addition, the FDDC NCO can be manually configure with the target APIs that are detailed in Table 42.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 42. FDDC Variable IF Dual Modulus and Integer-N Mode APIs

Function	Description
adi_adxxxx_device_startup_rx	Function to configure the full receive datapath, including the channelizer FDDC NCOs
adi_adxxxx_adc_ddc_fine_nco_ftw_set	Function to configure the FDDC NCO for variable IF dual modulus (fractional-N) mode and the integer-N mode
adi_adxxxx_adc_ddc_fine_chip_xfer_set	Function to update the phase increment and phase offset settings
adi_adxxxx_adc_ddc_fine_chip_xfer_status_get	Function to indicate when the phase data and offset data transfer is complete

Receive Channelizer Decimation Stage

The cascaded decimation filter lineup shown in Figure 50 provides a selectable decimation factor of 2, 3, 4, 6, 8, 12, 16, and 24 as well as a bypass option (or 1) based on the FINE_DEC_SEL setting in Register 0x0283, Bits[2:0]. The maximum f_{IQ_IN} into this decimation stage is limited to 1500 MSPS. Table 44 shows the characteristics with f_{IQ_IN} equal to 1500 MSPS for each decimation factor.

The usable pass band is the frequency band over which the response maintains a pass-band ripple of less than ±0.001 dB with an alias (or image) rejection of >100 dB. Note that the pass band for a single filter when driven with a real input is half of the complex pass band. Table 44 shows the filter line up used to achieve the different decimation factors where the resulting I/Q output data rate and usable pass band assume a maximum input I/Q rate of 1500 MSPS.

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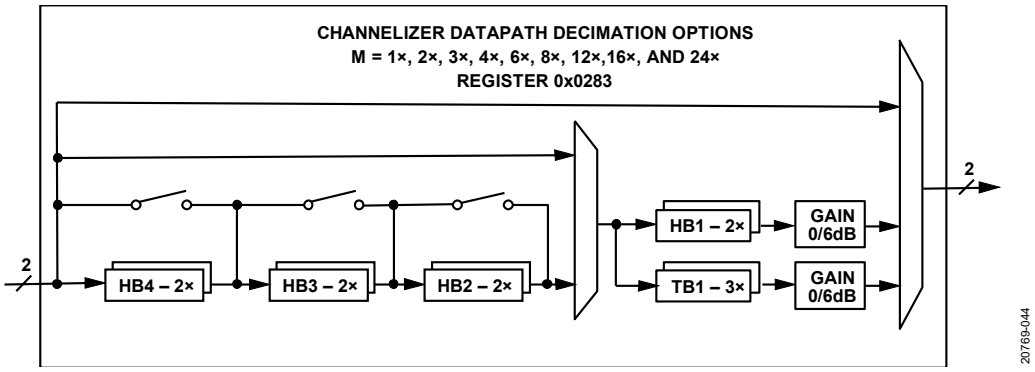

Figure 50. Receive Channelizer Datapath Decimation Filter Lineup

Table 43. Channelizer Decimation Filter Characteristics

Filter Name	Decimation Ratio	Pass Band (% of f_{IQ_OUT})
HB4	2	0.102
HB3	2	0.204
HB2	2	0.407
HB1	2	0.814x
TB1	3	0.814

Table 44. DDC Filter Configurations vs. Decimation Ratio/ Usable Complex Passband vs. Data Rate with f_{IQ_IN} = 1500 MSPS

Decimation Ratio	Filter Lineup	f_{IQ_OUT} (MSPS)	Pass Band (MHz)
2	HB1	750.0	610.5
3	TB1	500.0	407.0
4	HB2 + HB1	375.0	305.3
6	HB2 + TB1	250.0	203.5
8	HB3 + HB2 + HB1	187.5	152.6
12	HB3 + HB2 + TB1	125.0	101.8
16	HB4 + HB3 + HB2 + HB1	93.8	76.3
24	HB4 + HB3 + HB2 + TB1	62.5	50.9

Receive Channelizer Decimation API

The API library fully supports configuration of the receive channelizer decimation filters. The top level API function adi_adxxxx_device_start-up_rx configures the FDDC decimation filter per the use case described by its parameters. In addition, the channelizer decimation filters can be manually configured with the target APIs that are listed in Table 45.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 45. Receive Channelizer Decimation APIs

Function	Description
adi_adxxxx_device_startup_rx	Function to configure the full receive datapath, including the channelizer decimation filters
adi_adxxxx_adc_ddc_fine_dcm_set	Function to configure the FDDC decimation filter

Bypassable 6 dB Gain Stage and C2R Conversion

Each receive channelizer path contains a 6 dB gain stage and C2R conversion block. These blocks can be bypassed if not they are not needed and can be independently controlled. These features are controlled by the FINE_GAIN and FINE_C2R_EN bits, Bits[5:4], in Register 0x0283.

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The gain is selectable as either 0 dB or 6 dB and compensates for the 6 dB loss in signal incurred when downconverting a real input signal with the associated sideband image sufficiently filtered via the decimation filter(s) in the signal path. To prevent possible overflow, only apply the 6 dB compensation to the receive channelizer and disable the compensation to the receive main datapath.

The C2R block can only be enabled for channelizer decimation factors that have the form of 2^N because of the implementation. The block reuses the last half-band filter in the filtering stage with an $f_S/4$ complex mixer to upconvert the signal. When the signal is upconverted, the Q output from the complex mixer is disregarded and the I output represents the real output. Note that the total decimation factor programmed into the DDC_OVERALL_ DECIM register (Address 0x0284) must be one half of what is calculated based on the M_{RX} and N_{RX} decimation factor settings because the real data that appears on the I output is twice the rate when the C2R block is disabled.

Channelizer 6 dB Gain Stage and Complex-to-Real Conversion API

The API library fully supports configuration of the receive channelizer, including the 6 dB gain stage and the C2R conversion blocks. The top level API function adi_adxxxx_device_startup_rx configures the proper chip decimation and C2R conversion block per the use case described by its parameters. In addition, the chip decimation, 6 dB gain stage, and the C2R conversion block can be manually configured via the API. Table 46 lists the APIs provided to support these blocks.

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 46. Channelizer 6 dB Gain Stage and Complex-to-Real Conversion APIs

Function	Description
adi_adxxxx_device_startup_rx	Function to configure the full receive datapath, including the channelizer decimation filters
adi_adxxxx_adc_chip_dcm_ratio_set	Function to configure the total decimation factor for the receive datapath
adi_adxxxx_adc_chip_dcm_ratio_get	Function to read back the configured total decimation factor for the receive datapath
adi_adxxxx_adc_ddc_fine_c2r_set	Function to configure the FDDC complex to real conversion setting

Upsampler

An upsampler block resides after the receive channelizers to match the I/Q data rates of all channelizer outputs assigned to a JESD204B/C link. This feature allows the host processor to still benefit from the on-chip decimation filter capability in cases where different decimation factors are assigned to the channelizers, provided that the decimation factors are related by a factor of 2^N. The upsampler repeats the samples of the lower data rate channels by $2^N - 1$ to match the highest data rate channel and the host processor performs the opposite action of removing these redundant samples to reduce the data rate back to the original rate. For more details on the upsampler operation, see the Receive Datapath Configuration Considerations section.

MUX3 (Data Format and Selection)

Referring to Figure 39, Mux3 consists of two crossbar multiplexers (1 per JESD204B/C transmitter link) used for data formatting and data source selection prior to the JESD204B data router multiplexer. The JTX_PAGE register specifies the multiplexer to be configured with the data format and resolution options listed in Table 47. The DFORMAT_RES selection must match the N value assigned to the JESD204B/C link configuration. The default setting supports twos complement, noninverted, 16-bit data.

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Table 47. Data Formatting Registers

Address	Bits	Bit Name	Description
0x02A3	2	DFORMAT_INV	Set to 1 to invert data
0x02A3	[1:0]	DFORMAT_SEL	Data output format 00: twos complement (default) 01: offset binary 10: gray code 11: reserved
0x02A8	[3:0]	DFORMAT_RES (must match JESD204B/C N value)	Data output resolution 0x0: 16-bit resolution 0x1: 15-bit resolution 0x2: 14-bit resolution 0x3: 13-bit resolution 0x4: 12-bit resolution 0x5: 11-bit resolution 0x6: 10-bit resolution 0x7: 9-bit resolution 0x8: 8-bit resolution 0x9-F: reserved

Because up to 16 virtual converters can be assigned to any link (M = 16), the multiplexer provides 16 outputs designated as $DF_{OUT}0$ to $DF_{OUT}15$ into the JESD204B/C Mux4 router. The input data to any virtual converter can represent data from any one of the following four sources:

- Decimated data from any channelizer or main datapath. This data is typically I/Q data (unless the C2R feature is used) with I and Q data each assigned a virtual converter. Note that if a designated channelizer path is bypassed, the data source becomes the main datapath to which the channelizer is mapped.
- The fractional delay line in the form of I/Q data. This data is down sampled by 8 and requires the FDELAY_ DOWNSAMPLE_EN bit (Register 0x0B06, Bit 4) to be set.
- A test source supporting a different test pattern.
- The undecimated output of a logical ADC that includes any processing by the integer delay or PFILT block. This data source is referenced as a logical ADC output given that a crossbar multiplexer after the ADC can route data to different logical paths. This option is only available for the AD9081 and AD9082 because the data represents the full Nyquist bandwidth of the ADC.

The default setting for Mux3 selects all I/Q output pairs from the eight channelizers. The mapping is in sequential order such that the Channelizer 0 I/Q outputs are mapped to $DF_{OUT}0$ and $DF_{OUT}1$, and the Channelizer 7 I/Q outputs are mapped to $DF_{OUT}14$ and $DF_{OUT}15$ at the end. Any of these outputs can be remapped to a logical ADC output or test source using the 16-bit multiplexer selection registers listed in Table 48. Each bit assignment pertains to the numeric equivalent DF_{OUT}, such that Bit 0 corresponds to $DF_{OUT}0$. This assignment is considered even when selecting a test source pattern. Setting the bit assignment to 1 maps the designated DF_{OUT} to that data source specified by the register name. Note that the same bit assignment of the other data source registers must be assigned a value of 0. If the data source is selected to be a test source, use the TMODE_I_TYPE_SEL and TMODE_Q_TYPE_ SEL bit fields in Register 0x02B0 and Register 0x02D4, respectively, to select the type of test pattern for even and odd assignments of DF_{OUT}, respectively.

Table 48. Data Source Selection Registers

Addess	Register Name	Description
0x02AB	FBW_SEL_0	16-bit register enables a logical ADC output source to be mapped to the designated virtual converter defined by the bit location (valid for the AD9081 and AD9082 only)
0x02AC	FBW_SEL_1	
0x02AD	TMODE_SEL_0	Same as FBW_SEL_0 and FBW_SEL_1, but for direct test mode data source
0x02AE	TMODE_SEL_1	

Although any DF_{OUT} can be assigned to a test source using the TMODE_SEL register, mapping the logical ADC output sources to DF_{OUT} outputs is more restrictive as shown in Table 49. These restrictions include the following:

- Logical ADC output mapping is restricted in that each output can be assigned to any (or all) of the four DF_{OUT} assignments.

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- Because the AD9082 has only two logical ADC outputs designated as ADC0_x and ADC2_x, the other two logical outputs, ADC1_x and ADC3, are not applicable and must be ignored.

Table 49. DF_{OUT} Mapping of Logical ADC Output

Logical ADC Output	DF_{OUT} Bit Assignment for the FBW_SEL Register
ADC0_x	0, 4, 8, 12
ADC1_x	1, 5, 9 ,13
ADC2_x	2, 6, 10,14
ADC3_x	3, 7, 11, 15

Up to three control bits can be appended to the data source payload data depending on the N value assigned to the JESD204B/C link setting. Note that N must be set such that NP − N = CS, where CS designates how many control bits are appended after the Nth bit. The CTRL_0_1_SEL and CTRL_2_SEL registers (Register 0x02A1 and Register 0x02A2, respectively) have 4-bit data fields that define the status bit assigned to each control bit, as shown in Table 50. The DFORMAT_CTRL_ BIT_2_SEL pertains to the 1st control bit that follows the LSB of the payload data when N is set to less than 16, with DFORMAT_ CTRL_BIT_1_SEL and DFORMAT_CTRL_BIT_0_SEL pertaining to the 2nd and 3rd control bits for N = 14 and N = 13. Note that the NCO channel selection bit assignments shown in Table 50 apply to the AD9081 and AD9082 only when configured for receive frequency hopping, and pertain to the receive NCO profile selection of the I/Q data samples.

Table 50. Status Bit Selection Field for Appended Control Bits

Field Name	Status Bit
DFORMAT_CTRL_BIT_n_SEL (where n = 0, 1, or 2)	0x0: overrange bit 0x1: tie low (1'b0) 0x2: signal monitor (SMON) Bit 0x3: fast detect (FD) Bit 0x4: reserved 0x5: SYSREF 0x6: reserved 0x7: reserved 0x8: NCO channel selection Bit 0 0x9: NCO channel selection Bit 1 0xA: NCO channel selection Bit 2 0xB: NCO channel selection Bit 3

MUX3 Data Selection and Data Formatting APIs

The API library supports data formatting resolution and delay configuration functions per the features described in the MUX3 (Data Format and Selection) section.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 51. Mux3 Data Selection and Data Formatting APIs

Function	Description
adi_adxxxx_jesd_tx_format_sel_set	Function to select data formatting, grey code, twos complement, or offset binary
adi_adxxxx_jesd_tx_res_sel_set	Function to set the data output format resolution. Must be set to match JESDB/C N setting
adi_adxxxx_adc_test_mode_config_set	Function to enable test mode data as the logical data source
adi_adxxxx_adc_fractional_delay_down_sample_enable_set	Function to enable the fractional delay.
adi_adxxxx_jesd_tx_fbw_sel_set	Function to manually override the default logical ADC output to virtual converter mapping.

Mux4 (JESD204B/C Transmitter JESD Data Router)

This data router multiplexer maps a specified virtual converter to one of the 16 DFOUT outputs of the data format block (Mux3) using the JTX_PAGE register (Register 0x001A, Bit 0) to specify the link. Mapping is selected in the JTX_CORE_0_ CONVn registers. Register 0x0600 is JTX_CORE_0_CONV0 and represents Virtual Converter 0. Register 0x060F is JTX_ CORE_0_CONV15 and represents Virtual Converter 15. The JESD204B/C parameter, M, specifies the number of virtual converters in a link. Only registers pertaining to Virtual Converter 0 to Virtual Converter M − 1 must be specified, sequentially starting from Virtual Converter 0 (Register 0x0600 JTX_CORE_0_CONV0), and incrementally

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up through Virtual Converter M-1. For these registers, use the JTX_CONV_SEL bit field to select one of the sixteen DFOUT data sources. Refer to Table 61 for more information on these register bit fields.

MUX4 API

The API supports Mux4 link selection with the adi_ad9081_ jesd_tx_link_select_set function. This function is in the **adi_adxxxx_jesd.c** file.

Virtual converter selection and masking is accomplished with the adi_ad9081_jesd_tx_conv_sel_set and adi_ad9081_jesd_ tx_conv_mask_set functions. These functions are in the **adi_adxxxx_jesd.c** file.

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

JESD204B/C TRANSMITTER

Functional Overview

Eight JESD204B/C transmit data lanes are available to transmit the serialized sample data to a digital processing device. The eight JESD204B/C lanes can be combined to form either one (single link) or two (dual link) identical links.

Each link can provide data to an individual datapath with a unique set of channelizers. Both single link and dual link JESD204B/C modes align individual (local) clocks to the same system reference (SYSREF±) and device clock (CLKIN±) signals.

When operating with the 8-bit/10-bit link layer (JESD204B enabled) the SYNC0INB+, SYNC0INB−, SYNC1INB+, and SYNC1INB− signals are specific to the respective JESD204B link, and in dual link mode the two links can operate independently from one another. For example, one link can be powered down while the other link is running. If the 8-bit/10-bit link layer option is selected, the link operation complies to both the JESD204B and JESD204C standards, and the link lane rates can be between 1.5 Gbps and 15.5 Gbps.

The two links can also operate independently from one another when operating with the 64-bit/66-bit link layer (JESD204C enabled) in dual-link mode. If the 64-bit /66-bit link layer option is selected, the link operation complies to the JESD204C standard including the new synchronization process (SYNC0INB+, SYNC0INB−, SYNC1INB+, and SYNC1INB− pins are not used) and the link lane rates can be between 6 Gbps and 24.75 Gbps.

The JESD204B/C serial interface hardware is grouped into three layers: the physical layer, the data link layer, and the transport layer. Figure 51 shows the functional block diagram of the JESD204B/C transmitter.

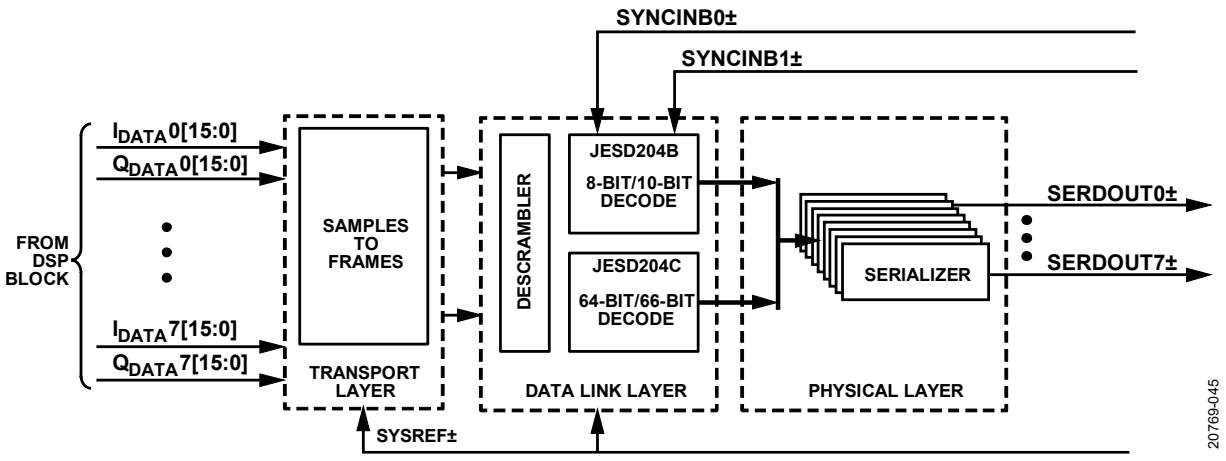

Figure 51. Functional Block Diagram of the JESD204B/C Transmitter

JESD204B/C Transmitter Clock Relationships

The following clock rates are used throughout the rest of the JESD204B/C section. The relationship between any of the clocks can be derived from the following equations:

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- Data Rate = ADC Rate/ Total Decimation
- PCLK Factor = 4/F

For 8-bit/10-bit encoding:

- Lane Rate = (M/L)×NP×(10/8)×Data Rate
- PCLK Rate = Lane Rate/40

For 64-bit/66-bit encoding:

- Lane Rate = (M/L)×NP×(66/64)×Data Rate
- PCLK Rate = Lane Rate/66

The data rate is the rate at which data is sent to the JRx from the JTx, in samples per second (sps)

The lane rate, or the bitrate, is the rate at which sample bits are sent across the physical lanes (SERDOUTx±)

The PCLK rate is the rate of the processing clock (PCLK) that is used for the quad byte framer.

M is the JESD204B/C parameter for converters per link, which is the effective number of converters, or virtual converters, as seen by the JESD204B/C interface (not necessarily equal to the number of ADC cores in the device).

L is the JESD204B/C parameter for lanes per link.

F is the JESD204B/C parameter for octets per frame per lane.

NP is the JESD204B/C parameter for the total number of bits per sample.

Transport Layer

The transport layer packs the data that consists of samples and optional control bits into JESD204B/C frames that are mapped to 8-bit octets. These octets are sent to the data link layer. The transport layer mapping is controlled by rules derived from the link parameters.

For more information on the transport layer, refer to the Analog Devices webcast on the JESD204B transport layer.

Data Link Layer Selection, Selecting the Encode Scheme

The JESD204B/C transmitter in the device DAC path can operate using the 8-bit/10-bit link layer (JESD204B) or the 64-bit/66-bit link layer (JESD204C). To make this selection, use the JTX_LINK_204C_SEL bit field (Register 0x0611, Bits[5:4]), as described in Table 53. When selecting the encoding scheme, the user must select the proper parallel data width (40 vs. 66) for the data being passed to the serializer core using the PARDATAMODE_SER_RC bit field (Register 0x0762, Bits[1:0]). These bits are also described in Table 53.

8-Bit/10-Bit Link Layer

The 8-bit/10-bit data link layer is responsible for the low level functions available to pass data across the link. These functions include optionally scrambling the data, encoding 8-bit octets into 10-bit symbols, and inserting control characters for multichip synchronization, lane alignment, and monitoring.

The data link layer is also responsible for sending the ILAS, which contains the link configuration data used by the receiver to verify the settings in the transport layer.

SYNC0INB± and SYNC1INB± Interface Options

The SYNCxINB receiver input shown in Figure 52 supports DC-coupled, single-ended CMOS logic sources and differential LVDS sources. Table 53 includes the SPI control registers used to configure the SYNC0INB± and SYNC1INB± input settings.

The receiver is only required in the establishment of a JESD204B link (or possible use as a GPIO input) and is powered down by default. For a differential LVDS input, set the register(s) (Register 0x0797 and/or Register 0x0798) to 0x03 and note that the differential, on-chip, 100 Ω termination is also enabled. For single-ended CMOS operation, set the register(s) (Register 0x0797 and/or Register 0x0798) to 0x00 and ensure that the logic input level into SYNCxINB+ does not exceed the DVDD1P8 supply. The register descriptions for Register 0x0797 and

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Register 0x0798 can be found in Table 53. If necessary, use a voltage-divider or level translator to reduce the maximum logic voltage input such that it does not exceed the DVDD1P8 supply.

For CMOS inputs, ensure that the logic input level is referenced to the same DVDD1P8 supply used by the digital CMOS inputs and outputs on the device. When running SYNCxINB± in CMOS mode, connect the CMOS SYNC0INB signal to Pin B13 (SYNC0INB+) and leave Pin A13 (SYNC0INB−) floating. If using dual link mode, follow the same guidance for Pin B12 (SYNC1INB+) and Pin A12 (SYNC1INB−).

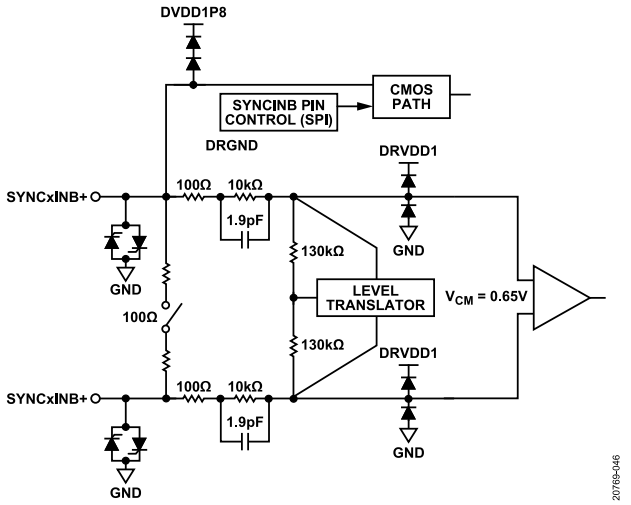

Figure 52. SYNCxINB± Receiver Block Diagram

JESD204B (8-Bit/10-Bit) Link Establishment

The JESD204B transmitter interface of the device operates in Subclass 1, as defined in JESD204B. The link establishment process is divided into the following steps: code group synchronization, ILAS, and user data and error correction.

CGS

The CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver must locate /K28.5/ characters in the input data stream using CDR techniques.

The receiver asserts the SYNCxINB± pins of the device low to issue a synchronization request, and then the JESD204B transmitter begins sending /K/ characters. When the receiver has synchronized, the receiver waits for the correct reception of at least four consecutive /K/ symbols and then deasserts the SYNCxINB± pins. The device transmits an ILAS on the following LMFC boundary.

ILAS

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four multiframes with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS first sends an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 53. The four multiframes include the following:

- Multiframe 1: begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2: begins with an /R/ character followed by a /Q/ character (/K28.4/), followed by link configuration parameters over 14 configuration octets (see Table 52), and then ends with an /A/ character. Many parameter values are of the value – 1 notation.
- Multiframe 3: begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4: begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

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User Data and Error Detection

When the ILAS completes, the user data is sent. Typically, all characters are considered user data within a frame. However, to monitor the frame clock and multiframe clock synchronization, a mechanism replaces characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default but can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/, and any 0x7C character at the end of a multiframe is replaced with an /A/. The JESD204B receiver checks for /F/ and /A/ characters in the received data stream and verifies that these characters only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation using dynamic realignment or by asserting the SYNCxINB± signals for more than four frames to initiate a resynchronization. For unscrambled data, if the final character of two subsequent frames are equal, the second character is replaced with an /F/ if the character is at the end of a frame and an /A/ if the character is at the end of a multiframe.

Insertion of alignment characters can be modified using the SPI. The frame alignment character insertion (FACI) is enabled by default. The user can also program the device to insert multiframe characters (/A/, K28.3) as well using the JTX_DL_204B_LSYNC_ EN_CFG bit (Register 0x065A, Bit 2 = 1). The JTX_DL_204B_ BYP_ACG_CFG bit can be used to disable the alignment character generation (Register 0x0659, Bit 0 = 1).

8-Bit/10-Bit Encoder

The 8-bit/10-bit encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 52. The 8-bit/10-bit encoding uses the same number of ones and zeros across multiple symbols to ensure that the signal is DC balanced.

The 8-bit/10-bit interface has options that can be controlled through the SPI. These operations include bypass and invert. These options are troubleshooting tools for the verification of the digital front end.

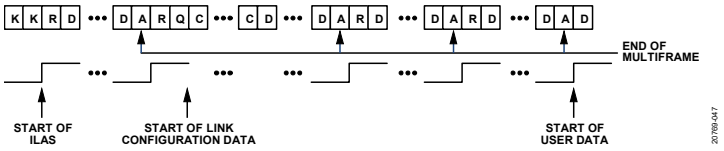

Figure 53. Initial Lane Alignment Sequence

Table 52. Control Characters Used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = −1	10-Bit Value, RD[1] = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD means running disparity.

64-Bit/66-Bit Link Layer and Link Establishment

When using the 64-bit/66-bit link layer, scrambling is always enabled. Therefore, there is no register control for this function. As described in Table 10, the only synchronization word function beyond the EoEMB function is the 12-bit CRC function (CRC-12). The CRC-12 function is always enabled and carries the 12-bit CRC value of the data transmitted during the previous multiblock.

The JTX_CRC_REVERSE_CFG bit described in Table 53 is available to reverse the bit order of the 12-bit CRC value. Scrambling when using the 64-bit/66-bit link layer is performed on a per block per lane basis. All 8 octets of each lane block are scrambled (64 bits of scrambled data followed by an unscrambled synchronization header).

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Synchronization Header Alignment

The synchronization transition bit in the synchronization header ensures that there is a data transition at every block boundary (66 bits). A state machine in the JESD204C receiver detects a data transition and then looks for another transition 66 bits later. If the state machine detects bit transitions at 66-bit intervals for 64 consecutive blocks, the SH_LOCK state is achieved. The machine is restarted if 64 consecutive transitions are not detected.

Extended Multiblock Sync

When the synchronization header alignment is achieved, the receiver looks for the end of the EoEMB sequence (100001) in the transition bits. The structure of the synchronization word ensures that this sequence can only happen at the appropriate time.

When an EoEMB sequence is identified, the state machine examines every 32nd synchronization word to ensure that the end of multiblock pilot signal (00001) is present. If E = 1, the EoEMB bit is also present with the pilot signal.

If E is >1, the pilot signal includes the EoEMB bit for every E×32 transition bit. When four consecutive valid sequences are detected, the EMB_LOCK state is achieved. The monitoring of every E×32 transition bit continues. If a valid sequence is not detected, the EMB_LOCK is lost, and the alignment process resets.

Extended Multiblock (Lane) Alignment

Extended multiblock alignment achieves lane alignment when using the 64-bit/66-bit link layer, which is similar to using the 8-bit/10-bit link layer in that an elastic buffer is employed in the JESD204C receiver on each lane to store incoming data. During extended multiblock alignment, the buffers for each lane start storing data at the incoming data EoEMB boundary (rather than the /K/ to /R/ boundary during ILAS when using the 8-bit/10-bit link layer) and all lanes release the respective buffered data coincident with the last arriving lane EoEMB boundary.

Figure 54 shows how extended multiblock lane alignment is achieved. Each lane receive buffer, except for on the last arriving lane, starts buffering data when the last bit of the EoEMB synchronization word bit field (see Table 10) is received. When the last arriving lane EoEMB synchronization word bit field is received, the release of all lane receive buffers is triggered so that all lanes align.

Error Monitoring and Resynchronization

Error monitoring during the transmission of sample data is achieved by monitoring the CRC-12 data bits transmitted as part of the synchronization word and comparing it to the CRC-12 value that is calculated in the JESD204C receiver. See the 64-Bit/66-Bit Link Establishment Overview section for more details.

If the receiver detects too many CRC-12 errors, synchronization is lost. In this case, the receiver restarts the synchronization state machines automatically. The transmitter continues sending data. The receiver must resynchronize.

System software can monitor the status of both the synchronization header alignment and the extended multiblock alignment state machines to allow the system master to be informed of the respective states. If resynchronization is required, the system master must power down both sides of the link. If a reconfiguration or clocking change is required, do so while the link is powered down. Resynchronization takes place automatically at link power-up.

If the receiver detects too many CRC-12 errors, synchronization is lost. In this case, the receiver restarts the synchronization state machines automatically. The transmitter continues sending data. The receiver must resynchronize.

Monitor the status of both the synchronization header alignment and extended multiblock alignment state machines so the system master is informed of their respective states. If resynchronization is required, the system master powers down both sides of the link. If a reconfiguration or clocking change is required, perform it while the link is powered down. Resynchronization takes place automatically at link power up.

While the most useful link status is gained through the JESD204C receiver status register described in the 64-Bit/66-Bit Error Monitoring and Resynchronization section, there are a couple of status bits on the JESD204B/C transmitter side that are helpful when debugging link errors. These are the JTX_PLL_LOCKED (0x0701[7]) and JTX_PHASE_ESTABLISHED (0x0713[0]) bits, as described in Table 53. Both these bits can be accessed using the adi_ad9081_jesd_tx_link_status_get() function of the API.

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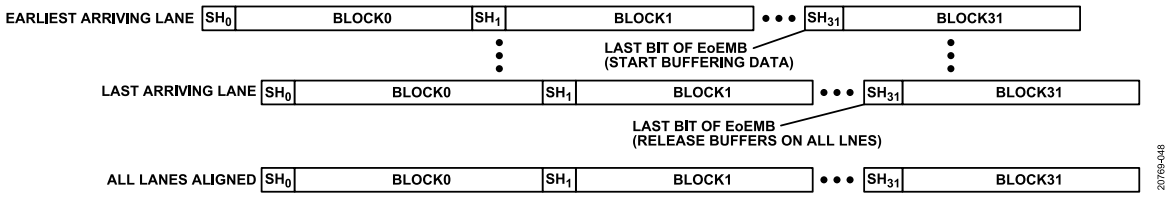

Figure 54. JESD204C Extended Multiblock (Lane) Alignment

Table 53. ADC Path Link Layer Function Registers

Address	Bits	Bit Name	Description	Reset	Access
0x0611	[5:4]	JTX_LINK_204C_SEL	2b'00 selects 8-bit/10-bit link layer (JESD204B mode). 2b'01 selects 64-bit/66-bit link layer (JESD204C mode). Values 2b'10 and 2b'11 are invalid.	0	R/W
0x063D	7	JTX_SCR_CFG	JESD204B/C Transmitter Scrambler Enable. 0 = scrambling disabled. 1 = scrambling enabled.	0	R/W
0x0659	0	JTX_DL_204B_BYP_8B10B_CFG	1 = bypass alignment character generation (JESD204B mode).	0	R/W
0x065A	2	JTX_DL_204B_LSYNC_EN_CFG	Character Insertion for Lane Alignment Configuration. 0 = inserts K28.7 (/F/ for frame alignment) characters only. 1 = inserts K28.7 and K28.3 (/A/ for multiframe alignment) characters.	0x0	R/W
0x0667	0	JTX_CRC_REVERSE_CFG	1 = reverse bit ordering of CRC in metaword (JESD204C mode).	0	R/W
0x0668	[7:0]	JTX_E_CFG	Number of multiblocks in extended multiblock (minus 1). JESD204C mode only. 0 = 1 multiblock in the extended multiblock. 2 = 3 multiblocks in the extended multiblock. All other values are invalid.	0	R/W
0x0762	[1:0]	PARDATAMODE_SER_RC	Selects JESD204B/C Parallel Data Processing Width. 0 = 66 bits (JESD204C mode). 1 = 40 bits (JESD204B mode).	0x1	R/W
0x0701	7	JTX_PLL_LOCKED	JTX PLL Locked Status Bit 0 = JTx PLL is not locked 1 = JTx PLL is locked	0x0	R
0x0713	0	JTX_PHASE_ESTABLISHED	JTX and receive path clocking phase are established. Both JTX_PLL_LOCKED and JTX_PHASE_ESTABLISHED must be 1 for proper operation of the receiver. 0 = phase is not established. 1 = phase established between JTx and receive path readback	0x0	R
0x0797	3	PD_SYNCA_RX_RC	SYNC0INB± Receiver Power Down. 1 = power down.	0x1	R/W
	2	SYNCA_RX_PN_INV_RC	SYNC0INB± Invert Signal Polarity. 1 = invert ± polarity.	0x0	R/W
	1	SYNCA_RX_ONCHIP_TERM_RC	SYNC0INB± On-Chip 100 Ω Termination Enable. 1 = termination enabled.	0x0	R/W
	0	SYNCA_RX_MODE_RC	SYNC0INB± Input Mode Select. 0 = CMOS mode. 1 = differential mode.	0x0	R/W
0x0798	3	PD_SYNCB_RX_RC	SYNC1INB± Receiver Power Down. 1= power down.	0x1	R/W
	2	SYNCB_RX_PN_INV_RC	SYNC1INB± Invert Signal Polarity. 1 = invert ± polarity.	0x0	R/W
	1	SYNCB_RX_ONCHIP_TERM_RC	SYNC1INB± On-Chip 100 Ω Termination Enable. 1 = termination enabled.	0x0	R/W

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Table 53. ADC Path Link Layer Function Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
	0	SYNCB_RX_MODE_RC	SYNC1INB± Input Mode Select. 0 = CMOS mode. 1 = differential mode.	0x0	R/W

JESD204B/C Transmitter Physical Layer

As shown in Figure 55, the physical layer consists of the serializer, FFE, and the output driver clocked at the serial clock rate. In this layer, parallel data is converted into up to eight lanes of high speed differential serial data. The differential digital outputs are powered up by default. The drivers use a dynamic, 100 Ω internal termination to reduce unwanted reflections.

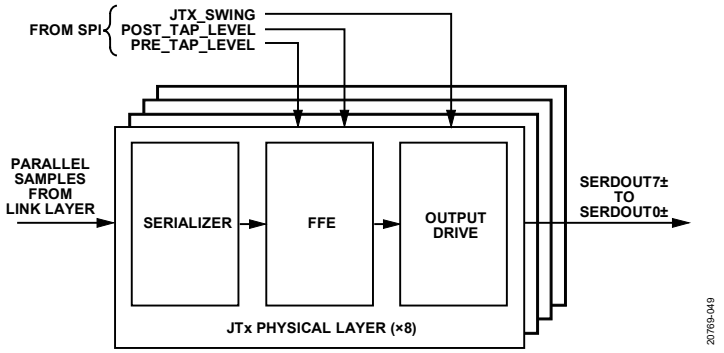

Figure 55. JESD204B/C Transmit Physical Layer Block Diagram

JESD204B/C Transmitter PHY Power and Lane Controls

Per lane SPI control and status bits are available for lane power down, lane polarity inversion, and logical lane assignments (lane crossbar). The control and status bits of each lane are identical and are located from Register 0x061B (Lane 0) to Register 0x0622 (Lane 7) (see Table 55). In addition to lane power control, a separate power control for the JESD204B/C transmitter serializers (one per lane) is also available. Register PD_SER, Bits[7:0] (Register 0x0750) provides per lane control of the serializer power (see Table 55).

A logical lane source can be from either Link 0 or Link 1 (if used) with the JTX_LINK0_PAGE or JTX_LINK1_PAGE bit field specifying the link. To assign the logical lane source for each PHY, select the desired link and write to each JTX_LANE_ASSIGN bit field with the desired logical lane source. By default, all physical lanes use the corresponding logical lane as the data source. For example, the JTX_LANE_ASSIGN bit field within the JTX_CORE_2_LANE0 register (Register 0x061B) is set to 0 by default, thus mapping this physical Lane 0 to Logical Lane 0.

The API supports logical to physical lane mapping with the adi_ad9081_jesd_tx_lane_xbar_set function, which is in the **adi_adxxxx_jesd.c** file.

Digital Outputs, Timing, and Controls

Place a 100 Ω differential termination resistor at each receiver input to achieve a nominal 0.85×DRVDD1 V p-p swing at the receiver, as shown in Figure 56.

The swing is adjustable through the SPI registers. AC coupling is recommended to connect to the receiver. See Table 56 for more details.

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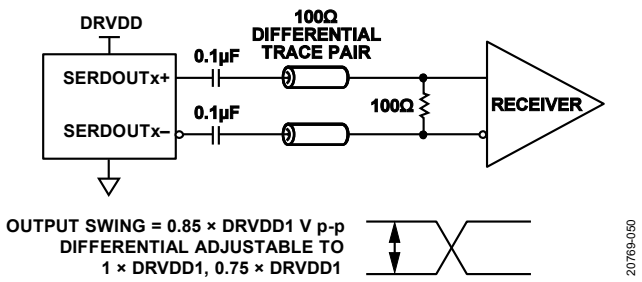

Figure 56. AC-Coupled Digital Output Termination Example

The device digital outputs can interface with custom application specific integrated circuits (ASICs) and FPGA receivers and provide superior switching performance in noisy environments. Single point to point network topologies are recommended with a single differential, 100 Ω termination resistor placed as close to the receiver inputs as possible. The format of the output data is twos complement by default. To change the output data format, see the description for the DFORMAT_SEL bit field in Table 47.

FFE

The FFE consists of both pre-tap and post-tap de-emphasis and enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B/C specification.

Only use FFE settings that enable de-emphasis when the receiver is unable to recover the clock because of excessive insertion loss. For links with well-designed PCB channels that have low insertion loss, disable de-emphasis to conserve power.

Use nonzero de-emphasis settings with caution because these settings can increase electromagnetic interference (EMI). Table 56 describes the register that sets the de-emphasis level for the pre-tap and post-tap filters for each of the eight JESD204B/C lanes. Use the bit field descriptions in Table 56 as a guideline for how to set the pre-tap and post-tap de-emphasis bit fields. For example, if the PCB channel has an insertion loss between 3 dB and 6 dB, use a setting of 0x2 (6 dB).

JESD204B/C Transmitter Physical Layer API

The device API supports many JESD204B/C transmitter PHY level functions. The high level API function adi_ad9xxx_device_ startup_rx() calls the mid-level function adi_adxxx_jesd_tx_ link_config_set to set up the JESD204B/C transmitter side of the link. Several lower level functions are called to configure the JESD204B/C transmitter PHY. These function calls are briefly described in Table 54.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 54. JESD204B/C Transmitter PHY Power and Lane Control API Functions

Function Call	<C file>	Description
adi_adxxxx_jesd_tx_startup_ser	**adi_adxxxx_jesd.c**	Powers down unused lanes
adi_adxxxx_jesd_tx_lane_xbar_set	**adi_adxxxx_jesd.c**	Assigns logical lane source for each PHY lane
adi_adxxxx_jesd_tx_set_pre_emp	**adi_adxxxx_jesd.c**	Sets the pre-tap cursor weight
adi_adxxxx_jesd_tx_set_post_emp	**adi_adxxxx_jesd.c**	Sets the post-tap cursor weight
adi_adxxxx_jesd_tx_set_swing	**adi_adxxxx_jesd.c**	Sets the output swing (also known as the main tap weight)

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Table 55. JESD204B/C Transmitter PHY Power and Lane Control Registers

Address	Bits	Bit Name	Description	Reset	Access
0x061B	7	JTX_LANE_PD_STATUS0	JESD204B/C Transmitter Lane 0 Power-Down Status. JTX_LANE_PD_STATUS reflects the power status of the lane based on the JTX_LANE_ASSIGN setting. 0 = lane in use. 1 = lane is powered down.	0	R
	6	JTX _FORCE_LANE_PD0	JESD204B/C Transmitter Force Power-Down. 0 = lane power set by JTX_LANE_ASSIGN setting. 1 = lane is off, Transmit 0s.	0	R/W
	5	JTX_LANE_INV0	Invert JESD204B/C Transmitter Logical Lane Data. 0 = do not invert. 1 = invert logical polarity.	0	R/W
	[4:0]	JTX_LANE_ASSIGN0	PHY Lane 0 assignment. 0 = from Logical lane 0, etc.	0x00	R/W
0x061C	7	JTX_LANE_PD_STATUS1	JESD204B/C Transmitter Lane 1 Power-Down Status. JTX_LANE_PD_STATUS reflects the power status of the lane based on the JTX_LANE_ASSIGN setting. 0 = lane in use. 1 = lane is powered down.	0	R
	6	JTX _FORCE_LANE_PD1	JESD204B/C Transmitter Force Lane 1 Power-Down. 0 = lane power set by JTX_LANE_ASSIGN setting. 1 = lane is off, transmit 0s.	0	R/W
	5	JTX_LANE_INV1	Invert JESD204B/C Transmitter Logical Lane 1 Data. 0 = do not invert. 1 = invert logical polarity.	0	R/W
	4:0	JTX_LANE_ASSIGN1	PHY Lane 1 assignment. 1 = from Logical lane 1, etc.	0x01	R/W
0x061D	7	JTX_LANE_PD_STATUS2	JESD204B/C Transmitter Lane 2 Power-Down Status. JTX_LANE_PD_STATUS reflects the power status of the lane based on the JTX_LANE_ASSIGN setting. 0 = lane in use. 1 = lane is powered down.	0	R
	6	JTX _FORCE_LANE_PD2	JESD204B/C Transmitter Force Lane 2 Power-Down. 0 = lane power set by JTX_LANE_ASSIGN setting. 1 = lane is off, Transmit 0s.	0	R/W
	5	JTX_LANE_INV2	Invert JESD204B/C Transmitter Logical Lane 2 Data. 0 = do not invert. 1 = invert logical polarity.	0	R/W
	4:0	JTX_LANE_ASSIGN1	PHY Lane 2 assignment. 2 = from Logical Lane 2, etc.	0x02	R/W
0x061E	7	JTX_LANE_PD_STATUS3	JESD204B/C Transmitter Lane 3 Power-Down Status. JTX_LANE_PD_STATUS reflects the power status of the lane based on the JTX_LANE_ASSIGN setting. 0 = lane in use. 1 = lane is powered down.	0	R
	6	JTX _FORCE_LANE_PD3	JESD204B/C Transmitter Force Lane 3 Power-Down. 0 = lane power set by JTX_LANE_ASSIGN setting. 1 = lane is off, Transmit 0s.	0	R/W
	5	JTX_LANE_INV3	Invert JESD204B/C Transmitter Logical Lane 3 Data. 0 = do not invert. 1 = invert logical polarity.	0	R/W
	4:0	JTX_LANE_ASSIGN3	PHY Lane 3assignment. 3 = from Logical lane 3, etc.	0x03	R/W
0x061F	7	JTX_LANE_PD_STATUS4	JESD204B/C Transmitter Lane 4 Power-Down Status. JTX_LANE_PD_STATUS reflects the power status of the lane based on the JTX_LANE_ASSIGN setting. 0 = lane in use. 1 = lane is powered down.	0	R
	6	JTX _FORCE_LANE_PD4	JESD204B/C Transmitter Force Lane 4 Power-Down.	0	R/W

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Table 55. JESD204B/C Transmitter PHY Power and Lane Control Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
			0 = lane power set by JTX_LANE_ASSIGN setting. 1 = lane is off, Transmit 0s.		
	5	JTX_LANE_INV4	Invert JESD204B/C Transmitter Logical Lane 4 Data. 0 = do not invert. 1 = invert logical polarity.	0	R/W
	4:0	JTX_LANE_ASSIGN4	PHY Lane 4 assignment. 4 = from Logical lane 4, etc.	0x04	R/W
0x0620	7	JTX_LANE_PD_STATUS5	JESD205B/C Transmitter Lane 5 Power-Down Status. JTX_LANE_PD_STATUS reflects the power status of the lane based on the JTX_LANE_ASSIGN setting. 0 = lane in use. 1 = lane is powered down.	0	R
	6	JTX _FORCE_LANE_PD5	JESD205B/C Transmitter Force Lane 5 Power-Down. 0 = lane power set by JTX_LANE_ASSIGN setting. 1 = lane is off, Transmit 0s.	0	R/W
	5	JTX_LANE_INV5	Invert JESD205B/C Transmitter Logical Lane 5 Data. 0 = do not invert. 1 = invert logical polarity.	0	R/W
	4:0	JTX_LANE_ASSIGN5	PHY Lane 5 assignment. 5 = from Logical lane 5, etc.	0x05	R/W
0x0621	7	JTX_LANE_PD_STATUS6	JESD204B/C Transmitter Lane 6 Power-Down Status. JTX_LANE_PD_STATUS reflects the power status of the lane based on the JTX_LANE_ASSIGN setting. 0 = lane in use. 1 = lane is powered down.	0	R
	6	JTX _FORCE_LANE_PD6	JESD204B/C Transmitter Force Lane 6 Power-Down. 0 = lane power set by JTX_LANE_ASSIGN setting. 1 = lane is off, Transmit 0s.	0	R/W
	5	JTX_LANE_INV6	Invert JESD204B/C Transmitter Logical Lane 6 Data. 0 = do not invert. 1 = invert logical polarity.	0	R/W
	4:0	JTX_LANE_ASSIGN6	PHY Lane 6 assignment. 6 = from Logical lane 6, etc.	0x06	R/W
0x0622	7	JTX_LANE_PD_STATUS7	JESD204B/C Transmitter Lane 7 Power-Down Status. JTX_LANE_PD_STATUS reflects the power status of the lane based on the JTX_LANE_ASSIGN setting. 0 = lane in use. 1 = lane is powered down.	0	R
	6	JTX _FORCE_LANE_PD7	JESD204B/C Transmitter Force Lane 7 Power-Down. 0 = lane power set by JTX_LANE_ASSIGN setting. 1 = lane is off, Transmit 0s.	0	R/W
	5	JTX_LANE_INV7	Invert JESD204B/C Transmitter Logical Lane 7 Data. 0 = do not invert. 1 = invert logical polarity.	0	R/W
	4:0	JTX_LANE_ASSIGN7	PHY Lane 7 assignment. 7 = from Logical lane 7, etc.	0x07	R/W
0x0750	[7:0]	PD_SER	Bit Per PHY Lane Control of the Serializer Power. 0 = serializer is on. 1 = sterilizer is off.	0xFF	R/W

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Table 56. ADC Path De-Emphasis and Output Control Registers

Address	Bits	Bit Name	Description	Reset	Access
0x0752 to 0x0755 (Per Lane Control)	[6:4]	JTX_LANE[1,3,5,7]_SWING (odd lanes)	Sets Output Swing Level Relative to the SVDD1 Supply.	0x11	R/W
	[2:0]	JTX_LANE[0,2,4,6]_SWING (even lanes)	000 = 1.0×SVDD1. 001 = 0.85×SVDD1. 010 = 0.75×SVDD1. 011 = 0.50×SVDD1. 100 to 111 = invalid.		
0x075A to 0x075D (Per Lane Control)	[6:4]	JTX_LANE[1,3,5,7]_POST_TAP_LEVEL (odd lanes)	Sets Output Swing Level Relative to the SVDD1 Supply.	0x0	R/W
	[2:0]	JTX_LANE[0,2,4,6]_POST_TAP_LEVEL (even lanes)	000 = 0 dB. 001 = 3 dB. 010 = 6 dB. 011 = 9 dB. 100 = 12 dB. 101 to 111 are invalid.	0x0	
0x0763 to 0x076A (Per Lane Control)	[7:0]	JTX_LANE[0..7]_PRE_TAP_LEVEL	Sets Output Swing Level Relative to the SVDD1 Supply. 0x00= 0 dB. 0x01 = 3 dB. 0x02 = 6 dB. else = invalid.	0x00	R/W

ADC Path Deterministic Latency

Both ends of the JESD204B/C link contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B/C link. These ambiguities lead to non-repeatable latencies across the link from one power cycle or link reset to the next. The JESD204C specification addresses the issue of deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The device supports JESD204B/C Subclass 0 and Subclass 1 operation. The JTX_SUBCLASSV_CFG bits (Register 0x0642, Bits[7:5]) sets the subclass mode for the device and the default is set for Subclass 0 operating mode (Register 0x0642, Bits[7:5] = 0). If deterministic latency is not a system requirement, Subclass 0 operation is recommended and the SYSREF signal may not be required.

Subclass 0 Operation

If there is no requirement for multichip synchronization while operating in Subclass 0 mode, the SYSREF input can be left disconnected. In this mode, the relationship of the JESD204B/C clocks between the JESD204B/C transmitter and receiver are arbitrary but does not affect the ability of the receiver to capture and align the lanes within the link. Note that, even in subclass 0 mode, some internal synchronization is still required using a one shot sync as described in the SYSREF Receiver Input and Interface Options section and SYSREF Setup/Sync Procedure section. In subclass 0 mode, the one shot sync pulse is provided internally instead of an external SYSREF, based on the arbitrary phase of the LMFC/LEMC.

Subclass 1 Operation

The JESD204B/C protocol organizes data samples into octets, frames, and multiframes (or multiblocks), as described in the Transport Layer section. The LMFC/LEMC is synchronous with the beginnings of these multiframes/multiblocks. In Subclass 1 operation, the SYSREF signal synchronizes the LMFC/LEMCs for each device in a link or across multiple links. Within the AD9081 and AD9082, the SYSREF signal also synchronizes the internal sample dividers. This synchronization is shown in Figure 57. The JESD204B receiver uses the multiframe boundaries and buffering to achieve consistent latency across lanes (or across multiple devices) and to achieve a fixed latency between power cycles and link reset conditions. Similarly, the JESD204C receiver uses the extended multiblock boundaries and buffering to achieve consistent latency.

The device features both averaged SYSREF mode and sampled SYSREF mode for JESD204B/C Subclass 1 operation. See the SYSREF Modes section for more details.

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Deterministic Latency Requirements

Key factors that are required for achieving deterministic latency in a JESD204B/C Subclass 1 system include the following:

- SYSREF signal distribution skew within the system must be less than the desired uncertainty for the system.
- SYSREF setup and hold time requirements must be met for each device in the system. When using averaged SYSREF mode, the setup and hold time requirements are eased for the externally applied SYSREF signal. References to the SYSREF setup and hold times are in the context of the sampled SYSREF mode.
- The total latency variation across all lanes, links, and devices must be ≤ 1 LMFC/LEMC period (see Figure 57). This variation includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system. For more requirements regarding latency variation related to the device JESD204B/C receiver, see the Deterministic Latency Requirements section.

Setting Deterministic Latency Registers

The JESD204B/C receive buffer in the logic device buffers data. If the total link latency in the system is near an integer multiple of the LMFC/LEMC period, the data arrival time of the incoming LMFC/LEMC boundary at the receive buffer can straddle the JESD204B/C receiver's local LMFC/LEMC boundary from one power cycle to the next. To ensure deterministic latency in this case, perform a phase adjustment of the LMFC/LEMC at either the JESD204B/C transmitter or JESD204B/C receiver. Typically, adjustments to accommodate the receive buffer are made to the receiver LMFC/LEMC. In the JESD204B/C transmitter of the device, this adjustment can be made using the JTX_TPL_PHASE_ADJUST[15:0] bit field (MSBs at Register 0x0633, Bits[7:0], LSBs at Register 0x0632, Bits[7:0]). The step size for this adjustment is in the JTX_SAMPLE_CLK cycles where (see Table 57),

JTX_SAMPLE_CLK = f_{ADC}/(DCM×NS)

where:

f_{ADC} = ADC sample clock

DCM = total decimation

NS = number of samples processed per the JTX_SAMPLE_CLK in the datapath

Table 57. M vs. NS

M	NS
≤8	8
12	4
16	4

Figure 58 shows that when the link latency is near an LMFC/LEMC boundary, the local LMFC/LEMC of the device can be delayed to allow all instances of the data arrival time at the receiver to occur within the same LMFC/LEMC cycle. Figure 59 shows how a delay of the LMFC/LEMC in the receiver accommodates the receive buffer timing. Consult the applicable JESD204B/C receiver user guide of the logic device being used for details on making this adjustment. If the total latency in the system is not near an integer multiple of the LMFC/LEMC period or if the appropriate adjustments have been made to the LMFC/LEMC phase at the clock source, variable latency from one power cycle to the next is still possible. In this case, check for the possibility that the setup and hold time requirements for the SYSREF signal are not being met. To check these requirements, use the SYSREF_SETUP register and SYSREF_HOLD register (Register 0x0FB7 and Register 0x0FB7, respectively) (see the SYSREF Setup and Hold Time Monitor section).

If the read from these registers indicates a potential timing problem, the phase of the SYSREF signal supplied to the device must be adjusted until the SYSREF_SETUP register and SYSREF_HOLD register indicate that there is no potential timing problem.

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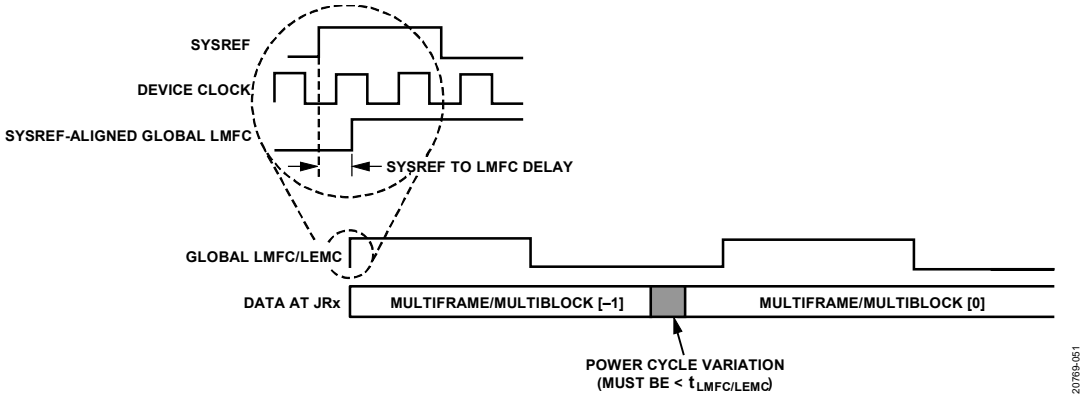

Figure 57. SYSREF and LMFC/LEMC

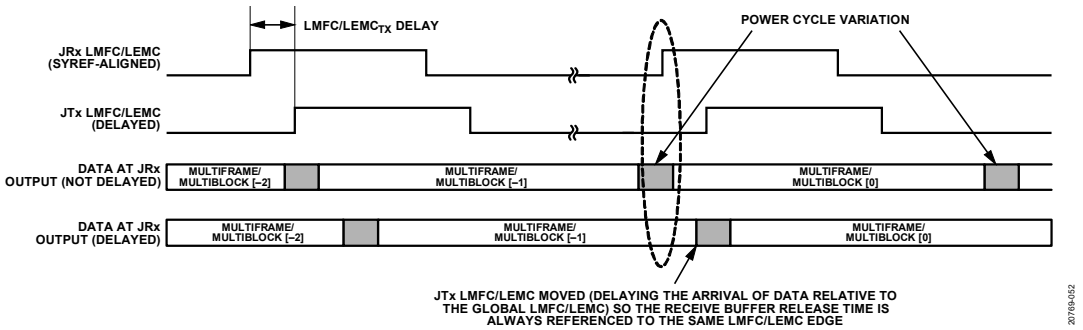

Figure 58. Adjusting the JESD204B/C Transmitter LMFC/LEMC in the AD9081 and AD9082

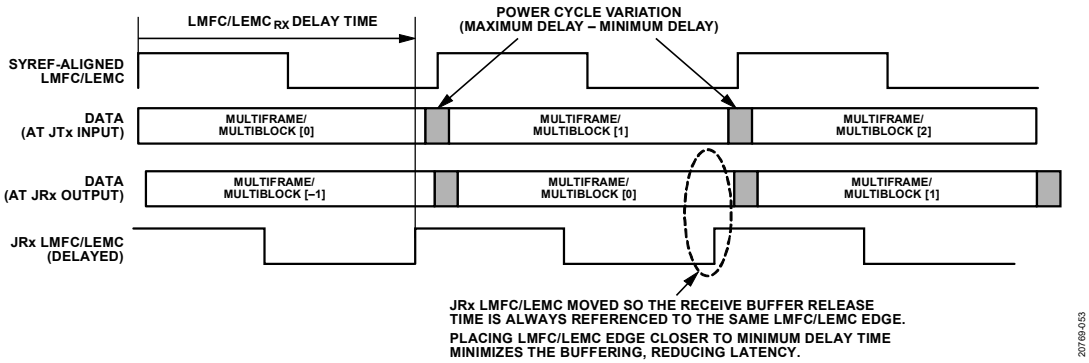

Figure 59. Adjusting the JESD204B/C Receiver LMFC/LEMC in the Logic Device

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Table 58. ADC Path Deterministic Latency Registers

Address	Bits	Bit Name	Description	Reset	Access
0x0642	[7:5]	JTX_SUBCLASSV_CFG[2:0]	Sets the Subclass Operation for the JESD204B/C Transmitter. 000 = Subclass 0. 001 = Subclass 1. 010 to 111 are invalid.	0x00	R/W
0x0633	[7:0]	JTX_TPL_PHASE_ADJUST[15:8]	JESD204B/C Transmitter Transport Layer LMFC Phase Adjust. Bits[15:8] of the bit field setting are used to delay the transport layer LMFC/LEMC relative to the device local LMFC/LEMC in JTX_SAMPLE_CLOCK cycles.	0x00	R/W
0x0632	[7:0]	JTX_TPL_PHASE_ADJUST[7:0]	JESD204B/C Transmitter Transport Layer LMFC Phase Adjust. Bits[7:0] of the bit field setting are used to delay the transport layer LMFC/LEMC relative to the device local LMFC/LEMC in JTX_SAMPLE_CLOCK cycles.	0x00	R/W

JESD204B/C Transmitter Multichip Synchronization

The device has a JESD204B/C Subclass 1 compatible SYSREF input that provides flexible options for synchronizing the internal blocks of the device. For applications requiring multichip synchronization, use the averaged SYSREF mode, as described in the SYSREF and Subclass 1 Operation section.

To achieve multichip synchronization using multiple devices when operating in Subclass 1 mode, apply the same principles for setting deterministic latency related registers across all links in the system requiring synchronization. That is, on the ADC path, use the JTX_TPL_PHASE_ADJUST register to ensure that the data arriving at the logic devices JESD204B/C receiver transport layer has an LMFC/LEMC boundary and does not arrive near the JESD204B/C receiver's local LMFC/LEMC boundary across all links and devices in the system.

CONFIGURING THE JESD204B/C TRANSMITTER LINK

High Level Configuration Process

Table 59 provides a general process specifically aimed at bringing up the JESD204B/C transmitter that may prove to be useful when reconfiguring or re-starting the link. This process assumes that the PLL and receive datapath are already configured per the procedure described in the SERDES PLL and Configuration section and the Receive Input and Digital Datapath section. Users must consider the start-up within the context of their entire system however, and can refer to the device API for this context.

The user may choose to have a dual link configuration on the receive path. In this case, each of the configuration steps starting with Step 8 (except where explicitly noted) must be repeated for each link. Use the JTX_LINK[1:0]_PAGE bits (Register 0x001A, Bits[1:0]) to select Link 0 or Link 1. Otherwise, perform the configuration once using Link Page 0. The JTX_LINK_EN bit (Register 0x62E, Bit 0) is part of a paged register. To enable dual link operation, set the JTX_LINK_EN bit for 1 for both links. For dual-link operation, the lane rate of one link must have a power of 2 ratio with the lane rate of the second link. If the lane rate is different between the two links, use the JTX_BR_LOG2_RATIO register to enable bit repeat mode for one or both links. For example, if Link 0 = 24.75 Gbps and Link 1 = 12.375 Gbps, the Link 1 PHY lanes require the JTX_BR_LOG2_RATIO to be set to 1 (factor of 2). If Link 0 = 3.5 Gbps and Link 1 = 7 Gbps, the Link 0 PHY lanes require a JTX_BR_LOG2_RATIO value of 2 (factor of 4) and the Link 1 PHY lanes require a BR JTX_BR_LOG2_RATIO value of 1 (factor of 2). In the latter case, BR JTX_BR_LOG2_RATIO is used for both links but the link with the lowest (not the highest) lane rate requires an extra BR factor of 2 to match the other link lane rate.

JESD204B/C Transmitter Configuration API

The bulk of the JESD204B/C transmitter configuration is performed in the adi_ad9xxx_jesd_tx_link_config_set() API function which is called by the high level API function adi_ad9xxx_device_startup_rx(). Many lower level APIs are called as part of this startup sequence, some of which are identified in Table 59.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Table 59. JESD204B/C Transmitter High Level Configuration Process

Step	Action	Description	Lower API Functions
1	If receiver-only operation setup PLL. For receive and transmit operation, transmit is configured first, including the PLL, then proceed to Step 2	Configure PLL according to steps outlined in the SERDES PLL and Configuration section. Set the LMFC period in DAC_CLK/4 units. LMFC_PERIOD_SPI_EN (Register 0x00C8, Bit 4) = 1 Set the LMFC_PERIOD_SPI[10:0] bit field (Register 0X00C8, Bits[2:0], Register 0C00C7, Bits[7:0]) = ((FDAC/FADC)×JTX_S ×JTX_K / Total Receive Decimation) / 4 If prior step yields value < 32, New LMFC_PERIOD_SPI = ((32/ LMFC_PERIOD_SPI_OLD) + 1)×LMFC_PERIOD_SPI_OLD	adi_ad9xxx_jesd_tx_startup_rx()
2	Serializer configuration	Power up appropriate serializers, PD_SER[7:0] (Register 0x0750, Bits[7:0] are bit per channel). Set Register 0x0782 to 0x0F. Set parallel data width for serializer input (Register 0x0762, Bits[1:0]), 0 = 66 bits (204C), 1 = 40 bits (204B) Reset serializers, RSTB_SER (Register 0x0773) = 0x01, wait 10 ms, RSTB_SER (Register 0x0773) = 0x00	adi_ad9xxx_jesd_tx_startup_rx()
3	Set the RX_TX_LMFC_LCM register (Register 0x00BD, Bits[3:0]) according to the transmit and receive lane rates	If receive/transmit operation, see Table 16 in the SYSREF Setup/Sync Procedure section. If receive only mode and LMFC_PERIOD_SPI > 2047, RX_TX_LMFC_LCM = 7, divide LMFC_PERIOD_SPI value from Step 1) by 8.	adi_ad9xxx_spi_register_set, adi_ad9xxx_spi_register_sget
4	Set the DIVM_LCPLL_RC_RX register (Register 0x0717, Bits[1:0]) according to the lane rate	If in JESD204B mode: 0 = lane rate > 8 Gbps, 1= lane rate ≤ 8 Gbps If in JESD204C mode: 0 = lane rate > 16 Gbps, 1= lane rate ≤ 16 Gbps	adi_ad9xxx_jesd_tx_startup_rx()
5	Physical layer adjustments as needed	JTX_SWING registers (Register 0x0752 to Register 0x0755), nominally set to default. POST_TAP_LEVEL registers (Register 0x075A to Register 0x075D), settings for 0, 3, 6, 9, and 12 dB of boost.	adi_ad9xxx_jesd_tx_startup_rx()
6	Configure JESD204B/C transmitter crossbar mux	Set JTX_CONV_SEL[0:15] (Register 0x0600 to Register 0x060F, Bits[6:0]) (see Mux4 (JESD204B/C Transmitter JESD Data Router) section for details). Unmask all channels being used by setting bit 7 (JTX_CONV_MASK) of the appropriate register to 0.	adi_ad9xxx_device_startup_rx(), adi_ad9xxx_jesd_tx_link_conv_sel_set(), adi_ad9xxx_jesd_tx_conv_mask_set()
7	Force link reset	Set the force_link_reset register (Register 0x0710, Bit 0) = 1.	adi_ad9xxx_device_startup_rx()
8	Select link page. Note that remaining steps are paged. If in dual-link mode, steps must be repeated for each link.	Set the JTX_LINK_PAGE (Register 0x001A, Bits[1:0]) appropriately: 2b'01 = select link 0. 2b'10 = select link 1 (only needed when in dual-link mode).	adi_ad9xxx_device_startup_rx()
9	Disable link	Set the JTX_LINK_EN (Register 0x062E, Bit 0) = 0.	adi_ad9xxx_device_startup_rx()
10	Set Register 0x0721, Bit 5 = 0	This bit must be set.	adi_ad9xxx_device_startup_rx()
11	Set Register 0x0712, Bit 0 = 1	This bit must be set.	adi_ad9xxx_spi_register_set, adi_ad9xxx_spi_register_sget
12	Set JESD204B/C parameter registers per mode tables.	Set JTX_MODE and JTX_MODE_S_SEL (For AD9986 and AD9988 only) or the JESD204B/C parameters (L, M, F, S, NP, E, K, N, and HD) individually according to Table 65 through Table 76. Set the SUBCLASS_CFG (Register 0x04AE, Bits[7:5]) and SCR (Register 0x063D, Bit 7) appropriately. Set the JTX_SUBCLASSV_CFG (Register 0x0642, Bit 5) appropriately (0 = Subclass 0, 1 = Subclass 1).	adi_ad9xxx_device_startup_rx()

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Table 59. JESD204B/C Transmitter High Level Configuration Process (Continued)

Step	Action	Description	Lower API Functions
13	Enable the appropriate data link layer.	Set the JTX_LINK_204C_SEL (Register 0x0611, Bits[5:4]). 2b'00 = 8-bit/10-bit link layer (JESD204B). 2b'01 = 64-bit/66-bit link layer (JESD204C).	adi_ad9xxx_device_startup_rx()
14	JTX_TPL_SYSREF_MASK set according to subclass	This register must be set as follows: 0x20 = Subclass 0. 0x00 = Subclass 1.	adi_ad9xxx_device_startup_rx(), adi_ad9xxx_jesd_tx_link_config_set()
15	Check if using an asynchronous mode according to Table 65 through Table 76.	If ASYNC attribute is true, set the JTX_CONV_ASYNCHRONOUS (Register 0x0630, Bit 2) = 1.	adi_ad9xxx_jesd_tx_link_config_set(), adi_ad9xxx_hal_bf_set()
16	Configure the PHY lane crossbar (PHY lane to logical lane assignment)	Power down unused lanes (bits are not paged), set the JTX_LANE_PD[0:7] (Register 0x061B to Register 0x0622, Bit 7) Make lane assignment (bits are paged). Set the JTX_LANE_ASSIGN[0:7] (Register 0x061B to Register 0x0622, Bits[4:0]). If in single link mode, still assign lanes on the 2nd link (Link1). Make the appropriate lane ID assignments per above lane assignment. Set the JTX_LID_CFG[0:7] (Register 0x0650 to Register 0x0657, Bits[4:0]).	adi_ad9xxx_jesd_tx_lanes_xbar_set(), adi_ad9xxx_device_startup_rx()
17	Set bit repeat mode (per lane), if necessary, according to mode Table 65 through Table 76 if operating the receive path only. If using both transmit and receive path, set according to the JTX_BR_LOG2_RATIO bit field description in Table 61.	Set the JTX_BR_LOG2_RATIO (Register 0x0670 to Register 0x0677, Bits[3:0]). If single link or identical dual links , set according to Table 65 through Table 76. If dual-link link and the lane rates are not identical: JTX link lane rate spread = QUOTE $\frac{\text{maximum JTX link lane rate}}{\text{minimum JTX link lane rate}}$ $\frac{\text{maximumJTXlinklanerate}}{\text{minimumJTXlinklanerate}}$. JTX bit repeat ratio spread = $\frac{2^{\text{maximum JTX bit repeat ratio}}}{2^{\text{minimum JTX bit repeat ratio}}}$ QUOTE $\frac{2^{\text{maximum JTX bit repeat ratio}}}{2^{\text{minimum JTX bit repeat ratio}}}$. if JTX link lane rate spread ≠ JTX bit repeat ratio spread do: JTX bit repeat adjust value = QUOTE $\log_2\left(\frac{\text{jtx bit repeat ratio spread}}{\text{jtx link lane rate spread}}\right)$ $\log_2\left(\frac{\text{jtxbitrepeatratiospread}}{\text{jtxlinklaneratespread}}\right)$. JTX bit repeat ratio for fastest link = JTX bit repeat ratio value from Step 2 calculated using the link with the highest lane rate. JTX bit repeat ratio for slowest link = JTX bit repeat ratio value from Step 2 calculated using the link with the lowest lane rate + JTX bit repeat adjust value.	adi_ad9xxx_device_startup_rx()
18	If in ASYNC mode, set Register 0x070A, Bit 0 = 1	This bit must be set (not paged).	adi_ad9xxx_device_startup_rx()
19	If in special JESD204C mode, set LCM_DIVx bit fields.	If JTX mode is in Table 60, set the LCM_DIV_FORCE_EN bit (Register 0x070C, Bit 0) to 1 and LCM_DIV1 (Register 0x070D) to 0x2F.	Not currently supported in API, use adi_ad9xxx_spi_register_set and adi_ad9xxx_spi_register_sget
20	Enable link(s)	JTX_link_en (Register 0x062E, Bit 0) = 1.	adi_ad9xxx_jesd_tx_link_enable_se()
21	SYNCxINB receiver(s) configuration	If in JESD204B mode, see the SYNC0INB± and SYNC1INB± Interface Options section to set Register 0x0797 and Register 0x0798 appropriately. If in dual-link mode, select the SYNCxINB± input pin via JTX_SYNC_N_SEL (Register 0x062D, Bit 5). If in JESD204C mode, power down the SYNCxINB± receivers (Register 0x0797, Bit 3, and Register 0x0798, Bit 3 = 1).	adi_ad9xxx_device_startup_rx()
22	Disable link reset	Set the FORCE_LINK_RESET (Register 0x0710, Bit 0) = 0.	adi_ad9xxx_jesd_tx_link_reset()

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Table 59. JESD204B/C Transmitter High Level Configuration Process (Continued)

Step	Action	Description	Lower API Functions
23	Configure SYSREF if operating in Subclass 1 mode (If receive is on, assuming SYSREF is configured during transmit setup)	SYSREF_MODE (Register 0x00B8), enable one shot or continuous (Bits[1:0]), check status (Bits[5:4]).	adi_ad9xxx_dac_nco_sync_sysref_mode_set, adi_ad9xxx_jesd_oneshot_sync()

Table 60. JTX Modes Requiring LCM_DIVx Intervention

L	M	S	F	K	E	NP	Decimation
1	1	2	3	256	3	12	6×2
1	1	4	6	128	3	12	6×2
2	2	2	3	256	3	12	6×2
2	2	4	6	128	3	12	6×2
4	4	2	3	256	3	12	6×2
4	4	4	6	128	3	12	6×2
8	4	2	3	256	3	24	6×2
8	4	4	6	128	3	24	6×2

Table 61. ADC Path JESD204B/C Start-Up Registers

Address	Bits	Bit Name	Description	Reset	Access
0x001A	[1:0]	JTX_LINK[1:0]_PAGE	Selects which framer is being written to (only needed when in dual-link mode). 2b'01: selects Link 0. 2b'10: selects Link 1.	0x3	R/W
0x00B8	5	INIT_SYNC_DONE	Initial sync done flag (after initial power-up).	0x0	R
	4	ONESHOT_SYNC_DONE	One shot synchronization done flag (after enabling SYSREF and following the procedure in the SYSREF Setup/Sync Procedure section)	0x0	R
	1	SYSREF_MODE_ONESHOT	Enable one shot synchronization rotation mode.	0x0	R/W
0x00BD	[3:0]	RX_TX_LMFC_LCM	If the JESD204B/C transmitter LMFC/LEMC period is an integer multiple of the JESD204B/C receiver LMFC/LEMC, set these bits to 0. Otherwise, set these bits to the value of LCM to 1. For example, if Rx/Tx = 3/2, set to 5. If Rx/Tx = 2, set to 1. If Tx/Rx = 5/3, set to 14.	0x0	R/W
0x00C8	4	LMFC_PERIOD_SPI_EN	Enable the LMFC period from SPI. The LMFC period from the SPI setting instead of the JESD mode setting.	0x0	R/W
	[2:0]	LMFC_PERIOD_SPI[10:8]	Bits [10:8] of the LMFC period from the SPI setting in F_{DAC}/4 units.	0x1	R/W
0x00C7	[7:0]	LMFC_PERIOD_SPI[7:0]	Bits [7:0] of the LMFC period from the SPI setting in F_{DAC} /4 units.	0x80	R/W
0x0600 to 0x060F	7	JTX_CONV_MASK	Converter sample mask to 0. Per formatter output control for masking channels not being used. Set appropriate reg bits to 0 to unmask	0x1	R/W
	[6:0]	JTX_CONV_SEL[0:15]	Converter sample crossbar selection (see the Mux4 (JESD204B/C Transmitter JESD Data Router) section), per-formatter output control for mapping to virtual converters. 0 = map formatter output to Converter 0. 1 = map formatter output to Converter 1. 15 = map formatter output to Converter 15.	0x0F	R/W
0x0611	[5:4]	JTX_LINK_204C_SEL	0 = use 8-bit/10-bit Link Layer (204B) 1 = use 64-bit/66-bit Link Layer (204C)	0x0	R/W
0x061B to 0x0622	[4:0]	JTX_LANE_ASSIGN[0:7]	Per-lane control for setting the logical lane source for each physical lane. (little endian to 0x061B assigns logical lane for PHY Lane 0)	0x0-0x7	R/W
0x062D	5	JTX_SYNC_N_SEL	Selects which SYNCxINB± pin to source the SYNC_IN signal 0 = SYNC0INB± 1 = SYNC1INB±	0x0	R/W
0x062E	0	JTX_LINK_EN	Enables the JESD204B/C transmitter 0 = link off	0	R/W

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Table 61. ADC Path JESD204B/C Start-Up Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
			1 = link on		
0x0630	2	JTX_CONV_ASYNCHRONOUS	JESD204B/C Transport Layer mode is asynchronous. This bit identifies asynchronous modes and must be set according to Table 65 through Table 76 in the JESD204B/C Transmitter Mode Tables section.	0x0	R/W
0x0636	5	JTX_ TPL_SYSREF_MASK	Mask the SYSREF input for Subclass 0 operation. 0 = SYSREF is not masked (Subclass 1 mode). 1 = SYSREF is masked (Subclass 0 mode).	0	R/W
0x063D	7	JTX_SCR_CFG	JTX Scrambler Enable. 0 = scrambling disabled. 1 = scrambling is enabled.	0	R/W
	[4:0]	JTX_L_CFG	JTX Number of Lanes Per Link + 1. 0 = 1 lane. 1 = 2 lanes. Values of 4, 6, and ≥8 are not valid.	0	R/W
0x063E	[7:0]	JTX_F_CFG	JTX Number of Octets Per Frame (F = JTX F Configuration + 1). 0 = 1 octet. 1 = 2 octets. 2 = 3 octets. 3 = 4 octets. 5 = 6 octets. 7 = 8 octets. 11 = 12 octets. 15 = 16 octets. 23 = 24 octets. All other values are invalid.	0	R/W
0x063F	[7:0]	JTX_K_CFG	JESD204B/C Transmitter number of frames per multiframe (K = JESD204B/C Transmitter K configuration + 1). Only values where F×K is divisible by 4 can be used.	0	R/W
0x0640	[7:0]	JTX_M_CFG	JESD204B/C transmitter number of virtual converters per link (M= JESD204B/C Transmitter M configuration + 1). 0 = 1 virtual converter 1 = 2 virtual converters 2 = 3 virtual converters 3 = 4 virtual converters 5 = 6 virtual converters 7 = 8 virtual converters 11 = 12 virtual converters 15 = 16 virtual converters All other values are invalid	0	R/W
0x0641	[7:6]	JTX_CS_CFG	Number of Control Bits (CS) Per Sample. 0 = no control bits (CS = 0). 1 = 1 control bit (CS = 1), Control Bit 2 only. 2 = 2 control bits (CS = 2), Control Bit 2 and Control Bit 1 only. 3 = 3 control bits (CS = 3), all control bits (Control Bit 2, Control Bit 1, and Control Bit 0).	0	R/W
	[4:0]	JTX_N_CFG	ADC Converter Resolution (N = JESD204B/C Transmitter N Configuration + 1) 7 = 8-bit resolution 8 = 9-bit resolution 9 = 10-bit resolution	0	R/W

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Table 61. ADC Path JESD204B/C Start-Up Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
			10 = 11-bit resolution 11 = 12-bit resolution 12 = 13-bit resolution 13 = 14-bit resolution 14 = 15-bit resolution 15 = 16-bit resolution All other values are invalid.		
0x0642	[7:5]	JTX_SUBCLASSV_CFG	Subclass Support. 0 = Subclass 0. 1 = Subclass 1. All other values are invalid.	0	R/W
	[4:0]	JTX_NP_CFG	ADC Number of Bits Per Sample (N'). 11 = 12 bits. 15 = 16 bits. 23 = 24 bits. All other values are invalid.	0	R/W
0x0643	[7:5]	JTX_JESDV_CFG	Reflects the JESD204x version. This is only used to populate the JESDV field in the link configuration parameters that are sent across the link during the 2nd multiframe of ILAS when the 8-bit/10-bit link layer is used. 000 = JESD204A 001 = JESD204B All other values are invalid	0	R/W
	[4:0]	JTX_S_CFG	Samples per Converter Frame Cycle (S = JESD204B/C Transmitter S Configuration + 1). 0 = 1 samples per converter. 1 = 2 samples per converter. 3 = 4 samples per converter. 7 = 8 samples per converter. All other values are invalid.	0	R/W
0x0644	7	JTX_HD_CFG	Reflects the status of the JESD204 high density (HD) mode (indicates when converter samples are split across multiple lanes). This is only used to populate the HD field in the Link configuration parameters that are sent across the link during the 2nd multiframe of ILAS when the 8-bit/10-bit link layer is used. HD = 1 for cases where M*S < L 0 = Samples are not split across lanes 1 = Samples are split across 2 lanes	0	R/W
0x0670 to 0x0677	[3:0]	JTX_BR_LOG2_RATIO	For receiver only operation and AD9207 and AD9209: 0 = no bit repeat, for lane rates > 8 Gbps 1 = 2×bit repeat, for lane rates > 4 Gbps and ≤ 8 Gbps 2 = 4×bit repeat, for lane rates > 2 Gbps and ≤ 4 Gbps 3 = 8×bit repeat, for lane rates ≥ 1 Gbps and ≤ 2 Gbps else = not valid For transmit and receive operation, JTX_BR_LOG2_RATIO is set such that the bit rate is > 8Gbps OR equal to the JRx bit rate, whichever yields the greater ratio value. 0 = no bit repeat, JESD204B/C receive to JESD204B/C transmit lane rate ratio is 1:1 and JTx lane rate > 8Gbps 1 = 2×bit repeat, JESD204B/C receive to JESD204B/C transmit lane rate ratio is 2:1 or JTx lane rate is > 4 Gbps and ≤ 8 Gbps	0x0	R/W

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Table 61. ADC Path JESD204B/C Start-Up Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
			2 = 4×bit repeat, JESD204B/C receive to JESD204B/C transmit lane rate ratio is 4:1 or JTx lane rate is > 2 Gbps and ≤ 4 Gbps 3 = 8×bit repeat, JESD204B/C receive to JESD204B/C transmit lane rate ratio is 8:1 or JTx lane rate is ≥ 1 Gbps and ≤ 2 Gbps		
0x0701	7	JTX_PLL_LOCKED	JTX PLL Locked Status Bit 0 = JTx PLL is not locked 1 = JTx PLL is locked	0x0	R
0x070A	0	JTX_SER_BIT FIELD	This bit must be set to 1 if in and asynchronous (ASYNC) mode	0x0	R/W
0x0710	0	FORCE_LINK_RESET	Resets the JESD204B/C Transmitter Link 0 and Link 1 independently (must use JTX_LINK_PAGE bit). 0 = disable reset. 1 = force reset.	0	R/W
0x0713	0	JTX_PHASE_ESTABLISHED	JTX and receive path clocking phase is established. Both JTX_PLL_LOCKED and JTX_PHASE_ESTABLISHED must be 1 for proper operation of the receiver. 0 = phase is not established. 1 = phase established between JTx and receive path readback.	0x0	R
0x0717	[1:0]	DIVM_LCPLL_RC_RX	If in JESD204B mode: 0 = lane rate > 8 Gbps, 1= lane rate ≤ 8 Gbps. If in JESD204C mode: 0 = lane rate ≤ 16 Gbps, 1= lane rate > 16 Gbps. All other values are invalid.	2	R/W
0x0750	[7:0]	PD_SER[7:0]	Power Down Serializer Channel, Bit Per Channel (for example, <0> = ch0 and <1> = ch1). 1 = channel off.	0xFF	R/W
0x0752 to 0x0755	[6:4]	JTX_SWING[2:0] (odd lanes)	These bits set the output swing level relative to the SVDD1 supply.	0x11	R/W
	[2:0]	JTX_SWING[2:0] (even lanes)	000 = 1.0×SVDD1. 001 = 0.85×SVDD1. 010 = 0.75×SVDD1. 011 = 0.50×SVDD1. 1xx = invalid.		
0x075A to0x0761	[6:0]	POST_TAP_LEVEL[0:7]	These bits set the post-tap de-emphasis level in 3 dB steps. 000 = 0 dB. 001 = 3 dB. 010 = 6 dB. 011 = 9 dB. 100 = 12 dB. 101 to 111 are invalid.	0x00	R/W
0x0762	[1:0]	PARDATAMODE_SER_RC	These bits select the JESD204B/C parallel data processing width. 0 = 66 bits (JESD204C). 1 = 40 bits (JESD204B).	0x1	R/W
0x0763 to 0x076A	[7:0]	PRE_TAP_LEVEL[0:7]	These bits set the pre-tap de-emphasis level in 3 dB steps. 000 = 0 dB. 001 = 3 dB. 010 = 6 dB. 011 = 9 dB. 100 = 12 dB. 101 to 111 are invalid.	0x00	R/W

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JESD204B/C Mode Selector Tool and Transmitter Mode Tables

There are over 500 combinations of JESD204B/C and decimation modes represented in Table 65 through Table 76. To simplify the mode selection process, use the JESD204B/C Mode selector tool to narrow down only those modes that support the user's specific application use case. The tool guides the user through the use case description flow chart shown in Figure 60, and gives a small list of applicable transmit and/or receive modes to choose from. This tool is available on the product page for the device.

Mode selection, using the mode selector tool, starts with selecting the device, and then selecting how many transmit and/or receive data paths per link are implemented in the system design. The number of data paths is derived from the number of channels, and how many digital up converters (DUCs) and digital down converters (DDCs) are being implemented. Some examples are provided in the following sub-sections. Once the number of data paths are determined, the subsequent prompts are straightforward to answer. For the minimum instantaneous bandwidth (iBW) requirement, use 80% of the I-Q data rate if using DUCs/DDCs, or use 50% of the converter sample rate if operating in full bandwidth mode (DUCs/DDCs are bypassed). See the following examples for better understanding. In the examples, bold green text indicates user input.

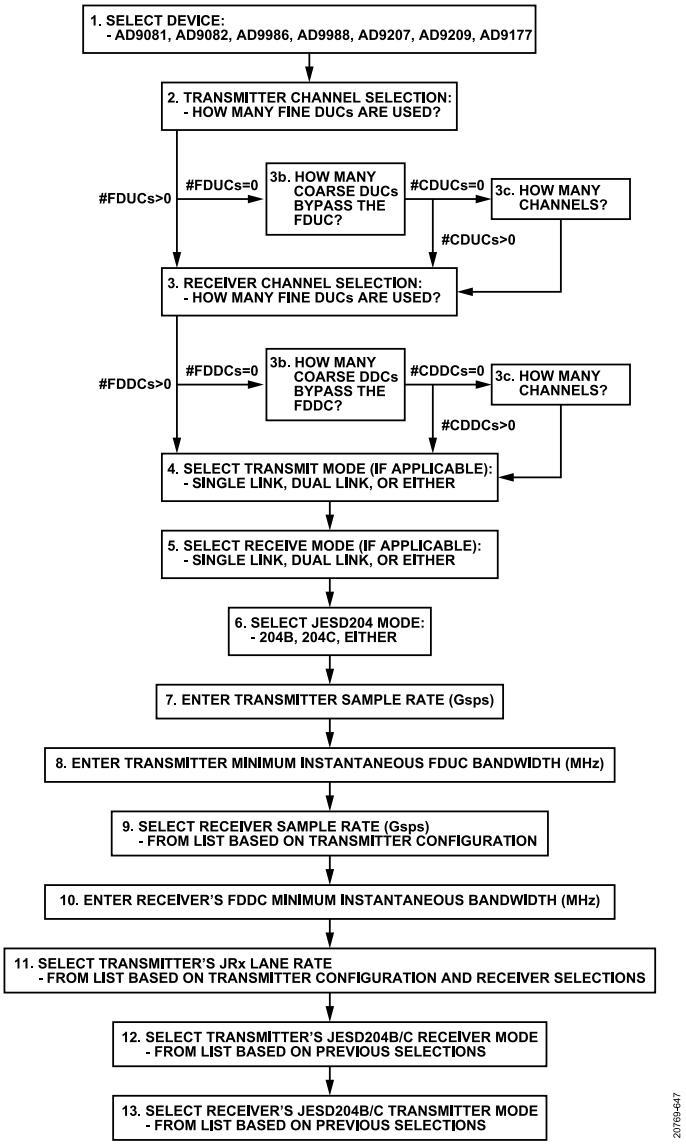

Figure 60. JESD204B/C Mode Selector Flow Diagram

The device ADC path supports many JESD204B and JESD204C modes, as described in the JESD204B/C transmitter mode tables (Table 65 through Table 76).

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For the AD9081, AD9082, AD9207, and AD9209, the JESD204B/C mode is set by setting the L. M, F, S, N, NP, K, and E (JESD204C only) registers along with the coarse and fine decimation and other registers defined in the mode tables as well as Table 61.

For the AD9986, AD9988, and AD9081-4D4AB, the JESD204B/C mode can be selected by using the JTX_MODE and JTX_MODE_S_SEL bits in Register 0x0702 as described in Table 65 through Table 76. Note that, if the JESD204B/C mode number, JTX_MODE, and JTX_MODE_S_SEL columns in the mode tables have N/A values, then these modes are not supported by the AD9081-4D4AB, AD9986 and AD9988. In addition, modes with coarse x fine decimation of 1×1 are not supported by the AD9081-4D4AB, AD9986, and AD9988. Another limitation on the AD9081-4D4AB device is that it does not support modes with an I/Q data rate > 750 MSPS.

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Mode Selector Example 1 Use Case: 2D2A, DAC in 6 GSPS Real Mode, ADC in 6 GSPS Full Bandwidth Mode

Table 62. 2D2A, DAC in 6 GSPS Real Mode, ADC in 6 GSPS Full Bandwidth Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (GSPS)	Output Data Rate from ADC (GSPS)
AD9082	2	2	6	6	6	6

```
Please select product
    1    AD9081
    2    AD9082
    3    AD9986
    4    AD9988
    5    AD9207
    6    AD9209
    7    AD9177
Enter index of selection: 2
How many Fine Digital Up-Converter (FDUC) are used? (0 to bypass, up to 8): 0
How many Coarse Digital Up-Converter (CDUC) will be used? (0 to bypass, up to 4): 0
How many Channels bypass the Digital Up-Converter? (0 to disable, up to 4): 2
How many Fine Digital Down-Converter (FDDC) are used? (0 to bypass, up to 8): 0
How many Coarse Digital Down-Converter (CDDC) will be used? (0 to bypass, up to 4): 0
How many Channels bypass the Digital Down-Converter? (0 to disable, up to 2): 2
For Tx, consider the following modes:
    1    Single Link
    2    Dual Link
    3    Single And Dual Link
Enter index of selection: 1
For Rx, consider the following modes:
    1    Single Link
    2    Dual Link
    3    Single And Dual Link
Enter index of selection: 1
Select the following JESD modes to include
    1    JESD204B
    2    JESD204C
    3    JESD204B AND JESD204C
Enter index of selection: 2
Please enter desired Tx Sample rate (GSPS) [2.9-12]: 6
Please enter min Tx instantaneous Bandwidth (MHz) (6000MHz max): 3000
Please choose Rx Sample Rate from these Tx clock division options (GSPS) [1.45-6]:
    1    6.0
    2    3.0
    3    2.0
    4    1.5
Enter index of selection: 1
Please enter min Rx instantaneous Bandwidth (MHz) (3000MHz max): 3000
Choose a Tx Lane Rate, the below Tx Lane Rates support Tx/Rx with previous constraints (GBPS):
    1    18.5625
    2    24.75
Enter index of selection: 1
Please choose Tx mode from the list:
    1    JESD Mode Number 36  txBW 2400.0  Total Int 1  Coarse Int 1  Fine Int 1  Dual Link False  JESD Deframer JESD204C  L 8  M 2  F 3  S 8  K 256
         N 12  NP 12  LaneRate 18.5625
Enter index of selection: 1
Please choose Rx mode from the list:
    1    JESD Mode Number 28.00  rxBW 3000.0  Total Dec 1  Coarse Dec 1  Fine Dec 1  Dual Link False  JESD Framer JESD204C  Async True  L 8  M
         2  F 3  S 8  K 256  NP 12  LaneRate 18.5625
Enter index of selection: 1
Tx Mode:
JESD Mode Number 36  txBW 2400.0  Total Int 1  Coarse Int 1  Fine Int 1  Dual Link False  JESD Deframer JESD204C  L 8  M 2  F 3  S 8  K 256  N 12
NP 12  LaneRate 18.5625
Rx Mode:
JESD Mode Number 28.00  rxBW 3000.0  Total Dec 1  Coarse Dec 1  Fine Dec 1  Dual Link False  JESD Framer JESD204C  Async True  L 8  M 2  F 3  S 8
K 256  NP 12  LaneRate 18.5625
Script complete
```

Notes on User Input:

1. Full Bandwidth bypasses all DUCs/DDCs
2. Enter number of channels
3. Full bandwidth iBW = sample rate/2

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Mode Selector Example 2 Use Case: 4D2A Dual Band, Dual Link, DAC in 375 MSPS I/Q Mode, ADC in 187.5 MSPS I/Q Mode

Table 63. 4D2A Dual Band, Dual Link, DAC in 375 MSPS I/Q Mode, ADC in 187.5 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (GSPS)	Output Data Rate from ADC (GSPS)
AD9081, AD9082, AD9986, AD9988	4	2	12	3	375 (I/Q)	187.5 (I/Q)

```
Please select product (not all options shown)
    1    AD9081
          *
          *
Enter index of selection: 1
How many Fine Digital Up-Converter (FDUC) are used? (0 to bypass, up to 8): 8
How many Fine Digital Down-Converter (FDDC) are used? (0 to bypass, up to 8): 4
For Tx, consider the following modes:
    1    Single Link
    2    Dual Link
    3    Single And Dual Link
Enter index of selection: 2
For Rx, consider the following modes:
    1    Single Link
    2    Dual Link
    3    Single And Dual Link
Enter index of selection: 2
Select the following JESD modes to include
    1    JESD204B
    2    JESD204C
    3    JESD204B AND JESD204C
Enter index of selection: 3
Please enter desired Tx Sample rate (GSPS) [2.9-12]: 12
Please enter min Tx instantaneous Bandwidth (MHz) (600MHz max): 300
Please choose Rx Sample Rate from these Tx clock division options (GSPS) [1.45-4]:
    1    4.0
    2    3.0
Enter index of selection: 2
Please enter min Rx instantaneous Bandwidth (MHz) (610MHz max): 150
Supported Tx Lane rates (GBPS): [12.375, 15.0, 16.5, 18.5625, 22.0, 24.75]
Supported Rx Lane rates (GBPS): [3.75, 5.0, 6.1875, 7.5, 8.25, 9.2812, 10.0, 12.375, 15.0, 16.5, 18.5625, 24.75]
Choose a Tx Lane Rate, the below Tx Lane Rates support Tx/Rx with previous constraints (GBPS):
    1    12.375
    2    15.0
    3    16.5
    4    18.5625
    5    24.75
Enter index of selection 2
Choose an Rx Lane Rate, the below Rx Lane Rates support Tx/Rx with previous constraints (GBPS):
    1    3.75
    2    7.5
    3    15.0
Enter index of selection 3
Please choose Tx mode from the list:
    1    JESD Mode Number 9  txBW 300.0  Total Int 32  Coarse Int 8  Fine Int 4  Dual Link True  JESD Deframer JESD204B  L 4  M 8  F 4  S 1  K 32  N
16  NP 16  LaneRate 15.0
    2    JESD Mode Number 9  txBW 300.0  Total Int 32  Coarse Int 4  Fine Int 8  Dual Link True  JESD Deframer JESD204B  L 4  M 8  F 4  S 1  K 32  N
16  NP 16  LaneRate 15.0
Enter index of selection: 1
Please choose Rx mode from the list: (not all options shown)
    1    JESD Mode Number 6.00  rxBW 305.25  Total Dec 8  Coarse Dec 2  Fine Dec 4  Dual Link True  JESD Framer JESD204B  Async False  L 2  M 4
          F 4  S 1  K 32  NP 16  LaneRate 15.0
                *
                *
   15    JESD Mode Number 2.00  rxBW 152.62  Total Dec 16  Coarse Dec 4  Fine Dec 4  Dual Link True  JESD Framer JESD204B  Async False  L 1  M
          4  F 8  S 1  K 32  NP 16  LaneRate 15.0
                *
                *
   20    JESD Mode Number 2.10  rxBW 152.62  Total Dec 16  Coarse Dec 4  Fine Dec 4  Dual Link True  JESD Framer JESD204B  Async False  L 1  M
          4  F 16  S 2  K 32  NP 16  LaneRate 15.0
Enter index of selection: 15
Tx Mode: JESD Mode Number 9  txBW 300.0  Total Int 32  Coarse Int 8  Fine Int 4  Dual Link True  JESD Deframer JESD204B  L 4  M 8  F 4  S 1  K 32
N 16  NP 16  LaneRate 15.0
Rx Mode: JESD Mode Number 2.00  rxBW 152.62  Total Dec 16  Coarse Dec 4  Fine Dec 4  Dual Link True  JESD Framer JESD204B  Async False  L 1  M
4  F 8  S 1  K 32  NP 16  LaneRate 15.0
Script complete
```

Notes on User Input:

4. Number of data paths = number of channels x 2 if data is complex and using Fine DUCs/DDCs. Number of data paths = number of channels if data is complex and using Coarse DUCs/DDCs
5. Dual link use case
6. Full bandwidth iBW = 80% of I/Q data rate

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Mode Selector Example 3 Use Case: 4D4A, DAC in 1 GSPS I/Q Mode, ADC in 1 GSPS I/Q Mode

Table 64. 4D2A Dual Band, Dual Link, DAC in 375 MSPS I/Q Mode, ADC in 187.5 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (GSPS)	Output Data Rate from ADC (GSPS)
AD9081, AD9988	4	4	12	4	1 (I/Q)	1 (I/Q)

```
Please select product (not all options shown)
    1    AD9081
         *
         *
Enter index of selection: 1
How many Fine Digital Up-Converter (FDUC) are used? (0 to bypass, up to 8): 0
How many Coarse Digital Up-Converter (CDUC) will be used? (0 to bypass, up to 4): 4
How many Fine Digital Down-Converter (FDDC) are used? (0 to bypass, up to 8): 0
How many Coarse Digital Down-Converter (CDDC) will be used? (0 to bypass, up to 4): 4
For Tx, consider the following modes:
    1    Single Link
    2    Dual Link
    3    Single And Dual Link
Enter index of selection: 1
For Rx, consider the following modes:
    1    Single Link
    2    Dual Link
    3    Single And Dual Link
Enter index of selection: 1
Select the following JESD modes to include
    1    JESD204B
    2    JESD204C
    3    JESD204B AND JESD204C
Enter index of selection: 3
Please enter desired Tx Sample rate (GSPS) [2.9-12]: 12
Please enter min Tx instantaneous Bandwidth (MHz) (1600MHz max): 800
Please choose Rx Sample Rate from these Tx clock division options (GSPS) [1.45-4]:
    1    4.0
    2    3.0
Enter index of selection: 1
Please enter min Rx instantaneous Bandwidth (MHz) (1221MHz max): 800
Choose a Tx Lane Rate, the below Tx Lane Rates support Tx/Rx with previous constraints (GBPS):
    1    12.375
    2    16.5
    3    24.75
Enter index of selection: 2
Please choose Tx mode from the list:
    1    JESD Mode Number 15  txBW 800.0  Total Int 12  Coarse Int 12  Fine Int 1  Dual Link False  JESD Defframer JESD204C  L 8  M 8  F 2  S 1  K
           128  N 16  NP 16  LaneRate 16.5
Enter index of selection: 1
Please choose Rx mode from the list:
    1    JESD Mode Number 16.00  rxBW 814.0  Total Dec 4  Coarse Dec 4  Fine Dec 1  Dual Link False  JESD Framer JESD204C  Async False  L 8  M 8
           F 2  S 1  K 128  NP 16  LaneRate 16.5
    2    JESD Mode Number 16.10  rxBW 814.0  Total Dec 4  Coarse Dec 4  Fine Dec 1  Dual Link False  JESD Framer JESD204C  Async False  L 8  M 8
           F 4  S 2  K 64  NP 16  LaneRate 16.5
    3    JESD Mode Number 26.10  rxBW 1085.33  Total Dec 3  Coarse Dec 3  Fine Dec 1  Dual Link False  JESD Framer JESD204C  Async False  L 8
           M 8  F 6  S 4  K 128  NP 12  LaneRate 16.5
    4    JESD Mode Number 26.00  rxBW 1085.33  Total Dec 3  Coarse Dec 3  Fine Dec 1  Dual Link False  JESD Framer JESD204C  Async False  L 8
           M 8  F 3  S 2  K 256  NP 12  LaneRate 16.5
Enter index of selection: 1
Tx Mode:
JESD Mode Number 15  txBW 800.0  Total Int 12  Coarse Int 12  Fine Int 1  Dual Link False  JESD Defframer JESD204C  L 8  M 8  F 2  S 1  K 128  N 16
NP 16  LaneRate 16.5
Rx Mode:
JESD Mode Number 16.00  rxBW 814.0  Total Dec 4  Coarse Dec 4  Fine Dec 1  Dual Link False  JESD Framer JESD204C  Async False  L 8  M 8  F 2  S 1
K 128  NP 16  LaneRate 16.5

Script complete
```

Notes on User Input:

1. Number of data paths = number of channels x 2 if data is complex and using Fine DUCs/DDCs. Number of data paths = number of channels if data is complex and using Coarse DUCs/DDCs
2. Full bandwidth iBW = 80% of I/Q data rate

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ADC Path Supported JESD204B Modes

ADC Path Supported JESD204B Modes (L = 1)

Table 65. ADC Path Supported JESD204B Modes (L = 1) [1]

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0] [3]	Register 0x0728	Register 0x00CA, Bits[5:0]
3.01	1	1	2	1	32	16	16	0	6	3×2	2.400 to 4.650	>8.000 to 15.500	False	N/A[4]	N/A	0	5	3
3.01	1	1	2	1	32	16	16	0	6	3×2	1.450 to 2.400	4.833 to 8.000	True	N/A	N/A	1	10	3
3.01	1	1	2	1	32	16	16	0	8	2×4, 4×2	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
3.01	1	1	2	1	32	16	16	0	8	2×4, 4×2	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
3.01	1	1	2	1	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
3.01	1	1	2	1	32	16	16	0	12	3×4, 6×2	4.800 to 6.000	>8.000 to 10.000	False	N/A	N/A	0	5	6
3.01	1	1	2	1	32	16	16	0	12	3×4, 6×2	2.400 to 4.800	>4.000 to 8.000	False	N/A	N/A	1	10	6
3.01	1	1	2	1	32	16	16	0	12	3×4, 6×2	1.450 to 2.400	2.417 to 4.000	True	N/A	N/A	2	20	6
3.01	1	1	2	1	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
3.01	1	1	2	1	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
3.01	1	1	2	1	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
3.01	1	1	2	1	32	16	16	0	24	6×4	4.800 to 6.000	>4.000 to 5.000	False	N/A	N/A	1	10	12
3.01	1	1	2	1	32	16	16	0	24	6×4	2.400 to 4.800	>2.000 to 4.000	False	N/A	N/A	2	20	12
3.01	1	1	2	1	32	16	16	0	24	6×4	1.450 to 2.400	1.208 to 2.000	True	N/A	N/A	3	40	12
3.01	1	1	2	1	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
3.01	1	1	2	1	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
3.01	1	1	2	1	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	N/A	N/A	2	20	24
3.01	1	1	2	1	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	N/A	N/A	3	40	24
3.11	1	1	4	2	32	16	16	0	8	2×4, 4×2	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
3.11	1	1	4	2	32	16	16	0	8	2×4, 4×2	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
3.11	1	1	4	2	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
3.11	1	1	4	2	32	16	16	0	12	3×4, 6×2	4.800 to 6.000	>8.000 to 10.000	False	N/A	N/A	0	5	6
3.11	1	1	4	2	32	16	16	0	12	3×4, 6×2	2.400 to 4.800	>4.000 to 8.000	False	N/A	N/A	1	10	6
3.11	1	1	4	2	32	16	16	0	12	3×4, 6×2	1.450 to 2.400	2.417 to 4.000	True	N/A	N/A	2	20	6
3.11	1	1	4	2	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
3.11	1	1	4	2	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
3.11	1	1	4	2	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
3.11	1	1	4	2	32	16	16	0	24	6×4	4.800 to 6.000	>4.000 to 5.000	False	N/A	N/A	1	10	12
3.11	1	1	4	2	32	16	16	0	24	6×4	2.400 to 4.800	>2.000 to 4.000	False	N/A	N/A	2	20	12
3.11	1	1	4	2	32	16	16	0	24	6×4	1.450 to 2.400	1.208 to 2.000	True	N/A	N/A	3	40	12
3.11	1	1	4	2	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
3.11	1	1	4	2	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
3.11	1	1	4	2	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	N/A	N/A	2	20	24
3.11	1	1	4	2	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	N/A	N/A	3	40	24

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Table 65. ADC Path Supported JESD204B Modes (L = 1) [1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0] [3]	Register 0x0728	Register 0x00CA, Bits[5:0]
3.11	1	1	4	2	32	16	16	0	6	3×2	2.400 to 4.650	>8.000 to 15.500	False	N/A	N/A	0	5	3
3.11	1	1	4	2	32	16	16	0	6	3×2	1.450 to 2.400	4.833 to 8.000	True	N/A	N/A	1	10	3
3.00	1	2	4	1	32	16	16	0	12	4×3, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	3	0	0	5	3
3.00	1	2	4	1	32	16	16	0	12	4×3, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	3	0	1	10	3
3.00	1	2	4	1	32	16	16	0	16	2×8, 4×4	3.200 to 6.000	>8.000 to 15.000	False	3	0	0	5	4
3.00	1	2	4	1	32	16	16	0	16	2×8, 4×4	1.600 to 3.200	>4.000 to 8.000	False	3	0	1	10	4
3.00	1	2	4	1	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	3.625 to 4.000	False	3	0	2	20	4
3.00	1	2	4	1	32	16	16	0	24	3×8, 4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	3	0	0	5	6
3.00	1	2	4	1	32	16	16	0	24	3×8, 4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	3	0	1	10	6
3.00	1	2	4	1	32	16	16	0	24	3×8, 4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	3	0	2	20	6
3.00	1	2	4	1	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	3	0	1	10	8
3.00	1	2	4	1	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	3	0	2	20	8
3.00	1	2	4	1	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	3	0	3	40	8
3.00	1	2	4	1	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	3	0	1	10	12
3.00	1	2	4	1	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	3	0	2	20	12
3.00	1	2	4	1	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	3	0	3	40	12
3.00	1	2	4	1	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	3	0	0	5	2
3.00	1	2	4	1	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	3	0	1	10	2
3.00	1	2	4	1	32	16	16	0	64	4×16	3.200 to 6.000	>2.000 to 3.750	False	3	0	2	20	16
3.00	1	2	4	1	32	16	16	0	64	4×16	1.600 to 3.200	>1.000 to 2.000	False	3	0	3	40	16
3.00	1	2	4	1	32	16	16	0	96	6×16	4.800 to 6.000	>2.000 to 2.500	False	3	0	2	20	24
3.00	1	2	4	1	32	16	16	0	96	6×16	2.400 to 4.800	>1.000 to 2.000	False	3	0	3	40	24
3.10	1	2	8	2	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	3	1	0	5	2
3.10	1	2	8	2	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	3	1	1	10	2
3.10	1	2	8	2	32	16	16	0	12	4×3, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	3	1	0	5	3
3.10	1	2	8	2	32	16	16	0	12	4×3, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	3	1	1	10	3
3.10	1	2	8	2	32	16	16	0	16	2×8, 4×4	3.200 to 6.000	>8.000 to 15.000	False	3	1	0	5	4
3.10	1	2	8	2	32	16	16	0	16	2×8, 4×4	1.600 to 3.200	>4.000 to 8.000	False	3	1	1	10	4
3.10	1	2	8	2	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	3.625 to 4.000	False	3	1	2	20	4
3.10	1	2	8	2	32	16	16	0	24	3×8, 4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	3	1	0	5	6
3.10	1	2	8	2	32	16	16	0	24	3×8, 4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	3	1	1	10	6
3.10	1	2	8	2	32	16	16	0	24	3×8, 4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	3	1	2	20	6
3.10	1	2	8	2	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	3	1	1	10	8
3.10	1	2	8	2	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	3	1	2	20	8
3.10	1	2	8	2	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	3	1	3	40	8
3.10	1	2	8	2	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	3	1	1	10	12
3.10	1	2	8	2	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	3	1	2	20	12

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Table 65. ADC Path Supported JESD204B Modes (L = 1) [1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0] [3]	Register 0x0728	Register 0x00CA, Bits[5:0]
3.10	1	2	8	2	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	3	1	3	40	12
3.10	1	2	8	2	32	16	16	0	64	4×16	3.200 to 6.000	>2.000 to 3.750	False	3	1	2	20	16
3.10	1	2	8	2	32	16	16	0	64	4×16	1.600 to 3.200	>1.000 to 2.000	False	3	1	3	40	16
3.10	1	2	8	2	32	16	16	0	96	6×16	4.800 to 6.000	>2.000 to 2.500	False	3	1	2	20	24
3.10	1	2	8	2	32	16	16	0	96	6×16	2.400 to 4.800	>1.000 to 2.000	False	3	1	3	40	24
3.10	1	2	8	2	32	16	16	0	6	2×3, 6×1, 3×2	1.450 to 2.325	9.667 to 15.500	True	3	1	0	10	3
2.00	1	4	8	1	32	16	16	0	16	2×8, 4×4	1.600 to 3.100	>8.000 to 15.500	False	2	0	0	5	2
2.00	1	4	8	1	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	7.250 to 8.000	False	2	0	1	10	2
2.00	1	4	8	1	32	16	16	0	24	3×8, 4×6, 6×4	2.400 to 4.650	>8.000 to 15.500	False	2	0	0	5	3
2.00	1	4	8	1	32	16	16	0	24	3×8, 4×6, 6×4	1.450 to 2.400	4.833 to 8.000	True	2	0	1	10	3
2.00	1	4	8	1	32	16	16	0	32	4×8	3.200 to 6.000	>8.000 to 15.000	False	2	0	0	5	4
2.00	1	4	8	1	32	16	16	0	32	4×8	1.600 to 3.200	>4.000 to 8.000	False	2	0	1	10	4
2.00	1	4	8	1	32	16	16	0	32	4×8	1.450 to 1.600	3.625 to 4.000	False	2	0	2	20	4
2.00	1	4	8	1	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>8.000 to 10.000	False	2	0	0	5	6
2.00	1	4	8	1	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>4.000 to 8.000	False	2	0	1	10	6
2.00	1	4	8	1	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	2.417 to 4.000	True	2	0	2	20	6
2.00	1	4	8	1	32	16	16	0	64	4×16	3.200 to 6.000	>4.000 to 7.500	False	2	0	1	10	8
2.00	1	4	8	1	32	16	16	0	64	4×16	1.600 to 3.200	>2.000 to 4.000	False	2	0	2	20	8
2.00	1	4	8	1	32	16	16	0	64	4×16	1.450 to 1.600	1.812 to 2.000	False	2	0	3	40	8
2.00	1	4	8	1	32	16	16	0	96	4×24, 6×16	4.800 to 6.000	>4.000 to 5.000	False	2	0	1	10	12
2.00	1	4	8	1	32	16	16	0	96	4×24, 6×16	2.400 to 4.800	>2.000 to 4.000	False	2	0	2	20	12
2.00	1	4	8	1	32	16	16	0	96	4×24, 6×16	1.450 to 2.400	1.208 to 2.000	True	2	0	3	40	12
2.10	1	4	16	2	32	16	16	0	24	3×8, 4×6, 6×4	2.400 to 4.650	>8.000 to 15.500	False	2	1	0	5	3
2.10	1	4	16	2	32	16	16	0	24	3×8, 4×6, 6×4	1.450 to 2.400	4.833 to 8.000	True	2	1	1	10	3
2.10	1	4	16	2	32	16	16	0	16	2×8, 4×4	1.600 to 3.100	>8.000 to 15.500	False	2	1	0	5	2
2.10	1	4	16	2	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	7.250 to 8.000	False	2	1	1	10	2
2.10	1	4	16	2	32	16	16	0	32	4×8	3.200 to 6.000	>8.000 to 15.000	False	2	1	0	5	4
2.10	1	4	16	2	32	16	16	0	32	4×8	1.600 to 3.200	>4.000 to 8.000	False	2	1	1	10	4
2.10	1	4	16	2	32	16	16	0	32	4×8	1.450 to 1.600	3.625 to 4.000	False	2	1	2	20	4
2.10	1	4	16	2	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>8.000 to 10.000	False	2	1	0	5	6
2.10	1	4	16	2	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>4.000 to 8.000	False	2	1	1	10	6
2.10	1	4	16	2	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	2.417 to 4.000	True	2	1	2	20	6
2.10	1	4	16	2	32	16	16	0	64	4×16	3.200 to 6.000	>4.000 to 7.500	False	2	1	1	10	8
2.10	1	4	16	2	32	16	16	0	64	4×16	1.600 to 3.200	>2.000 to 4.000	False	2	1	2	20	8
2.10	1	4	16	2	32	16	16	0	64	4×16	1.450 to 1.600	1.812 to 2.000	False	2	1	3	40	8
2.10	1	4	16	2	32	16	16	0	96	4×24, 6×16	4.800 to 6.000	>4.000 to 5.000	False	2	1	1	10	12
2.10	1	4	16	2	32	16	16	0	96	4×24, 6×16	2.400 to 4.800	>2.000 to 4.000	False	2	1	2	20	12

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Table 65. ADC Path Supported JESD204B Modes (L = 1) [1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0] [3]	Register 0x0728	Register 0x00CA, Bits[5:0]
2.10	1	4	16	2	32	16	16	0	96	4×24, 6×16	1.450 to 2.400	1.208 to 2.000	True	2	1	3	40	12
N/A	1	16	32	1	32	16	16	0	96	6×16	2.400 to 4.650	>8.000 to 15.500	False	N/A	N/A	0	5	3
N/A	1	16	32	1	32	16	16	0	96	6×16	1.450 to 2.400	4.833 to 8.000	False	N/A	N/A	1	10	3
N/A	1	16	32	1	32	16	16	0	64	4×16	1.600 to 3.100	>8.000 to 15.500	False	N/A	N/A	0	5	2
N/A	1	16	32	1	32	16	16	0	64	4×16	1.450 to 1.600	7.250 to 8.000	False	N/A	N/A	1	10	2

[1] N/A means not applicable.

[2] JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually.

[3] If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in FDDC Variable IF Dual Modulus and Integer-N Mode APIs. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For transmit and receive path operation, refer to the bit field descriptions for these registers in ADC Path JESD204B/C Start-Up Registers to determine the appropriate setting.

[4] Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

ADC Path Supported JESD204B Modes (L = 2)

Table 66. ADC Path Supported JESD204B Modes (L = 2)[1]

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702 Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
7.01	2	1	1	1	32	16	16	1	4	2×2, 4×1	3.200 to 6.000	>8.000 to 15.000	False	N/A[4]	N/A	0	5	4
7.01	2	1	1	1	32	16	16	1	4	2×2, 4×1	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
7.01	2	1	1	1	32	16	16	1	4	2×2, 4×1	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
7.01	2	1	1	1	32	16	16	1	6	3×2	4.800 to 6.000	>8.000 to 10.000	False	N/A	N/A	0	5	6
7.01	2	1	1	1	32	16	16	1	6	3×2	2.400 to 4.800	>4.000 to 8.000	False	N/A	N/A	1	10	6
7.01	2	1	1	1	32	16	16	1	8	4×2	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
7.01	2	1	1	1	32	16	16	1	8	4×2	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
7.01	2	1	1	1	32	16	16	1	8	4×2	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
7.01	2	1	1	1	32	16	16	1	12	6×2	4.800 to 6.000	>4.000 to 5.000	False	N/A	N/A	1	10	12
7.01	2	1	1	1	32	16	16	1	12	6×2	2.400 to 4.800	>2.000 to 4.000	False	N/A	N/A	2	20	12
7.01	2	1	1	1	32	16	16	1	16	4×4	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
7.01	2	1	1	1	32	16	16	1	16	4×4	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
7.01	2	1	1	1	32	16	16	1	24	6×4	4.800 to 6.000	>2.000 to 2.500	False	N/A	N/A	2	20	24
7.01	2	1	1	1	32	16	16	1	24	6×4	2.400 to 4.800	>1.000 to 2.000	False	N/A	N/A	3	40	24
7.01	2	1	1	1	32	16	16	1	32	4×8	3.200 to 6.000	>1.000 to 1.875	False	N/A	N/A	3	40	32
7.11	2	1	2	2	32	16	16	0	4	2×2, 4×1	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
7.11	2	1	2	2	32	16	16	0	4	2×2, 4×1	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
7.11	2	1	2	2	32	16	16	0	4	2×2, 4×1	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
7.11	2	1	2	2	32	16	16	0	6	3×2	4.800 to 6.000	>8.000 to 10.000	False	N/A	N/A	0	5	6
7.11	2	1	2	2	32	16	16	0	6	3×2	2.400 to 4.800	>4.000 to 8.000	False	N/A	N/A	1	10	6

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Table 66. ADC Path Supported JESD204B Modes (L = 2)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702 Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
7.11	2	1	2	2	32	16	16	0	6	3×2	1.450 to 2.400	2.417 to 4.000	True	N/A	N/A	2	20	6
7.11	2	1	2	2	32	16	16	0	8	4×2	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
7.11	2	1	2	2	32	16	16	0	8	4×2	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
7.11	2	1	2	2	32	16	16	0	8	4×2	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
7.11	2	1	2	2	32	16	16	0	12	6×2	4.800 to 6.000	>4.000 to 5.000	False	N/A	N/A	1	10	12
7.11	2	1	2	2	32	16	16	0	12	6×2	2.400 to 4.800	>2.000 to 4.000	False	N/A	N/A	2	20	12
7.11	2	1	2	2	32	16	16	0	12	6×2	1.450 to 2.400	1.208 to 2.000	True	N/A	N/A	3	40	12
7.11	2	1	2	2	32	16	16	0	16	4×4	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
7.11	2	1	2	2	32	16	16	0	16	4×4	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
7.11	2	1	2	2	32	16	16	0	24	6×4	4.800 to 6.000	>2.000 to 2.500	False	N/A	N/A	2	20	24
7.11	2	1	2	2	32	16	16	0	24	6×4	2.400 to 4.800	>1.000 to 2.000	False	N/A	N/A	3	40	24
7.11	2	1	2	2	32	16	16	0	32	4×8	3.200 to 6.000	>1.000 to 1.875	False	N/A	N/A	3	40	32
7.00	2	2	2	1	32	16	16	0	4	2×2, 4×1	1.600 to 3.100	>8.000 to 15.500	False	7	0	0	5	2
7.00	2	2	2	1	32	16	16	0	4	2×2, 4×1	1.450 to 1.600	7.250 to 8.000	False	7	0	1	10	2
7.00	2	2	2	1	32	16	16	0	6	3×2, 6×1, 2×3	2.400 to 4.650	>8.000 to 15.500	False	7	0	0	5	3
7.00	2	2	2	1	32	16	16	0	6	6×1, 2×3	1.450 to 2.400	4.833 to 8.000	True	7	0	1	10	3
7.00	2	2	2	1	32	16	16	0	8	4×2, 2×4	3.200 to 6.000	>8.000 to 15.000	False	7	0	0	5	4
7.00	2	2	2	1	32	16	16	0	8	4×2, 2×4	1.600 to 3.200	>4.000 to 8.000	False	7	0	1	10	4
7.00	2	2	2	1	32	16	16	0	8	4×2, 2×4	1.450 to 1.600	3.625 to 4.000	False	7	0	2	20	4
7.00	2	2	2	1	32	16	16	0	12	3×4, 4×3, 6×2	4.800 to 6.000	>8.000 to 10.000	False	7	0	0	5	6
7.00	2	2	2	1	32	16	16	0	12	3×4, 4×3, 6×2	2.400 to 4.800	>4.000 to 8.000	False	7	0	1	10	6
7.00	2	2	2	1	32	16	16	0	12	3×4, 4×3, 6×2	1.450 to 2.400	2.417 to 4.000	True	7	0	2	20	6
7.00	2	2	2	1	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	7	0	1	10	8
7.00	2	2	2	1	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	7	0	2	20	8
7.00	2	2	2	1	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	7	0	3	40	8
7.00	2	2	2	1	32	16	16	0	18	6x3	3.600 to 6.000	>4.000 to 6.667	True	7	0	1	10	9
7.00	2	2	2	1	32	16	16	0	18	6x3	1.800 to 3.600	>2.000 to 4.000	True	7	0	2	20	9
7.00	2	2	2	1	32	16	16	0	18	6x3	1.450 to 1.800	1.611 to 2.000	True	7	0	3	40	9
7.00	2	2	2	1	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>4.000 to 5.000	False	7	0	1	10	12
7.00	2	2	2	1	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>2.000 to 4.000	False	7	0	2	20	12
7.00	2	2	2	1	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	1.208 to 2.000	True	7	0	3	40	12
7.00	2	2	2	1	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	7	0	2	20	16
7.00	2	2	2	1	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	7	0	3	40	16
7.00	2	2	2	1	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	7	0	2	20	24
7.00	2	2	2	1	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	7	0	3	40	24
7.00	2	2	2	1	32	16	16	0	18	6x3	3.600 to 6.000	>4.000 to 6.667	True	7	0	1	10	9
7.00	2	2	2	1	32	16	16	0	18	6x3	1.800 to 3.600	>2.000 to 4.000	True	7	0	2	20	9

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Table 66. ADC Path Supported JESD204B Modes (L = 2)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702 Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
7.00	2	2	2	1	32	16	16	0	18	6×3	1.450 to 1.800	1.611 to 2.000	True	7	0	3	40	9
7.10	2	2	4	2	32	16	16	0	4	2×2, 4×1	1.600 to 3.100	>8.000 to 15.500	False	7	1	0	5	2
7.10	2	2	4	2	32	16	16	0	4	2×2, 4×1	1.450 to 1.600	7.250 to 8.000	False	7	1	1	10	2
7.10	2	2	4	2	32	16	16	0	6	3×2, 6×1	2.400 to 4.650	>8.000 to 15.500	False	7	1	0	5	3
7.10	2	2	4	2	32	16	16	0	6	3×2, 6×1	1.450 to 2.400	4.833 to 8.000	True	7	1	1	10	3
7.10	2	2	4	2	32	16	16	0	8	4×2, 2×4	3.200 to 6.000	>8.000 to 15.000	False	7	1	0	5	4
7.10	2	2	4	2	32	16	16	0	8	4×2, 2×4	1.600 to 3.200	>4.000 to 8.000	False	7	1	1	10	4
7.10	2	2	4	2	32	16	16	0	8	4×2, 2×4	1.450 to 1.600	3.625 to 4.000	False	7	1	2	20	4
7.10	2	2	4	2	32	16	16	0	12	3×4, 4×3, 6×2	4.800 to 6.000	>8.000 to 10.000	False	7	1	0	5	6
7.10	2	2	4	2	32	16	16	0	12	3×4, 4×3, 6×2	2.400 to 4.800	>4.000 to 8.000	False	7	1	1	10	6
7.10	2	2	4	2	32	16	16	0	12	3×4, 4×3, 6×2	1.450 to 2.400	2.417 to 4.000	True	7	1	2	20	6
7.10	2	2	4	2	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	7	1	1	10	8
7.10	2	2	4	2	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	7	1	2	20	8
7.10	2	2	4	2	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	7	1	3	40	8
7.10	2	2	4	2	32	16	16	0	18	6×3	3.600 to 6.000	>4.000 to 6.667	True	7	1	1	10	9
7.10	2	2	4	2	32	16	16	0	18	6×3	1.800 to 3.600	>2.000 to 4.000	True	7	1	2	20	9
7.10	2	2	4	2	32	16	16	0	18	6×3	1.450 to 1.800	1.611 to 2.000	True	7	1	3	40	9
7.10	2	2	4	2	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>4.000 to 5.000	False	7	1	1	10	12
7.10	2	2	4	2	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>2.000 to 4.000	False	7	1	2	20	12
7.10	2	2	4	2	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	1.208 to 2.000	True	7	1	3	40	12
7.10	2	2	4	2	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	7	1	2	20	16
7.10	2	2	4	2	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	7	1	3	40	16
7.10	2	2	4	2	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	7	1	2	20	24
7.10	2	2	4	2	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	7	1	3	40	24
5.01	2	4	3	1	32	12	12	0	12	3×4, 6×2	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
5.01	2	4	3	1	32	12	12	0	12	3×4, 6×2	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
5.01	2	4	3	1	32	12	12	0	12	3×4, 6×2	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
5.01	2	4	3	1	32	12	12	0	24	6×4	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
5.01	2	4	3	1	32	12	12	0	24	6×4	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
5.01	2	4	3	1	32	12	12	0	24	6×4	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
5.01	2	4	3	1	32	12	12	0	48	6×8	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
5.01	2	4	3	1	32	12	12	0	48	6×8	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
5.01	2	4	3	1	32	12	12	0	96	6×16	3.200 to 6.000	>1.000 to 1.875	False	N/A	N/A	3	40	32
6.00	2	4	4	1	32	16	16	0	6	3×2, 6×1, 2×3	1.450 to 2.325	9.667 to 15.500	TRUE	N/A	N/A	0	10	3
6.00	2	4	4	1	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	6.0	0	0	5	2
6.00	2	4	4	1	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	6.0	0	1	10	2
6.00	2	4	4	1	32	16	16	0	12	4×3, 2×6, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	6.0	0	0	5	3

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Table 66. ADC Path Supported JESD204B Modes (L = 2)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702 Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
6.00	2	4	4	1	32	16	16	0	12	4×3, 2×6, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	6.0	0	1	10	3
6.00	2	4	4	1	32	16	16	0	16	2×8, 4×4	3.200 to 6.000	>8.000 to 15.000	False	6.0	0	0	5	4
6.00	2	4	4	1	32	16	16	0	16	2×8, 4×4	1.600 to 3.200	>4.000 to 8.000	False	6.0	0	1	10	4
6.00	2	4	4	1	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	3.625 to 4.000	False	6.0	0	2	20	4
6.00	2	4	4	1	32	16	16	0	24	3×8, 4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	6	0	0	5	6
6.00	2	4	4	1	32	16	16	0	24	3×8, 4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	6	0	1	10	6
6.00	2	4	4	1	32	16	16	0	24	3×8, 4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	6	0	2	20	6
6.00	2	4	4	1	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	6	0	1	10	8
6.00	2	4	4	1	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	6	0	2	20	8
6.00	2	4	4	1	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	6	0	3	40	8
6.00	2	4	4	1	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	6	0	1	10	12
6.00	2	4	4	1	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	6	0	2	20	12
6.00	2	4	4	1	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	6	0	3	40	12
6.00	2	4	4	1	32	16	16	0	64	4×16	3.200 to 6.000	>2.000 to 3.750	False	6	0	2	20	16
6.00	2	4	4	1	32	16	16	0	64	4×16	1.600 to 3.200	>1.000 to 2.000	False	6	0	3	40	16
6.00	2	4	4	1	32	16	16	0	96	6×16	4.800 to 6.000	>2.000 to 2.500	False	6	0	2	20	24
6.00	2	4	4	1	32	16	16	0	96	6×16	2.400 to 4.800	>1.000 to 2.000	False	6	0	3	40	24
5.11	2	4	6	2	32	12	12	0	12	3×4, 6×2	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
5.11	2	4	6	2	32	12	12	0	12	3×4, 6×2	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
5.11	2	4	6	2	32	12	12	0	12	3×4, 6×2	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
5.11	2	4	6	2	32	12	12	0	24	6×4	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
5.11	2	4	6	2	32	12	12	0	24	6×4	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
5.11	2	4	6	2	32	12	12	0	24	6×4	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
5.11	2	4	6	2	32	12	12	0	48	6×8	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
5.11	2	4	6	2	32	12	12	0	48	6×8	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
5.11	2	4	6	2	32	12	12	0	96	6×16	3.200 to 6.000	>1.000 to 1.875	False	N/A	N/A	3	40	32
30.01	2	4	6	1	32	16	24	0	12	3×4, 6×2	1.600 to 3.100	>8.000 to 15.500	False	N/A	N/A	0	5	2
30.01	2	4	6	1	32	16	24	0	12	3×4, 6×2	1.450 to 1.600	7.250 to 8.000	False	N/A	N/A	1	10	2
30.01	2	4	6	1	32	16	24	0	24	3×8, 6×4	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
30.01	2	4	6	1	32	16	24	0	24	3×8, 6×4	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
30.01	2	4	6	1	32	16	24	0	24	3×8, 6×4	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
30.01	2	4	6	1	32	16	24	0	48	6×8	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
30.01	2	4	6	1	32	16	24	0	48	6×8	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
30.01	2	4	6	1	32	16	24	0	48	6×8	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
30.01	2	4	6	1	32	16	24	0	96	6×16	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
30.01	2	4	6	1	32	16	24	0	96	6×16	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16

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Table 66. ADC Path Supported JESD204B Modes (L = 2)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702 Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
6.10	2	4	8	2	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	6	1	0	5	2
6.10	2	4	8	2	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	6	1	1	10	2
6.10	2	4	8	2	32	16	16	0	12	4×3, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	6	1	0	5	3
6.10	2	4	8	2	32	16	16	0	12	4×3, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	6	1	1	10	3
6.10	2	4	8	2	32	16	16	0	16	2×8, 4×4	3.200 to 6.000	>8.000 to 15.000	False	6	1	0	5	4
6.10	2	4	8	2	32	16	16	0	16	2×8, 4×4	1.600 to 3.200	>4.000 to 8.000	False	6	1	1	10	4
6.10	2	4	8	2	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	3.625 to 4.000	False	6	1	2	20	4
6.10	2	4	8	2	32	16	16	0	24	3×8, 4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	6	1	0	5	6
6.10	2	4	8	2	32	16	16	0	24	3×8, 4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	6	1	1	10	6
6.10	2	4	8	2	32	16	16	0	24	3×8, 4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	6	1	2	20	6
6.10	2	4	8	2	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	6	1	1	10	8
6.10	2	4	8	2	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	6	1	2	20	8
6.10	2	4	8	2	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	6	1	3	40	8
6.10	2	4	8	2	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	6	1	1	10	12
6.10	2	4	8	2	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	6	1	2	20	12
6.10	2	4	8	2	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	6	1	3	40	12
6.10	2	4	8	2	32	16	16	0	64	4×16	3.200 to 6.000	>2.000 to 3.750	False	6	1	2	20	16
6.10	2	4	8	2	32	16	16	0	64	4×16	1.600 to 3.200	>1.000 to 2.000	False	6	1	3	40	16
6.10	2	4	8	2	32	16	16	0	96	6×16	4.800 to 6.000	>2.000 to 2.500	False	6	1	2	20	24
6.10	2	4	8	2	32	16	16	0	96	6×16	2.400 to 4.800	>1.000 to 2.000	False	6	1	3	40	24
6.10	2	4	8	2	32	16	16	0	6	2×3, 6×1, 3×2	1.450 to 2.325	9.667 to 15.500	True	6	1	0	10	3
30.11	2	4	12	2	32	16	24	0	24	3×8, 6×4	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
30.11	2	4	12	2	32	16	24	0	24	3×8, 6×4	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
30.11	2	4	12	2	32	16	24	0	24	3×8, 6×4	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
30.11	2	4	12	2	32	16	24	0	12	3×4, 6×2	1.600 to 3.100	>8.000 to 15.500	False	N/A	N/A	0	5	2
30.11	2	4	12	2	32	16	24	0	12	3×4, 6×2	1.450 to 1.600	7.250 to 8.000	False	N/A	N/A	1	10	2
30.11	2	4	12	2	32	16	24	0	48	6×8	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
30.11	2	4	12	2	32	16	24	0	48	6×8	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
30.11	2	4	12	2	32	16	24	0	48	6×8	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
30.11	2	4	12	2	32	16	24	0	96	6×16	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
30.11	2	4	12	2	32	16	24	0	96	6×16	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
5.00	2	8	6	1	32	12	12	0	12	4×3, 6×2, 3×4, 2×6	1.600 to 3.100	>8.000 to 15.500	False	5	0	0	5	2
5.00	2	8	6	1	32	12	12	0	12	4×3, 6×2, 3×4, 2×6	1.450 to 1.600	7.250 to 8.000	False	5	0	1	10	2
5.00	2	8	6	1	32	12	12	0	18	6×3, 3×6	2.400 to 4.650	>8.000 to 15.500	False	5	0	0	5	3
5.00	2	8	6	1	32	12	12	0	18	6×3, 3×6	1.450 to 2.400	4.833 to 8.000	True	5	0	1	10	3
5.00	2	8	6	1	32	12	12	0	24	4×6, 6×4	3.200 to 6.000	>8.000 to 15.000	False	5	0	0	5	4
5.00	2	8	6	1	32	12	12	0	24	4×6, 6×4	1.600 to 3.200	>4.000 to 8.000	False	5	0	1	10	4

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Table 66. ADC Path Supported JESD204B Modes (L = 2)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702 Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
5.00	2	8	6	1	32	12	12	0	24	4×6, 6×4	1.450 to 1.600	3.625 to 4.000	False	5	0	2	20	4
5.00	2	8	6	1	32	12	12	0	48	4×12, 6×8	3.200 to 6.000	>4.000 to 7.500	False	5	0	1	10	8
5.00	2	8	6	1	32	12	12	0	48	4×12, 6×8	1.600 to 3.200	>2.000 to 4.000	False	5	0	2	20	8
5.00	2	8	6	1	32	12	12	0	48	4×12, 6×8	1.450 to 1.600	1.812 to 2.000	False	5	0	3	40	8
5.00	2	8	6	1	32	12	12	0	96	4×24, 6×16	3.200 to 6.000	>2.000 to 3.750	False	5	0	2	20	16
5.00	2	8	6	1	32	12	12	0	96	4×24, 6×16	1.600 to 3.200	>1.000 to 2.000	False	5	0	3	40	16
5.00	2	8	6	1	32	12	12	0	16	4×4	2.133 to 4.133	>8.000 to 15.500	True	5	0	0	15	8
5.00	2	8	6	1	32	12	12	0	16	4×4	1.450 to 2.133	5.438 to 8.000	True	5	0	1	30	8
4.00	2	8	8	1	32	16	16	0	16	2×8, 4×4	1.600 to 3.100	>8.000 to 15.500	False	4	0	0	5	2
4.00	2	8	8	1	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	7.250 to 8.000	False	4	0	1	10	2
4.00	2	8	8	1	32	16	16	0	24	3×8, 4×6, 2×12, 6×4	2.400 to 4.650	>8.000 to 15.500	False	4	0	0	5	3
4.00	2	8	8	1	32	16	16	0	24	3×8, 4×6, 2×12, 6×4	1.450 to 2.400	4.833 to 8.000	True	4	0	1	10	3
4.00	2	8	8	1	32	16	16	0	32	2×16, 4×8	3.200 to 6.000	>8.000 to 15.000	False	4	0	0	5	4
4.00	2	8	8	1	32	16	16	0	32	2×16, 4×8	1.600 to 3.200	>4.000 to 8.000	False	4	0	1	10	4
4.00	2	8	8	1	32	16	16	0	32	2×16, 4×8	1.450 to 1.600	3.625 to 4.000	False	4	0	2	20	4
4.00	2	8	8	1	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>8.000 to 10.000	False	4	0	0	5	6
4.00	2	8	8	1	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>4.000 to 8.000	False	4	0	1	10	6
4.00	2	8	8	1	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	2.417 to 4.000	True	4	0	2	20	6
4.00	2	8	8	1	32	16	16	0	64	4×16	3.200 to 6.000	>4.000 to 7.500	False	4	0	1	10	8
4.00	2	8	8	1	32	16	16	0	64	4×16	1.600 to 3.200	>2.000 to 4.000	False	4	0	2	20	8
4.00	2	8	8	1	32	16	16	0	64	4×16	1.450 to 1.600	1.812 to 2.000	False	4	0	3	40	8
4.00	2	8	8	1	32	16	16	0	96	4×24, 6×16	4.800 to 6.000	>4.000 to 5.000	False	4	0	1	10	12
4.00	2	8	8	1	32	16	16	0	96	4×24, 6×16	2.400 to 4.800	>2.000 to 4.000	False	4	0	2	20	12
4.00	2	8	8	1	32	16	16	0	96	4×24, 6×16	1.450 to 2.400	1.208 to 2.000	True	4	0	3	40	12
5.10	2	8	12	2	32	12	12	0	12	4×3, 6×2, 3×4, 2×6	1.600 to 3.100	>8.000 to 15.500	False	5	1	0	5	2
5.10	2	8	12	2	32	12	12	0	12	4×3, 6×2, 3×4, 2×6	1.450 to 1.600	7.250 to 8.000	False	5	1	1	10	2
5.10	2	8	12	2	32	12	12	0	18	6×3, 3×6	2.400 to 4.650	>8.000 to 15.500	False	5	1	0	5	3
5.10	2	8	12	2	32	12	12	0	18	6×3, 3×6	1.450 to 2.400	4.833 to 8.000	True	5	1	1	10	3
5.10	2	8	12	2	32	12	12	0	24	4×6, 6×4	3.200 to 6.000	>8.000 to 15.000	False	5	1	0	5	4
5.10	2	8	12	2	32	12	12	0	24	4×6, 6×4	1.600 to 3.200	>4.000 to 8.000	False	5	1	1	10	4
5.10	2	8	12	2	32	12	12	0	24	4×6, 6×4	1.450 to 1.600	3.625 to 4.000	False	5	1	2	20	4
5.10	2	8	12	2	32	12	12	0	48	4×12, 6×8	3.200 to 6.000	>4.000 to 7.500	False	5	1	1	10	8
5.10	2	8	12	2	32	12	12	0	48	4×12, 6×8	1.600 to 3.200	>2.000 to 4.000	False	5	1	2	20	8
5.10	2	8	12	2	32	12	12	0	48	4×12, 6×8	1.450 to 1.600	1.812 to 2.000	False	5	1	3	40	8
5.10	2	8	12	2	32	12	12	0	96	4×24, 6×16	3.200 to 6.000	>2.000 to 3.750	False	5	1	2	20	16
5.10	2	8	12	2	32	12	12	0	96	4×24, 6×16	1.600 to 3.200	>1.000 to 2.000	False	5	1	3	40	16
30.00	2	8	12	1	32	16	24	0	12	3×4, 6×2, 4×3, 2×6	1.450 to 1.550	14.500 to 15.500	False	30	0	0	5	1

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Table 66. ADC Path Supported JESD204B Modes (L = 2)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702 Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
30.00	2	8	12	1	32	16	24	0	12	6×3, 3×6	1.450 to 2.325	9.667 to 15.500	True	30	0	0	10	3
30.00	2	8	12	1	32	16	24	0	24	3×8, 4×6, 6×4, 2×12	1.600 to 3.100	>8.000 to 15.500	False	30	0	0	5	2
30.00	2	8	12	1	32	16	24	0	24	3×8, 4×6, 6×4, 2×12	1.450 to 1.600	7.250 to 8.000	False	30	0	1	10	2
30.00	2	8	12	1	32	16	24	0	48	2×24, 4×12, 3×16, 6×8	3.200 to 6.000	>8.000 to 15.000	False	30	0	0	5	4
30.00	2	8	12	1	32	16	24	0	48	2×24, 4×12, 3×16, 6×8	1.600 to 3.200	>4.000 to 8.000	False	30	0	1	10	4
30.00	2	8	12	1	32	16	24	0	48	2×24, 4×12, 3×16, 6×8	1.450 to 1.600	3.625 to 4.000	False	30	0	2	20	4
30.00	2	8	12	1	32	16	24	0	96	4×24, 6×16	3.200 to 6.000	>4.000 to 7.500	False	30	0	1	10	8
30.00	2	8	12	1	32	16	24	0	96	4×24, 6×16	1.600 to 3.200	>2.000 to 4.000	False	30	0	2	20	8
30.00	2	8	12	1	32	16	24	0	96	4×24, 6×16	1.450 to 1.600	1.812 to 2.000	False	30	0	3	40	8
4.10	2	8	16	2	32	16	16	0	16	2×8, 4×4	1.600 to 3.100	>8.000 to 15.500	False	4	1	0	5	2
4.10	2	8	16	2	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	7.250 to 8.000	False	4	1	1	10	2
4.10	2	8	16	2	32	16	16	0	24	3×8, 4×6, 6×4	2.400 to 4.650	>8.000 to 15.500	False	4	1	0	5	3
4.10	2	8	16	2	32	16	16	0	24	3×8, 4×6, 6×4	1.450 to 2.400	4.833 to 8.000	True	4	1	1	10	3
4.10	2	8	16	2	32	16	16	0	32	4×8	3.200 to 6.000	>8.000 to 15.000	False	4	1	0	5	4
4.10	2	8	16	2	32	16	16	0	32	4×8	1.600 to 3.200	>4.000 to 8.000	False	4	1	1	10	4
4.10	2	8	16	2	32	16	16	0	32	4×8	1.450 to 1.600	3.625 to 4.000	False	4	1	2	20	4
4.10	2	8	16	2	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>8.000 to 10.000	False	4	1	0	5	6
4.10	2	8	16	2	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>4.000 to 8.000	False	4	1	1	10	6
4.10	2	8	16	2	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	2.417 to 4.000	True	4	1	2	20	6
4.10	2	8	16	2	32	16	16	0	64	4×16	3.200 to 6.000	>4.000 to 7.500	False	4	1	1	10	8
4.10	2	8	16	2	32	16	16	0	64	4×16	1.600 to 3.200	>2.000 to 4.000	False	4	1	2	20	8
4.10	2	8	16	2	32	16	16	0	64	4×16	1.450 to 1.600	1.812 to 2.000	False	4	1	3	40	8
4.10	2	8	16	2	32	16	16	0	96	4×24, 6×16	4.800 to 6.000	>4.000 to 5.000	False	4	1	1	10	12
4.10	2	8	16	2	32	16	16	0	96	4×24, 6×16	2.400 to 4.800	>2.000 to 4.000	False	4	1	2	20	12
4.10	2	8	16	2	32	16	16	0	96	4×24, 6×16	1.450 to 2.400	1.208 to 2.000	True	4	1	3	40	12
30.10	2	8	24	2	32	16	24	0	18	3×6, 6×3	1.450 to 2.325	9.667 to 15.500	True	30	1	0	10	3
30.10	2	8	24	2	32	16	24	0	12	4×3, 6×2, 3×4, 2×6	1.450 to 1.550	14.500 to 15.500	False	30	1	0	5	1
30.10	2	8	24	2	32	16	24	0	24	3×8, 4×6, 6×4, 2×12	1.600 to 3.100	>8.000 to 15.500	False	30	1	0	5	2
30.10	2	8	24	2	32	16	24	0	24	3×8, 4×6, 6×4, 2×12	1.450 to 1.600	7.250 to 8.000	False	30	1	1	10	2
30.10	2	8	24	2	32	16	24	0	48	2×24, 4×12, 3×16, 6×8	3.200 to 6.000	>8.000 to 15.000	False	30	1	0	5	4
30.10	2	8	24	2	32	16	24	0	48	2×24, 4×12, 3×16, 6×8	1.600 to 3.200	>4.000 to 8.000	False	30	1	1	10	4
30.10	2	8	24	2	32	16	24	0	48	2×24, 4×12, 3×16, 6×8	1.450 to 1.600	3.625 to 4.000	False	30	1	2	20	4
30.10	2	8	24	2	32	16	24	0	96	4×24, 6×16	3.200 to 6.000	>4.000 to 7.500	False	30	1	1	10	8
30.10	2	8	24	2	32	16	24	0	96	4×24, 6×16	1.600 to 3.200	>2.000 to 4.000	False	30	1	2	20	8

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Table 66. ADC Path Supported JESD204B Modes (L = 2)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702 Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
30.10	2	8	24	2	32	16	24	0	96	4×24, 6×16	1.450 to 1.600	1.812 to 2.000	False	30	1	3	40	8

[1] N/A means not applicable.

[2] JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually.

[3] If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in Table 42. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For Transmit and receive path operation, refer to the bit field descriptions for these registers in Table 61 to determine the appropriate setting.

[4] Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

ADC Path Supported JESD204B Modes (L = 3)

Table 67. ADC Path Supported JESD204B Modes (L = 3)[1]

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
9.01	3	3	2	1	32	16	16	0	8	3×2	3.200 to 6.000	>8.000 to 15.000	False	N/A[4]	N/A	0	5	3
9.01	3	3	2	1	32	16	16	0	8	3×2	1.600 to 3.200	4.833 to 8.000	True	N/A	N/A	1	10	3
9.01	3	3	2	1	32	16	16	0	8	2×4, 4×2	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
9.01	3	3	2	1	32	16	16	0	8	2×4, 4×2	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
9.01	3	3	2	1	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
9.01	3	3	2	1	32	16	16	0	12	3×4, 6×2	4.800 to 6.000	>8.000 to 10.000	False	N/A	N/A	0	5	6
9.01	3	3	2	1	32	16	16	0	12	3×4, 6×2	2.400 to 4.800	>4.000 to 8.000	False	N/A	N/A	1	10	6
9.01	3	3	2	1	32	16	16	0	12	3×4, 6×2	1.450 to 2.400	2.417 to 4.000	True	N/A	N/A	2	20	6
9.01	3	3	2	1	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
9.01	3	3	2	1	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
9.01	3	3	2	1	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
9.01	3	3	2	1	32	16	16	0	24	6×4	4.800 to 6.000	>4.000 to 5.000	False	N/A	N/A	1	10	12
9.01	3	3	2	1	32	16	16	0	24	6×4	2.400 to 4.800	>2.000 to 4.000	False	N/A	N/A	2	20	12
9.01	3	3	2	1	32	16	16	0	24	6×4	1.450 to 2.400	1.208 to 2.000	True	N/A	N/A	3	40	12
9.01	3	3	2	1	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
9.01	3	3	2	1	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
9.01	3	3	2	1	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	N/A	N/A	2	20	24
9.01	3	3	2	1	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	N/A	N/A	3	40	24
9.11	3	3	4	2	32	16	16	0	8	2×4, 4×2	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
9.11	3	3	4	2	32	16	16	0	8	2×4, 4×2	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
9.11	3	3	4	2	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
9.11	3	3	4	2	32	16	16	0	12	3×4, 6×2	4.800 to 6.000	>8.000 to 10.000	False	N/A	N/A	0	5	6
9.11	3	3	4	2	32	16	16	0	12	3×4, 6×2	2.400 to 4.800	>4.000 to 8.000	False	N/A	N/A	1	10	6
9.11	3	3	4	2	32	16	16	0	12	3×4, 6×2	1.450 to 2.400	2.417 to 4.000	True	N/A	N/A	2	20	6
9.11	3	3	4	2	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8

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Table 67. ADC Path Supported JESD204B Modes (L = 3)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
9.11	3	3	4	2	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
9.11	3	3	4	2	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
9.11	3	3	4	2	32	16	16	0	24	6×4	4.800 to 6.000	>4.000 to 5.000	False	N/A	N/A	1	10	12
9.11	3	3	4	2	32	16	16	0	24	6×4	2.400 to 4.800	>2.000 to 4.000	False	N/A	N/A	2	20	12
9.11	3	3	4	2	32	16	16	0	24	6×4	1.450 to 2.400	1.208 to 2.000	True	N/A	N/A	3	40	12
9.11	3	3	4	2	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
9.11	3	3	4	2	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
9.11	3	3	4	2	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	N/A	N/A	2	20	24
9.11	3	3	4	2	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	N/A	N/A	3	40	24
9.11	3	3	4	2	32	16	16	0	6	3×2	2.400 to 4.650	>8.000 to 15.500	False	N/A	N/A	0	5	3
9.11	3	3	4	2	32	16	16	0	6	3×2	1.450 to 2.400	4.833 to 8.000	True	N/A	N/A	1	10	3
9.00	3	6	4	1	32	16	16	0	8	2×3, 3×2, 6x1	1.450 to 2.325	9.667 to 15.500	True	9	0	0	10	3
9.00	3	6	4	1	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	9	0	0	5	2
9.00	3	6	4	1	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	9	0	1	10	2
9.00	3	6	4	1	32	16	16	0	12	4×3, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	9	0	0	5	3
9.00	3	6	4	1	32	16	16	0	12	4×3, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	9	0	1	10	3
9.00	3	6	4	1	32	16	16	0	16	4×4	3.200 to 6.000	>8.000 to 15.000	False	9	0	0	5	4
9.00	3	6	4	1	32	16	16	0	16	4×4	1.600 to 3.200	>4.000 to 8.000	False	9	0	1	10	4
9.00	3	6	4	1	32	16	16	0	16	4×4	1.450 to 1.600	3.625 to 4.000	False	9	0	2	20	4
9.00	3	6	4	1	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	9	0	0	5	6
9.00	3	6	4	1	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	9	0	1	10	6
9.00	3	6	4	1	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	9	0	2	20	6
9.00	3	6	4	1	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	9	0	1	10	8
9.00	3	6	4	1	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	9	0	2	20	8
9.00	3	6	4	1	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	9	0	3	40	8
9.00	3	6	4	1	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	9	0	1	10	12
9.00	3	6	4	1	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	9	0	2	20	12
9.00	3	6	4	1	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	9	0	3	40	12
9.10	3	6	8	2	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	9	1	0	5	2
9.10	3	6	8	2	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	9	1	1	10	2
9.10	3	6	8	2	32	16	16	0	12	4×3, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	9	1	0	5	3
9.10	3	6	8	2	32	16	16	0	12	4×3, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	9	1	1	10	3
9.10	3	6	8	2	32	16	16	0	16	4×4	3.200 to 6.000	>8.000 to 15.000	False	9	1	0	5	4
9.10	3	6	8	2	32	16	16	0	16	4×4	1.600 to 3.200	>4.000 to 8.000	False	9	1	1	10	4
9.10	3	6	8	2	32	16	16	0	16	4×4	1.450 to 1.600	3.625 to 4.000	False	9	1	2	20	4
9.10	3	6	8	2	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	9	1	0	5	6
9.10	3	6	8	2	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	9	1	1	10	6
9.10	3	6	8	2	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	9	1	2	20	6

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Table 67. ADC Path Supported JESD204B Modes (L = 3)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
9.10	3	6	8	2	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	9	1	1	10	8
9.10	3	6	8	2	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	9	1	2	20	8
9.10	3	6	8	2	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	9	1	3	40	8
9.10	3	6	8	2	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	9	1	1	10	12
9.10	3	6	8	2	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	9	1	2	20	12
9.10	3	6	8	2	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	9	1	3	40	12
9.10	3	6	8	2	32	16	16	0	6	2×3, 6×1, 3×2	1.450 to 2.325	9.667 to 15.500	True	9	1	0	10	3

[1] N/A means not applicable.

[2] JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually.

[3] If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in Table 42. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For Transmit and receive path operation, refer to the bit field descriptions for these registers in Table 61 to determine the appropriate setting.

[4] Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

ADC Path Supported JESD204B Modes (L = 4)

Table 68. ADC Path Supported JESD204B Modes (L = 4)[1]

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
13.01	4	1	1	2	32	16	16	1	1	1×1	1.600 to 3.100	>8.000 to 15.500	False	N/A[4]	N/A	0	5	2
13.01	4	1	1	2	32	16	16	1	1	1×1	1.450 to 1.600	7.250 to 8.000	False	N/A	N/A	1	10	2
13.01	4	1	1	2	32	16	16	1	2	2×1	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
13.01	4	1	1	2	32	16	16	1	2	2×1	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
13.01	4	1	1	2	32	16	16	1	2	2×1	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
13.01	4	1	1	2	32	16	16	1	4	4×1	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
13.01	4	1	1	2	32	16	16	1	4	4×1	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
13.01	4	1	1	2	32	16	16	1	4	4×1	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
13.01	4	1	1	2	32	16	16	1	8	2×4, 4×2	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
13.01	4	1	1	2	32	16	16	1	8	2×4, 4×2	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
13.11	4	1	2	4	32	16	16	0	1	1×1	1.600 to 3.100	>8.000 to 15.500	False	N/A	N/A	0	5	2
13.11	4	1	2	4	32	16	16	0	1	1×1	1.450 to 1.600	7.250 to 8.000	False	N/A	N/A	1	10	2
13.11	4	1	2	4	32	16	16	0	2	2×1	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
13.11	4	1	2	4	32	16	16	0	2	2×1	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
13.11	4	1	2	4	32	16	16	0	2	2×1	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
13.11	4	1	2	4	32	16	16	0	4	4×1	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
13.11	4	1	2	4	32	16	16	0	4	4×1	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
13.11	4	1	2	4	32	16	16	0	4	4×1	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
13.11	4	1	2	4	32	16	16	0	8	2×4, 4×2	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16

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Table 68. ADC Path Supported JESD204B Modes (L = 4)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
13.11	4	1	2	4	32	16	16	0	8	2×4, 4×2	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
13.00	4	2	1	1	32	16	16	1	1	1×1	1.450 to 1.550	14.500 to 15.500	False	13	0	0	5	1
13.00	4	2	1	1	32	16	16	1	2	2×1	1.600 to 3.100	>8.000 to 15.500	False	13	0	0	5	2
13.00	4	2	1	1	32	16	16	1	2	2×1	1.450 to 1.600	7.250 to 8.000	False	13	0	1	10	2
13.00	4	2	1	1	32	16	16	1	3	3×1	2.400 to 4.650	>8.000 to 15.500	False	13	0	0	5	3
13.00	4	2	1	1	32	16	16	1	4	2×2, 4×1	3.200 to 6.000	>8.000 to 15.000	False	13	0	0	5	4
13.00	4	2	1	1	32	16	16	1	4	2×2, 4×1	1.600 to 3.200	>4.000 to 8.000	False	13	0	1	10	4
13.00	4	2	1	1	32	16	16	1	4	2×2, 4×1	1.450 to 1.600	3.625 to 4.000	False	13	0	2	20	4
13.00	4	2	1	1	32	16	16	1	6	3×2, 6×1	4.800 to 6.000	>8.000 to 10.000	False	13	0	0	5	6
13.00	4	2	1	1	32	16	16	1	6	3×2, 6×1	2.400 to 4.800	>4.000 to 8.000	False	13	0	1	10	6
13.00	4	2	1	1	32	16	16	1	8	4×2, 2×4	3.200 to 6.000	>4.000 to 7.500	False	13	0	1	10	8
13.00	4	2	1	1	32	16	16	1	8	4×2, 2×4	1.600 to 3.200	>2.000 to 4.000	False	13	0	2	20	8
13.00	4	2	1	1	32	16	16	1	8	4×2, 2×4	1.450 to 1.600	1.812 to 2.000	False	13	0	3	40	8
13.00	4	2	1	1	32	16	16	1	12	6×2	4.800 to 6.000	>4.000 to 5.000	False	13	0	1	10	12
13.00	4	2	1	1	32	16	16	1	12	6×2	2.400 to 4.800	>2.000 to 4.000	False	13	0	2	20	12
13.00	4	2	1	1	32	16	16	1	16	4×4	3.200 to 6.000	>2.000 to 3.750	False	13	0	2	20	16
13.00	4	2	1	1	32	16	16	1	16	4×4	1.600 to 3.200	>1.000 to 2.000	False	13	0	3	40	16
13.00	4	2	1	1	32	16	16	1	24	6×4	4.800 to 6.000	>2.000 to 2.500	False	13	0	2	20	24
13.00	4	2	1	1	32	16	16	1	24	6×4	2.400 to 4.800	>1.000 to 2.000	False	13	0	3	40	24
13.00	4	2	1	1	32	16	16	1	32	4×8	3.200 to 6.000	>1.000 to 1.875	False	13	0	3	40	32
13.10	4	2	2	2	32	16	16	0	1	1×1	1.450 to 1.550	14.500 to 15.500	False	13	1	0	5	1
13.10	4	2	2	2	32	16	16	0	2	2×1	1.600 to 3.100	>8.000 to 15.500	False	13	1	0	5	2
13.10	4	2	2	2	32	16	16	0	2	2×1	1.450 to 1.600	7.250 to 8.000	False	13	1	1	10	2
13.10	4	2	2	2	32	16	16	0	3	3×1	2.400 to 4.650	>8.000 to 15.500	False	13	1	0	5	3
13.10	4	2	2	2	32	16	16	0	3	3×1	1.450 to 2.400	4.833 to 8.000	True	13	1	1	10	3
13.10	4	2	2	2	32	16	16	0	4	2×2, 4×1	3.200 to 6.000	>8.000 to 15.000	False	13	1	0	5	4
13.10	4	2	2	2	32	16	16	0	4	2×2, 4×1	1.600 to 3.200	>4.000 to 8.000	False	13	1	1	10	4
13.10	4	2	2	2	32	16	16	0	4	2×2, 4×1	1.450 to 1.600	3.625 to 4.000	False	13	1	2	20	4
13.10	4	2	2	2	32	16	16	0	6	3×2, 6×1	4.800 to 6.000	>8.000 to 10.000	False	13	1	0	5	6
13.10	4	2	2	2	32	16	16	0	6	3×2, 6×1	2.400 to 4.800	>4.000 to 8.000	False	13	1	1	10	6
13.10	4	2	2	2	32	16	16	0	6	3×2, 6×1	1.450 to 2.400	2.417 to 4.000	True	13	1	2	20	6
13.10	4	2	2	2	32	16	16	0	8	4×2, 2×4	3.200 to 6.000	>4.000 to 7.500	False	13	1	1	10	8
13.10	4	2	2	2	32	16	16	0	8	4×2, 2×4	1.600 to 3.200	>2.000 to 4.000	False	13	1	2	20	8
13.10	4	2	2	2	32	16	16	0	8	4×2, 2×4	1.450 to 1.600	1.812 to 2.000	False	13	1	3	40	8
13.10	4	2	2	2	32	16	16	0	12	6×2	4.800 to 6.000	>4.000 to 5.000	False	13	1	1	10	12
13.10	4	2	2	2	32	16	16	0	12	6×2	2.400 to 4.800	>2.000 to 4.000	False	13	1	2	20	12

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Table 68. ADC Path Supported JESD204B Modes (L = 4)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
13.10	4	2	2	2	32	16	16	0	12	6×2	1.450 to 2.400	1.208 to 2.000	True	13	1	3	40	12
13.10	4	2	2	2	32	16	16	0	16	4×4	3.200 to 6.000	>2.000 to 3.750	False	13	1	2	20	16
13.10	4	2	2	2	32	16	16	0	16	4×4	1.600 to 3.200	>1.000 to 2.000	False	13	1	3	40	16
13.10	4	2	2	2	32	16	16	0	24	6×4	4.800 to 6.000	>2.000 to 2.500	False	13	1	2	20	24
13.10	4	2	2	2	32	16	16	0	24	6×4	2.400 to 4.800	>1.000 to 2.000	False	13	1	3	40	24
13.10	4	2	2	2	32	16	16	0	32	4×8	3.200 to 6.000	>1.000 to 1.875	False	13	1	3	40	32
11.00	4	4	2	1	32	16	16	0	4	2×2, 4×1	1.600 to 3.100	>8.000 to 15.500	False	11	0	0	5	2
11.00	4	4	2	1	32	16	16	0	4	2×2, 4×1	1.450 to 1.600	7.250 to 8.000	False	11	0	1	10	2
11.00	4	4	2	1	32	16	16	0	6	3×2, 6×1, 2×3	2.400 to 4.650	>8.000 to 15.500	False	11	0	0	5	3
11.00	4	4	2	1	32	16	16	0	6	6×1, 2×3	1.450 to 2.400	4.833 to 8.000	True	11	0	1	10	3
11.00	4	4	2	1	32	16	16	0	8	4×2, 2×4	3.200 to 6.000	>8.000 to 15.000	False	11	0	0	5	4
11.00	4	4	2	1	32	16	16	0	8	4×2, 2×4	1.600 to 3.200	>4.000 to 8.000	False	11	0	1	10	4
11.00	4	4	2	1	32	16	16	0	8	4×2, 2×4	1.450 to 1.600	3.625 to 4.000	False	11	0	2	20	4
11.00	4	4	2	1	32	16	16	0	12	3×4, 2×6, 4×3, 6×2	4.800 to 6.000	>8.000 to 10.000	False	11	0	0	5	6
11.00	4	4	2	1	32	16	16	0	12	3×4, 2×6, 4×3, 6×2	2.400 to 4.800	>4.000 to 8.000	False	11	0	1	10	6
11.00	4	4	2	1	32	16	16	0	12	3×4, 2×6, 4×3, 6×2	1.450 to 2.400	2.417 to 4.000	True	11	0	2	20	6
11.00	4	4	2	1	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	11	0	1	10	8
11.00	4	4	2	1	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	11	0	2	20	8
11.00	4	4	2	1	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	11	0	3	40	8
11.00	4	4	2	1	32	16	16	0	24	6×3	3.600 to 6.000	>4.000 to 6.667	True	11	0	1	10	9
11.00	4	4	2	1	32	16	16	0	24	6×3	1.800 to 3.600	>2.000 to 4.000	True	11	0	2	20	9
11.00	4	4	2	1	32	16	16	0	24	6×3	1.450 to 1.800	1.611 to 2.000	True	11	0	3	40	9
11.00	4	4	2	1	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>4.000 to 5.000	False	11	0	1	10	12
11.00	4	4	2	1	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>2.000 to 4.000	False	11	0	2	20	12
11.00	4	4	2	1	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	1.208 to 2.000	True	11	0	3	40	12
11.00	4	4	2	1	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	11	0	2	20	16
11.00	4	4	2	1	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	11	0	3	40	16
11.00	4	4	2	1	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	11	0	2	20	24
11.00	4	4	2	1	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	11	0	3	40	24
31.01	4	4	3	1	32	16	24	0	12	3×4, 6×2	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
31.01	4	4	3	1	32	16	24	0	12	3×4, 6×2	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
31.01	4	4	3	1	32	16	24	0	12	3×4, 6×2	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
31.01	4	4	3	1	32	16	24	0	24	3×8, 6×4	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
31.01	4	4	3	1	32	16	24	0	24	3×8, 6×4	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
31.01	4	4	3	1	32	16	24	0	24	3×8, 6×4	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
31.01	4	4	3	1	32	16	24	0	48	6×8	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16

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Table 68. ADC Path Supported JESD204B Modes (L = 4)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
31.01	4	4	3	1	32	16	24	0	48	6×8	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
31.01	4	4	3	1	32	16	24	0	96	6×16	3.200 to 6.000	>1.000 to 1.875	False	N/A	N/A	3	40	32
11.10	4	4	4	2	32	16	16	0	4	2×2, 4×1	1.600 to 3.100	>8.000 to 15.500	False	11	1	0	5	2
11.10	4	4	4	2	32	16	16	0	4	2×2, 4×1	1.450 to 1.600	7.250 to 8.000	False	11	1	1	10	2
11.10	4	4	4	2	32	16	16	0	6	3×2, 6×1	2.400 to 4.650	>8.000 to 15.500	False	11	1	0	5	3
11.10	4	4	4	2	32	16	16	0	6	3×2, 6×1	1.450 to 2.400	4.833 to 8.000	True	11	1	1	10	3
11.10	4	4	4	2	32	16	16	0	8	4×2, 2×4	3.200 to 6.000	>8.000 to 15.000	False	11	1	0	5	4
11.10	4	4	4	2	32	16	16	0	8	4×2, 2×4	1.600 to 3.200	>4.000 to 8.000	False	11	1	1	10	4
11.10	4	4	4	2	32	16	16	0	8	4×2, 2×4	1.450 to 1.600	3.625 to 4.000	False	11	1	2	20	4
11.10	4	4	4	2	32	16	16	0	12	3×4, 4×3, 6×2	4.800 to 6.000	>8.000 to 10.000	False	11	1	0	5	6
11.10	4	4	4	2	32	16	16	0	12	3×4, 4×3, 6×2	2.400 to 4.800	>4.000 to 8.000	False	11	1	1	10	6
11.10	4	4	4	2	32	16	16	0	12	3×4, 4×3, 6×2	1.450 to 2.400	2.417 to 4.000	True	11	1	2	20	6
11.10	4	4	4	2	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	11	1	1	10	8
11.10	4	4	4	2	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	11	1	2	20	8
11.10	4	4	4	2	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	11	1	3	40	8
11.10	4	4	4	2	32	16	16	0	18	6×3	3.600 to 6.000	>4.000 to 6.667	True	11	1	1	10	9
11.10	4	4	4	2	32	16	16	0	18	6×3	1.800 to 3.600	>2.000 to 4.000	True	11	1	2	20	9
11.10	4	4	4	2	32	16	16	0	18	6×3	1.450 to 1.800	1.611 to 2.000	True	11	1	3	40	9
11.10	4	4	4	2	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>4.000 to 5.000	False	11	1	1	10	12
11.10	4	4	4	2	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>2.000 to 4.000	False	11	1	2	20	12
11.10	4	4	4	2	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	1.208 to 2.000	True	11	1	3	40	12
11.10	4	4	4	2	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	11	1	2	20	16
11.10	4	4	4	2	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	11	1	3	40	16
11.10	4	4	4	2	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	11	1	2	20	24
11.10	4	4	4	2	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	11	1	3	40	24
31.11	4	4	6	2	32	16	24	0	24	3×8, 6×4	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
31.11	4	4	6	2	32	16	24	0	24	3×8, 6×4	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
31.11	4	4	6	2	32	16	24	0	24	3×8, 6×4	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
31.11	4	4	6	2	32	16	24	0	12	3×4, 6×2	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
31.11	4	4	6	2	32	16	24	0	12	3×4, 6×2	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
31.11	4	4	6	2	32	16	24	0	12	3×4, 6×2	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
31.11	4	4	6	2	32	16	24	0	48	6×8	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
31.11	4	4	6	2	32	16	24	0	48	6×8	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
31.11	4	4	6	2	32	16	24	0	96	6×16	3.200 to 6.000	>1.000 to 1.875	False	N/A	N/A	3	40	32
10.00	4	8	4	1	32	16	16	0	8	3×2, 6×1, 2×3	1.450 to 2.325	9.667 to 15.500	TRUE	10	0	0	10	3
10.00	4	8	4	1	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	10	0	0	5	2
10.00	4	8	4	1	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	10	0	1	10	2

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Table 68. ADC Path Supported JESD204B Modes (L = 4)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
10.00	4	8	4	1	32	16	16	0	12	4×3, 2×6, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	10	0	0	5	3
10.00	4	8	4	1	32	16	16	0	12	4×3, 2×6, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	10	0	1	10	3
10.00	4	8	4	1	32	16	16	0	16	2×8, 4×4	3.200 to 6.000	>8.000 to 15.000	False	10	0	0	5	4
10.00	4	8	4	1	32	16	16	0	16	2×8, 4×4	1.600 to 3.200	>4.000 to 8.000	False	10	0	1	10	4
10.00	4	8	4	1	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	3.625 to 4.000	False	10	0	2	20	4
10.00	4	8	4	1	32	16	16	0	24	3×8, 4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	10	0	0	5	6
10.00	4	8	4	1	32	16	16	0	24	3×8, 4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	10	0	1	10	6
10.00	4	8	4	1	32	16	16	0	24	3×8, 4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	10	0	2	20	6
10.00	4	8	4	1	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	10	0	1	10	8
10.00	4	8	4	1	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	10	0	2	20	8
10.00	4	8	4	1	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	10	0	3	40	8
10.00	4	8	4	1	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	10	0	1	10	12
10.00	4	8	4	1	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	10	0	2	20	12
10.00	4	8	4	1	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	10	0	3	40	12
10.00	4	8	4	1	32	16	16	0	64	4×16	3.200 to 6.000	>2.000 to 3.750	False	10	0	2	20	16
10.00	4	8	4	1	32	16	16	0	64	4×16	1.600 to 3.200	>1.000 to 2.000	False	10	0	3	40	16
10.00	4	8	4	1	32	16	16	0	96	6×16	4.800 to 6.000	>2.000 to 2.500	False	10	0	2	20	24
10.00	4	8	4	1	32	16	16	0	96	6×16	2.400 to 4.800	>1.000 to 2.000	False	10	0	3	40	24
31.00	4	8	6	1	32	16	24	0	12	3×4, 6×2, 4×3, 2×6	1.600 to 3.100	>8.000 to 15.500	False	31	0	0	5	2
31.00	4	8	6	1	32	16	24	0	12	3×4, 6×2, 4×3, 2×6	1.450 to 1.600	7.250 to 8.000	False	31	0	1	10	2
31.00	4	8	6	1	32	16	24	0	18	6×3, 3×6	2.400 to 4.650	>8.000 to 15.500	False	31	0	0	5	3
31.00	4	8	6	1	32	16	24	0	18	6×3, 3×6	1.450 to 2.400	4.833 to 8.000	True	31	0	1	10	3
31.00	4	8	6	1	32	16	24	0	24	4×6, 6×4	3.200 to 6.000	>8.000 to 15.000	False	31	0	0	5	4
31.00	4	8	6	1	32	16	24	0	24	4×6, 6×4	1.600 to 3.200	>4.000 to 8.000	False	31	0	1	10	4
31.00	4	8	6	1	32	16	24	0	24	4×6, 6×4	1.450 to 1.600	3.625 to 4.000	False	31	0	2	20	4
31.00	4	8	6	1	32	16	24	0	48	4×12, 6×8	3.200 to 6.000	>4.000 to 7.500	False	31	0	1	10	8
31.00	4	8	6	1	32	16	24	0	48	4×12, 6×8	1.600 to 3.200	>2.000 to 4.000	False	31	0	2	20	8
31.00	4	8	6	1	32	16	24	0	48	4×12, 6×8	1.450 to 1.600	1.812 to 2.000	False	31	0	3	40	8
31.00	4	8	6	1	32	16	24	0	96	4×24, 6×16	3.200 to 6.000	>2.000 to 3.750	False	31	0	2	20	16
31.00	4	8	6	1	32	16	24	0	96	4×24, 6×16	1.600 to 3.200	>1.000 to 2.000	False	31	0	3	40	16
10.10	4	8	8	2	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	10	1	0	5	2
10.10	4	8	8	2	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	10	1	1	10	2
10.10	4	8	8	2	32	16	16	0	12	4×3, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	10	1	0	5	3
10.10	4	8	8	2	32	16	16	0	12	4×3, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	10	1	1	10	3
10.10	4	8	8	2	32	16	16	0	16	2×8, 4×4	3.200 to 6.000	>8.000 to 15.000	False	10	1	0	5	4
10.10	4	8	8	2	32	16	16	0	16	2×8, 4×4	1.600 to 3.200	>4.000 to 8.000	False	10	1	1	10	4
10.10	4	8	8	2	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	3.625 to 4.000	False	10	1	2	20	4

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Table 68. ADC Path Supported JESD204B Modes (L = 4)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
10.10	4	8	8	2	32	16	16	0	24	3×8, 4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	10	1	0	5	6
10.10	4	8	8	2	32	16	16	0	24	3×8, 4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	10	1	1	10	6
10.10	4	8	8	2	32	16	16	0	24	3×8, 4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	10	1	2	20	6
10.10	4	8	8	2	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	10	1	1	10	8
10.10	4	8	8	2	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	10	1	2	20	8
10.10	4	8	8	2	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	10	1	3	40	8
10.10	4	8	8	2	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	10	1	1	10	12
10.10	4	8	8	2	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	10	1	2	20	12
10.10	4	8	8	2	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	10	1	3	40	12
10.10	4	8	8	2	32	16	16	0	64	4×16	3.200 to 6.000	>2.000 to 3.750	False	10	1	2	20	16
10.10	4	8	8	2	32	16	16	0	64	4×16	1.600 to 3.200	>1.000 to 2.000	False	10	1	3	40	16
10.10	4	8	8	2	32	16	16	0	96	6×16	4.800 to 6.000	>2.000 to 2.500	False	10	1	2	20	24
10.10	4	8	8	2	32	16	16	0	96	6×16	2.400 to 4.800	>1.000 to 2.000	False	10	1	3	40	24
10.10	4	8	8	2	32	16	16	0	6	2×3, 6×1, 3×2	1.450 to 2.325	9.667 to 15.500	True	10	1	0	10	3
31.10	4	8	12	2	32	16	24	0	18	3×6, 6×3	2.400 to 4.650	>8.000 to 15.500	False	31	1	0	5	3
31.10	4	8	12	2	32	16	24	0	18	3×6, 6×3	1.450 to 2.400	4.833 to 8.000	True	31	1	1	10	3
31.10	4	8	12	2	32	16	24	0	12	4×3, 6×2, 3×4, 2×6	1.600 to 3.100	>8.000 to 15.500	False	31	1	0	5	2
31.10	4	8	12	2	32	16	24	0	12	4×3, 6×2, 3×4, 2×6	1.450 to 1.600	7.250 to 8.000	False	31	1	1	10	2
31.10	4	8	12	2	32	16	24	0	24	4×6, 6×4	3.200 to 6.000	>8.000 to 15.000	False	31	1	0	5	4
31.10	4	8	12	2	32	16	24	0	24	4×6, 6×4	1.600 to 3.200	>4.000 to 8.000	False	31	1	1	10	4
31.10	4	8	12	2	32	16	24	0	24	4×6, 6×4	1.450 to 1.600	3.625 to 4.000	False	31	1	2	20	4
31.10	4	8	12	2	32	16	24	0	48	4×12, 6×8	3.200 to 6.000	>4.000 to 7.500	False	31	1	1	10	8
31.10	4	8	12	2	32	16	24	0	48	4×12, 6×8	1.600 to 3.200	>2.000 to 4.000	False	31	1	2	20	8
31.10	4	8	12	2	32	16	24	0	48	4×12, 6×8	1.450 to 1.600	1.812 to 2.000	False	31	1	3	40	8
31.10	4	8	12	2	32	16	24	0	96	4×24, 6×16	3.200 to 6.000	>2.000 to 3.750	False	31	1	2	20	16
31.10	4	8	12	2	32	16	24	0	96	4×24, 6×16	1.600 to 3.200	>1.000 to 2.000	False	31	1	3	40	16
12.00	4	16	8	1	32	16	16	0	16	2×8, 4×4	1.600 to 3.100	>8.000 to 15.500	False	12	0	0	5	2
12.00	4	16	8	1	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	7.250 to 8.000	False	12	0	1	10	2
12.00	4	16	8	1	32	16	16	0	24	3×8, 4×6, 6×4	2.400 to 4.650	>8.000 to 15.500	False	12	0	0	5	3
12.00	4	16	8	1	32	16	16	0	24	3×8, 4×6, 6×4	1.450 to 2.400	4.833 to 8.000	True	12	0	1	10	3
12.00	4	16	8	1	32	16	16	0	32	4×8	3.200 to 6.000	>8.000 to 15.000	False	12	0	0	5	4
12.00	4	16	8	1	32	16	16	0	32	4×8	1.600 to 3.200	>4.000 to 8.000	False	12	0	1	10	4
12.00	4	16	8	1	32	16	16	0	32	4×8	1.450 to 1.600	3.625 to 4.000	False	12	0	2	20	4
12.00	4	16	8	1	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>8.000 to 10.000	False	12	0	0	5	6
12.00	4	16	8	1	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>4.000 to 8.000	False	12	0	1	10	6
12.00	4	16	8	1	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	2.417 to 4.000	True	12	0	2	20	6
12.00	4	16	8	1	32	16	16	0	64	4×16	3.200 to 6.000	>4.000 to 7.500	False	12	0	1	10	8

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Table 68. ADC Path Supported JESD204B Modes (L = 4)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
12.00	4	16	8	1	32	16	16	0	64	4×16	1.600 to 3.200	>2.000 to 4.000	False	12	0	2	20	8
12.00	4	16	8	1	32	16	16	0	64	4×16	1.450 to 1.600	1.812 to 2.000	False	12	0	3	40	8
12.00	4	16	8	1	32	16	16	0	96	4×24, 6×16	4.800 to 6.000	>4.000 to 5.000	False	12	0	1	10	12
12.00	4	16	8	1	32	16	16	0	96	4×24, 6×16	2.400 to 4.800	>2.000 to 4.000	False	12	0	2	20	12
12.00	4	16	8	1	32	16	16	0	96	4×24, 6×16	1.450 to 2.400	1.208 to 2.000	True	12	0	3	40	12
12.10	4	16	16	2	32	16	16	0	24	3×8, 4×6, 6×4	2.400 to 4.650	>8.000 to 15.500	False	12	1	0	5	3
12.10	4	16	16	2	32	16	16	0	24	3×8, 4×6, 6×4	1.450 to 2.400	4.833 to 8.000	True	12	1	1	10	3
12.10	4	16	16	2	32	16	16	0	16	2×8, 4×4	1.600 to 3.100	>8.000 to 15.500	False	12	1	0	5	2
12.10	4	16	16	2	32	16	16	0	16	2×8, 4×4	1.450 to 1.600	7.250 to 8.000	False	12	1	1	10	2
12.10	4	16	16	2	32	16	16	0	32	4×8	3.200 to 6.000	>8.000 to 15.000	False	12	1	0	5	4
12.10	4	16	16	2	32	16	16	0	32	4×8	1.600 to 3.200	>4.000 to 8.000	False	12	1	1	10	4
12.10	4	16	16	2	32	16	16	0	32	4×8	1.450 to 1.600	3.625 to 4.000	False	12	1	2	20	4
12.10	4	16	16	2	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>8.000 to 10.000	False	12	1	0	5	6
12.10	4	16	16	2	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>4.000 to 8.000	False	12	1	1	10	6
12.10	4	16	16	2	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	2.417 to 4.000	True	12	1	2	20	6
12.10	4	16	16	2	32	16	16	0	64	4×16	3.200 to 6.000	>4.000 to 7.500	False	12	1	1	10	8
12.10	4	16	16	2	32	16	16	0	64	4×16	1.600 to 3.200	>2.000 to 4.000	False	12	1	2	20	8
12.10	4	16	16	2	32	16	16	0	64	4×16	1.450 to 1.600	1.812 to 2.000	False	12	1	3	40	8
12.10	4	16	16	2	32	16	16	0	96	4×24, 6×16	4.800 to 6.000	>4.000 to 5.000	False	12	1	1	10	12
12.10	4	16	16	2	32	16	16	0	96	4×24, 6×16	2.400 to 4.800	>2.000 to 4.000	False	12	1	2	20	12
12.10	4	16	16	2	32	16	16	0	96	4×24, 6×16	1.450 to 2.400	1.208 to 2.000	True	12	1	3	40	12

[1] N/A means not applicable.

[2] JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually.

[3] If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in Table 42. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For Transmit and receive path operation, refer to the bit field descriptions for these registers in Table 61 to determine the appropriate setting.

[4] Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

ADC Path Supported JESD204B Modes (L = 6)

Table 69. ADC Path Supported JESD204B Modes (L = 6)[1]

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
15.01	6	6	2	1	32	16	16	0	6	3×2	2.400 to 4.650	>8.000 to 15.500	False	N/A[4]	N/A	0	5	3
15.01	6	6	2	1	32	16	16	0	6	3×2	1.450 to 2.400	4.833 to 8.000	True	N/A	N/A	1	10	3
15.01	6	6	2	1	32	16	16	0	8	2×4, 4×2	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
15.01	6	6	2	1	32	16	16	0	8	2×4, 4×2	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
15.01	6	6	2	1	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
15.01	6	6	2	1	32	16	16	0	12	3×4, 6×2	4.800 to 6.000	>8.000 to 10.000	False	N/A	N/A	0	5	6

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Table 69. ADC Path Supported JESD204B Modes (L = 6)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
15.01	6	6	2	1	32	16	16	0	12	3×4, 6×2	2.400 to 4.800	>4.000 to 8.000	False	N/A	N/A	1	10	6
15.01	6	6	2	1	32	16	16	0	12	3×4, 6×2	1.450 to 2.400	2.417 to 4.000	True	N/A	N/A	2	20	6
15.01	6	6	2	1	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
15.01	6	6	2	1	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
15.01	6	6	2	1	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
15.01	6	6	2	1	32	16	16	0	24	6×4	4.800 to 6.000	>4.000 to 5.000	False	N/A	N/A	1	10	12
15.01	6	6	2	1	32	16	16	0	24	6×4	2.400 to 4.800	>2.000 to 4.000	False	N/A	N/A	2	20	12
15.01	6	6	2	1	32	16	16	0	24	6×4	1.450 to 2.400	1.208 to 2.000	True	N/A	N/A	3	40	12
15.01	6	6	2	1	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
15.01	6	6	2	1	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
15.01	6	6	2	1	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	N/A	N/A	2	20	24
15.01	6	6	2	1	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	N/A	N/A	3	40	24
15.11																		
15.11	6	6	4	2	32	16	16	0	8	2×4, 4×2	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
15.11	6	6	4	2	32	16	16	0	8	2×4, 4×2	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
15.11	6	6	4	2	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
15.11	6	6	4	2	32	16	16	0	12	3×4, 6×2	4.800 to 6.000	>8.000 to 10.000	False	N/A	N/A	0	5	6
15.11	6	6	4	2	32	16	16	0	12	3×4, 6×2	2.400 to 4.800	>4.000 to 8.000	False	N/A	N/A	1	10	6
15.11	6	6	4	2	32	16	16	0	12	3×4, 6×2	1.450 to 2.400	2.417 to 4.000	True	N/A	N/A	2	20	6
15.11	6	6	4	2	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
15.11	6	6	4	2	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
15.11	6	6	4	2	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
15.11	6	6	4	2	32	16	16	0	24	6×4	4.800 to 6.000	>4.000 to 5.000	False	N/A	N/A	1	10	12
15.11	6	6	4	2	32	16	16	0	24	6×4	2.400 to 4.800	>2.000 to 4.000	False	N/A	N/A	2	20	12
15.11	6	6	4	2	32	16	16	0	24	6×4	1.450 to 2.400	1.208 to 2.000	True	N/A	N/A	3	40	12
15.11	6	6	4	2	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
15.11	6	6	4	2	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
15.11	6	6	4	2	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	N/A	N/A	2	20	24
15.11	6	6	4	2	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	N/A	N/A	3	40	24
15.11	6	6	4	2	32	16	16	0	6	3×2	2.400 to 4.650	>8.000 to 15.500	False	N/A	N/A	0	5	3
15.00	6	6	4	2	32	16	16	0	6	3×2	1.450 to 2.400	4.833 to 8.000	True	N/A	N/A	1	10	3
15.00	6	12	4	1	32	16	16	0	6	3×2, 2×3, 6×1	1.450 to 2.325	9.667 to 15.500	TRUE	15	0	0	10	3
15.00	6	12	4	1	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	15	0	0	5	2
15.00	6	12	4	1	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	15	0	1	10	2
15.00	6	12	4	1	32	16	16	0	12	4×3, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	15	0	0	5	3
15.00	6	12	4	1	32	16	16	0	12	4×3, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	15	0	1	10	3
15.00	6	12	4	1	32	16	16	0	16	4×4	3.200 to 6.000	>8.000 to 15.000	False	15	0	0	5	4

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Table 69. ADC Path Supported JESD204B Modes (L = 6)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
15.00	6	12	4	1	32	16	16	0	16	4×4	1.600 to 3.200	>4.000 to 8.000	False	15	0	1	10	4
15.00	6	12	4	1	32	16	16	0	16	4×4	1.450 to 1.600	3.625 to 4.000	False	15	0	2	20	4
15.00	6	12	4	1	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	15	0	0	5	6
15.00	6	12	4	1	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	15	0	1	10	6
15.00	6	12	4	1	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	15	0	2	20	6
15.00	6	12	4	1	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	15	0	1	10	8
15.00	6	12	4	1	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	15	0	2	20	8
15.00	6	12	4	1	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	15	0	3	40	8
15.00	6	12	4	1	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	15	0	1	10	12
15.00	6	12	4	1	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	15	0	2	20	12
15.10	6	12	4	1	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	15	0	3	40	12
15.10	6	12	8	2	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	15	1	0	5	2
15.10	6	12	8	2	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	15	1	1	10	2
15.10	6	12	8	2	32	16	16	0	12	4×3, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	15	1	0	5	3
15.10	6	12	8	2	32	16	16	0	12	4×3, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	15	1	1	10	3
15.10	6	12	8	2	32	16	16	0	16	4×4	3.200 to 6.000	>8.000 to 15.000	False	15	1	0	5	4
15.10	6	12	8	2	32	16	16	0	16	4×4	1.600 to 3.200	>4.000 to 8.000	False	15	1	1	10	4
15.10	6	12	8	2	32	16	16	0	16	4×4	1.450 to 1.600	3.625 to 4.000	False	15	1	2	20	4
15.10	6	12	8	2	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	15	1	0	5	6
15.10	6	12	8	2	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	15	1	1	10	6
15.10	6	12	8	2	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	15	1	2	20	6
15.10	6	12	8	2	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	15	1	1	10	8
15.10	6	12	8	2	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	15	1	2	20	8
15.10	6	12	8	2	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	15	1	3	40	8
15.10	6	12	8	2	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	15	1	1	10	12
15.10	6	12	8	2	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	15	1	2	20	12
15.10	6	12	8	2	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	15	1	3	40	12
15.10	6	12	8	2	32	16	16	0	6	2×3, 6×1, 3×2	1.450 to 2.325	9.667 to 15.500	True	15	1	0	10	3

1 N/A means not applicable.

2 JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually.

3 If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in Table 42. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For Transmit and receive path operation, refer to the bit field descriptions for these registers in Table 61 to determine the appropriate setting.

4 Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

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ADC Path Supported JESD204B Modes (L = 8)

Table 70. ADC Path Supported JESD204B Modes (L = 8)[1]

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
19.01	8	1	1	4	32	16	16	1	1	1×1	3.200 to 6.000	>8.000 to 15.000	False	N/A[4]	N/A	0	5	4
19.01	8	1	1	4	32	16	16	1	1	1×1	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
19.01	8	1	1	4	32	16	16	1	1	1×1	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
19.01	8	1	1	4	32	16	16	1	2	2×1	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
19.01	8	1	1	4	32	16	16	1	2	2×1	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
19.01	8	1	1	4	32	16	16	1	2	2×1	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
19.01	8	1	1	4	32	16	16	1	4	4×1	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
19.01	8	1	1	4	32	16	16	1	4	4×1	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
19.11	8	1	2	8	32	16	16	0	1	1×1	3.200 to 6.000	>8.000 to 15.000	False	N/A	N/A	0	5	4
19.11	8	1	2	8	32	16	16	0	1	1×1	1.600 to 3.200	>4.000 to 8.000	False	N/A	N/A	1	10	4
19.11	8	1	2	8	32	16	16	0	1	1×1	1.450 to 1.600	3.625 to 4.000	False	N/A	N/A	2	20	4
19.11	8	1	2	8	32	16	16	0	2	2×1	3.200 to 6.000	>4.000 to 7.500	False	N/A	N/A	1	10	8
19.11	8	1	2	8	32	16	16	0	2	2×1	1.600 to 3.200	>2.000 to 4.000	False	N/A	N/A	2	20	8
19.11	8	1	2	8	32	16	16	0	2	2×1	1.450 to 1.600	1.812 to 2.000	False	N/A	N/A	3	40	8
19.11	8	1	2	8	32	16	16	0	4	4×1	3.200 to 6.000	>2.000 to 3.750	False	N/A	N/A	2	20	16
19.11	8	1	2	8	32	16	16	0	4	4×1	1.600 to 3.200	>1.000 to 2.000	False	N/A	N/A	3	40	16
19.00	8	2	1	2	32	16	16	1	1	1×1	1.600 to 3.100	>8.000 to 15.500	False	19	0	0	5	2
19.00	8	2	1	2	32	16	16	1	1	1×1	1.450 to 1.600	7.250 to 8.000	False	19	0	1	10	2
19.00	8	2	1	2	32	16	16	1	2	2×1	3.200 to 6.000	>8.000 to 15.000	False	19	0	0	5	4
19.00	8	2	1	2	32	16	16	1	2	2×1	1.600 to 3.200	>4.000 to 8.000	False	19	0	1	10	4
19.00	8	2	1	2	32	16	16	1	2	2×1	1.450 to 1.600	3.625 to 4.000	False	19	0	2	20	4
19.00	8	2	1	2	32	16	16	1	3	3×1	4.800 to 6.000	>8.000 to 10.000	False	19	0	0	5	6
19.00	8	2	1	2	32	16	16	1	3	3×1	2.400 to 4.800	>4.000 to 8.000	False	19	0	1	10	6
19.00	8	2	1	2	32	16	16	1	3	3×1	1.450 to 2.400	2.417 to 4.000	True	19	0	2	20	6
19.00	8	2	1	2	32	16	16	1	4	4×1	3.200 to 6.000	>4.000 to 7.500	False	19	0	1	10	8
19.00	8	2	1	2	32	16	16	1	4	4×1	1.600 to 3.200	>2.000 to 4.000	False	19	0	2	20	8
19.00	8	2	1	2	32	16	16	1	4	4×1	1.450 to 1.600	1.812 to 2.000	False	19	0	3	40	8
19.00	8	2	1	2	32	16	16	1	6	6×1	4.800 to 6.000	>4.000 to 5.000	False	19	0	1	10	12
19.00	8	2	1	2	32	16	16	1	6	6×1	2.400 to 4.800	>2.000 to 4.000	False	19	0	2	20	12
19.00	8	2	1	2	32	16	16	1	6	6×1	1.450 to 2.400	1.208 to 2.000	True	19	0	3	40	12
19.00	8	2	1	2	32	16	16	1	8	2×4, 4×2	3.200 to 6.000	>2.000 to 3.750	False	19	0	2	20	16
19.00	8	2	1	2	32	16	16	1	8	2×4, 4×2	1.600 to 3.200	>1.000 to 2.000	False	19	0	3	40	16
19.10	8	2	2	4	32	16	16	0	1	1×1	1.600 to 3.100	>8.000 to 15.500	False	19	1	0	5	2
19.10	8	2	2	4	32	16	16	0	1	1×1	1.450 to 1.600	7.250 to 8.000	False	19	1	1	10	2
19.10	8	2	2	4	32	16	16	0	2	2×1	3.200 to 6.000	>8.000 to 15.000	False	19	1	0	5	4
19.10	8	2	2	4	32	16	16	0	2	2×1	1.600 to 3.200	>4.000 to 8.000	False	19	1	1	10	4

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Table 70. ADC Path Supported JESD204B Modes (L = 8)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
19.10	8	2	2	4	32	16	16	0	2	2×1	1.450 to 1.600	3.625 to 4.000	False	19	1	2	20	4
19.10	8	2	2	4	32	16	16	0	3	3×1	4.800 to 6.000	>8.000 to 10.000	False	19	1	0	5	6
19.10	8	2	2	4	32	16	16	0	3	3×1	2.400 to 4.800	>4.000 to 8.000	False	19	1	1	10	6
19.10	8	2	2	4	32	16	16	0	3	3×1	1.450 to 2.400	2.417 to 4.000	True	19	1	2	20	6
19.10	8	2	2	4	32	16	16	0	4	4×1	3.200 to 6.000	>4.000 to 7.500	False	19	1	1	10	8
19.10	8	2	2	4	32	16	16	0	4	4×1	1.600 to 3.200	>2.000 to 4.000	False	19	1	2	20	8
19.10	8	2	2	4	32	16	16	0	4	4×1	1.450 to 1.600	1.812 to 2.000	False	19	1	3	40	8
19.10	8	2	2	4	32	16	16	0	6	6×1	4.800 to 6.000	>4.000 to 5.000	False	19	1	1	10	12
19.10	8	2	2	4	32	16	16	0	6	6×1	2.400 to 4.800	>2.000 to 4.000	False	19	1	2	20	12
19.10	8	2	2	4	32	16	16	0	6	6×1	1.450 to 2.400	1.208 to 2.000	True	19	1	3	40	12
19.10	8	2	2	4	32	16	16	0	8	2×4, 4×2	3.200 to 6.000	>2.000 to 3.750	False	19	1	2	20	16
19.10	8	2	2	4	32	16	16	0	8	2×4, 4×2	1.600 to 3.200	>1.000 to 2.000	False	19	1	3	40	16
18.00	8	4	1	1	32	16	16	1	1	1×1	1.450 to 1.550	14.500 to 15.500	False	18	0	0	5	1
18.00	8	4	1	1	32	16	16	1	2	2×1	1.600 to 3.100	>8.000 to 15.500	False	18	0	0	5	2
18.00	8	4	1	1	32	16	16	1	2	2×1	1.450 to 1.600	7.250 to 8.000	False	18	0	1	10	2
18.00	8	4	1	1	32	16	16	1	3	3×1	2.400 to 4.650	>8.000 to 15.500	False	18	0	0	5	3
18.00	8	4	1	1	32	16	16	1	4	2×2, 4×1	3.200 to 6.000	>8.000 to 15.000	False	18	0	0	5	4
18.00	8	4	1	1	32	16	16	1	4	2×2, 4×1	1.600 to 3.200	>4.000 to 8.000	False	18	0	1	10	4
18.00	8	4	1	1	32	16	16	1	4	2×2, 4×1	1.450 to 1.600	3.625 to 4.000	False	18	0	2	20	4
18.00	8	4	1	1	32	16	16	1	6	3×2, 6×1	4.800 to 6.000	>8.000 to 10.000	False	18	0	0	5	6
18.00	8	4	1	1	32	16	16	1	6	3×2, 6×1	2.400 to 4.800	>4.000 to 8.000	False	18	0	1	10	6
18.00	8	4	1	1	32	16	16	1	8	4×2, 2×4	3.200 to 6.000	>4.000 to 7.500	False	18	0	1	10	8
18.00	8	4	1	1	32	16	16	1	8	4×2, 2×4	1.600 to 3.200	>2.000 to 4.000	False	18	0	2	20	8
18.00	8	4	1	1	32	16	16	1	8	4×2, 2×4	1.450 to 1.600	1.812 to 2.000	False	18	0	3	40	8
18.00	8	4	1	1	32	16	16	1	12	6×2	4.800 to 6.000	>4.000 to 5.000	False	18	0	1	10	12
18.00	8	4	1	1	32	16	16	1	12	6×2	2.400 to 4.800	>2.000 to 4.000	False	18	0	2	20	12
18.00	8	4	1	1	32	16	16	1	16	4×4	3.200 to 6.000	>2.000 to 3.750	False	18	0	2	20	16
18.00	8	4	1	1	32	16	16	1	16	4×4	1.600 to 3.200	>1.000 to 2.000	False	18	0	3	40	16
18.00	8	4	1	1	32	16	16	1	24	6×4	4.800 to 6.000	>2.000 to 2.500	False	18	0	2	20	24
18.00	8	4	1	1	32	16	16	1	24	6×4	2.400 to 4.800	>1.000 to 2.000	False	18	0	3	40	24
18.00	8	4	1	1	32	16	16	1	32	4×8	3.200 to 6.000	>1.000 to 1.875	False	18	0	3	40	32
18.10	8	4	2	2	32	16	16	0	1	1×1	1.450 to 1.550	14.500 to 15.500	False	18	1	0	5	1
18.10	8	4	2	2	32	16	16	0	2	2×1	1.600 to 3.100	>8.000 to 15.500	False	18	1	0	5	2
18.10	8	4	2	2	32	16	16	0	2	2×1	1.450 to 1.600	7.250 to 8.000	False	18	1	1	10	2
18.10	8	4	2	2	32	16	16	0	3	3×1	2.400 to 4.650	>8.000 to 15.500	False	18	1	0	5	3
18.10	8	4	2	2	32	16	16	0	3	3×1	1.450 to 2.400	4.833 to 8.000	True	18	1	1	10	3

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Table 70. ADC Path Supported JESD204B Modes (L = 8)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
18.10	8	4	2	2	32	16	16	0	4	2×2, 4×1	3.200 to 6.000	>8.000 to 15.000	False	18	1	0	5	4
18.10	8	4	2	2	32	16	16	0	4	2×2, 4×1	1.600 to 3.200	>4.000 to 8.000	False	18	1	1	10	4
18.10	8	4	2	2	32	16	16	0	4	2×2, 4×1	1.450 to 1.600	3.625 to 4.000	False	18	1	2	20	4
18.10	8	4	2	2	32	16	16	0	6	3×2, 6×1	4.800 to 6.000	>8.000 to 10.000	False	18	1	0	5	6
18.10	8	4	2	2	32	16	16	0	6	3×2, 6×1	2.400 to 4.800	>4.000 to 8.000	False	18	1	1	10	6
18.10	8	4	2	2	32	16	16	0	6	3×2, 6×1	1.450 to 2.400	2.417 to 4.000	True	18	1	2	20	6
18.10	8	4	2	2	32	16	16	0	8	4×2, 2×4	3.200 to 6.000	>4.000 to 7.500	False	18	1	1	10	8
18.10	8	4	2	2	32	16	16	0	8	4×2, 2×4	1.600 to 3.200	>2.000 to 4.000	False	18	1	2	20	8
18.10	8	4	2	2	32	16	16	0	8	4×2, 2×4	1.450 to 1.600	1.812 to 2.000	False	18	1	3	40	8
18.10	8	4	2	2	32	16	16	0	12	6×2	4.800 to 6.000	>4.000 to 5.000	False	18	1	1	10	12
18.10	8	4	2	2	32	16	16	0	12	6×2	2.400 to 4.800	>2.000 to 4.000	False	18	1	2	20	12
18.10	8	4	2	2	32	16	16	0	12	6×2	1.450 to 2.400	1.208 to 2.000	True	18	1	3	40	12
18.10	8	4	2	2	32	16	16	0	16	4×4	3.200 to 6.000	>2.000 to 3.750	False	18	1	2	20	16
18.10	8	4	2	2	32	16	16	0	16	4×4	1.600 to 3.200	>1.000 to 2.000	False	18	1	3	40	16
18.10	8	4	2	2	32	16	16	0	24	6×4	4.800 to 6.000	>2.000 to 2.500	False	18	1	2	20	24
18.10	8	4	2	2	32	16	16	0	24	6×4	2.400 to 4.800	>1.000 to 2.000	False	18	1	3	40	24
18.10	8	4	2	2	32	16	16	0	32	4×8	3.200 to 6.000	>1.000 to 1.875	False	18	1	3	40	32
16.00	8	8	2	1	32	16	16	0	4	2×2, 4×1	1.600 to 3.100	>8.000 to 15.500	False	16	0	0	5	2
16.00	8	8	2	1	32	16	16	0	4	2×2, 4×1	1.450 to 1.600	7.250 to 8.000	False	16	0	1	10	2
16.00	8	8	2	1	32	16	16	0	6	3×2, 6×1, 2×3	2.400 to 4.650	>8.000 to 15.500	False	16	0	0	5	3
16.00	8	8	2	1	32	16	16	0	6	6×1, 2×3	1.450 to 2.400	4.833 to 8.000	True	16	0	1	10	3
16.00	8	8	2	1	32	16	16	0	8	4×2, 2×4	3.200 to 6.000	>8.000 to 15.000	False	16	0	0	5	4
16.00	8	8	2	1	32	16	16	0	8	4×2, 2×4	1.600 to 3.200	>4.000 to 8.000	False	16	0	1	10	4
16.00	8	8	2	1	32	16	16	0	8	4×2, 2×4	1.450 to 1.600	3.625 to 4.000	False	16	0	2	20	4
16.00	8	8	2	1	32	16	16	0	12	3×4, 4×3, 6×2	4.800 to 6.000	>8.000 to 10.000	False	16	0	0	5	6
16.00	8	8	2	1	32	16	16	0	12	3×4, 4×3, 6×2	2.400 to 4.800	>4.000 to 8.000	False	16	0	1	10	6
16.00	8	8	2	1	32	16	16	0	12	3×4, 4×3, 6×2	1.450 to 2.400	2.417 to 4.000	True	16	0	2	20	6
16.00	8	8	2	1	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	16	0	1	10	8
16.00	8	8	2	1	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	16	0	2	20	8
16.00	8	8	2	1	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	16	0	3	40	8
16.00	8	8	2	1	32	16	16	0	16	6×3	3.600 to 6.000	>4.000 to 6.667	True	16	0	1	10	9
16.00	8	8	2	1	32	16	16	0	16	6×3	1.800 to 3.600	>2.000 to 4.000	True	16	0	2	20	9
16.00	8	8	2	1	32	16	16	0	16	6×3	1.450 to 1.800	1.611 to 2.000	True	16	0	3	40	9
16.00	8	8	2	1	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>4.000 to 5.000	False	16	0	1	10	12
16.00	8	8	2	1	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>2.000 to 4.000	False	16	0	2	20	12
16.00	8	8	2	1	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	1.208 to 2.000	True	16	0	3	40	12
16.00	8	8	2	1	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	16	0	2	20	16

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Table 70. ADC Path Supported JESD204B Modes (L = 8)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
16.00	8	8	2	1	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	16	0	3	40	16
16.00	8	8	2	1	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	16	0	2	20	24
16.00	8	8	2	1	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	16	0	3	40	24
16.10	8	8	4	2	32	16	16	0	4	2×2, 4×1	1.600 to 3.100	>8.000 to 15.500	False	16	1	0	5	2
16.10	8	8	4	2	32	16	16	0	4	2×2, 4×1	1.450 to 1.600	7.250 to 8.000	False	16	1	1	10	2
16.10	8	8	4	2	32	16	16	0	6	3×2, 6×1	2.400 to 4.650	>8.000 to 15.500	False	16	1	0	5	3
16.10	8	8	4	2	32	16	16	0	6	3×2, 6×1	1.450 to 2.400	4.833 to 8.000	True	16	1	1	10	3
16.10	8	8	4	2	32	16	16	0	8	4×2, 2×4	3.200 to 6.000	>8.000 to 15.000	False	16	1	0	5	4
16.10	8	8	4	2	32	16	16	0	8	4×2, 2×4	1.600 to 3.200	>4.000 to 8.000	False	16	1	1	10	4
16.10	8	8	4	2	32	16	16	0	8	4×2, 2×4	1.450 to 1.600	3.625 to 4.000	False	16	1	2	20	4
16.10	8	8	4	2	32	16	16	0	12	3×4, 4×3, 6×2	4.800 to 6.000	>8.000 to 10.000	False	16	1	0	5	6
16.10	8	8	4	2	32	16	16	0	12	3×4, 4×3, 6×2	2.400 to 4.800	>4.000 to 8.000	False	16	1	1	10	6
16.10	8	8	4	2	32	16	16	0	12	3×4, 4×3, 6×2	1.450 to 2.400	2.417 to 4.000	True	16	1	2	20	6
16.10	8	8	4	2	32	16	16	0	16	4×4	3.200 to 6.000	>4.000 to 7.500	False	16	1	1	10	8
16.10	8	8	4	2	32	16	16	0	16	4×4	1.600 to 3.200	>2.000 to 4.000	False	16	1	2	20	8
16.10	8	8	4	2	32	16	16	0	16	4×4	1.450 to 1.600	1.812 to 2.000	False	16	1	3	40	8
16.10	8	8	4	2	32	16	16	0	18	6×3	3.600 to 6.000	>4.000 to 6.667	True	16	1	1	10	9
16.10	8	8	4	2	32	16	16	0	18	6×3	1.800 to 3.600	>2.000 to 4.000	True	16	1	2	20	9
16.10	8	8	4	2	32	16	16	0	18	6×3	1.450 to 1.800	1.611 to 2.000	True	16	1	3	40	9
16.10	8	8	4	2	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>4.000 to 5.000	False	16	1	1	10	12
16.10	8	8	4	2	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>2.000 to 4.000	False	16	1	2	20	12
16.10	8	8	4	2	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	1.208 to 2.000	True	16	1	3	40	12
16.10	8	8	4	2	32	16	16	0	32	4×8	3.200 to 6.000	>2.000 to 3.750	False	16	1	2	20	16
16.10	8	8	4	2	32	16	16	0	32	4×8	1.600 to 3.200	>1.000 to 2.000	False	16	1	3	40	16
16.10	8	8	4	2	32	16	16	0	48	6×8	4.800 to 6.000	>2.000 to 2.500	False	16	1	2	20	24
16.10	8	8	4	2	32	16	16	0	48	6×8	2.400 to 4.800	>1.000 to 2.000	False	16	1	3	40	24
17.00	8	16	4	1	32	16	16	0	6	2×3, 3×2	1.450 to 2.325	9.667 to 15.500	True	17	0	0	10	3
17.00	8	16	4	1	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	17	0	0	5	2
17.00	8	16	4	1	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	17	0	1	10	2
17.00	8	16	4	1	32	16	16	0	12	4×3, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	17	0	0	5	3
17.00	8	16	4	1	32	16	16	0	12	4×3, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	17	0	1	10	3
17.00	8	16	4	1	32	16	16	0	16	4×4	3.200 to 6.000	>8.000 to 15.000	False	17	0	0	5	4
17.00	8	16	4	1	32	16	16	0	16	4×4	1.600 to 3.200	>4.000 to 8.000	False	17	0	1	10	4
17.00	8	16	4	1	32	16	16	0	16	4×4	1.450 to 1.600	3.625 to 4.000	False	17	0	2	20	4
17.00	8	16	4	1	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	17	0	0	5	6
17.00	8	16	4	1	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	17	0	1	10	6
17.00	8	16	4	1	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	17	0	2	20	6

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Table 70. ADC Path Supported JESD204B Modes (L = 8)[1] (Continued)

JESD204B Mode Number	L	M	F	S	K	N	NP	HD	Total DCM	Coarse × Fine Decimation DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
17.00	8	16	4	1	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	17	0	1	10	8
17.00	8	16	4	1	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	17	0	2	20	8
17.00	8	16	4	1	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	17	0	3	40	8
17.00	8	16	4	1	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	17	0	1	10	12
17.00	8	16	4	1	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	17	0	2	20	12
17.00	8	16	4	1	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	17	0	3	40	12
17.10	8	16	8	2	32	16	16	0	8	2×4, 4×2	1.600 to 3.100	>8.000 to 15.500	False	17	1	0	5	2
17.10	8	16	8	2	32	16	16	0	8	2×4, 4×2	1.450 to 1.600	7.250 to 8.000	False	17	1	1	10	2
17.10	8	16	8	2	32	16	16	0	12	4×3, 3×4, 6×2	2.400 to 4.650	>8.000 to 15.500	False	17	1	0	5	3
17.10	8	16	8	2	32	16	16	0	12	4×3, 3×4, 6×2	1.450 to 2.400	4.833 to 8.000	True	17	1	1	10	3
17.10	8	16	8	2	32	16	16	0	16	4×4	3.200 to 6.000	>8.000 to 15.000	False	17	1	0	5	4
17.10	8	16	8	2	32	16	16	0	16	4×4	1.600 to 3.200	>4.000 to 8.000	False	17	1	1	10	4
17.10	8	16	8	2	32	16	16	0	16	4×4	1.450 to 1.600	3.625 to 4.000	False	17	1	2	20	4
17.10	8	16	8	2	32	16	16	0	24	4×6, 6×4	4.800 to 6.000	>8.000 to 10.000	False	17	1	0	5	6
17.10	8	16	8	2	32	16	16	0	24	4×6, 6×4	2.400 to 4.800	>4.000 to 8.000	False	17	1	1	10	6
17.10	8	16	8	2	32	16	16	0	24	4×6, 6×4	1.450 to 2.400	2.417 to 4.000	True	17	1	2	20	6
17.10	8	16	8	2	32	16	16	0	32	4×8	3.200 to 6.000	>4.000 to 7.500	False	17	1	1	10	8
17.10	8	16	8	2	32	16	16	0	32	4×8	1.600 to 3.200	>2.000 to 4.000	False	17	1	2	20	8
17.10	8	16	8	2	32	16	16	0	32	4×8	1.450 to 1.600	1.812 to 2.000	False	17	1	3	40	8
17.10	8	16	8	2	32	16	16	0	48	4×12, 6×8	4.800 to 6.000	>4.000 to 5.000	False	17	1	1	10	12
17.10	8	16	8	2	32	16	16	0	48	4×12, 6×8	2.400 to 4.800	>2.000 to 4.000	False	17	1	2	20	12
17.10	8	16	8	2	32	16	16	0	48	4×12, 6×8	1.450 to 2.400	1.208 to 2.000	True	17	1	3	40	12
17.10	8	16	8	2	32	16	16	0	6	2×3, 3×2	1.450 to 2.325	9.667 to 15.500	True	17	1	0	10	3

[1] N/A means not applicable.

[2] JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually.

[3] If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in Table 42. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For Transmit and receive path operation, refer to the bit field descriptions for these registers in Table 61 to determine the appropriate setting.

[4] Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

ADC Path Supported JESD204C Modes

ADC Path Supported JESD204C Modes (L = 1

Table 71. ADC Path Supported JESD204C Modes (L = 1)[1]

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
3.01	1	1	2	1	128	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	N/A[4]	N/A	0	11	4
3.01	1	1	2	1	128	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
3.01	1	1	2	1	128	1	16	16	0	3×2	6	2.909 to 6.000	>8.000 to 16.500	False	N/A	N/A	0	11	6

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Table 71. ADC Path Supported JESD204C Modes (L = 1)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
3.01	1	1	2	1	128	1	16	16	0	4×2	8	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
3.01	1	1	2	1	128	1	16	16	0	4×2	8	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
3.01	1	1	2	1	128	1	16	16	0	6×2	12	5.818 to 6.000	>8.000 to 8.250	False	N/A	N/A	0	11	12
3.01	1	1	2	1	128	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
21.01	1	1	3	2	256	3	12	12	0	2×1	2	1.450 to 4.000	8.972 to 24.750	True	N/A	N/A	0	33	8
21.01	1	1	3	2	256	3	12	12	0	4×1	4	2.586 to 6.000	>8.000 to 18.562	True	N/A	N/A	0	33	16
21.01	1	1	3	2	256	3	12	12	0	6×2	12	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
3.11	1	1	4	2	64	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4
3.11	1	1	4	2	64	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
3.11	1	1	4	2	64	1	16	16	0	3×2	6	2.909 to 6.000	>8.000 to 16.500	False	N/A	N/A	0	11	6
3.11	1	1	4	2	64	1	16	16	0	4×2	8	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
3.11	1	1	4	2	64	1	16	16	0	4×2	8	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
3.11	1	1	4	2	64	1	16	16	0	6×2	12	5.818 to 6.000	>8.000 to 8.250	False	N/A	N/A	0	11	12
3.11	1	1	4	2	64	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
21.11	1	1	6	4	128	3	12	12	0	4×1	4	2.586 to 6.000	>8.000 to 18.562	True	N/A	N/A	0	33	16
21.11	1	1	6	4	128	3	12	12	0	2×1	2	1.450 to 4.000	8.972 to 24.750	True	N/A	N/A	0	33	8
21.11	1	1	6	4	128	3	12	12	0	6×2	12	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
21.00	1	2	3	1	256	3	12	12	0	2×1	2	1.450 to 2.000	17.944 to 24.750	True	21	0	0	33	4
21.00	1	2	3	1	256	3	12	12	0	3×2, 6×1	6	1.939 to 6.000	>8.000 to 24.750	False	21	0	0	11	4
21.00	1	2	3	1	256	3	12	12	0	3×2, 6×1	6	1.455 to 1.939	6.000 to 8.000	False	21	0	1	22	4
21.00	1	2	3	1	256	3	12	12	0	3×1	3	1.450 to 3.000	11.963 to 24.750	False	21	0	0	11	2
21.00	1	2	3	1	256	3	12	12	0	4×1	4	1.450 to 4.000	8.972 to 24.750	True	21	0	0	33	8
21.00	1	2	3	1	256	3	12	12	0	4×3, 6×2	12	3.879 to 6.000	>8.000 to 12.375	False	21	0	0	11	8
21.00	1	2	3	1	256	3	12	12	0	4×3, 6×2	12	2.909 to 3.879	6.000 to 8.000	False	21	0	1	22	8
21.00	1	2	3	1	256	3	12	12	0	6×4	24	5.818 to 6.000	6.000 to 6.188	False	21	0	1	22	16
21.00	1	2	3	1	256	3	12	12	0	4×2	8	2.586 to 6.000	>8.000 to 18.562	True	21	0	0	33	16
21.00	1	2	3	1	256	3	12	12	0	3×3	9	2.909 to 6.000	>8.000 to 16.500	False	21	0	0	11	6
3.00	1	2	4	1	64	1	16	16	0	2×2, 4×1	4	1.450 to 3.000	11.963 to 24.750	False	3	0	0	11	2
3.00	1	2	4	1	64	1	16	16	0	3×2, 6×1, 2×3	6	1.455 to 4.000	>8.000 to 24.750	False	3	0	0	11	3
3.00	1	2	4	1	64	1	16	16	0	3×2, 6×1, 2×3	6	1.450 to 1.455	7.975 to 8.000	True	3	0	1	22	3
3.00	1	2	4	1	64	1	16	16	0	4×2, 2×4	8	1.939 to 6.000	>8.000 to 24.750	False	3	0	0	11	4
3.00	1	2	4	1	64	1	16	16	0	4×2, 2×4	8	1.455 to 1.939	6.000 to 8.000	False	3	0	1	22	4
3.00	1	2	4	1	64	1	16	16	0	3×4, 2×6, 4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	3	0	0	11	6
3.00	1	2	4	1	64	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	3	0	0	11	8

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Table 71. ADC Path Supported JESD204C Modes (L = 1)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
3.00	1	2	4	1	64	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	3	0	1	22	8
3.00	1	2	4	1	64	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	3	0	0	11	9
3.00	1	2	4	1	64	1	16	16	0	6×3	18	3.273 to 4.364	6.000 to 8.000	True	3	0	1	22	9
3.00	1	2	4	1	64	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	3	0	0	11	12
3.00	1	2	4	1	64	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	3	0	1	22	16
21.10	1	2	6	2	128	3	12	12	0	3×1	3	1.450 to 3.000	11.963 to 24.750	False	21	1	0	11	2
21.10	1	2	6	2	128	3	12	12	0	3×2, 6×1	6	1.939 to 6.000	>8.000 to 24.750	False	21	1	0	11	4
21.10	1	2	6	2	128	3	12	12	0	3×2, 6×1	6	1.455 to 1.939	6.000 to 8.000	False	21	1	1	22	4
21.10	1	2	6	2	128	3	12	12	0	3×2, 6×1	6	1.450 to 1.455	7.975 to 8.000	True	21	1	1	22	3
21.10	1	2	6	2	128	3	12	12	0	2×1	2	1.450 to 2.000	17.944 to 24.750	True	21	1	0	33	4
21.10	1	2	6	2	128	3	12	12	0	4×1	4	1.450 to 4.000	8.972 to 24.750	True	21	1	0	33	8
21.10	1	2	6	2	128	3	12	12	0	4×3, 6×2	12	3.879 to 6.000	>8.000 to 12.375	False	21	1	0	11	8
21.10	1	2	6	2	128	3	12	12	0	4×3, 6×2	12	2.909 to 3.879	6.000 to 8.000	False	21	1	1	22	8
21.10	1	2	6	2	128	3	12	12	0	6×4	24	5.818 to 6.000	6.000 to 6.188	False	21	1	1	22	16
21.10	1	2	6	2	128	3	12	12	0	4×2	8	2.586 to 6.000	>8.000 to 18.562	True	21	1	0	33	16
21.10	1	2	6	2	128	3	12	12	0	3×3	9	2.909 to 6.000	>8.000 to 16.500	False	21	1	0	11	6
3.10	1	2	8	2	32	1	16	16	0	2×2, 4×1	4	1.450 to 3.000	11.963 to 24.750	False	3	1	0	11	2
3.10	1	2	8	2	32	1	16	16	0	3×2, 6×1	6	1.455 to 4.000	>8.000 to 24.750	False	3	1	0	11	3
3.10	1	2	8	2	32	1	16	16	0	3×2, 6×1	6	1.450 to 1.455	7.975 to 8.000	True	3	1	1	22	3
3.10	1	2	8	2	32	1	16	16	0	4×2, 2×4	8	1.939 to 6.000	>8.000 to 24.750	False	3	1	0	11	4
3.10	1	2	8	2	32	1	16	16	0	4×2, 2×4	8	1.455 to 1.939	6.000 to 8.000	False	3	1	1	22	4
3.10	1	2	8	2	32	1	16	16	0	3×4, 2×6, 4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	3	1	0	11	6
3.10	1	2	8	2	32	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	3	1	0	11	8
3.10	1	2	8	2	32	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	3	1	1	22	8
3.10	1	2	8	2	32	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	3	1	0	11	9
3.10	1	2	8	2	32	1	16	16	0	6×3	18	3.273 to 4.364	6.000 to 8.000	True	3	1	1	22	9
3.10	1	2	8	2	32	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	3	1	0	11	12
3.10	1	2	8	2	32	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	3	1	1	22	16
20.00	1	4	6	1	128	3	12	12	0	4×3, 3×4, 6×2	12	1.939 to 6.000	>8.000 to 24.750	False	20	0	0	11	4
20.00	1	4	6	1	128	3	12	12	0	4×3, 3×4, 6×2	12	1.455 to 1.939	6.000 to 8.000	False	20	0	1	22	4
20.00	1	4	6	1	128	3	12	12	0	6×4, 4×6	24	3.879 to 6.000	>8.000 to 12.375	False	20	0	0	11	8
20.00	1	4	6	1	128	3	12	12	0	6×4, 4×6	24	2.909 to 3.879	6.000 to 8.000	False	20	0	1	22	8
20.00	1	4	6	1	128	3	12	12	0	4×12, 6×8	48	5.818 to 6.000	6.000 to 6.188	False	20	0	1	22	16
20.00	1	4	6	1	128	3	12	12	0	2×3, 6×1, 3×2	6	1.450 to 3.000	11.963 to 24.750	False	20	0	0	11	2
20.00	1	4	6	1	128	3	12	12	0	3×3	9	1.455 to 4.000	>8.000 to 24.750	False	20	0	0	11	3
20.00	1	4	6	1	128	3	12	12	0	3×3	9	1.450 to 1.455	7.975 to 8.000	True	20	0	1	22	3

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Table 71. ADC Path Supported JESD204C Modes (L = 1)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
20.00	1	4	6	1	128	3	12	12	0	6×3	18	2.909 to 6.000	>8.000 to 16.500	False	20	0	0	11	6
2.00	1	4	8	1	32	1	16	16	0	2×4, 4×2	8	1.450 to 3.000	11.963 to 24.750	False	2	0	0	11	2
2.00	1	4	8	1	32	1	16	16	0	4×3, 2×6, 3×4, 6×2	12	1.455 to 4.000	>8.000 to 24.750	False	2	0	0	11	3
2.00	1	4	8	1	32	1	16	16	0	4×3, 2×6, 3×4, 6×2	12	1.450 to 1.455	7.975 to 8.000	True	2	0	1	22	3
2.00	1	4	8	1	32	1	16	16	0	2×8, 4×4	16	1.939 to 6.000	>8.000 to 24.750	False	2	0	0	11	4
2.00	1	4	8	1	32	1	16	16	0	2×8, 4×4	16	1.455 to 1.939	6.000 to 8.000	False	2	0	1	22	4
2.00	1	4	8	1	32	1	16	16	0	3×8, 4×6, 6×4	24	2.909 to 6.000	>8.000 to 16.500	False	2	0	0	11	6
2.00	1	4	8	1	32	1	16	16	0	4×8	32	3.879 to 6.000	>8.000 to 12.375	False	2	0	0	11	8
2.00	1	4	8	1	32	1	16	16	0	4×8	32	2.909 to 3.879	6.000 to 8.000	False	2	0	1	22	8
2.00	1	4	8	1	32	1	16	16	0	4×12, 6×8	48	5.818 to 6.000	>8.000 to 8.250	False	2	0	0	11	12
2.00	1	4	8	1	32	1	16	16	0	4×16	64	5.818 to 6.000	6.000 to 6.188	False	2	0	1	22	16
2.00	1	4	8	1	32	1	16	16	0	3×2	6	1.450 to 2.250	15.950 to 24.750	True	2	0	0	22	3
20.10	1	4	12	2	64	3	12	12	0	2×3, 6×1, 3×2	6	1.450 to 3.000	11.963 to 24.750	False	20	1	0	11	2
20.10	1	4	12	2	64	3	12	12	0	3×3	9	1.455 to 4.000	>8.000 to 24.750	False	20	1	0	11	3
20.10	1	4	12	2	64	3	12	12	0	3×3	9	1.450 to 1.455	7.975 to 8.000	True	20	1	1	22	3
20.10	1	4	12	2	64	3	12	12	0	4×3, 6×2	12	1.939 to 6.000	>8.000 to 24.750	False	20	1	0	11	4
20.10	1	4	12	2	64	3	12	12	0	4×3, 6×2	12	1.455 to 1.939	6.000 to 8.000	False	20	1	1	22	4
20.10	1	4	12	2	64	3	12	12	0	6×3	18	2.909 to 6.000	>8.000 to 16.500	False	20	1	0	11	6
20.10	1	4	12	2	64	3	12	12	0	4×6, 6×4	24	3.879 to 6.000	>8.000 to 12.375	False	20	1	0	11	8
20.10	1	4	12	2	64	3	12	12	0	4×6, 6×4	24	2.909 to 3.879	6.000 to 8.000	False	20	1	1	22	8
20.10	1	4	12	2	64	3	12	12	0	4×12, 6×8	48	5.818 to 6.000	6.000 to 6.188	False	20	1	1	22	16
29.01	1	4	12	1	64	3	16	24	0	3×8, 6×4	24	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4
29.01	1	4	12	1	64	3	16	24	0	3×8, 6×4	24	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
29.01	1	4	12	1	64	3	16	24	0	3×4, 6×2	12	1.450 to 3.000	11.963 to 24.750	False	N/A	N/A	0	11	2
29.01	1	4	12	1	64	3	16	24	0	6×8	48	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
29.01	1	4	12	1	64	3	16	24	0	6×8	48	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
29.01	1	4	12	1	64	3	16	24	0	6×16	96	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
2.10	1	4	16	2	16	1	16	16	0	2×4, 4×2	8	1.450 to 3.000	11.963 to 24.750	False	2	1	0	11	2
2.10	1	4	16	2	16	1	16	16	0	4×3, 3×4, 6×2	12	1.455 to 4.000	>8.000 to 24.750	False	2	1	0	11	3
2.10	1	4	16	2	16	1	16	16	0	4×3, 3×4, 6×2	12	1.450 to 1.455	7.975 to 8.000	True	2	1	1	22	3
2.10	1	4	16	2	16	1	16	16	0	2×8, 4×4	16	1.939 to 6.000	>8.000 to 24.750	False	2	1	0	11	4
2.10	1	4	16	2	16	1	16	16	0	2×8, 4×4	16	1.455 to 1.939	6.000 to 8.000	False	2	1	1	22	4
2.10	1	4	16	2	16	1	16	16	0	3×8, 4×6, 6×4	24	2.909 to 6.000	>8.000 to 16.500	False	2	1	0	11	6
2.10	1	4	16	2	16	1	16	16	0	4×8	32	3.879 to 6.000	>8.000 to 12.375	False	2	1	0	11	8
2.10	1	4	16	2	16	1	16	16	0	4×8	32	2.909 to 3.879	6.000 to 8.000	False	2	1	1	22	8
2.10	1	4	16	2	16	1	16	16	0	4×12, 6×8	48	5.818 to 6.000	>8.000 to 8.250	False	2	1	0	11	12
2.10	1	4	16	2	16	1	16	16	0	4×16	64	5.818 to 6.000	6.000 to 6.188	False	2	1	1	22	16
1.00	1	8	12	1	64	3	12	12	0	4×3, 6×2, 3×4, 2×6	12	1.450 to 3.000	11.963 to 24.750	False	1	0	0	11	2

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Table 71. ADC Path Supported JESD204C Modes (L = 1)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
1.00	1	8	12	1	64	3	12	12	0	6×3, 3×6	18	1.455 to 4.000	>8.000 to 24.750	False	1	0	0	11	3
1.00	1	8	12	1	64	3	12	12	0	6×3, 3×6	18	1.450 to 1.455	7.975 to 8.000	True	1	0	1	22	3
1.00	1	8	12	1	64	3	12	12	0	4×6, 6×4	24	1.939 to 6.000	>8.000 to 24.750	False	1	0	0	11	4
1.00	1	8	12	1	64	3	12	12	0	4×6, 6×4	24	1.455 to 1.939	6.000 to 8.000	False	1	0	1	22	4
1.00	1	8	12	1	64	3	12	12	0	4×12, 6×8	48	3.879 to 6.000	>8.000 to 12.375	False	1	0	0	11	8
1.00	1	8	12	1	64	3	12	12	0	4×12, 6×8	48	2.909 to 3.879	6.000 to 8.000	False	1	0	1	22	8
1.00	1	8	12	1	64	3	12	12	0	4×24, 6×16	96	5.818 to 6.000	6.000 to 6.188	False	1	0	1	22	16
0.00	1	8	16	1	32	2	16	16	0	2×8, 4×4	16	1.450 to 3.000	11.963 to 24.750	False	0	0	0	11	2
0.00	1	8	16	1	32	2	16	16	0	3×8, 4×6, 2×12, 6×4	24	1.455 to 4.000	>8.000 to 24.750	False	0	0	0	11	3
0.00	1	8	16	1	32	2	16	16	0	3×8, 4×6, 2×12, 6×4	24	1.450 to 1.455	7.975 to 8.000	True	0	0	1	22	3
0.00	1	8	16	1	32	2	16	16	0	2×16, 4×8	32	1.939 to 6.000	>8.000 to 24.750	False	0	0	0	11	4
0.00	1	8	16	1	32	2	16	16	0	2×16, 4×8	32	1.455 to 1.939	6.000 to 8.000	False	0	0	1	22	4
0.00	1	8	16	1	32	2	16	16	0	4×12, 6×8	48	2.909 to 6.000	>8.000 to 16.500	False	0	0	0	11	6
0.00	1	8	16	1	32	2	16	16	0	4×16	64	3.879 to 6.000	>8.000 to 12.375	False	0	0	0	11	8
0.00	1	8	16	1	32	2	16	16	0	4×16	64	2.909 to 3.879	6.000 to 8.000	False	0	0	1	22	8
0.00	1	8	16	1	32	2	16	16	0	4×24, 6×16	96	5.818 to 6.000	>8.000 to 8.250	False	0	0	0	11	12
29.00	1	8	24	1	32	3	16	24	0	4×8	32	1.450 to 4.000	8.972 to 24.750	True	29	0	0	33	8
29.00	1	8	24	1	32	3	16	24	0	3×4, 6×2, 4×3, 2×6	12	1.450 to 1.500	23.925 to 24.750	False	29	0	0	11	1
29.00	1	8	24	1	32	3	16	24	0	6×3, 3×6	18	1.450 to 2.250	15.950 to 24.750	True	29	0	0	22	3
29.00	1	8	24	1	32	3	16	24	0	3×8, 4×6, 6×4, 2×12	24	1.450 to 3.000	11.963 to 24.750	False	29	0	0	11	2
29.00	1	8	24	1	32	3	16	24	0	2×24, 4×12, 3×16, 6×8	48	1.939 to 6.000	>8.000 to 24.750	False	29	0	0	11	4
29.00	1	8	24	1	32	3	16	24	0	2×24, 4×12, 3×16, 6×8	48	1.455 to 1.939	6.000 to 8.000	False	29	0	1	22	4
29.00	1	8	24	1	32	3	16	24	0	4×24, 6×16	96	3.879 to 6.000	>8.000 to 12.375	False	29	0	0	11	8
29.00	1	8	24	1	32	3	16	24	0	4×24, 6×16	96	2.909 to 3.879	6.000 to 8.000	False	29	0	1	22	8

[1] N/A means not applicable.

[2] JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually. Modes with N/A are not supported by AD9986 and AD9988.

[3] If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in Table 42. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For Transmit and receive path operation, refer to the bit field descriptions for these registers in Table 61 to determine the appropriate setting.

[4] Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

ADC Path Supported JESD204C Modes (L = 2)

Table 72. ADC Path Supported JESD204C Modes (L = 2)[1]

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
7.01	2	1	1	1	256	1	16	16	1	1×1	1	1.450 to 3.000	11.963 to 24.750	False	N/A[4]	N/A	0	11	2
7.01	2	1	1	1	256	1	16	16	1	2×1	2	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4

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Table 72. ADC Path Supported JESD204C Modes (L = 2)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
7.01	2	1	1	1	256	1	16	16	1	2×1	2	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
7.01	2	1	1	1	256	1	16	16	1	4×1	4	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
7.01	2	1	1	1	256	1	16	16	1	4×1	4	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
7.01	2	1	1	1	256	1	16	16	1	2×4, 4×2	8	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
7.11	2	1	2	2	128	1	16	16	0	1×1	1	1.450 to 3.000	11.963 to 24.750	False	N/A	N/A	0	11	2
7.11	2	1	2	2	128	1	16	16	0	2×1	2	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4
7.11	2	1	2	2	128	1	16	16	0	2×1	2	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
7.11	2	1	2	2	128	1	16	16	0	4×1	4	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
7.11	2	1	2	2	128	1	16	16	0	4×1	4	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
7.11	2	1	2	2	128	1	16	16	0	2×4, 4×2	8	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
23.01	2	1	3	4	256	3	12	12	0	1×1	1	1.450 to 4.000	8.972 to 24.750	True	N/A	N/A	0	33	8
23.01	2	1	3	4	256	3	12	12	0	2×1	2	2.586 to 6.000	>8.000 to 18.562	True	N/A	N/A	0	33	16
23.01	2	1	3	4	256	3	12	12	0	4×1	4	5.172 to 6.000	>8.000 to 9.281	True	N/A	N/A	0	33	32
23.11	2	1	6	8	128	3	12	12	0	4×1	4	5.172 to 6.000	>8.000 to 9.281	True	N/A	N/A	0	33	32
23.11	2	1	6	8	128	3	12	12	0	1×1	1	1.450 to 4.000	8.972 to 24.750	True	N/A	N/A	0	33	8
23.11	2	1	6	8	128	3	12	12	0	2×1	2	2.586 to 6.000	>8.000 to 18.562	True	N/A	N/A	0	33	16
7.00	2	2	2	1	128	1	16	16	0	1×1	1	1.450 to 1.500	23.925 to 24.750	False	7	0	0	11	1
7.00	2	2	2	1	128	1	16	16	0	2×1	2	1.450 to 3.000	11.963 to 24.750	False	7	0	0	11	2
7.00	2	2	2	1	128	1	16	16	0	3×1	3	1.455 to 4.000	>8.000 to 24.750	False	7	0	0	11	3
7.00	2	2	2	1	128	1	16	16	0	3×1	3	1.450 to 1.455	7.975 to 8.000	True	7	0	1	22	3
7.00	2	2	2	1	128	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	7	0	0	11	4
7.00	2	2	2	1	128	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	7	0	1	22	4
7.00	2	2	2	1	128	1	16	16	0	3×2, 6×1	6	2.909 to 6.000	>8.000 to 16.500	False	7	0	0	11	6
7.00	2	2	2	1	128	1	16	16	0	4×2, 2×4	8	3.879 to 6.000	>8.000 to 12.375	False	7	0	0	11	8
7.00	2	2	2	1	128	1	16	16	0	4×2, 2×4	8	2.909 to 3.879	6.000 to 8.000	False	7	0	1	22	8
7.00	2	2	2	1	128	1	16	16	0	6×2	12	5.818 to 6.000	>8.000 to 8.250	False	7	0	0	11	12
7.00	2	2	2	1	128	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	7	0	1	22	16
23.00	2	2	3	2	256	3	12	12	0	1×1	1	1.450 to 2.000	17.944 to 24.750	True	23	0	0	33	4
23.00	2	2	3	2	256	3	12	12	0	2×1	2	1.450 to 4.000	8.972 to 24.750	True	23	0	0	33	8
23.00	2	2	3	2	256	3	12	12	0	3×1	3	1.939 to 6.000	>8.000 to 24.750	False	23	0	0	11	4
23.00	2	2	3	2	256	3	12	12	0	3×1	3	1.455 to 1.939	6.000 to 8.000	False	23	0	1	22	4
23.00	2	2	3	2	256	3	12	12	0	4×1	4	2.586 to 6.000	>8.000 to 18.562	True	23	0	0	33	16

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Table 72. ADC Path Supported JESD204C Modes (L = 2)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
23.00	2	2	3	2	256	3	12	12	0	6×1	6	3.879 to 6.000	>8.000 to 12.375	False	23	0	0	11	8
23.00	2	2	3	2	256	3	12	12	0	6×1	6	2.909 to 3.879	6.000 to 8.000	False	23	0	1	22	8
23.00	2	2	3	2	256	3	12	12	0	6×2	12	5.818 to 6.000	6.000 to 6.188	False	23	0	1	22	16
7.10	2	2	4	2	64	1	16	16	0	1×1	1	1.450 to 1.500	23.925 to 24.750	False	7	1	0	11	1
7.10	2	2	4	2	64	1	16	16	0	2×1	2	1.450 to 3.000	11.963 to 24.750	False	7	1	0	11	2
7.10	2	2	4	2	64	1	16	16	0	3×1	3	1.455 to 4.000	>8.000 to 24.750	False	7	1	0	11	3
7.10	2	2	4	2	64	1	16	16	0	3×1	3	1.450 to 1.455	7.975 to 8.000	True	7	1	1	22	3
7.10	2	2	4	2	64	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	7	1	0	11	4
7.10	2	2	4	2	64	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	7	1	1	22	4
7.10	2	2	4	2	64	1	16	16	0	3×2, 6×1	6	2.909 to 6.000	>8.000 to 16.500	False	7	1	0	11	6
7.10	2	2	4	2	64	1	16	16	0	4×2, 2×4	8	3.879 to 6.000	>8.000 to 12.375	False	7	1	0	11	8
7.10	2	2	4	2	64	1	16	16	0	4×2, 2×4	8	2.909 to 3.879	6.000 to 8.000	False	7	1	1	22	8
7.10	2	2	4	2	64	1	16	16	0	6×2	12	5.818 to 6.000	>8.000 to 8.250	False	7	1	0	11	12
7.10	2	2	4	2	64	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	7	1	1	22	16
23.10	2	2	6	4	128	3	12	12	0	3×1	3	1.939 to 6.000	>8.000 to 24.750	False	23	1	0	11	4
23.10	2	2	6	4	128	3	12	12	0	3×1	3	1.455 to 1.939	6.000 to 8.000	False	23	1	1	22	4
23.10	2	2	6	4	128	3	12	12	0	4×1	4	2.586 to 6.000	>8.000 to 18.562	True	23	1	0	33	16
23.10	2	2	6	4	128	3	12	12	0	1×1	1	1.450 to 2.000	17.944 to 24.750	True	23	1	0	33	4
23.10	2	2	6	4	128	3	12	12	0	2×1	2	1.450 to 4.000	8.972 to 24.750	True	23	1	0	33	8
23.10	2	2	6	4	128	3	12	12	0	6×1	6	3.879 to 6.000	>8.000 to 12.375	False	23	1	0	11	8
23.10	2	2	6	4	128	3	12	12	0	6×1	6	2.909 to 3.879	6.000 to 8.000	False	23	1	1	22	8
23.10	2	2	6	4	128	3	12	12	0	6×2	6	5.818 to 6.000	6.000 to 6.188	False	23	1	1	22	16
22.00	2	4	3	1	256	3	12	12	0	3×2, 6×1	6	1.939 to 6.000	>8.000 to 24.750	False	22	0	0	11	4
22.00	2	4	3	1	256	3	12	12	0	3×2, 6×1	6	1.455 to 1.939	6.000 to 8.000	False	22	0	1	22	4
22.00	2	4	3	1	256	3	12	12	0	4×3, 6×2	12	3.879 to 6.000	>8.000 to 12.375	False	22	0	0	11	8
22.00	2	4	3	1	256	3	12	12	0	4×3, 6×2	12	2.909 to 3.879	6.000 to 8.000	False	22	0	1	22	8
22.00	2	4	3	1	256	3	12	12	0	6×4	24	5.818 to 6.000	6.000 to 6.188	False	22	0	1	22	16
22.00	2	4	3	1	256	3	12	12	0	2×1	2	1.450 to 2.000	17.944 to 24.750	True	22	0	0	33	4
22.00	2	4	3	1	256	3	12	12	0	3×1	3	1.450 to 3.000	11.963 to 24.750	False	22	0	0	11	2
22.00	2	4	3	1	256	3	12	12	0	4×1	4	1.450 to 4.000	8.972 to 24.750	True	22	0	0	33	8
22.00	2	4	3	1	256	3	12	12	0	3×3	9	2.909 to 6.000	>8.000 to 16.500	False	22	0	0	11	6
6.00	2	4	4	1	64	1	16	16	0	2×2, 4×1	4	1.450 to 3.000	11.963 to 24.750	False	6	0	0	11	2
6.00	2	4	4	1	64	1	16	16	0	3×2, 6×1, 2×3	6	1.455 to 4.000	>8.000 to 24.750	False	6	0	0	11	3
6.00	2	4	4	1	64	1	16	16	0	3×2, 6×1, 2×3	6	1.450 to 1.455	7.975 to 8.000	True	6	0	1	22	3

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Table 72. ADC Path Supported JESD204C Modes (L = 2)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
6.00	2	4	4	1	64	1	16	16	0	4×2, 2×4	8	1.939 to 6.000	>8.000 to 24.750	False	6	0	0	11	4
6.00	2	4	4	1	64	1	16	16	0	4×2, 2×4	8	1.455 to 1.939	6.000 to 8.000	False	6	0	1	22	4
6.00	2	4	4	1	64	1	16	16	0	3×4, 2×6, 4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	6	0	0	11	6
6.00	2	4	4	1	64	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	6	0	0	11	8
6.00	2	4	4	1	64	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	6	0	1	22	8
6.00	2	4	4	1	64	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	6	0	0	11	9
6.00	2	4	4	1	64	1	16	16	0	6×3	18	3.273 to 4.364	6.000 to 8.000	True	6	0	1	22	9
6.00	2	4	4	1	64	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	6	0	0	11	12
6.00	2	4	4	1	64	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	6	0	1	22	16
22.10	2	4	6	2	128	3	12	12	0	3×2, 6×1	6	1.939 to 6.000	>8.000 to 24.750	False	2	0	0	11	4
22.10	2	4	6	2	128	3	12	12	0	3×2, 6×1	6	1.455 to 1.939	6.000 to 8.000	False	2	0	1	22	4
22.10	2	4	6	2	128	3	12	12	0	4×3, 6×2	12	3.879 to 6.000	>8.000 to 12.375	False	2	0	0	11	8
22.10	2	4	6	2	128	3	12	12	0	4×3, 6×2	12	2.909 to 3.879	6.000 to 8.000	False	2	0	1	22	8
22.10	2	4	6	2	128	3	12	12	0	6×4	24	5.818 to 6.000	6.000 to 6.188	False	2	0	1	22	16
22.10	2	4	6	2	128	3	12	12	0	3×1	3	1.450 to 3.000	11.963 to 24.750	False	2	0	0	11	2
22.10	2	4	6	2	128	3	12	12	0	2×1	2	1.450 to 2.000	17.944 to 24.750	True	2	0	0	33	4
22.10	2	4	6	2	128	3	12	12	0	4×1	4	1.450 to 4.000	8.972 to 24.750	True	2	0	0	33	8
22.10	2	4	6	2	128	3	12	12	0	3×3	9	2.909 to 6.000	>8.000 to 16.500	False	2	0	0	11	6
30.01	2	4	6	1	128	3	24	24	0	3×4, 6×2	12	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4
30.01	2	4	6	1	128	3	24	24	0	3×4, 6×2	12	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
30.01	2	4	6	1	128	3	24	24	0	6×4	24	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
30.01	2	4	6	1	128	3	24	24	0	6×4	24	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
30.01	2	4	6	1	128	3	24	24	0	6×8	48	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
30.01	2	4	6	1	128	3	24	24	0	2×3	6	1.450 to 3.000	11.963 to 24.750	False	N/A	N/A	0	11	2
6.10	2	4	8	2	32	1	16	16	0	2×2, 4×1	4	1.450 to 3.000	11.963 to 24.750	False	6	1	0	11	2
6.10	2	4	8	2	32	1	16	16	0	3×2, 6×1	6	1.455 to 4.000	>8.000 to 24.750	False	6	1	0	11	3
6.10	2	4	8	2	32	1	16	16	0	4×2, 2×4	8	1.939 to 6.000	>8.000 to 24.750	False	6	1	0	11	4
6.10	2	4	8	2	32	1	16	16	0	4×2, 2×4	8	1.455 to 1.939	6.000 to 8.000	False	6	1	1	22	4
6.10	2	4	8	2	32	1	16	16	0	3×4, 4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	6	1	0	11	6
6.10	2	4	8	2	32	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	6	1	0	11	8
6.10	2	4	8	2	32	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	6	1	1	22	8
6.10	2	4	8	2	32	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	6	1	0	11	9
6.10	2	4	8	2	32	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	6	1	0	11	12
6.10	2	4	8	2	32	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	6	1	1	22	16
30.11	2	4	12	2	64	3	16	24	0	6×4	24	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
30.11	2	4	12	2	64	3	16	24	0	6×4	24	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8

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Table 72. ADC Path Supported JESD204C Modes (L = 2)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
30.11	2	4	12	2	64	3	16	24	0	3×4, 6×2	12	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4
30.11	2	4	12	2	64	3	16	24	0	3×4, 6×2	12	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
30.11	2	4	12	2	64	3	16	24	0	6×8	48	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
30.11	2	4	12	2	64	3	16	24	0	2×3	6	1.450 to 3.000	11.963 to 24.750	False	N/A	N/A	0	11	2
5.00	2	8	6	1	128	3	12	12	0	2×3, 6×1, 3×2	6	1.450 to 3.000	11.963 to 24.750	False	5	5.0	0	11	2
5.00	2	8	6	1	128	3	12	12	0	3×3	9	1.455 to 4.000	>8.000 to 24.750	False	5	5.0	0	11	3
5.00	2	8	6	1	128	3	12	12	0	4×3, 6×2	12	1.939 to 6.000	>8.000 to 24.750	False	5	5.0	0	11	4
5.00	2	8	6	1	128	3	12	12	0	4×3, 6×2	12	1.455 to 1.939	6.000 to 8.000	False	5	5.0	1	22	4
5.00	2	8	6	1	128	3	12	12	0	6×3	18	2.909 to 6.000	>8.000 to 16.500	False	5	5.0	0	11	6
5.00	2	8	6	1	128	3	12	12	0	4×6, 6×4	24	3.879 to 6.000	>8.000 to 12.375	False	5	5.0	0	11	8
5.00	2	8	6	1	128	3	12	12	0	4×6, 6×4	24	2.909 to 3.879	6.000 to 8.000	False	5	5.0	1	22	8
5.00	2	8	6	1	128	3	12	12	0	4×12, 6×8	48	5.818 to 6.000	6.000 to 6.188	False	5	5.0	1	22	16
4.00	2	8	8	1	32	1	16	16	0	2×4, 4×2	8	1.450 to 3.000	11.963 to 24.750	False	4	0	0	11	2
4.00	2	8	8	1	32	1	16	16	0	4×3, 2×6, 3×4, 6×2	12	1.455 to 4.000	>8.000 to 24.750	False	4	0	0	11	3
4.00	2	8	8	1	32	1	16	16	0	2×8, 4×4	16	1.939 to 6.000	>8.000 to 24.750	False	4	0	0	11	4
4.00	2	8	8	1	32	1	16	16	0	2×8, 4×4	16	1.455 to 1.939	6.000 to 8.000	False	4	0	1	22	4
4.00	2	8	8	1	32	1	16	16	0	4×6, 6×4	24	2.909 to 6.000	>8.000 to 16.500	False	4	0	0	11	6
4.00	2	8	8	1	32	1	16	16	0	4×8	32	3.879 to 6.000	>8.000 to 12.375	False	4	0	0	11	8
4.00	2	8	8	1	32	1	16	16	0	4×8	32	2.909 to 3.879	6.000 to 8.000	False	4	0	1	22	8
4.00	2	8	8	1	32	1	16	16	0	4×12, 6×8	48	5.818 to 6.000	>8.000 to 8.250	False	4	0	0	11	12
5.10	2	8	12	2	64	3	12	12	0	2×3, 6×1, 3×2	6	1.450 to 3.000	11.963 to 24.750	False	5	1	0	11	2
5.10	2	8	12	2	64	3	12	12	0	3×3	9	1.455 to 4.000	>8.000 to 24.750	False	5	1	0	11	3
5.10	2	8	12	2	64	3	12	12	0	3×3	9	1.450 to 1.455	7.975 to 8.000	True	5	1	1	22	3
5.10	2	8	12	2	64	3	12	12	0	4×3, 6×2	12	1.939 to 6.000	>8.000 to 24.750	False	5	1	0	11	4
5.10	2	8	12	2	64	3	12	12	0	4×3, 6×2	12	1.455 to 1.939	6.000 to 8.000	False	5	1	1	22	4
5.10	2	8	12	2	64	3	12	12	0	6×3	18	2.909 to 6.000	>8.000 to 16.500	False	5	1	0	11	6
5.10	2	8	12	2	64	3	12	12	0	4×6, 6×4	24	3.879 to 6.000	>8.000 to 12.375	False	5	1	0	11	8
5.10	2	8	12	2	64	3	12	12	0	4×6, 6×4	24	2.909 to 3.879	6.000 to 8.000	False	5	1	1	22	8
5.10	2	8	12	2	64	3	12	12	0	4×12, 6×8	48	5.818 to 6.000	6.000 to 6.188	False	5	1	1	22	16
30.00	2	8	12	1	64	3	16	24	0	3×4, 6×2, 4×3, 2×6	12	1.450 to 3.000	11.963 to 24.750	False	30	0	0	11	2
30.00	2	8	12	1	64	3	16	24	0	6×3, 3×6	18	1.455 to 4.000	>8.000 to 24.750	False	30	0	0	11	3
30.00	2	8	12	1	64	3	16	24	0	6×3, 3×6	18	1.450 to 1.455	7.975 to 8.000	True	30	0	1	22	3
30.00	2	8	12	1	64	3	16	24	0	4×6, 6×4	24	1.939 to 6.000	>8.000 to 24.750	False	30	0	0	11	4
30.00	2	8	12	1	64	3	16	24	0	4×6, 6×4	24	1.455 to 1.939	6.000 to 8.000	False	30	0	1	22	4
30.00	2	8	12	1	64	3	16	24	0	4×12, 6×8	48	3.879 to 6.000	>8.000 to 12.375	False	30	0	0	11	8
30.00	2	8	12	1	64	3	16	24	0	4×12, 6×8	48	2.909 to 3.879	6.000 to 8.000	False	30	0	1	22	8
30.00	2	8	12	1	64	3	16	24	0	4×24, 6×16	96	5.818 to 6.000	6.000 to 6.188	False	30	0	1	22	16
30.00	2	8	12	1	64	3	16	24	0	4×8	32	2.586 to 6.000	>8.000 to 18.562	True	30	0	0	33	16

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Table 72. ADC Path Supported JESD204C Modes (L = 2)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
4.10	2	8	16	2	16	1	16	16	0	2×4, 4×2	8	1.450 to 3.000	11.963 to 24.750	False	4	1	0	11	2
4.10	2	8	16	2	16	1	16	16	0	4×3, 3×4, 6×2	12	1.455 to 4.000	>8.000 to 24.750	False	4	1	0	11	3
4.10	2	8	16	2	16	1	16	16	0	4×3, 3×4, 6×2	12	1.450 to 1.455	7.975 to 8.000	True	4	1	1	22	3
4.10	2	8	16	2	16	1	16	16	0	4×4	16	1.939 to 6.000	>8.000 to 24.750	False	4	1	0	11	4
4.10	2	8	16	2	16	1	16	16	0	4×4	16	1.455 to 1.939	6.000 to 8.000	False	4	1	1	22	4
4.10	2	8	16	2	16	1	16	16	0	4×6, 6×4	24	2.909 to 6.000	>8.000 to 16.500	False	4	1	0	11	6
4.10	2	8	16	2	16	1	16	16	0	4×8	32	3.879 to 6.000	>8.000 to 12.375	False	4	1	0	11	8
4.10	2	8	16	2	16	1	16	16	0	4×8	32	2.909 to 3.879	6.000 to 8.000	False	4	1	1	22	8
4.10	2	8	16	2	16	1	16	16	0	4×12, 6×8	48	5.818 to 6.000	>8.000 to 8.250	False	4	1	0	11	12
4.10	2	8	16	2	16	1	16	16	0	2×3, 6×1, 3×2	6	1.450 to 2.250	15.950 to 24.750	True	4	1	0	22	3
30.10	2	8	24	2	32	3	16	24	0	3×6, 6×3	18	1.455 to 4.000	>8.000 to 24.750	False	30	1	0	11	3
30.10	2	8	24	2	32	3	16	24	0	3×6, 6×3	18	1.450 to 1.455	7.975 to 8.000	True	30	1	1	22	3
30.10	2	8	24	2	32	3	16	24	0	3×6, 6×3	18	1.450 to 1.455	7.975 to 8.000	True	30	1	1	22	3
30.10	2	8	24	2	32	3	16	24	0	4×6, 6×4	24	1.939 to 6.000	>8.000 to 24.750	False	30	1	0	11	4
30.10	2	8	24	2	32	3	16	24	0	4×6, 6×4	24	1.455 to 1.939	6.000 to 8.000	False	30	1	1	22	4
30.10	2	8	24	2	32	3	16	24	0	4×12, 6×8	48	3.879 to 6.000	>8.000 to 12.375	False	30	1	0	11	8
30.10	2	8	24	2	32	3	16	24	0	4×12, 6×8	48	2.909 to 3.879	6.000 to 8.000	False	30	1	1	22	8
30.10	2	8	24	2	32	3	16	24	0	4×24, 6×16	96	5.818 to 6.000	6.000 to 6.188	False	30	1	1	22	16

[1] N/A means not applicable.

[2] JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually. Modes with N/A are not supported by AD9986 and AD9988.

[3] If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in Table 42. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For Transmit and receive path operation, refer to the bit field descriptions for these registers in Table 61 to determine the appropriate setting.

[4] Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

ADC Path Supported JESD204C Modes (L = 3)

Table 73. ADC Path Supported JESD204C Modes (L = 3)[1]

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
9.01	3	3	2	1	128	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	N/A[4]	N/A	0	11	4
9.01	3	3	2	1	128	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
9.01	3	3	2	1	128	1	16	16	0	3×2	6	2.909 to 6.000	>8.000 to 16.500	False	N/A	N/A	0	11	6
9.01	3	3	2	1	128	1	16	16	0	4×2	8	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
9.01	3	3	2	1	128	1	16	16	0	4×2	8	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
9.01	3	3	2	1	128	1	16	16	0	6×2	12	5.818 to 6.000	>8.000 to 8.250	False	N/A	N/A	0	11	12
9.01	3	3	2	1	128	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
9.11	3	3	4	2	64	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4

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Table 73. ADC Path Supported JESD204C Modes (L = 3)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
9.11	3	3	4	2	64	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
9.11	3	3	4	2	64	1	16	16	0	3×2	6	2.909 to 6.000	>8.000 to 16.500	False	N/A	N/A	0	11	6
9.11	3	3	4	2	64	1	16	16	0	4×2	8	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
9.11	3	3	4	2	64	1	16	16	0	4×2	8	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
9.11	3	3	4	2	64	1	16	16	0	6×2	12	5.818 to 6.000	>8.000 to 8.250	False	N/A	N/A	0	11	12
9.11	3	3	4	2	64	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
9.00	3	6	4	1	64	1	16	16	0	2×2, 4×1	4	1.450 to 3.000	11.963 to 24.750	False	9	0	0	11	2
9.00	3	6	4	1	64	1	16	16	0	3×2, 6×1, 2×3	6	1.455 to 4.000	>8.000 to 24.750	False	9	0	0	11	3
9.00	3	6	4	1	64	1	16	16	0	3×2, 6×1, 2×3	6	1.450 to 1.455	7.975 to 8.000	True	9	0	1	22	3
9.00	3	6	4	1	64	1	16	16	0	4×2, 2×4	8	1.939 to 6.000	>8.000 to 24.750	False	9	0	0	11	4
9.00	3	6	4	1	64	1	16	16	0	4×2, 2×4	8	1.455 to 1.939	6.000 to 8.000	False	9	0	1	22	4
9.00	3	6	4	1	64	1	16	16	0	3×4, 4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	9	0	0	11	6
9.00	3	6	4	1	64	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	9	0	0	11	8
9.00	3	6	4	1	64	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	9	0	1	22	8
9.00	3	6	4	1	64	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	9	0	0	11	9
9.00	3	6	4	1	64	1	16	16	0	6×3	18	3.273 to 4.364	6.000 to 8.000	True	9	0	1	22	9
9.00	3	6	4	1	64	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	9	0	0	11	12
9.00	3	6	4	1	64	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	9	0	1	22	16
9.10	3	6	8	2	32	1	16	16	0	2×2, 4×1	4	1.450 to 3.000	11.963 to 24.750	False	9	1	0	11	2
9.10	3	6	8	2	32	1	16	16	0	3×2, 6×1	6	1.455 to 4.000	>8.000 to 24.750	False	9	1	0	11	3
9.10	3	6	8	2	32	1	16	16	0	3×2, 6×1	6	1.450 to 1.455	7.975 to 8.000	True	9	1	1	22	3
9.10	3	6	8	2	32	1	16	16	0	4×2, 2×4	8	1.939 to 6.000	>8.000 to 24.750	False	9	1	0	11	4
9.10	3	6	8	2	32	1	16	16	0	4×2, 2×4	8	1.455 to 1.939	6.000 to 8.000	False	9	1	1	22	4
9.10	3	6	8	2	32	1	16	16	0	3×4, 4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	9	1	0	11	6
9.10	3	6	8	2	32	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	9	1	0	11	8
9.10	3	6	8	2	32	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	9	1	1	22	8
9.10	3	6	8	2	32	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	9	1	0	11	9
9.10	3	6	8	2	32	1	16	16	0	6×3	18	3.273 to 4.364	6.000 to 8.000	True	9	1	1	22	9
9.10	3	6	8	2	32	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	9	1	0	11	12
9.10	3	6	8	2	32	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	9	1	1	22	16
8.00	3	12	8	1	32	1	16	16	0	2×4, 4×2	8	1.450 to 3.000	11.963 to 24.750	False	8	0	0	11	2
8.00	3	12	8	1	32	1	16	16	0	4×3, 3×4, 6×2	12	1.455 to 4.000	>8.000 to 24.750	False	8	0	0	11	3
8.00	3	12	8	1	32	1	16	16	0	4×3, 3×4, 6×2	12	1.450 to 1.455	7.975 to 8.000	True	8	0	1	22	3
8.00	3	12	8	1	32	1	16	16	0	4×4	16	1.939 to 6.000	>8.000 to 24.750	False	8	0	0	11	4
8.00	3	12	8	1	32	1	16	16	0	4×4	16	1.455 to 1.939	6.000 to 8.000	False	8	0	1	22	4
8.00	3	12	8	1	32	1	16	16	0	4×6, 6×4	24	2.909 to 6.000	>8.000 to 16.500	False	8	0	0	11	6
8.00	3	12	8	1	32	1	16	16	0	4×8	32	3.879 to 6.000	>8.000 to 12.375	False	8	0	0	11	8
8.00	3	12	8	1	32	1	16	16	0	4×8	32	2.909 to 3.879	6.000 to 8.000	False	8	0	1	22	8

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Table 73. ADC Path Supported JESD204C Modes (L = 3)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
8.00	3	12	8	1	32	1	16	16	0	4×12, 6×8	48	5.818 to 6.000	>8.000 to 8.250	False	8	0	0	11	12
8.00	3	12	8	1	32	1	16	16	0	2×3, 6×1, 3×2	6	1.450 to 2.250	15.950 to 24.750	True	8	0	0	22	3
8.10	3	12	16	2	16	1	16	16	0	2×4, 4×2	8	1.450 to 3.000	11.963 to 24.750	False	8	1	0	11	2
8.10	3	12	16	2	16	1	16	16	0	4×3, 3×4, 6×2	12	1.455 to 4.000	>8.000 to 24.750	False	8	1	0	11	3
8.10	3	12	16	2	16	1	16	16	0	4×3, 3×4, 6×2	12	1.450 to 1.455	7.975 to 8.000	True	8	1	1	22	3
8.10	3	12	16	2	16	1	16	16	0	4×4	16	1.939 to 6.000	>8.000 to 24.750	False	8	1	0	11	4
8.10	3	12	16	2	16	1	16	16	0	4×4	16	1.455 to 1.939	6.000 to 8.000	False	8	1	1	22	4
8.10	3	12	16	2	16	1	16	16	0	4×6, 6×4	24	2.909 to 6.000	>8.000 to 16.500	False	8	1	0	11	6
8.10	3	12	16	2	16	1	16	16	0	4×8	32	3.879 to 6.000	>8.000 to 12.375	False	8	1	0	11	8
8.10	3	12	16	2	16	1	16	16	0	4×8	32	2.909 to 3.879	6.000 to 8.000	False	8	1	1	22	8
8.10	3	12	16	2	16	1	16	16	0	4×12, 6×8	48	5.818 to 6.000	>8.000 to 8.250	False	8	1	0	11	12
8.10	3	12	16	2	16	1	16	16	0	2×3, 6×1, 3×2	6	1.450 to 2.250	15.950 to 24.750	True	8	1	0	22	3

[1] N/A means not applicable.

[2] JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually. Modes with N/A are not supported by AD9986 and AD9988.

[3] If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in Table 42. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For Transmit and receive path operation, refer to the bit field descriptions for these registers in Table 61 to determine the appropriate setting.

[4] Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

ADC Path Supported JESD204C Modes (L = 4)

Table 74. ADC Path Supported JESD204C Modes (L = 4)[1]

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
13.01	4	1	1	2	256	1	16	16	1	1×1	1	1.939 to 6.000	>8.000 to 24.750	False	N/A[4]	N/A	0	11	4
13.01	4	1	1	2	256	1	16	16	1	1×1	1	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
13.01	4	1	1	2	256	1	16	16	1	2×1	2	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
13.01	4	1	1	2	256	1	16	16	1	2×1	2	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
13.01	4	1	1	2	256	1	16	16	1	4×1	4	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
13.11	4	1	2	4	128	1	16	16	0	1×1	1	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4
13.11	4	1	2	4	128	1	16	16	0	1×1	1	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
13.11	4	1	2	4	128	1	16	16	0	2×1	2	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
13.11	4	1	2	4	128	1	16	16	0	2×1	2	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
13.11	4	1	2	4	128	1	16	16	0	4×1	4	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
14.01	4	1	3	8	256	3	12	12	0	1×1	1	2.586 to 6.000	>8.000 to 18.562	True	N/A	N/A	0	33	16
14.01	4	1	3	8	256	3	12	12	0	2×1	2	5.172 to 6.000	>8.000 to 9.281	True	N/A	N/A	0	33	32

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Table 74. ADC Path Supported JESD204C Modes (L = 4)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
13.21	4	1	4	8	64	1	16	16	0	2×1	2	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
13.21	4	1	4	8	64	1	16	16	0	2×1	2	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
13.21	4	1	4	8	64	1	16	16	0	1×1	1	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4
13.21	4	1	4	8	64	1	16	16	0	1×1	1	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
13.21	4	1	4	8	64	1	16	16	0	4×1	4	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
13.00	4	2	1	1	256	1	16	16	1	1×1	1	1.450 to 3.000	11.963 to 24.750	False	13	0	0	11	2
13.00	4	2	1	1	256	1	16	16	1	2×1	2	1.939 to 6.000	>8.000 to 24.750	False	13	0	0	11	4
13.00	4	2	1	1	256	1	16	16	1	2×1	2	1.455 to 1.939	6.000 to 8.000	False	13	0	1	22	4
13.00	4	2	1	1	256	1	16	16	1	3×1	3	2.909 to 6.000	>8.000 to 16.500	False	13	0	0	11	6
13.00	4	2	1	1	256	1	16	16	1	4×1	4	3.879 to 6.000	>8.000 to 12.375	False	13	0	0	11	8
13.00	4	2	1	1	256	1	16	16	1	4×1	4	2.909 to 3.879	6.000 to 8.000	False	13	0	1	22	8
13.00	4	2	1	1	256	1	16	16	1	6×1	6	5.818 to 6.000	>8.000 to 8.250	False	13	0	0	11	12
13.00	4	2	1	1	256	1	16	16	1	2×4, 4×2	8	5.818 to 6.000	6.000 to 6.188	False	13	0	1	22	16
13.10	4	2	2	2	128	1	16	16	0	1×1	1	1.450 to 3.000	11.963 to 24.750	False	13	1	0	11	2
13.10	4	2	2	2	128	1	16	16	0	2×1	2	1.939 to 6.000	>8.000 to 24.750	False	13	1	0	11	4
13.10	4	2	2	2	128	1	16	16	0	2×1	2	1.455 to 1.939	6.000 to 8.000	False	13	1	1	22	4
13.10	4	2	2	2	128	1	16	16	0	3×1	3	2.909 to 6.000	>8.000 to 16.500	False	13	1	0	11	6
13.10	4	2	2	2	128	1	16	16	0	4×1	4	3.879 to 6.000	>8.000 to 12.375	False	13	1	0	11	8
13.10	4	2	2	2	128	1	16	16	0	4×1	4	2.909 to 3.879	6.000 to 8.000	False	13	1	1	22	8
13.10	4	2	2	2	128	1	16	16	0	6×1	6	5.818 to 6.000	>8.000 to 8.250	False	13	1	0	11	12
13.10	4	2	2	2	128	1	16	16	0	2×4, 4×2	8	5.818 to 6.000	6.000 to 6.188	False	13	1	1	22	16
14.00	4	2	3	4	256	3	12	12	0	1×1	1	1.450 to 4.000	8.972 to 24.750	True	14	0	0	33	8
14.00	4	2	3	4	256	3	12	12	0	2×1	2	2.586 to 6.000	>8.000 to 18.562	True	14	0	0	33	16
14.00	4	2	3	4	256	3	12	12	0	3×1	3	3.879 to 6.000	>8.000 to 12.375	False	14	0	0	11	8
14.00	4	2	3	4	256	3	12	12	0	3×1	3	2.909 to 3.879	6.000 to 8.000	False	14	0	1	22	8
14.00	4	2	3	4	256	3	12	12	0	3×2	6	5.818 to 6.000	6.000 to 6.188	False	14	0	1	22	16
14.00	4	2	3	4	256	3	12	12	0	4×1	4	5.172 to 6.000	>8.000 to 9.281	True	14	0	0	33	32
13.20	4	2	4	4	64	1	16	16	0	2×1	2	1.939 to 6.000	>8.000 to 24.750	False	13	2	0	11	4
13.20	4	2	4	4	64	1	16	16	0	2×1	2	1.455 to 1.939	6.000 to 8.000	False	13	2	1	22	4
13.20	4	2	4	4	64	1	16	16	0	1×1	1	1.450 to 3.000	11.963 to 24.750	False	13	2	0	11	2
13.20	4	2	4	4	64	1	16	16	0	3×1	3	2.909 to 6.000	>8.000 to 16.500	False	13	2	0	11	6
13.20	4	2	4	4	64	1	16	16	0	4×1	4	3.879 to 6.000	>8.000 to 12.375	False	13	2	0	11	8
13.20	4	2	4	4	64	1	16	16	0	4×1	4	2.909 to 3.879	6.000 to 8.000	False	13	2	1	22	8
13.20	4	2	4	4	64	1	16	16	0	6×1	6	5.818 to 6.000	>8.000 to 8.250	False	13	2	0	11	12
13.20	4	2	4	4	64	1	16	16	0	4×2, 2×4	8	5.818 to 6.000	6.000 to 6.188	False	13	2	1	22	16

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Table 74. ADC Path Supported JESD204C Modes (L = 4)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
14.10	4	2	6	8	128	3	12	12	0	1×1	1	1.450 to 4.000	8.972 to 24.750	True	14	1	0	33	8
14.10	4	2	6	8	128	3	12	12	0	2×1	2	2.586 to 6.000	>8.000 to 18.562	True	14	1	0	33	16
14.10	4	2	6	8	128	3	12	12	0	3×1	3	3.879 to 6.000	>8.000 to 12.375	False	14	1	0	11	8
14.10	4	2	6	8	128	3	12	12	0	3×1	3	2.909 to 3.879	6.000 to 8.000	False	14	1	1	22	8
14.10	4	2	6	8	128	3	12	12	0	3×2	6	5.818 to 6.000	6.000 to 6.188	False	14	1	1	22	16
14.10	4	2	6	8	128	3	12	12	0	4×1	4	5.172 to 6.000	>8.000 to 9.281	True	14	0	0	33	32
13.30	4	2	8	8	32	1	16	16	0	2×1	2	1.939 to 6.000	>8.000 to 24.750	False	13	3	0	11	4
13.30	4	2	8	8	32	1	16	16	0	2×1	2	1.455 to 1.939	6.000 to 8.000	False	13	3	1	22	4
13.30	4	2	8	8	32	1	16	16	0	1×1	1	1.450 to 3.000	11.963 to 24.750	False	13	3	0	11	2
13.30	4	2	8	8	32	1	16	16	0	3×1	3	2.909 to 6.000	>8.000 to 16.500	False	13	3	0	11	6
13.30	4	2	8	8	32	1	16	16	0	4×1	4	3.879 to 6.000	>8.000 to 12.375	False	13	3	0	11	8
13.30	4	2	8	8	32	1	16	16	0	4×1	4	2.909 to 3.879	6.000 to 8.000	False	13	3	1	22	8
13.30	4	2	8	8	32	1	16	16	0	6×1	6	5.818 to 6.000	>8.000 to 8.250	False	13	3	0	11	12
11.00	4	4	2	1	128	1	16	16	0	1×1	1	1.450 to 1.500	23.925 to 24.750	False	11	0	0	11	1
11.00	4	4	2	1	128	1	16	16	0	2×1	2	1.450 to 3.000	11.963 to 24.750	False	11	0	0	11	2
11.00	4	4	2	1	128	1	16	16	0	3×1	3	1.455 to 4.000	>8.000 to 24.750	False	11	0	0	11	3
11.00	4	4	2	1	128	1	16	16	0	3×1	3	1.450 to 1.455	7.975 to 8.000	True	11	0	1	22	3
11.00	4	4	2	1	128	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	11	0	0	11	4
11.00	4	4	2	1	128	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	11	0	1	22	4
11.00	4	4	2	1	128	1	16	16	0	3×2, 6×1, 2×3	6	2.909 to 6.000	>8.000 to 16.500	False	11	0	0	11	6
11.00	4	4	2	1	128	1	16	16	0	4×2, 2×4	8	3.879 to 6.000	>8.000 to 12.375	False	11	0	0	11	8
11.00	4	4	2	1	128	1	16	16	0	4×2, 2×4	8	2.909 to 3.879	6.000 to 8.000	False	11	0	1	22	8
11.00	4	4	2	1	128	1	16	16	0	3×4, 6×2	12	5.818 to 6.000	>8.000 to 8.250	False	11	0	0	11	12
11.00	4	4	2	1	128	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	11	0	1	22	16
25.00	4	4	3	2	256	3	12	12	0	1×1	1	1.450 to 2.000	17.944 to 24.750	True	25	0	0	33	4
25.00	4	4	3	2	256	3	12	12	0	2×1	2	1.450 to 4.000	8.972 to 24.750	True	25	0	0	33	8
25.00	4	4	3	2	256	3	12	12	0	3×1	3	1.939 to 6.000	>8.000 to 24.750	False	25	0	0	11	4
25.00	4	4	3	2	256	3	12	12	0	3×1	3	1.455 to 1.939	6.000 to 8.000	False	25	0	1	22	4
25.00	4	4	3	2	256	3	12	12	0	4×1	4	2.586 to 6.000	>8.000 to 18.562	True	25	0	0	33	16
25.00	4	4	3	2	256	3	12	12	0	6×1	6	3.879 to 6.000	>8.000 to 12.375	False	25	0	0	11	8
25.00	4	4	3	2	256	3	12	12	0	6×1	6	2.909 to 3.879	6.000 to 8.000	False	25	0	1	22	8
25.00	4	4	3	2	256	3	12	12	0	6×2	12	5.818 to 6.000	6.000 to 6.188	False	25	0	1	22	16
31.01	4	4	3	1	256	3	16	24	0	3×2	6	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4

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Table 74. ADC Path Supported JESD204C Modes (L = 4)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
31.01	4	4	3	1	256	3	16	24	0	3×2	6	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
31.01	4	4	3	1	256	3	16	24	0	6×2	12	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
31.01	4	4	3	1	256	3	16	24	0	6×2	12	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
31.01	4	4	3	1	256	3	16	24	0	6×4	24	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
11.10	4	4	4	2	64	1	16	16	0	1×1	1	1.450 to 1.500	23.925 to 24.750	False	11	1	0	11	1
11.10	4	4	4	2	64	1	16	16	0	2×1	2	1.450 to 3.000	11.963 to 24.750	False	11	1	0	11	2
11.10	4	4	4	2	64	1	16	16	0	3×1	3	1.455 to 4.000	>8.000 to 24.750	False	11	1	0	11	3
11.10	4	4	4	2	64	1	16	16	0	3×1	3	1.450 to 1.455	7.975 to 8.000	True	11	1	1	22	3
11.10	4	4	4	2	64	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	11	1	0	11	4
11.10	4	4	4	2	64	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	11	1	1	22	4
11.10	4	4	4	2	64	1	16	16	0	3×2, 6×1	6	2.909 to 6.000	>8.000 to 16.500	False	11	1	0	11	6
11.10	4	4	4	2	64	1	16	16	0	4×2, 2×4	8	3.879 to 6.000	>8.000 to 12.375	False	11	1	0	11	8
11.10	4	4	4	2	64	1	16	16	0	4×2, 2×4	8	2.909 to 3.879	6.000 to 8.000	False	11	1	1	22	8
11.10	4	4	4	2	64	1	16	16	0	6×2	12	5.818 to 6.000	>8.000 to 8.250	False	11	1	0	11	12
11.10	4	4	4	2	64	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	11	1	1	22	16
25.10	4	4	6	4	128	3	12	12	0	3×1	3	1.939 to 6.000	>8.000 to 24.750	False	25	1	0	11	4
25.10	4	4	6	4	128	3	12	12	0	3×1	3	1.455 to 1.939	6.000 to 8.000	False	25	1	1	22	4
25.10	4	4	6	4	128	3	12	12	0	4×1	4	2.586 to 6.000	>8.000 to 18.562	True	25	1	0	33	16
25.10	4	4	6	4	128	3	12	12	0	2×1	2	1.450 to 4.000	8.972 to 24.750	True	25	1	0	33	8
25.10	4	4	6	4	128	3	12	12	0	1×1	1	1.450 to 2.000	17.944 to 24.750	True	25	1	0	33	4
25.10	4	4	6	4	128	3	12	12	0	6×1	6	3.879 to 6.000	>8.000 to 12.375	False	25	1	0	11	8
25.10	4	4	6	4	128	3	12	12	0	6×1	6	2.909 to 3.879	6.000 to 8.000	False	25	1	1	22	8
25.10	4	4	6	4	128	3	12	12	0	6×2	12	5.818 to 6.000	6.000 to 6.188	False	25	1	1	22	16
31.11	4	4	6	2	128	3	16	24	0	3×2	6	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4
31.11	4	4	6	2	128	3	16	24	0	3×2	6	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
31.11	4	4	6	2	128	3	16	24	0	6×2	12	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
31.11	4	4	6	2	128	3	16	24	0	6×2	12	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
31.11	4	4	6	2	128	3	16	24	0	6×4	24	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
11.20	4	4	8	4	32	1	16	16	0	1×1	1	1.450 to 1.500	23.925 to 24.750	False	11	2	0	11	1
11.20	4	4	8	4	32	1	16	16	0	2×1	2	1.450 to 3.000	11.963 to 24.750	False	11	2	0	11	2
11.20	4	4	8	4	32	1	16	16	0	3×1	3	1.455 to 4.000	>8.000 to 24.750	False	11	2	0	11	3
11.20	4	4	8	4	32	1	16	16	0	3×1	3	1.450 to 1.455	7.975 to 8.000	True	11	2	1	22	3
11.20	4	4	8	4	32	1	16	16	0	4×1	4	1.939 to 6.000	>8.000 to 24.750	False	11	2	0	11	4
11.20	4	4	8	4	32	1	16	16	0	4×1	4	1.455 to 1.939	6.000 to 8.000	False	11	2	1	22	4
11.20	4	4	8	4	32	1	16	16	0	6×1	6	2.909 to 6.000	>8.000 to 16.500	False	11	2	0	11	6

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Table 74. ADC Path Supported JESD204C Modes (L = 4)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
11.20	4	4	8	4	32	1	16	16	0	4×2, 2×4	8	3.879 to 6.000	>8.000 to 12.375	False	11	2	0	11	8
11.20	4	4	8	4	32	1	16	16	0	4×2, 2×4	8	2.909 to 3.879	6.000 to 8.000	False	11	2	1	22	8
24.00	4	8	3	1	256	3	12	12	0	2×1	2	1.450 to 2.000	17.944 to 24.750	True	24	0	0	33	4
24.00	4	8	3	1	256	3	12	12	0	3×1	3	1.450 to 3.000	11.963 to 24.750	False	24	0	0	11	2
24.00	4	8	3	1	256	3	12	12	0	4×1	4	1.450 to 4.000	8.972 to 24.750	True	24	0	0	33	8
24.00	4	8	3	1	256	3	12	12	0	6×1	6	1.939 to 6.000	>8.000 to 24.750	False	24	0	0	11	4
24.00	4	8	3	1	256	3	12	12	0	6×1	6	1.455 to 1.939	6.000 to 8.000	False	24	0	1	22	4
24.00	4	8	3	1	256	3	12	12	0	4×3, 6×2	12	3.879 to 6.000	>8.000 to 12.375	False	24	0	0	11	8
24.00	4	8	3	1	256	3	12	12	0	4×3, 6×2	12	2.909 to 3.879	6.000 to 8.000	False	24	0	1	22	8
24.00	4	8	3	1	256	3	12	12	0	3×3	9	2.909 to 6.000	>8.000 to 16.500	False	24	0	0	11	6
10.00	4	8	4	1	64	1	16	16	0	2×2, 4×1	4	1.450 to 3.000	11.963 to 24.750	False	10	0	0	11	2
10.00	4	8	4	1	64	1	16	16	0	3×2, 6×1, 2×3	6	1.455 to 4.000	>8.000 to 24.750	False	10	0	0	11	3
10.00	4	8	4	1	64	1	16	16	0	3×2, 6×1, 2×3	6	1.450 to 1.455	7.975 to 8.000	True	10	0	1	22	3
10.00	4	8	4	1	64	1	16	16	0	4×2, 2×4	8	1.939 to 6.000	>8.000 to 24.750	False	10	0	0	11	4
10.00	4	8	4	1	64	1	16	16	0	4×2, 2×4	8	1.455 to 1.939	6.000 to 8.000	False	10	0	1	22	4
10.00	4	8	4	1	64	1	16	16	0	3×4, 4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	10	0	0	11	6
10.00	4	8	4	1	64	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	10	0	0	11	8
10.00	4	8	4	1	64	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	10	0	1	22	8
10.00	4	8	4	1	64	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	10	0	0	11	9
10.00	4	8	4	1	64	1	16	16	0	6×3	18	3.273 to 4.364	6.000 to 8.000	True	10	0	1	22	9
10.00	4	8	4	1	64	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	10	0	0	11	12
10.00	4	8	4	1	64	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	10	0	1	22	16
24.10	4	8	6	2	128	3	12	12	0	3×1	3	1.450 to 3.000	11.963 to 24.750	False	24	1	0	11	2
24.10	4	8	6	2	128	3	12	12	0	2×1	2	1.450 to 2.000	17.944 to 24.750	True	24	1	0	33	4
24.10	4	8	6	2	128	3	12	12	0	4×1	4	1.450 to 4.000	8.972 to 24.750	True	24	1	0	33	8
24.10	4	8	6	2	128	3	12	12	0	6×1	6	1.939 to 6.000	>8.000 to 24.750	False	24	1	0	11	4
24.10	4	8	6	2	128	3	12	12	0	6×1	6	1.455 to 1.939	6.000 to 8.000	False	24	1	1	22	4
24.10	4	8	6	2	128	3	12	12	0	4×3, 6×2	12	3.879 to 6.000	>8.000 to 12.375	False	24	1	0	11	8
24.10	4	8	6	2	128	3	12	12	0	4×3, 6×2	12	2.909 to 3.879	6.000 to 8.000	False	24	1	1	22	8
24.10	4	8	6	2	128	3	12	12	0	3×3	9	2.909 to 6.000	>8.000 to 16.500	False	24	1	0	11	6
31.00	4	8	6	1	128	3	16	24	0	2×3, 6×1, 3×2	6	1.450 to 3.000	11.963 to 24.750	False	31	0	0	11	2
31.00	4	8	6	1	128	3	16	24	0	4×2	8	1.450 to 4.000	8.972 to 24.750	True	31	0	0	33	8
31.00	4	8	6	1	128	3	16	24	0	3×3	9	1.455 to 4.000	>8.000 to 24.750	False	31	0	0	11	3
31.00	4	8	6	1	128	3	16	24	0	3×3	9	1.450 to 1.455	7.975 to 8.000	True	31	0	1	22	3

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Table 74. ADC Path Supported JESD204C Modes (L = 4)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
31.00	4	8	6	1	128	3	16	24	0	4×3, 6×2	12	1.939 to 6.000	>8.000 to 24.750	False	31	0	0	11	4
31.00	4	8	6	1	128	3	16	24	0	4×3, 6×2	12	1.455 to 1.939	6.000 to 8.000	False	31	0	1	22	4
31.00	4	8	6	1	128	3	16	24	0	6×3	18	2.909 to 6.000	>8.000 to 16.500	False	31	0	0	11	6
31.00	4	8	6	1	128	3	16	24	0	4×6, 6×4	24	3.879 to 6.000	>8.000 to 12.375	False	31	0	0	11	8
31.00	4	8	6	1	128	3	16	24	0	4×6, 6×4	24	2.909 to 3.879	6.000 to 8.000	False	31	0	1	22	8
31.00	4	8	6	1	128	3	16	24	0	4×12, 6×8	48	5.818 to 6.000	6.000 to 6.188	False	31	0	1	22	16
10.10	4	8	8	2	32	1	16	16	0	2×2, 4×1	4	1.450 to 3.000	11.963 to 24.750	False	10	1	0	11	2
10.10	4	8	8	2	32	1	16	16	0	3×2, 6×1	6	1.455 to 4.000	>8.000 to 24.750	False	10	1	0	11	3
10.10	4	8	8	2	32	1	16	16	0	3×2, 6×1	6	1.450 to 1.455	7.975 to 8.000	True	10	1	1	22	3
10.10	4	8	8	2	32	1	16	16	0	4×2, 2×4	8	1.939 to 6.000	>8.000 to 24.750	False	10	1	0	11	4
10.10	4	8	8	2	32	1	16	16	0	4×2, 2×4	8	1.455 to 1.939	6.000 to 8.000	False	10	1	1	22	4
10.10	4	8	8	2	32	1	16	16	0	3×4, 4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	10	1	0	11	6
10.10	4	8	8	2	32	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	10	1	0	11	8
10.10	4	8	8	2	32	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	10	1	1	22	8
10.10	4	8	8	2	32	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	10	1	0	11	9
10.10	4	8	8	2	32	1	16	16	0	6×3	18	3.273 to 4.364	6.000 to 8.000	True	10	1	1	22	9
10.10	4	8	8	2	32	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	10	1	0	11	12
10.10	4	8	8	2	32	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	10	1	1	22	16
31.10	4	8	12	2	64	3	16	24	0	2×3, 6×1, 3×2	6	1.450 to 3.000	11.963 to 24.750	False	31	1	0	11	2
31.10	4	8	12	2	64	3	16	24	0	3×3	9	1.455 to 4.000	>8.000 to 24.750	False	31	1	0	11	3
31.10	4	8	12	2	64	3	16	24	0	3×3	9	1.450 to 1.455	7.975 to 8.000	True	31	1	1	22	3
31.10	4	8	12	2	64	3	16	24	0	4×3, 6×2	12	1.939 to 6.000	>8.000 to 24.750	False	31	1	0	11	4
31.10	4	8	12	2	64	3	16	24	0	4×3, 6×2	12	1.455 to 1.939	6.000 to 8.000	False	31	1	1	22	4
31.10	4	8	12	2	64	3	16	24	0	6×3	18	2.909 to 6.000	>8.000 to 16.500	False	31	1	0	11	6
31.10	4	8	12	2	64	3	16	24	0	4×6, 6×4	24	3.879 to 6.000	>8.000 to 12.375	False	31	1	0	11	8
31.10	4	8	12	2	64	3	16	24	0	4×6, 6×4	24	2.909 to 3.879	6.000 to 8.000	False	31	1	1	22	8
31.10	4	8	12	2	64	3	16	24	0	4×12, 6×8	48	5.818 to 6.000	6.000 to 6.188	False	31	1	1	22	16
12.00	4	16	8	1	32	1	16	16	0	2×4, 4×2	8	1.450 to 3.000	11.963 to 24.750	False	12	0	0	11	2
12.00	4	16	8	1	32	1	16	16	0	4×3, 3×4, 6×2	12	1.455 to 4.000	>8.000 to 24.750	False	12	0	0	11	3
12.00	4	16	8	1	32	1	16	16	0	4×3, 3×4, 6×2	12	1.450 to 1.455	7.975 to 8.000	True	12	0	1	22	3
12.00	4	16	8	1	32	1	16	16	0	4×4	16	1.939 to 6.000	>8.000 to 24.750	False	12	0	0	11	4
12.00	4	16	8	1	32	1	16	16	0	4×4	16	1.455 to 1.939	6.000 to 8.000	False	12	0	1	22	4
12.00	4	16	8	1	32	1	16	16	0	4×6, 6×4	24	2.909 to 6.000	>8.000 to 16.500	False	12	0	0	11	6
12.00	4	16	8	1	32	1	16	16	0	4×8	32	3.879 to 6.000	>8.000 to 12.375	False	12	0	0	11	8
12.00	4	16	8	1	32	1	16	16	0	4×8	32	2.909 to 3.879	6.000 to 8.000	False	12	0	1	22	8
12.00	4	16	8	1	32	1	16	16	0	4×12, 6×8	48	5.818 to 6.000	>8.000 to 8.250	False	12	0	0	11	12
12.00	4	16	8	1	32	1	16	16	0	2×3, 3×2	6	1.450 to 2.250	15.950 to 24.750	True	12	0	0	22	3

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Table 74. ADC Path Supported JESD204C Modes (L = 4)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[2] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
12.10	4	16	16	2	16	1	16	16	0	2×4, 4×2	8	1.450 to 3.000	11.963 to 24.750	False	12	1	0	11	2
12.10	4	16	16	2	16	1	16	16	0	4×3, 3×4, 6×2	12	1.455 to 4.000	>8.000 to 24.750	False	12	1	0	11	3
12.10	4	16	16	2	16	1	16	16	0	4×3, 3×4, 6×2	12	1.450 to 1.455	7.975 to 8.000	True	12	1	1	22	3
12.10	4	16	16	2	16	1	16	16	0	4×4	16	1.939 to 6.000	>8.000 to 24.750	False	12	1	0	11	4
12.10	4	16	16	2	16	1	16	16	0	4×4	16	1.455 to 1.939	6.000 to 8.000	False	12	1	1	22	4
12.10	4	16	16	2	16	1	16	16	0	4×6, 6×4	24	2.909 to 6.000	>8.000 to 16.500	False	12	1	0	11	6
12.10	4	16	16	2	16	1	16	16	0	4×8	32	3.879 to 6.000	>8.000 to 12.375	False	12	1	0	11	8
12.10	4	16	16	2	16	1	16	16	0	4×8	32	2.909 to 3.879	6.000 to 8.000	False	12	1	1	22	8
12.10	4	16	16	2	16	1	16	16	0	4×12, 6×8	48	5.818 to 6.000	>8.000 to 8.250	False	12	1	0	11	12
12.10	4	16	16	2	16	1	16	16	0	2×3, 3×2	6	1.450 to 2.250	15.950 to 24.750	True	12	1	0	22	3

[1] N/A means not applicable.

[2] JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually. Modes with N/A are not supported by AD9986 and AD9988.

[3] If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in Table 42. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For Transmit and receive path operation, refer to the bit field descriptions for these registers in Table 61 to determine the appropriate setting.

[4] Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

ADC Path Supported JESD204C Modes (L = 6)

Table 75. ADC Path Supported JESD204C Modes (L = 6)[1]

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702 Bits[5:0])	JTX_MODE_S_SEL[xl iv] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3])	Register 0x0728	Register 0x00CA, Bits[5:0]
15.01	6	6	2	1	128	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	N/A[4]	N/A	0	11	4
15.01	6	6	2	1	128	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
15.01	6	6	2	1	128	1	16	16	0	3×2	6	2.909 to 6.000	>8.000 to 16.500	False	N/A	N/A	0	11	6
15.01	6	6	2	1	128	1	16	16	0	4×2	8	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
15.01	6	6	2	1	128	1	16	16	0	4×2	8	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
15.01	6	6	2	1	128	1	16	16	0	6×2	12	5.818 to 6.000	>8.000 to 8.250	False	N/A	N/A	0	11	12
15.01	6	6	2	1	128	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
15.11	6	6	4	2	64	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	N/A	N/A	0	11	4
15.11	6	6	4	2	64	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	N/A	N/A	1	22	4
15.11	6	6	4	2	64	1	16	16	0	3×2	6	2.909 to 6.000	>8.000 to 16.500	False	N/A	N/A	0	11	6
15.11	6	6	4	2	64	1	16	16	0	4×2	8	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
15.11	6	6	4	2	64	1	16	16	0	4×2	8	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
15.11	6	6	4	2	64	1	16	16	0	6×2	12	5.818 to 6.000	>8.000 to 8.250	False	N/A	N/A	0	11	12
15.11	6	6	4	2	64	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
15.00	6	12	4	1	64	1	16	16	0	2×2, 4×1	4	1.450 to 3.000	11.963 to 24.750	False	15	0	0	11	2

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Table 75. ADC Path Supported JESD204C Modes (L = 6)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702 Bits[5:0])	JTX_MODE_S_SEL[xl iv] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677, Bits[3:0][3])	Register 0x0728	Register 0x00CA, Bits[5:0]
15.00	6	12	4	1	64	1	16	16	0	3×2, 6×1	6	1.455 to 4.000	>8.000 to 24.750	False	15	0	0	11	3
15.00	6	12	4	1	64	1	16	16	0	4×2	8	1.939 to 6.000	>8.000 to 24.750	False	15	0	0	11	4
15.00	6	12	4	1	64	1	16	16	0	4×2	8	1.455 to 1.939	6.000 to 8.000	False	15	0	1	22	4
15.00	6	12	4	1	64	1	16	16	0	4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	15	0	0	11	6
15.00	6	12	4	1	64	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	15	0	0	11	8
15.00	6	12	4	1	64	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	15	0	1	22	8
15.00	6	12	4	1	64	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	15	0	0	11	9
15.00	6	12	4	1	64	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	15	0	0	11	12
15.00	6	12	4	1	64	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	15	0	1	22	16
15.10	6	12	8	2	32	1	16	16	0	2×2, 4×1	4	1.450 to 3.000	11.963 to 24.750	False	15	1	0	11	2
15.10	6	12	8	2	32	1	16	16	0	3×2, 6×1	6	1.455 to 4.000	>8.000 to 24.750	False	15	1	0	11	3
15.10	6	12	8	2	32	1	16	16	0	4×2	8	1.939 to 6.000	>8.000 to 24.750	False	15	1	0	11	4
15.10	6	12	8	2	32	1	16	16	0	4×2	8	1.455 to 1.939	6.000 to 8.000	False	15	1	1	22	4
15.10	6	12	8	2	32	1	16	16	0	4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	15	1	0	11	6
15.10	6	12	8	2	32	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	15	1	0	11	8
15.10	6	12	8	2	32	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	15	1	1	22	8
15.10	6	12	8	2	32	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	15	1	0	11	9
15.10	6	12	8	2	32	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	15	1	0	11	12
15.10	6	12	8	2	32	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	15	1	1	22	16

[1] N/A means not applicable.

[2] JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually. Modes with N/A are not supported by AD9986 and AD9988.

[3] If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in Table 42. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For Transmit and receive path operation, refer to the bit field descriptions for these registers in Table 61 to determine the appropriate setting.

[4] Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

ADC Path Supported JESD204C Modes (L = 8)

Table 76. ADC Path Supported JESD204C Modes (L = 8)[1]

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[xl viii] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677 Bits[3:0][3])	Register 0x0728	Register 0x00CA, Bits[5:0]
19.01	8	1	1	4	256	1	16	16	1	2×1	2	5.818 to 6.000	6.000 to 6.188	False	N/A[4]	N/A	1	22	16
19.01	8	1	1	4	256	1	16	16	1	1×1	1	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
19.01	8	1	1	4	256	1	16	16	1	1×1	1	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8
19.11	8	1	2	8	128	1	16	16	0	2×1	2	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
19.11	8	1	2	8	128	1	16	16	0	1×1	1	3.879 to 6.000	>8.000 to 12.375	False	N/A	N/A	0	11	8
19.11	8	1	2	8	128	1	16	16	0	1×1	1	2.909 to 3.879	6.000 to 8.000	False	N/A	N/A	1	22	8

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Table 76. ADC Path Supported JESD204C Modes (L = 8)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[xi] [viii] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677 Bits[3:0][3])	Register 0x0728	Register 0x00CA, Bits[5:0]
19.00	8	2	1	2	256	1	16	16	1	1×1	1	1.939 to 6.000	>8.000 to 24.750	False	19	0	0	11	4
19.00	8	2	1	2	256	1	16	16	1	1×1	1	1.455 to 1.939	6.000 to 8.000	False	19	0	1	22	4
19.00	8	2	1	2	256	1	16	16	1	2×1	2	3.879 to 6.000	>8.000 to 12.375	False	19	0	0	11	8
19.00	8	2	1	2	256	1	16	16	1	2×1	2	2.909 to 3.879	6.000 to 8.000	False	19	0	1	22	8
19.00	8	2	1	2	256	1	16	16	1	4×1	4	5.818 to 6.000	6.000 to 6.188	False	19	0	1	22	16
19.10	8	2	2	4	128	1	16	16	0	1×1	1	1.939 to 6.000	>8.000 to 24.750	False	19	1	0	11	4
19.10	8	2	2	4	128	1	16	16	0	1×1	1	1.455 to 1.939	6.000 to 8.000	False	19	1	1	22	4
19.10	8	2	2	4	128	1	16	16	0	2×1	2	3.879 to 6.000	>8.000 to 12.375	False	19	1	0	11	8
19.10	8	2	2	4	128	1	16	16	0	2×1	2	2.909 to 3.879	6.000 to 8.000	False	19	1	1	22	8
19.10	8	2	2	4	128	1	16	16	0	4×1	4	5.818 to 6.000	6.000 to 6.188	False	19	1	1	22	16
28.00	8	2	3	8	256	3	12	12	0	1×1	1	2.586 to 6.000	>8.000 to 18.562	True	28	0	0	33	16
28.00	8	2	3	8	256	3	12	12	0	2×1	2	5.172 to 6.000	>8.000 to 9.281	True	28	0	0	33	32
18.00	8	4	1	1	256	1	16	16	1	1×1	1	1.450 to 3.000	11.963 to 24.750	False	18	0	0	11	2
18.00	8	4	1	1	256	1	16	16	1	2×1	2	1.939 to 6.000	>8.000 to 24.750	False	18	0	0	11	4
18.00	8	4	1	1	256	1	16	16	1	2×1	2	1.455 to 1.939	6.000 to 8.000	False	18	0	1	22	4
18.00	8	4	1	1	256	1	16	16	1	3×1	3	2.909 to 6.000	>8.000 to 16.500	False	18	0	0	11	6
18.00	8	4	1	1	256	1	16	16	1	4×1	4	3.879 to 6.000	>8.000 to 12.375	False	18	0	0	11	8
18.00	8	4	1	1	256	1	16	16	1	4×1	4	2.909 to 3.879	6.000 to 8.000	False	18	0	1	22	8
18.00	8	4	1	1	256	1	16	16	1	6×1	6	5.818 to 6.000	>8.000 to 8.250	False	18	0	0	11	12
18.00	8	4	1	1	256	1	16	16	1	2×4, 4×2	8	5.818 to 6.000	6.000 to 6.188	False	18	0	1	22	16
18.10	8	4	2	2	128	1	16	16	0	1×1	1	1.450 to 3.000	11.963 to 24.750	False	18	1	0	11	2
18.10	8	4	2	2	128	1	16	16	0	2×1	2	1.939 to 6.000	>8.000 to 24.750	False	18	1	0	11	4
18.10	8	4	2	2	128	1	16	16	0	2×1	2	1.455 to 1.939	6.000 to 8.000	False	18	1	1	22	4
18.10	8	4	2	2	128	1	16	16	0	3×1	3	2.909 to 6.000	>8.000 to 16.500	False	18	1	0	11	6
18.10	8	4	2	2	128	1	16	16	0	4×1	4	3.879 to 6.000	>8.000 to 12.375	False	18	1	0	11	8
18.10	8	4	2	2	128	1	16	16	0	4×1	4	2.909 to 3.879	6.000 to 8.000	False	18	1	1	22	8
18.10	8	4	2	2	128	1	16	16	0	6×1	6	5.818 to 6.000	>8.000 to 8.250	False	18	1	0	11	12
18.10	8	4	2	2	128	1	16	16	0	2×4, 4×2	8	5.818 to 6.000	6.000 to 6.188	False	18	1	1	22	16
27.00	8	4	3	4	256	3	12	12	0	1×1	1	1.450 to 4.000	8.972 to 24.750	True	27	0	0	33	8
27.00	8	4	3	4	256	3	12	12	0	2×1	2	2.586 to 6.000	>8.000 to 18.562	True	27	0	0	33	16
27.00	8	4	3	4	256	3	12	12	0	4×1	4	5.172 to 6.000	>8.000 to 9.281	True	27	0	0	33	32
32.01	8	4	3	2	256	3	16	24	0	2×1	2	1.450 to 4.000	8.972 to 24.750	True	N/A	N/A	0	33	8

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Table 76. ADC Path Supported JESD204C Modes (L = 8)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[xi] [viii] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677 Bits[3:0][3])	Register 0x0728	Register 0x00CA, Bits[5:0]
32.01	8	4	3	2	256	3	16	24	0	4×1	4	2.586 to 6.000	>8.000 to 18.562	True	N/A	N/A	0	33	16
32.01	8	4	3	2	256	3	16	24	0	6×2	12	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
27.10	8	4	6	8	128	3	12	12	0	2×1	2	2.586 to 6.000	>8.000 to 18.562	True	27	1	0	33	16
27.10	8	4	6	8	128	3	12	12	0	4×1	4	5.172 to 6.000	>8.000 to 9.281	True	27	1	0	33	32
27.10	8	4	6	8	128	3	12	12	0	1×1	1	1.450 to 4.000	8.972 to 24.750	True	27	1	0	33	8
32.11	8	4	6	4	128	3	16	24	0	4×1	4	2.586 to 6.000	>8.000 to 18.562	True	N/A	N/A	0	33	16
32.11	8	4	6	4	128	3	16	24	0	6×2	12	5.818 to 6.000	6.000 to 6.188	False	N/A	N/A	1	22	16
32.11	8	4	6	4	128	3	24	24	0	2×1	2	1.450 to 4.000	8.972 to 24.750	True	N/A	N/A	0	33	8
16.00	8	8	2	1	128	1	16	16	0	1×1	1	1.450 to 1.500	23.925 to 24.750	False	16	0	0	11	1
16.00	8	8	2	1	128	1	16	16	0	2×1	2	1.450 to 3.000	11.963 to 24.750	False	16	0	0	11	2
16.00	8	8	2	1	128	1	16	16	0	3×1	3	1.455 to 4.000	>8.000 to 24.750	False	16	0	0	11	3
16.00	8	8	2	1	128	1	16	16	0	3×1	3	1.450 to 1.455	7.975 to 8.000	True	16	0	1	22	3
16.00	8	8	2	1	128	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	16	0	0	11	4
16.00	8	8	2	1	128	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	16	0	1	22	4
16.00	8	8	2	1	128	1	16	16	0	3×2, 6×1, 2×3	6	2.909 to 6.000	>8.000 to 16.500	False	16	0	0	11	6
16.00	8	8	2	1	128	1	16	16	0	4×2, 2×4	8	3.879 to 6.000	>8.000 to 12.375	False	16	0	0	11	8
16.00	8	8	2	1	128	1	16	16	0	4×2, 2×4	8	2.909 to 3.879	6.000 to 8.000	False	16	0	1	22	8
16.00	8	8	2	1	128	1	16	16	0	6×2	12	5.818 to 6.000	>8.000 to 8.250	False	16	0	0	11	12
16.00	8	8	2	1	128	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	16	0	1	22	16
26.00	8	8	3	2	256	3	12	12	0	1×1	1	1.450 to 2.000	17.944 to 24.750	True	26	0	0	33	4
26.00	8	8	3	2	256	3	12	12	0	2×1	2	1.450 to 4.000	8.972 to 24.750	True	26	0	0	33	8
26.00	8	8	3	2	256	3	12	12	0	3×1	3	1.939 to 6.000	>8.000 to 24.750	False	26	0	0	11	4
26.00	8	8	3	2	256	3	12	12	0	3×1	3	1.455 to 1.939	6.000 to 8.000	False	26	0	1	22	4
26.00	8	8	3	2	256	3	12	12	0	4×1	4	2.586 to 6.000	>8.000 to 18.562	True	26	0	0	33	16
26.00	8	8	3	2	256	3	12	12	0	6×1	6	3.879 to 6.000	>8.000 to 12.375	False	26	0	0	11	8
26.00	8	8	3	2	256	3	12	12	0	6×1	6	2.909 to 3.879	6.000 to 8.000	False	26	0	1	22	8
32.00	8	8	3	1	256	3	16	24	0	2×1	2	1.450 to 2.000	17.944 to 24.750	True	32	0	0	33	4
32.00	8	8	3	1	256	3	16	24	0	3×1	3	1.450 to 3.000	11.963 to 24.750	False	32	0	0	11	2
32.00	8	8	3	1	256	3	16	24	0	4×1	4	1.450 to 4.000	8.972 to 24.750	True	32	0	0	33	8
32.00	8	8	3	1	256	3	16	24	0	6×1	6	1.939 to 6.000	>8.000 to 24.750	False	32	0	0	11	4
32.00	8	8	3	1	256	3	16	24	0	6×1	6	1.455 to 1.939	6.000 to 8.000	False	32	0	1	22	4
32.00	8	8	3	1	256	3	16	24	0	4×3, 6×2	12	3.879 to 6.000	>8.000 to 12.375	False	32	0	0	11	8

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Table 76. ADC Path Supported JESD204C Modes (L = 8)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[xi] [viii] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677 Bits[3:0][3])	Register 0x0728	Register 0x00CA, Bits[5:0]
32.00	8	8	3	1	256	3	16	24	0	4×3, 6×2	12	2.909 to 3.879	6.000 to 8.000	False	32	0	1	22	8
32.00	8	8	3	1	256	3	16	24	0	3×3	9	2.909 to 6.000	>8.000 to 16.500	False	32	0	0	11	6
16.10	8	8	4	2	64	1	16	16	0	1×1	1	1.450 to 1.500	23.925 to 24.750	False	16	1	0	11	1
16.10	8	8	4	2	64	1	16	16	0	2×1	2	1.450 to 3.000	11.963 to 24.750	False	16	1	0	11	2
16.10	8	8	4	2	64	1	16	16	0	3×1	3	1.455 to 4.000	>8.000 to 24.750	False	16	1	0	11	3
16.10	8	8	4	2	64	1	16	16	0	3×1	3	1.450 to 1.455	7.975 to 8.000	True	16	1	1	22	3
16.10	8	8	4	2	64	1	16	16	0	2×2, 4×1	4	1.939 to 6.000	>8.000 to 24.750	False	16	1	0	11	4
16.10	8	8	4	2	64	1	16	16	0	2×2, 4×1	4	1.455 to 1.939	6.000 to 8.000	False	16	1	1	22	4
16.10	8	8	4	2	64	1	16	16	0	3×2, 6×1	6	2.909 to 6.000	>8.000 to 16.500	False	16	1	0	11	6
16.10	8	8	4	2	64	1	16	16	0	4×2, 2×4	8	3.879 to 6.000	>8.000 to 12.375	False	16	1	0	11	8
16.10	8	8	4	2	64	1	16	16	0	4×2, 2×4	8	2.909 to 3.879	6.000 to 8.000	False	16	1	1	22	8
16.10	8	8	4	2	64	1	16	16	0	6×2	12	5.818 to 6.000	>8.000 to 8.250	False	16	1	0	11	12
16.10	8	8	4	2	64	1	16	16	0	4×4	16	5.818 to 6.000	6.000 to 6.188	False	16	1	1	22	16
26.10	8	8	6	4	128	3	12	12	0	3×1	3	1.939 to 6.000	>8.000 to 24.750	False	26	1	0	11	4
26.10	8	8	6	4	128	3	12	12	0	3×1	3	1.455 to 1.939	6.000 to 8.000	False	26	1	1	22	4
26.10	8	8	6	4	128	3	12	12	0	1×1	1	1.450 to 2.000	17.944 to 24.750	True	26	1	0	33	4
26.10	8	8	6	4	128	3	12	12	0	2×1	2	1.450 to 4.000	8.972 to 24.750	True	26	1	0	33	8
26.10	8	8	6	4	128	3	12	12	0	4×1	4	2.586 to 6.000	>8.000 to 18.562	True	26	1	0	33	16
26.10	8	8	6	4	128	3	12	12	0	6×1	6	3.879 to 6.000	>8.000 to 12.375	False	26	1	0	11	8
26.10	8	8	6	4	128	3	12	12	0	6×1	6	2.909 to 3.879	6.000 to 8.000	False	26	1	1	22	8
32.10	8	8	6	2	128	3	16	24	0	3×1	3	1.450 to 3.000	11.963 to 24.750	False	32	1	0	11	2
32.10	8	8	6	2	128	3	16	24	0	2×1	2	1.450 to 2.000	17.944 to 24.750	True	32	1	0	33	4
32.10	8	8	6	2	128	3	16	24	0	4×1	4	1.450 to 4.000	8.972 to 24.750	True	32	1	0	33	8
32.10	8	8	6	2	128	3	16	24	0	6×1	6	1.939 to 6.000	>8.000 to 24.750	False	32	1	0	11	4
32.10	8	8	6	2	128	3	16	24	0	6×1	6	1.455 to 1.939	6.000 to 8.000	False	32	1	1	22	4
32.10	8	8	6	2	128	3	16	24	0	4×3, 6×2	12	3.879 to 6.000	>8.000 to 12.375	False	32	1	0	11	8
32.10	8	8	6	2	128	3	16	24	0	4×3, 6×2	12	2.909 to 3.879	6.000 to 8.000	False	32	1	1	22	8
32.10	8	8	6	2	128	3	16	24	0	3×3	9	2.909 to 6.000	>8.000 to 16.500	False	32	1	0	11	6
17.00	8	16	4	1	64	1	16	16	0	2×2	4	1.450 to 3.000	11.963 to 24.750	False	17	0	0	11	2
17.00	8	16	4	1	64	1	16	16	0	3×2, 2×3	6	1.455 to 4.000	>8.000 to 24.750	False	17	0	0	11	3
17.00	8	16	4	1	64	1	16	16	0	3×2, 2×3	6	1.450 to 1.455	7.975 to 8.000	True	17	0	1	22	3
17.00	8	16	4	1	64	1	16	16	0	4×2	8	1.939 to 6.000	>8.000 to 24.750	False	17	0	0	11	4
17.00	8	16	4	1	64	1	16	16	0	4×2	8	1.455 to 1.939	6.000 to 8.000	False	17	0	1	22	4
17.00	8	16	4	1	64	1	16	16	0	4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	17	0	0	11	6

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Table 76. ADC Path Supported JESD204C Modes (L = 8)[1] (Continued)

JESD204C Mode Number	L	M	F	S	K	E	N	NP	HD	Coarse × Fine Decimation DCM	Total DCM	FADC Range (GSPS)	Lane Rate Range (Gbps)	JTX Async	JTX_MODE[2] (Register 0x0702, Bits[5:0])	JTX_MODE_S_SEL[xi] [viii] (Register 0x0702, Bits[7:6])	Register 0x0670 to Register 0x0677 Bits[3:0][3]	Register 0x0728	Register 0x00CA, Bits[5:0]
17.00	8	16	4	1	64	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	17	0	0	11	8
17.00	8	16	4	1	64	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	17	0	1	22	8
17.00	8	16	4	1	64	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	17	0	0	11	9
17.00	8	16	4	1	64	1	16	16	0	6×3	18	3.273 to 4.364	6.000 to 8.000	True	17	0	1	22	9
17.00	8	16	4	1	64	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	17	0	0	11	12
17.00	8	16	4	1	64	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	17	0	1	22	16
17.10	8	16	8	2	32	1	16	16	0	2×2	4	1.450 to 3.000	11.963 to 24.750	False	17	1	0	11	2
17.10	8	16	8	2	32	1	16	16	0	3×2	6	1.455 to 4.000	>8.000 to 24.750	False	17	1	0	11	3
17.10	8	16	8	2	32	1	16	16	0	3×2	6	1.450 to 1.455	7.975 to 8.000	True	17	1	1	22	3
17.10	8	16	8	2	32	1	16	16	0	4×2	8	1.939 to 6.000	>8.000 to 24.750	False	17	1	0	11	4
17.10	8	16	8	2	32	1	16	16	0	4×2	8	1.455 to 1.939	6.000 to 8.000	False	17	1	1	22	4
17.10	8	16	8	2	32	1	16	16	0	4×3, 6×2	12	2.909 to 6.000	>8.000 to 16.500	False	17	1	0	11	6
17.10	8	16	8	2	32	1	16	16	0	4×4	16	3.879 to 6.000	>8.000 to 12.375	False	17	1	0	11	8
17.10	8	16	8	2	32	1	16	16	0	4×4	16	2.909 to 3.879	6.000 to 8.000	False	17	1	1	22	8
17.10	8	16	8	2	32	1	16	16	0	6×3	18	4.364 to 6.000	>8.000 to 11.000	False	17	1	0	11	9
17.10	8	16	8	2	32	1	16	16	0	6×3	18	3.273 to 4.364	6.000 to 8.000	True	17	1	1	22	9
17.10	8	16	8	2	32	1	16	16	0	4×6, 6×4	24	5.818 to 6.000	>8.000 to 8.250	False	17	1	0	11	12
17.10	8	16	8	2	32	1	16	16	0	4×8	32	5.818 to 6.000	6.000 to 6.188	False	17	1	1	22	16

1 N/A means not applicable.

2 JTX_MODE and JTX_MODE_S_SEL bit fields are not supported on AD9081, AD9082, AD9207, and AD9209. The JESD204 parameters for these modes must be programmed individually. Modes with N/A are not supported by AD9986 and AD9988.

3 If in dual link mode and lane rates per link are different, then set these bits per lane rate according to the bit field description in Table 42. This column applies to MxFE and TxFE devices operating the receive path only and the AD9207 and AD9209. For Transmit and receive path operation, refer to the bit field descriptions for these registers in Table 61 to determine the appropriate setting.

4 Modes with N/A in the JTX_MODE columns are not supported by AD9081-4D4AB, AD9986, and AD9988.

ADC Path Supported JESD204B Mode Selection Registers

Table 77. ADC Path Supported JESD204B Mode Selection Registers

Address	Bits	Bit Name	Description	Reset	Access
0x0611	[5:4]	JTX_LINK_204C_SEL1	Set these bits to 2b'00 to select 8-bit/10-bit Link Layer (204B). Set these bits to 2b'01 to select 64-bit/66-bit Link Layer (204C).	0	R/W
0x063D	7	JTX_SCR_CFG	JESD204B/C Transmitter Scrambler Enable. 0 = scrambling disabled. 1 = scrambling enabled.	0	R/W
	[4:0]	JTX_L_CFG	JESD204B/C Transmitter Number of Lanes per Link + 1. 0 = 1 lane. 1 = 2 lanes. Values of 4, 6 and ≥8 are not valid.	0	R/W
0x063E	[7:0]	JTX_F_CFG	JESD204B/C Transmitter Number of Octets per Frame (F = JESD204B/C Transmitter F Configuration + 1). 0 = 1 octet. 1 = 2 octets. 2 = 3 octets.	0	R/W

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Table 77. ADC Path Supported JESD204B Mode Selection Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
			3 = 4 octets. 5 = 6 octets.		
			7 = 8 octets. 11 = 12 octets. 15 = 16 octets. 23 = 24 octets. All other values are invalid.		
0x063F	[7:0]	JTX_K_CFG	JTX Number of Frames per Multiframe (K = JTX K Configuration + 1). Only values where F×K is divisible by 4 can be used.	0	R/W
0x0640	[7:0]	JTX_M_CFG	JTX Number of Virtual Converters per Link (M = JTX M Configuration + 1). 0 = 1 virtual converter. 1 = 2 virtual converters. 2 = 3 virtual converters. 3 = 4 virtual converters. 5 = 6 virtual converters. 7 = 8 virtual converters. 11 = 12 virtual converters. 15 = 16 virtual converters. All other values are invalid.	0	R/W
0x0641	[7:6]	JTX_CS_CFG	Number of Control Bits (CS) per Sample. 0 = no control bits (CS = 0). 1 = 1 control bit (CS = 1), Control Bit 2 only. 2 = 2 control bits (CS = 2), Control Bit 2 and Control Bit 1 only. 3 = 3 control bits (CS = 3), all control bits (Control Bit 2, Control Bit 1, and Control Bit 0).	0	R/W
	[4:0]	JTX_N_CFG	ADC Converter Resolution (N = JTX N Configuration + 1). 7 = 8-bit resolution 8 = 9-bit resolution 9 = 10-bit resolution 10 = 11-bit resolution 11 = 12-bit resolution. 12 = 13-bit resolution 13 = 14-bit resolution 14 = 15-bit resolution 15 = 16-bit resolution. All other values are invalid.	0	R/W
0x0642	[7:5]	JTX_SUBCLASSV_CFG	Subclass Support. 0 = Subclass 0. 1 = Subclass 1. All other values are invalid.	0	R/W
	[4:0]	JTX_NP_CFG	ADC Number of Bits per Sample(N'). 11 = 12-bits. 15 = 16-bits. 23 = 24-bits. All other values are invalid.	0	R/W
0x0643	[7:5]	JTX_JESDV_CFG	Always set these bits to 1.	0	R/W
	[4:0]	JTX_S_CFG	Samples per Converter Frame Cycle (S = JESD204B/C Transmitter S Configuration + 1). 0 = 1 samples per converter. 1 = 2 samples per converter.	0	R/W

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Table 77. ADC Path Supported JESD204B Mode Selection Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
			3 = 4 samples per converter. 7 = 8 samples per converter. All other values are invalid.		
0x0644	7	JTX_HD_CFG	Reflects the status of the JESD204 high density (HD) mode (indicates when converter samples are split across multiple lanes). This is only used to populate the HD field in the link configuration parameters that are sent across the link during the 2nd multiframe of ILAS when the 8-bit/10-bit link layer is used. HD = 1 for cases where M×S < L. 0 = Samples are not split across lanes 1 = Samples are split across 2 lanes	0	R/W
0x0702	7:6	JTX_MODE_S_SEL	Select the S value for the JESD mode enabled by JTX_QUICK_CFG. See JTX JESD204B/C mode tables. Not valid for AD9081, AD9082, AD9207, and AD9209	0	R/W
	5:0	JTX_MODE	Quick configuration setting for JESD204B/C transmitter parameters according to the JESD204B_Mode and JESD204C_Mode numbers in Table 65 through Table 76 in the JESD204B/C Transmitter Mode Tables section. Not valid for AD9081, AD9082, AD9207, and AD9209.	0	R/W

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JESD204B/C RECEIVER FUNCTIONAL OVERVIEW

Eight JESD204B/C receive data lanes (JESD204B/C receiver) are available to receive the input sample data sent to the device. The eight JESD204B/C lanes can be combined to form either one (single-link) or two (dual-link) identical links.

Each link can provide data to an individual datapath, each with a unique set of channelizers. Both single-link and dual-link JESD204B/ JESD204C modes align the individual (local) clocks to the same system reference (SYSREF±) and device clock CLKIN±) signals.

When operating with the 8-bit/10-bit link layer (JESD204B enabled) the SYNC0OUTB± and SYNC1OUTB± signals are specific to the respective JESD204B link, and in dual-link mode (Register 0x0596, Bit 3 = 1) the two links can operate independently from one another. For example, one link can be powered down while the other link is running. If the 8-bit/10-bit link layer option is selected, the link operation complies to both the JESD204B and JESD204C standards and the link lane rates can be between 1.5 Gbps and 15.5 Gbps.

Similarly, the two links can also operate independently from one another when operating with the 64-bit/66-bit link layer (JESD204C enabled) in dual-link mode. If the 64-bit/66-bit link layer option is selected, the link operation complies to the JESD204C standard, including the new synchronization process (SYNCxOUTB± pins are not used) and the link lane rates can be between 6 Gbps and 24.75 Gbps.

The JESD204B/C serial interface hardware is grouped into three layers: the physical layer, the data link layer, and the transport layer. The functional block diagram of the JESD204B/ JESD204C device receiver is shown in Figure 61.

JESD204B/C Receiver Clock Relationships

The following clock rates are used throughout the rest of the JESD204B/C section. The relationship between any of the clocks can be derived from the following equations:

- Data Rate = DAC Rate/ Total Interpolation
- PCLK Factor = 4/F

For 8-bit/10-bit encoding:

- Lane Rate = (M/L)×NP×(10/8)×Data Rate
- PCLK Rate = Lane Rate/40

For 64-bit/66-bit encoding:

- Lane Rate = (M/L)×NP×(66/64)×Data Rate
- PCLK Rate = Lane Rate/66

The data rate is the rate at which data is sent to the JRx from the JTx, in samples per second (sps).

The lane rate, or the bitrate, is the rate at which sample bits are sent across the physical lanes (SERDINx±).

PCLK rate is the rate of the processing clock (PCLK) that is used for the quad-byte decoder.

M is the JESD204B/C parameter for converters per link, which is the effective number of converters, or virtual converters, as seen by the JESD204B/C interface (not necessarily equal to the number of DAC cores).

L is the JESD204B/C parameter for lanes per link.

F is the JESD204B/C parameter for octets per frame per lane.

NP is the JESD204B/C parameter for the total number of bits per sample.

Physical Layer

JESD204B/C data is input to the device at the physical interface (referred to as the deserializer) via the SERDINx± differential input pins. The physical layer has eight identical channels. Each channel consists of the termination, an equalizer, a clock and data recovery (CDR) circuit, and a demultiplexer function, as shown in Figure 62.

To optimize power and performance of the JESD204B/C receiver PHY, several DESER_CBUS registers must be written. These register locations and settings are described in the JESD204B/C Receiver PHY Register Writes for Proper Operation section.

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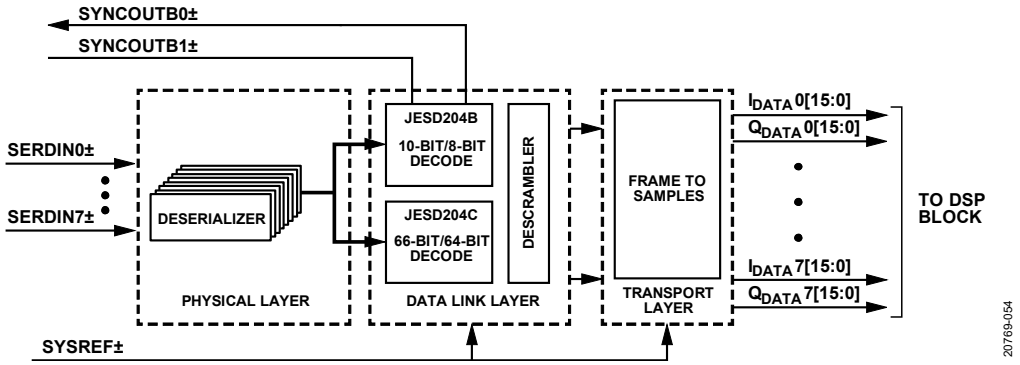

Figure 61. Functional Block Diagram of the JESD204B/C Receiver

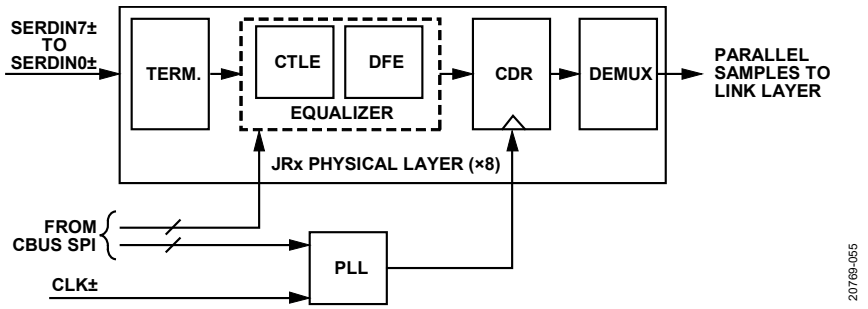

Figure 62. Deserializer Block Diagram

Power Down Unused PHY Lanes

Any unused physical lanes (SERDINx±) that are left enabled consume extra power. Unused lanes may be powered off by writing a 1 to the corresponding bit of the PHY_PD register (Register 0x0401). The PHY_PD register provides bit per lane control of the PHY power and is described in Table 82.

Inverting PHY Lane Data

It may be convenient for PCB layout purposes to swap the polarity on some of the differential SERDINx± inputs, which is equivalent to swapping the SERDINx+ with the SERDINx- in the PCB layout for a particular lane. The bit per lane control for this is in the JRX_DES_DATA-INV_CH[7:0] (Register 0x0419) bits and is described in Table 82.

Equalizer (CTLE and DFE)

There are two stages to the equalizer in the device. The first stage is a CTLE. The CTLE provides a filter with the inverse frequency response of the PCB channel that conditions the signal and improves the performance of DFE that follows. Note that the DFE stage is only activated at lane rates above 16 Gbps.

To optimize the filter response of the CTLE, several registers must be written. The register settings depend on the amount of insertion loss in the PCB channel and the lane rate. The register locations and settings for lane rates 16 Gbps and below are described in Table 78 If operating at lane rates above 16 Gbps, only one CTLE register needs to be written with the value depending on the insertion loss of the channel, as described in Table 79. The other CTLE / DFE settings are automatically set by device firmware.

The registers described in Table 78 and Table 79 are located in the deserializer control bus (DESER_CBUS) register space and each register setting requires a sequence of register writes to the main register map. Note that each lane deserializer is individually controlled using a write strobe. Register 0x0406 to Register 0x0408 of the main register map provides access to the DESER_CBUS registers that are detailed in Table 78 and Table 79. To access these registers, take the following steps:

1. Write the value of the CBUS_ADDR_DES_RC register (Register 0x0406, Bits[7:0]) to the appropriate DESER_CBUS register address, as described in Table 78.

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2. Write the value of the CBUS_WDATA_DES_RC register (Register 0x0408, Bits[7:0]) to the appropriate value, as described in Table 78 based on the PCB trace insertion loss (IL)
3. For each deserializer lane that requires a value written to Register 0x0408, set the appropriate bits in the CBUS_ WSTROBE_DES_RC_CH register (Register 0x0407, Bits[7:0]) to 1.
4. Write the value of the CBUS_WSTROBE_DES_RC_CH register (Register 0x0407, Bits[7:0]) back to 0x00 to reset the strobe.

After executing the last DESER_CBUS write, the values must be latched in by toggling Bit 4 of the DESER_CBUS register 0x0F5 using the same process described above. Refer to the JESD204B/C Receiver Physical Layer API section for information on API support for configuring the CTLE.

Table 78. CTLE Registers Settings for Lane Rate ≤16 Gbps

			Settings		
Register Map	Address	Bits	IL[1] 10	IL > 10	Reset
DESER_CBUS	0x04	[7:0]	0x66	0x66	0xA6
DESER_CBUS	0x05	[7:0]	0x08	0x08	0x00
DESER_CBUS	0x06	[7:0]	0x03	0x03	0x00
DESER_CBUS	0x07	[7:0]	0x65	0x63	0x0

[1] IL = insertion loss.

Table 79. CTLE Registers Settings for Lane Rate >16 Gbps

			Setting per Channel IL[1] Range		
Register Map	Address	Bits	0 dB to 6 dB	4 dB to 10 dB	8 dB to 20 dB
DESER_CBUS	0xFD	[3:0]	0x3	0x1	0x0

[1] IL = insertion loss.

JESD204C Receiver DFE Operation Above 16 Gbps

If operating at lane rates above 16Gbps, the decision feedback equalization (DFE) is activated and a calibration routine is required to achieve optimal performance from the PHY. Internal circuitry does most of the heavy lifting of the calibration, but some user interaction is required as detailed in the following procedure. This PHY calibration routine has been validated with input amplitudes in the 550 mV to 900 mV range. For the most robust operation (maximum margin), adjust the amplitude of the logic device's JESD204C transmitter to achieve a 650 +/- 25 mV input amplitude. Also note that the PHY calibration relies on a minimal amount of slewing of the input signal to detect the eye shape, and make CTLE and DFE adjustments accordingly. Therefore, the best practice is to design the JESD204C pcb channels with at least 3 dB of insertion loss.

1. Confirm that the calibration state machine is idle by reading RX_RESET_STATE (Register 0x21C1, Bit 7). If RX_RESET_STATE = 0b'0, proceed to step 2. Otherwise, wait until RX_RESET_STATE = 0b'0.
2. Reset calibration state machine by setting RX_RESET_STATE to 0b'1.
   - Wait for RX_RESET_STATE to self clear.
3. Identify lanes on which calibration is to run (all active lanes in the JESD204B/C mode) in the RX_RUN_CAL_MASK register (0x21C4).
4. Set register 0x21C2 to 0x31 to ensure proper operation of the calibration state machine.
5. Start calibration by setting rx_fg_cal_only_run and RX_BG_CAL_RUN (bits 4:3 of register 0x21C1) to 2b'11.
   - Wait for RX_BG_CAL_RUN to self clear.
   - Wait for RX_AT_IDLE = 1 state (Register 0x21DD, Bit 0).
6. Place the calibration state machine in adaption mode by setting RX_FG_CAL_ONLY_RUN to 0b'0 and then RX_BG_CAL_RUN to 0b'1.

After performing the calibration, the DFE stage of the equalizer is fully adaptable and does not require further intervention in the form of register writes. Note that while the calibration routine is running, users may not access the DESER_CBUS or the calibration data is corrupted

Refer to the JESD204B/C Receiver Physical Layer API section for information on API support for calibrating the JESD204B/C receiver PHY.

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CDR

The deserializer is equipped with a CDR circuit. Instead of recovering the clock from the serial lanes, the CDR recovers the clocks from the SERDES PLL. The SERDES PLL uses the PCLK as a reference and the PCLK is derived from the DAC clock. The user must ensure that the transmitter clock is frequency locked to the device clock provided to the CLKINP and CLKINN inputs.

The CDR circuit synchronizes the phase used to sample the data on each serial lane independently. This independent phase adjustment per serial interface ensures accurate data sampling and simplifies the implementation of multiple serial interfaces on a PCB.

JESD204B/C Receiver PHY Register Writes for Proper Operation

Several PHY registers must be written to optimize performance of the JESD204B/C receiver PHY depending on the lane rate. These register writes are described in Table 80. Because these registers are part of the deserializer control bus (DESER_CBUS), use Register 0x0406 to Register 0x0408 of the main register map to make the appropriate register writes using the following steps:

1. Write the value of the CBUS_ADDR_DES_RC register (Register 0x0406, Bits[7:0]) to the appropriate DESER_CBUS register address, as described in Table 80.
2. Write the value of the CBUS_WDATA_DES_RC register (Register 0x0408, Bits[7:0]) to the appropriate value, as described in Table 80 based on the operating lane rate of the link.
3. For each deserializer lane that requires the value written to Register 0x0407, set the appropriate bits in the CBUS_WSTROBE_DES_RC_CH register (Register 0x0407, Bits[7:0]) to 1.
4. Write the value of the CBUS_wstrobe_DES_RC_CH register (Register 0x0408, Bits[7:0]) back to 0x00 to reset the strobe.

Table 80. Required DESER_CBUS Registers and Settings to Write

Address	Lane Rate (Gbps)			Reset
	1.5 to 8.0	8.0 to 16	16 to 24.75	
0x08	0x02	0x02	0x02	0x01
0x15	0x01	0x00	0x01	0x00
0x50	0x04	0x04	0x04	0x00
0xbc	0x80	0x80	0x00	0x00
0xbe	0x80	0x80	0x00	0x00
0xc0	0xff	0xff	0x00	0x00
0xcd	0x40	0x00	0x00	0x00
0xd2	0xf0	0xf0	0x00	0x00
0xd3	0xee	0xee	0x00	0x00
0xdc	0xee	0xee	0x00	0x00
0xe2	0xf0	0xF0	0x00	0x00
0xe3	0xff	0xee	0x00	0x00
0xec	0xff	0xee	0x00	0x00
0xf4	0x01	0x05	0x05	0x05

JESD204B/C Receiver Physical Layer API

The device API supports many JESD204B/C transmitter PHY configuration functions. These function calls are briefly described in Table 81. Note that many settings and functions use the lane rate as one of the variables. In the API, when the PHY operates at lane rates below 8 Gbps, PHY operation is referred to as full rate mode. Between 8 Gbps and 16 Gbps, it is referred to as half rate mode and at lane rates above 16 Gbps it is called quarter rate mode.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Table 81. JESD204B/C Receiver PHY API Functions

Function Call	<C file>	Description
adi_adxxxx_jesd_rx_startup_des	**adi_adxxxx_jesd.c**	High level API adi_ad9xxx_jesd_rx_bring_up calls this function that sets CTLE filter settings according to lane rate
adi_txfe_jesd_rx_load_cbus_table	**adi_adxxxx_jesd.c**	Mid-level API adi_ad9xxx_jesd_rx_startup_des calls this function that sets Mandatory writes to DESER_CBUS
adi_adxxxx_jesd_rx_calibrate_204c	**adi_adxxxx_jesd.c**	Runs the PHY calibration routine
adi_adxxxx_jesd_rx_lane_invert_set	adi_adxxxx_jesd.c	Swap P/N polarities on JESD lanes
adi_adxxxx_jesd_rx_bring_up	adi_adxxxx_jesd.c	power down unused lanes

Table 82. JESD204B/C Receiver PHY and Deserializer CBUS Access Registers

Address	Bits	Bit Name	Description	Reset	Access
0x0400	0	PD_MASTER_RC	Master Power-Down for JESD204B/C Deserializers. Set this register to 0 to unmask individual PHY_PD bits.	0x1	R/W
0x0401	[7:0]	PHY_PD	PHY Power-Down. Bit per lane. For example, a setting of 0xF0 powers down Physical Lane 7 to Physical Lane 4.	0xEE	R/W
	6	JRX_LINK_LANE_INVERSE0	Swap ± Polarity on Logical Lane 0	0x0	R/W
0x0406	[7:0]	CBUS_ADDR_DES_RC	Deserializer Control Bus Address Select. This register sets the address within the deserializer CBUS to access.	0x00	R/W
0x0407	[7:0]	CBUS_WSTROBE_DES_RC_CH	Strobe signal sent to selected deserializers to load data in the CBUS_WDATA_DES_RC register, Bits[7:0]. Bits are decoded as follows: 0x00 = no strobe sent to deserializers to write data 0x01 = write strobe sent to Lane 0 deserializer to write data 0x02 = write strobe sent to Lane 1 deserializer to write data 0x03 = write strobe sent to Lane 0 and Lane 1 deserializers to write data 0x04 = write strobe sent to Lane 2 deserializer to write data 0x05 = write strobe sent to Lane 0 and Lane 2 to write data 0x06 = write strobe sent to Lane 1 and Lane 2 deserializers to write data 0x07 = write strobe sent to Lane 0 to Lane 2 deserializers to write data 0x0F = write strobe sent to Lane 0 to Lane 3 deserializers to write data 0x1F = write strobe sent to Lane 0 to Lane 4 deserializers to write data 0xFF = write strobe sent to Lane 0 to Lane 7 deserializers to write data	0x00	R/W
0x0408	[7:0]	CBUS_WDATA_DES_RC	Control Bus Data. The channel is selected using the CBUS_WSTROBE_DES_RC_CH register.	0x00	R/W
0x0419	7	JRX_DES_DATAINV_CH7	0 = SERDIN7± not inverted, 1 = SERDIN7± P/N polarity is inverted	0	R/W
	6	JRX_DES_DATAINV_CH6	0 = SERDIN6± not inverted, 1 = SERDIN6± P/N polarity is inverted	0	R/W
	5	JRX_DES_DATAINV_CH5	0 = SERDIN5± not inverted, 1 = SERDIN5± P/N polarity is inverted	0	R/W
	4	JRX_DES_DATAINV_CH4	0 = SERDIN4± not inverted, 1 = SERDIN4± P/N polarity is inverted	0	R/W
	3	JRX_DES_DATAINV_CH3	0 = SERDIN3± not inverted, 1 = SERDIN3± P/N polarity is inverted	0	R/W
	2	JRX_DES_DATAINV_CH2	0 = SERDIN2± not inverted, 1 = SERDIN2± P/N polarity is inverted	0	R/W
	1	JRX_DES_DATAINV_CH1	0 = SERDIN1± not inverted, 1 = SERDIN1± P/N polarity is inverted	0	R/W
	0	JRX_DES_DATAINV_CH0	0 = SERDIN0± not inverted, 1 = SERDIN0± P/N polarity is inverted	0	R/W
0x21C1	7	RX_RESET_STATE	1 = Reset JESD204B/C receiver calibration state machine. Bit self clears bit for acknowledgment.	0	R/W
	4	RX_FG_CAL_ONLY_RUN	When high, the rx_bg_cal_run setting causes the FG/BG cal state machine to only run through the foreground section and exit back to the idle state.	0	R/W
	3	RX_BG_CAL_RUN	When high, state machine runs through the foreground / background cal indefinitely until brought back low or the state machine is reset.	0	R/W
0x21C2	7:0	RX_SET_STATE	JESD204B/C receiver PHY calibration configuration. Must be set to 0x31 to optimize the PHY calibration.	0xF0	R/W
0x21C4	7:0	RX_RUN_CAL_MASK	Bit per lane enable for PHY calibration. 0x00 = Calibrate no lanes, 0xFF = calibrate all lanes, for example	0xFF	R/W
0x21DD	0	RX_AT_IDLE	If high, calibration state machine is currently in the idle state.	0	R/W

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Data Link Layer

Lane Crossbar Multiplexer

Each SERDINx± physical lane from the physical layer must be properly mapped to its corresponding logical lane in the data link layer. Although the physical lanes for a JESD204B/C link can be selected arbitrarily, possibly to accommodate PCB layout requirements, the logical lanes must be mapped sequentially according to the frame structure of the desired JESD204B/C mode.

The JRX_SRC_LANEx registers for each JESD204B/C lane (Lane 0 to Lane 7, Address 0x058D to Address 0x0594 allow the SERDINx± physical lanes to be mapped to the logical lanes used by the SERDES deframers. Write to each JRX_SRC_LANEx register with the number (x) of the desired SERDINx± physical lane from which the data is obtained. By default, all logical lanes use the corresponding SERDINx± physical lane as the data source. For example, by default, JRX_SRC_LANE0 = 0. Therefore, Logical Lane 0 obtains data from Physical Lane 0.

Table 83 shows the definition for each register associated with the lane crossbar multiplexer. Note that these registers are paged and need to be set for each link individually if in a dual link configuration.

JESD204B/C Receiver Crossbar Mux API Function

Configuration of the JESD204B/C receiver crossbar mux is implemented in the adi_ad9xxx_ jesd_rx_lanes_xbar_set() API function that is included in the adi_ad9xxx_jesd.c code. This low level API is called in the adi_ad9081_jesd_rx_bring_up() function which is called in the top level adi_ad9081_device_ startup_tx() API function.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Selecting the Encoding Scheme

The JESD204B/C receiver in the device DAC path can operate using the 8-bit/10-bit (JESD204B) or 64-bit/66-bit (JESD204C) link layer. To make this selection, use the JRX_DL_204B_ENABLE register bits and the JRX_DL_204C_ENABLE register bits, as shown in Table 83.

When selecting the encoding scheme, it is also necessary to select the proper parallel data width (40 vs. 66) for the data being passed out of the deserializer core using the JRX_DES_ PARDATAMODE_DES_RC[0:7] bit fields (Register 0x0457 and Register 0x0458). These bit fields are also described in Table 83.

Table 83. Lane Crossbar Multiplexer and Link Layer Selection Registers

Address	Bits	Bit Name	Description	Reset	Access
0x0402	1	PD_SYNCA_TX_RC	0 = SYNC0OUTB± is on, 1 = SYNC0OUTB± is powered down	0	R/W
	0	PD_SYNCB_TX_RC	0 = SYNC1OUTB± is on, 1 = SYNC1OUTB± is powered down	1	R/W
0x0429	0	SEL_SYNCA_MODE_RC	This bit determines the output driver mode for the SYNC0OUTB± pin operation. 0 = SYNC0OUTB± is set to CMOS output. 1 = SYNC0OUTB± is set to LVDS output.	0	R/W
0x042A	0	SEL_SYNCB_MODE_RC	This bit determines the output driver mode for the SYNC1OUTB± pin operation. 0 = SYNC1OUTB± is set to CMOS output. 1= SYNC1OUTB± is set to LVDS output.	0	R/W
	6	JRX_LINK_LANE_INVERSE0	Swap ± Polarity on Logical Lane 0.	0	R/W
0x0457	[7:6]	JRX_DES_PARDATAMODE_CH3	00 = 66 bits (204C), 10 = 40 bit (204B)	0x0	R/W
	[5:4]	JRX_DES_PARDATAMODE_CH2	00 = 66 bits (204C), 10 = 40 bit (204B)	0x0	R/W
	[3:2]	JRX_DES_PARDATAMODE_CH1	00 = 66 bits (204C), 10 = 40 bit (204B)	0x0	R/W
	[1:0]	JRX_DES_PARDATAMODE_CH0	00 = 66 bits (204C), 10 = 40 bit (204B)	0x0	R/W
0x0458	[7:6]	JRX_DES_PARDATAMODE_CH7	00 = 66 bits (204C), 10 = 40 bit (204B)	0x0	R/W
	[5:4]	JRX_DES_PARDATAMODE_CH6	00 = 66 bits (204C), 10 = 40 bit (204B)	0x0	R/W
	[3:2]	JRX_DES_PARDATAMODE_CH5	00 = 66 bits (204C), 10 = 40 bit (204B)	0x0	R/W
	[1:0]	JRX_DES_PARDATAMODE_CH4	00 = 66 bits (204C), 10 = 40 bit (204B)	0x0	R/W
0x058D	[4:0]	JRX_SRC_LANE0	Logical Lane 0 Assignment. For example, 0 = value from PHY Lane 0.	0x0	R/W
	6	JRX_LINK_LANE_INVERSE1	Swap ± Polarity on Logical Lane 1.	0	R/W
0x058E	[4:0]	JRX_SRC_LANE1	Logical Lane 1 assignment. For example, 1 = value from PHY Lane 1.	0x1	R/W

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Table 83. Lane Crossbar Multiplexer and Link Layer Selection Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
	6	JRX_LINK_LANE_INVERSE2	Swap ± Polarity on Logical Lane 2.	0	R/W
0x058F	[4:0]	JRX_SRC_LANE2	Logical Lane 2 assignment. For example, 2 = value from PHY Lane 2.	0x2	R/W
	6	JRX_LINK_LANE_INVERSE3	Swap ± Polarity on Logical Lane 3.	0	R/W
0x0590	[4:0]	JRX_SRC_LANE3	Logical Lane 3 assignment. For example, 3 = value from PHY Lane 3.	0x3	R/W
	6	JRX_LINK_LANE_INVERSE4	Swap ± Polarity on Logical Lane 4.	0	R/W
0x0591	[4:0]	JRX_SRC_LANE4	Logical Lane 4 assignment. For example, 4 = value from PHY Lane 4.	0x4	R/W
	6	JRX_LINK_LANE_INVERSE5	Swap ± Polarity on Logical Lane 5.	0	R/W
0x0592	[4:0]	JRX_SRC_LANE5	Logical Lane 5 assignment. For example, 5 = value from PHY Lane 5.	0x5	R/W
	6	JRX_LINK_LANE_INVERSE6	Swap ± Polarity on Logical Lane 6.	0	R/W
0x0593	[4:0]	JRX_SRC_LANE6	Logical Lane 6 assignment. For example, 6 = value from PHY Lane 6.	0x6	R/W
	6	JRX_LINK_LANE_INVERSE7	Swap ± Polarity on Logical Lane 7.	0	R/W
0x0594	[4:0]	JRX_SRC_LANE7	Logical Lane 7 assignment. For example, 7 = value from PHY Lane 7.	0x7	R/W
0x04C0	5	JRX_DL_204B_ENABLE	Set to 0b'1 to select 8-bit/10-bit link layer (JESD204B).	0	R/W
0x055E	7:0	JRX_DL_204C_ENABLE	Set to 0b'1 to select 64-bit/66-bit link layer (JESD204C).	0	R/W

JESD204B Receiver 8-bit/10-bit Link Layer

The 8-bit/10-bit link layer of the device accepts the deserialized data from the PHYs and deframes and descrambles the data so that data octets are presented to the transport layer to be recombined into the original data samples ahead of the DAC core.

The device can be set up to receive data from either a single link or from two links. When operating in dual-link mode, the data link layer abstracts the interface to appear as two independent JESD204B/C links to the user, each occupying a maximum of four lanes.

In either mode, all JESD204B/C interface lanes independently handle link layer communications such as CGS, frame alignment, and FS.

The 8-bit/10-bit link layer decodes 8-bit/10-bit control characters, which mark the edges of the frame and help maintain alignment between serial lanes. Each link can issue a synchronization request by setting the SYNCxOUTB± signals low. The synchronization protocol follows the JESD204B and JESD204C standards for 8-bit/ 10-bit link layer operation.

When a stream of four consecutive /K/ symbols is received on any enabled JESD204B receiver lane, the device deactivates the synchronization request by setting the SYNCxOUTB± signals high at the next internal LMFC rising edge. Then, the 8-bit/10-bit link layer waits for the transmitter to issue an ILAS.

During the ILAS, all lanes are aligned using the /A/ to /R/ character transition, as described in the JESD204B and JESD204C standards. Elastic buffers hold early arriving lane data until the alignment character of the latest lane arrives. At this point, the buffers for all lanes are released and all lanes are aligned (see Figure 63).

SYNC0OUTB± and SYNC1OUTB± Outputs

The SYNC0OUTB± and SYNC1OUTB± signals are LVDS or CMOS selectable via the SEL_SYNCA_MODE_RC and SEL_SYNCB_MODE_RC register bits (Bit 0 of Register 0x0429 and Register 0x042A, respectively). When LVDS mode is selected, use controlled impedance traces routed as 100 Ω differential impedance and 50 Ω to ground when routing these signals.

If using a dual link configuration, the sync output of the secondary link (SYNC1OUTB±) must be powered on by setting the PD_SYNCB_TX_RC bit (Register 0x0402, Bit 0) to 0 because its default state is 1 (powered down). In a dual-link mode, it is also possible to combine the SYNC0OUTB± and SYNC1OUTB± signals on a single set of pins. Setting RX_LINK0_SYNCB_COMB_EN (0x0596[5]) to 1 logically ANDs the two SYNxCOUTB signals and routes the resulting signal to the SYNC0OUTB± pins. Alternatively, setting RX_LINK1_SYNCB_COMB_EN (0x0596[6]) to 1 logically ANDs the two SYNxCOUTB signals and routes the resulting signal to the SYNC1OUTB± pins. Note that combining the sync outputs in this way means that if one of the links detects errors requiring resynchronizations, the user must reset both links instead of just the one with the error.

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Lane First In/First Out (FIFO)

The FIFOs in front of the crossbar switch and deframer adjust the phase of the incoming data to synchronize the samples sent on the high speed serial data interface with the deframer clock. The FIFO absorbs timing variations between the data source and the deframer, which allows up to two PCLK cycles of drift from the transmitter.

The LANE_FIFO_FULL register and LANE_FIFO_EMPTY register (Register 0x05AD and Register 0x05AE, respectively) can be monitored to identify whether the FIFOs are full or empty.

Lane FIFO Interrupt Request Operation (IRQ)

An aggregate lane FIFO error bit is also available as an IRQ event. Use the EN_LANE_FIFO register (Register 0x0020, Bit 5) to enable the lane FIFO error bit, and then use the IRQ_LANE_ FIFO register (Register 0x0026, Bit 5) to read back the register status and reset the IRQ signal. See the IRQ section for more information. These bits are described in Table 84.

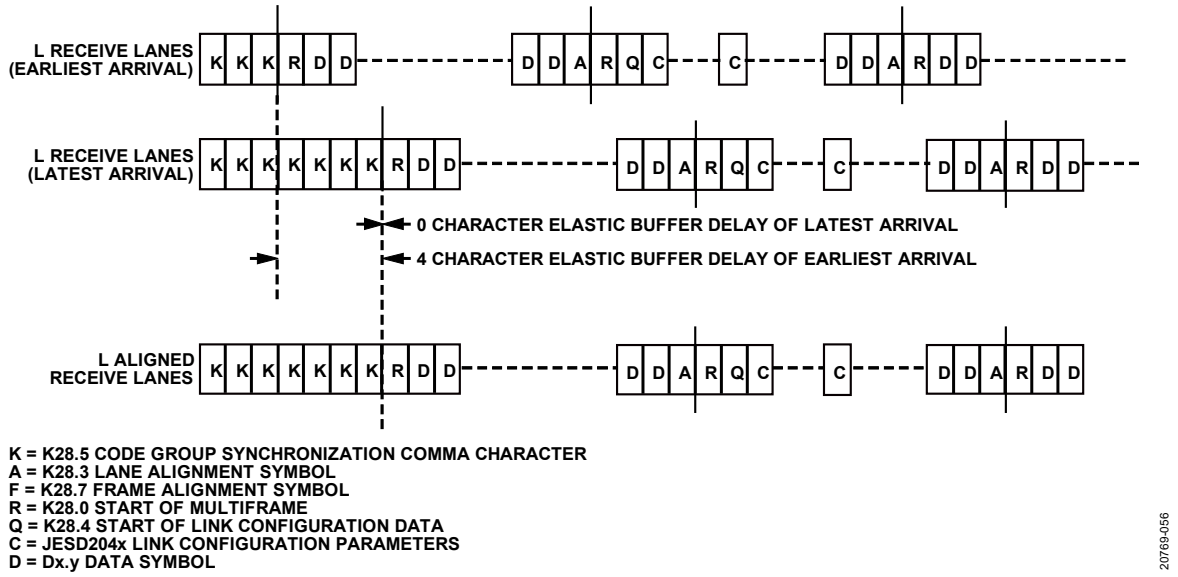

Figure 63. Lane Alignment During ILAS

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Table 84. Lane FIFO Registers

Address	Bits	Bit Name	Description	Reset	Access
0x0020	5	EN_LANE_FIFO	This bit enables lane FIFO overflow/underflow interrupt and sets the function of the IRQ_ LANE_FIFO bit.	0x0	R/W
			0 = IRQ_LANE_FIFO shows the current status of the lane FIFO error monitor (detects the FIFO full or empty conditions)		
			1 = IRQ_LANE_FIFO latches a FIFO error condition (becomes a sticky bit) if FIFO error ever occurs and enables the IRQ pin		
0x0026	5	IRQ_LANE_FIFO	If EN_LANE_FIFO_IRQ = 0, this bit shows the real time status of the FIFO error monitor.	0x0	R/W
			0 = lane FIFO is not currently in an overflow/underflow condition.		
			1 = lane FIFO is in an overflow/underflow condition.		
			If EN_LANE_FIFO_IRQ = 1, this bit indicates if a lane FIFO overflow/underflow condition has ever occurred (sticky bit) since the power-on reset or the last clearing of the bit.		
			0 = lane FIFO has not experienced an overflow/underflow condition since the last clearing of the bit.		
			1 = lane FIFO has experienced an overflow/underflow condition since the last clearing of the bit and triggered an interrupt by pulling the IRQB_x pin low (x = MUX_LANE_FIFO setting). Write any value to the IRQ_LANE_FIFO when latched to clear the register.		
0x05AD	[7:0]	LANE_FIFO_FULL	Bit x corresponds to FIFO full flag for data from SERDINx	0x0	R
0x05AE	[7:0]	LANE_FIFO_EMPTY	Bit x corresponds to FIFO empty flag for data from SERDINx	0x0	R

8-Bit/10-Bit Link Error Monitoring

Register 0x04CF to Register 0x04D6 allow the user to monitor the JESD204B link health. These registers are described in Table 86.

To monitor the status of the link synchronization process, read the status of the bit fields associated with CGS, FS, CKS, ILAS. When in the user data phase (link is synchronized, and sample data is being received by the DACs), 8-bit/10-bit errors, such as bad disparity (BD), not in table (NIT), and UEKC can be detected and counted. Read only Register 0x04EE to Register 0x04F5 contain each of these status bits on a per lane basis, as described in Table 86. Register 0x04EE provides status information for Logical Lane 0, Register 0x04EF provides status information for Logical Lane 1, and so on.

CGS, FS, CKS, ILAS and ILD Monitoring

The first phase of 8-bit/10-bit link synchronization is CGS. The JRX_204B_CGS bit (Bit 1) of the appropriate link lane register is high if the link lane received at least four K28.5 characters and passed code group synchronization.

The second phase of synchronization, FS, is achieved when the JRX_204B_FS bit (Bit 3) of the appropriate link lane register is high.

The JRX_204B_CKS bit (Bit 2)) of the appropriate link lane register is high if the CKS sent over the lane matches the sum of the JESD204B parameters sent over the lane during ILAS for the link lane. The parameters can be added either by summing the individual fields in the registers or by summing the full register values. The calculated CKS is the lower eight bits of the sum of the following fields: DID, BID, LID, SCR, L − 1, F − 1, K − 1, M − 1, N − 1, SUBCLASSV, NP − 1, JESDV, S − 1, and HD.

The JRX_204B_ILS bit (Bit 5) of the appropriate link lane register is high if the link lane passed the initial lane alignment sequence.

The JRX_204B_ILD bit (Bit 4) of the appropriate link lane register is high if the link lane has been successfully deskewed.

BD, NIT, UEKC Flags

Bit 0, Bit 6, and Bit 7 of Register 0x04EE to Register 0x04F5 are the status bits for BD, NIT, and UEK for each logical lane. A 1 on any of these bits indicates that the associated error has occurred on the respective link lane.

Checking Error Counts

The error counts can be checked for BD, NIT, and UEK errors. The error counts are on a per lane and per error type basis. A register is dedicated to each error type and lane. To check the error count, take the following steps:

1. Use Register 0x04CF to Register 0x04D6, Bits[2:0], to choose and enable which errors to monitor and write a 1 to the appropriate bit to select UEKC, BD, or NIT error monitoring for each lane, as described in Table 86. These bits are enabled by default.

2. The corresponding error counter reset bits are in Register 0x04CF to Register 0x04D6, Bits[6:4]. Write a 1 to the corresponding bit to reset that error counter.
3. Register 0x04DE to Register 0x04E5, Bits[2:0] have the terminal count hold indicator for each error counter. If this flag is enabled when the terminal error count of 0xFF is reached, the counter ceases counting and holds that value until reset. Otherwise, the counter wraps to 0x00 and continues counting. Select the desired behavior and program the corresponding register bits per lane.
4. Read the error counters. The JRX_204B_BD_CNT register, Bits[0:7], contain the BD count for Logical Lane 0 to Logical Lane 7. The JRX_204B_UEK_CNT register, Bits[0:7], contain the UEKC count for Logical Lane 0 to Logical Lane 7. The JRX_204B_NIT_CNT register, Bits[0:7], contain the NIT count for Logical Lane 0 to Logical Lane 7.

Checking for Error Count Over Threshold

To check for the error count over threshold, follow these steps:

1. Define the error counter threshold. The error counter threshold can be set to a user defined value in Register 0x04BF or left to the default value of 0xFF. When the error threshold is reached, an IRQ is generated, SYNCxOUTB± is asserted, or both occur, depending on the mask register settings. This one error threshold is used for all three types of errors (UEK, NIT, and BD). Note that if this setting is 0 and the counters enabled, the error flags always set to 1. So, the threshold value must be > 0.
2. Set the JRX_DL_204B_SYNC_ ASSERT_MASK bits (Register 0x04C0, Bits[3:1]). This bit field sets the SYNCxOUTB± assertion behavior. By default (Register 0x04C0, Bits[3:1] = 0b111) SYNCxOUTB± is asserted when any error counter of any lane is equal to the threshold. To disable SYNCxOUTB± assertion for any 8-bit/10-bit error type, set the appropriate bit(s) to 0. When setting the JRX_DL_204B_SYNC_ASSERT_MASK bits, the JRX_LINK_ MSK bits (Register 0x001D. Bits[1:0]) must be set to 2b'11.
3. Read the error count reached indicator. Register 0x04DE to Register 0x04E5, Bits[6:4], are the terminal count reached bits for each error counter. These bits are read-only and indicate that the terminal count is reached.

Monitoring Errors via SYNCxOUTB±

When one or more BD, NIT, or UEKC errors occur, the error is reported on the SYNCxOUTB± pins, per the JESD204C specification. The SYNCxOUTB± signals are asserted for exactly two frame periods when an error occurs. The width of the SYNCxOUTB± pulse can be programmed to ½, 1, or 2 PCLK cycles using the SYNCB_ERR_DUR register (Register 0x0598, Bits[7:4]). The settings to achieve a SYNCxOUTB± pulse of two frame clock cycles are given in the bit field description in Table 86.

8-Bit/10-Bit Link Error IRQs

A single interrupt is available to alert the host processor that an 8-bit/10-bit link error has occurred. These 8-bit/10-bit link error events are described in Table 85. By default, all events listed in Table 86 generate the interrupt. Bit 7 of the MUX_JESD_IRQ register (Register 0x002C, Bit 7) selects the IRQ output pin that the interrupt is routed to. To mask any or all events, write a 1 to the appropriate x_IRQ_CLR_MSK bit in Register 0x055B and Register 0x055C. If not masked, the status of each event is reflected in the respective x_IRQ_FLAG bit in Register 0x055A and Register 0x055C. If any 8-bit/10-bit link error event is not masked, the status of the IRQ is reflected in the JRX_DL_204B_IRQ_FLAG bit (Register 0x055C, Bit 0) See Table 86 for detailed descriptions of Register 0x055A to Register 0x055C.

Table 85. 8-Bit/10-Bit Link Error IRQs

Interrupt	Description
JRX_204B_CGS	CGS error has occurred
JRX_204B_FS	FS error has occurred
JRX_204B_CKS	CKS error has occurred
JRX_204B_ILS	ILAS error has occurred
JRX_204B_ILD	Interlane deskew (ILD) error has occurred
JRX_204B_UEK	UEKC error threshold reached
JRX_204B_NIT	NIT error threshold reached
JRX_204B_BDE	BD error threshold reached
JRX_204B_CMM	Configuration mismatch (CMM) error has occurred

8-Bit/10-Bit Link Error PA Protection

The device offers the feature to ramp down the DAC outputs to 0 V DC in the event of any 8-bit/10-bit link error except for CMM. The bits to use to ramp down the outputs are located at Register 0x05AA and are fully described in Table 86.

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Table 86. 8-Bit/10-Bit Error Monitoring and Lane Status Registers

Address	Bits	Bit Name	Description	Reset	Access
0x001D	1:0	JRX_LINK_MSK	DAC JRX link page mask. All registers in this table are paged so that each link 's registers are addressed independently. 2b'01 selects Link 0. 2b'10 selects Link 1 (only needed when in dual link mode).	0x3	R/W
0x02C	7	MUX_JESD_IRQ	Select which IRQ pin connects to the JESD204B sources 0 = Route IRQ signal to the IRQB_0 pin. 1 = Route IRQ signal to the IRQB_1 pin.	0x0	R/W
0x04BF	[7:0]	JRX_DL_204B_ETH	Error counter threshold value. BD, NIT and UEK errors are counted and compared to this value. A synchronization request (SYNCxOUTB± low) can be asserted if the error count exceeds this value and the error type is enabled by the JRX_DL_204B_SYN_ ASSERT_MASK bits. An IRQ may be asserted if the error count exceeds this value and the error type is enabled in Register 0x055A Bits[7:5]. This control is paged by the JRX_LINK_MSK control bit in Register 0x001D, Bits[1:0].	0xFF	R/W
0x04C0	[3:1]	JRX_DL_204B_SYN_ASSERT_MASK	This bit field sets the SYNCxOUTB± assertion behavior. Set bit to 1 to enable SYNCxOUTB± assertion for the assigned 8-bit/10-bit error type. Bit 3 = BD error. Bit 2 = NIT error. Bit 1 = UEK error.	3b'111	R/W
0x04CF to 0x04D6	6	JRX_204B_UEK_ECNT_RST[0:7]	To reset the 8-bit/10-bit error counters, toggle the appropriate bit to 1 and then back to 0. Per lane register addressing applies (Register x04CF applies to Lane0, Register 0x04D0 applies to Lane1, and so on). To enable the 8-bit/10-bit error counters, set the appropriate bit to 1. Per lane register addressing applies (Register 0x04CF applies to Lane0, Register 0x04D0 applies to Lane1, and so on).	0	R/W
	5	JRX_204B_NIT_ECNT_RST[0:7]		0	R/W
	4	JRX_204B_BD_ECNT_RST[0:7]		0	R/W
	2	JRX_204B_UEK_ECNT_ENA[0:7]		0	R/W
	1	JRX_204B_NIT_ECNT_ENA[0:7]		0	R/W
	0	JRX_204B_BD_ECNT_ENA[0:7]		0	R/W
0x04DE to 0x04E5	6	JRX_204B_UEK_ECNT_TCR[0:7]	Terminal Count Reached for 8-bit/10-bit Error Counters. Appropriate bit sets to 1 if the terminal count (0xFF) for that error is reached. Per lane register addressing applies (Register 0x04DE applies to Lane0, Register 0x04DF applies to Lane1, and so on).	0	R
	5	JRX_204B_NIT_ECNT_TCR[0:7]		0	R
	4	JRX_204B_BD_ECNT_TCR[0:7]		0	R
	2	JRX_204B_UEK_ECNT_TCH[0:7]	Terminal Count Hold Enable for 8-bit/10-bit Error Counters. Set these bits to 1 to hold counters at 0xFF until reset using Register 0x04CF to Register 0x04D6. Otherwise, the counter rolls over. Per lane register addressing applies (Register 0x04DE applies to Lane0, Register 0x04DF applies to Lane1, and so on).	0	R/W
	1	JRX_204B_NIT_ECNT_TCH[0:7]		0	R/W
	0	JRX_204B_BD_ECNT_TCH[0:7]		0	R/W
0x04EE to 0x04F5	7	JRX_204B_UEK[0:7]	UEKC errors status for lanes [L-1:0]. 1 = UEKC has occurred. Per lane register addressing for each of these bits applies (Register 0x04EE applies to Lane 0, Register 0x04EF applies to Lane 1, and so on).	0	R
	6	JRX_204B_NIT[0:7]	NIT Error Status for All Instantiated Lanes (According to the L Parameter). 1 = NIT has occurred.	0	R
	5	JRX_204B_ILS[0:7]	Initial Lane Synchronization Status for Lanes [L-1:0]. 1 = ILAS passes.	0	R
	4	JRX_204B_ILD[0:7]	ILD Status for Lanes [L-1:0]. 1 = lanes are deskewed.	0	R
	3	JRX_204B_FS[0:7]	Frame Synchronization Status for Lanes [L-1:0]. 1 = frame synchronization is achieved.	0	R
	2	JRX_204B_CKS[0:7]	Computed Checksum Status for Lanes [L-1:0]. 1 = CKS is correct.	0	R
	1	JRX_204B_CGS[0:7]	Code Group Synchronization Status for Lanes [L-1:0] 1 = CGS is achieved.	0	R
	0	JRX_204B_BDE[0:7]	BD Errors Status for Lanes [L-1:0]. 1 = BD has occurred.	0	R

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Table 86. 8-Bit/10-Bit Error Monitoring and Lane Status Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
0x04FE to 0x0505	[7:0]	JRX_204B_BD_CNT[0:7]	BD Error Counter. Per lane register addressing applies (Register 0x04FE applies to Lane 0, Register 0x04FF applies to Lane 1, and so on).	0x00	R
0x050E to 0x0515	[7:0]	JRX_204B_UEK_CNT[0:7]	UEKC Error Counter. Per lane register addressing applies (Register 0x050E applies to Lane 0, Register 0x050F applies to Lane 1, and so on).	0x00	R
0x051E to 0x0525	[7:0]	JRX_204B_NIT_CNT[0:7]	NIT Error Counter. Per lane register addressing applies (Register 0x051E applies to Lane 0, Register 0x051F applies to Lane1, and so on).	0x00	R
0x055A	7	JRX_204B_BDE_IRQ_FLAG	BD Error Flag. A BD error on any lane generates a flag.	0	R
	6	JRX_204B_NIT_IRQ_FLAG	NIT Error Flag. An NIT error on any lane generates a flag.	0	R
	5	JRX_204B_UEK_IRQ_FLAG	UEKC Error Flag. A UEKC error on any lane generates a flag.	0	R
	4	JRX_204B_ILD_IRQ_FLAG	ILD Error Flag. An ILD error on any lane generates a flag.	0	R
	3	JRX_204B_ILS_IRQ_FLAG	Initial Lane Synchronization (ILS) Error Flag. An ILS error on any lane generates a flag.	0	R
	2	JRX_204B_CKS_IRQ_FLAG	Good CKS Error Flag. A CKS error on any lane generates a flag. A CKS error occurs if the CKS of the JESD parameters calculated by the JESD204B receiver do not match the CKS of JESD204B transmitter configuration parameters that are sent over the link during ILAS.	0	R
	1	JRX_204B_FS_FLAG	FS Error flag. An FS error on any lane generates a flag.	0	R
	0	JRX_204B_CGS_FLAG	CGS Error Flag. A CGS error on any lane generates a flag.	0	R
0x055B	7	JRX_204B_BDE_IRQ_CLR_MSK	Clear/Mask BDE IRQ. 1 = BDE IRQ is disabled. 0 = BDE IRQ is enabled. Toggle this bit from 0 to 1 and then back to 0 to clear the interrupt and flag.	0	R/W
	6	JRX_204B_NIT_IRQ_CLR_MSK	Clear/Mask NIT Flag. 1 = NIT IRQ is disabled. 0 = NIT IRQ is enabled. Toggle this bit from 0 to 1 and then back to 0 to clear the interrupt and flag.	0	R/W
	5	JRX_204B_UEK_IRQ_CLR_MSK	Clear/Mask UEKC Flag. 1 = UEK IRQ is disabled. 0 = UEK IRQ is enabled. Toggle this bit from 0 to 1 and then back to 0 to clear the interrupt and flag.	0	R/W
	4	JRX_204B_ILD_IRQ_CLR_MSK	Clear/Mask ILD Flag. 0 = ILD IRQ is enabled Toggle this bit from 0 to 1 and then back to 0 to clear the interrupt and flag.	0	R/W
	3	JRX_204B_ILS_IRQ_CLR_MSK	Clear/Mask ILS Flag. 1 = ILS IRQ is disabled. 0 = ILS IRQ is enabled. Toggle this bit from 0 to 1 and then back to 0 to clear the interrupt and flag.	0	R/W
	2	JRX_204B_CKS_IRQ_CLR_MSK	Clear/Mask Good CKS Flag. 1 = CKS IRQ is disabled. 0 = CKS IRQ is enabled. Toggle this bit from 0 to 1 and then back to 0 to clear the interrupt and flag.	0	R/W
	1	JRX_204B_FS_IRQ_CLR_MSK	Clear/Mask FS Flag. 1 = FS IRQ is disabled. 0 = FS IRQ is enabled. Toggle this bit from 0 to 1 and then back to 0 to clear the interrupt and flag.	0	R/W
	0	JRX_204B_CGS_IRQ_CLR_MSK	Clear/Mask CGS Flag. 1 = CGS IRQ is disabled. 0 = CGS IRQ is enabled. Toggle this bit from 0 to 1 and then back to 0 to clear the interrupt and flag.	0	R/W

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Table 86. 8-Bit/10-Bit Error Monitoring and Lane Status Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
0x055C	2	JRX_DL_204B_IRQ_VEC	CMM Flag. A CMM error on Lane 0 generates a flag. A CMM error occurs if the configuration parameters of the JESD204B receiver do not match the JESD204B transmitter configuration parameters that are sent over the link during ILAS.	0	R/W
	1	JRX_DL_204B_IRQ_CLR	Clear/Mask Code Group Sync (CMM) flag. 1 = CMM IRQ is disabled. 0 = CMM IRQ is enabled. Toggle this bit from 0 to 1 and then back to 0 to clear the interrupt and flag.	0	R/W
	0	JRX_DL_204B_IRQ	8-Bit/10-Bit Link Error Interrupt and Flag 1 = 8-bit/10-bit link error has occurred (BD, NIT, UEK, ILD, ILS, CKS, FS, CGS, or CMM). IRQ/ flag is reset when all IRG conditions have been cleared using appropriate x_IRQ_CLR_MSK bit.	0	R/W
0x0598	[7:4]	SYNCB_ERR_DUR	The duration of the SYNCxOUTB± is low for the synchronization error report purposes. Duration =(.5 + code) PCLK cycles. To closely match the spec, set these bits as close as possible to F/2 PCLK cycles. This is shared between SYNCOUTB0 and SYNCOUTB1. 0 = SYNCxOUTB± low for 0.5 PCLK cycles. 1 = SYNCxOUTB± low for 1.5 PCLK cycles, and so on.	0x0	R/W
0x05AA	7	EN_204B_UEK_JRX_INT_GAINOFF	1 = Enables the JESD204B receiver UEKC soft off gain source. The device ramps the analog output down to 0 V DC if the UEKC threshold is reached.	0x0	R/W
	6	EN_204B_NIT_JRX_INT_GAINOFF	Enables the JESD204B receiver NIT soft off gain source. The device ramps the analog output down to 0 V DC if the NIT threshold is reached.	0x0	R/W
	5	EN_204B_BD_JRX_INT_GAINOFF	Enables the JESD204B receiver BD error soft off gain source. The device ramps the analog output down to 0 V DC if the BD threshold is reached.	0x0	R/W
	4	EN_204B_ILD_JRX_INT_GAINOFF	Enables the JESD204B receiver ILD soft off gain source. The device ramps the analog output down to 0 V DC an ILD error occurs.	0x0	R/W
	3	EN_204B_ILS_JRX_INT_GAINOFF	Enables the JESD204B receiver ILS soft off gain source. The device ramps the analog output down to 0 V DC if an ILS error occurs.	0x0	R/W
	2	EN_204B_GCS_JRX_INT_GAINOFF	Enables the JESD204B receiver good CKS soft off gain source. The device ramps the analog output down to 0 V DC if a CKS error occurs.	0x0	R/W
	1	EN_204B_FS_JRX_INT_GAINOFF	Enables the JESD204B receiver FS soft off gain source. The device ramps the analog output down to 0 V DC if an FS error occurs.	0x0	R/W
	0	EN_204B_CGS_JRX_INT_GAINOFF	Enables the JESD204B receiver CGS soft off gain source. The device ramps the analog output down to 0 V DC if a CGS error occurs.	0x0	R/W

JESD204C Receiver 64-bit/66-bit Link Layer

Monitoring the 64-Bit/66-Bit Synchronization Status

The 64-bit/66-bit link layer starts automatically when the link is powered on. The synchronization process begins with synchronization header alignment. When the JESD204C receiver aligns to the incoming synchronization header, it can be referred to as synchronization header lock (SH_LOCK).

When the SH_LOCK is achieved, the synchronization process progresses to extended multiblock synchronization, and then to extended multiblock alignment. Within the JESD204C receiver, this process is controlled by a state machine. The machine states can be monitored via the JRX_DL_204C_STATE bit field (Register 0x055E, Bit[6:4]).

The state machine operation is shown in Figure 64.

State 2, State 3, and State 4 represent the three phases of the synchronization process.

When these phases are complete, the state machine locks (state = 6) and the link is up. See Figure 63 for details on the JRX_DL_204C_STATE bit field.

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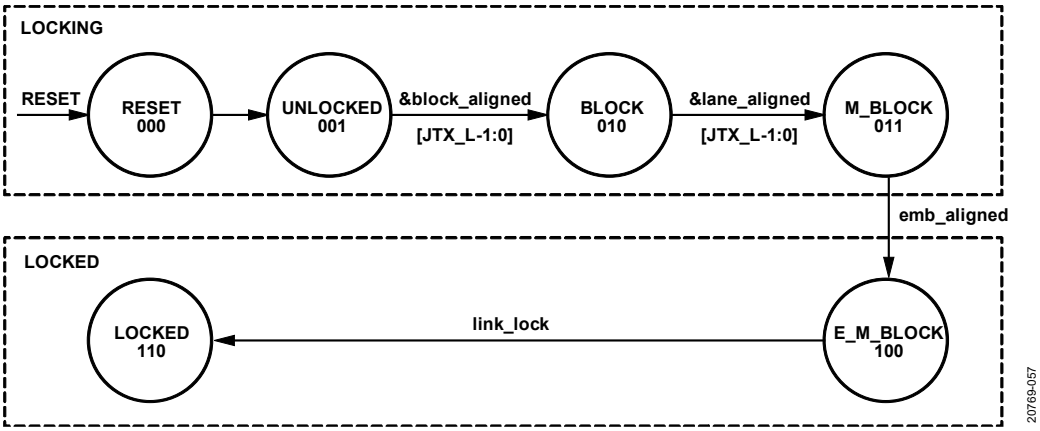

Figure 64. JESD204C Receiver Synchronization State Diagram

64-Bit/66-Bit Error Monitoring and Resynchronization

Error monitoring during the transmission of sample data is achieved by monitoring the CRC-12 data bits transmitted as part of the synchronization word and comparing the value to the CRC-12 value that is automatically calculated in the JESD204C receiver. See the 64-Bit/66-Bit Link Layer and Link Establishment section for details.

If the receiver detects too many CRC-12 errors, synchronization can be lost. In this case, the receiver restarts the synchronization state machines automatically. The JESD204C transmitter of the connected logic device continues sending data even if synchronization is lost at the JESD204C receiver. The receiver must resynchronize.

JESD204C CRC Interrupt

The JRX_204C_CRC_IRQ bit (Register 0x05BB, Bit 4) indicates if a CRC-12 error occurs. If the JRX_204C_CRC_IRQ_ENABLE bit (Register 0x05BB, Bit 0) is enabled, an interrupt informs the system master when a CRC-12 error occurs. Typically, the JRX_204C_CRC_IRQ_ENABLE bit must be set prior to enabling the JRX_LINK_EN bit (0x0596. Bits 1:0). After the link is fully synchronized and sample data is being sent across the link (JRX_DL_204C_STATE, register 0x055E, Bits[6:4] = 6), the JRX_204C_CRC_IRQ bit must be reset by writing any value to 0x05BB, Bit 4. After this, JRX_204C_CRC_IRQ can be monitored for valid CRC errors. If enabling the JRX_204C_CRC_ IRQ bit after the link is enabled, users must toggle the JRX_LINK_EN bit (off, then on). After the link is synced(JRX_DL_204C_STATE = 6), clear the IRQ (JRX_204C_CRC_IRQ = 1) before reading it again to check for errors.

If the CRC IRQ is set, users can check the status of each instantiated lane by reading each lane's JRX_DL_204C_ CRC_ERR_CNT register (0x0584-0x058B) to determine the lane(s) causing the error.

JESD204C State and Alignment Monitoring

The status of both the synchronization header alignment and extended multiblock alignment state machines can be monitored via the JRX_DL_204C_STATE bit field (Register 0x055E, Bits[6:4]) so the system master is informed of the respective states. If there are errors during synchronization (JRX_DL_204C_STATE ≠ 6), users can access the error counters for sync header (JRX_DL_204C_SH_ERR_CNT) , MB alignment (JRX_DL_204C_MB_ERR_CNT), and EMB alignment (JRX_DL_204C_EMB_ERR_CNT).

If resynchronization is required for any reason, the system master powers down both sides of the link. If a reconfiguration or clocking change is required, these processes must be done while the link is powered down. Resynchronization takes place automatically upon link power up.

JESD204C Receiver Status API

All of the link status bitfields described in the prior section and in Table 87 can be accessed using the app_show_link_ status() API function part of the ad9xxx_stra.c file. This function is described in the AD9081/AD9082/ AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Table 87. DAC Path 64-Bit/66-Bit Link Layer Registers

Address	Bits	Bit Name	Description	Reset	Access
0x055E	[6:4]	JRX_DL_204C_STATE	JESD204C Receiver State Machine Status 000 = reset 010 = synchronization header alignment complete 011 = extended multiblock synchronization complete 100 = extended multiblock alignment complete 110 = link is up and running	0	R
0x05BB	3	JRX_204C_CRC_IRQ	1 = CRC-12 mismatch between the JESD204C transmitter and the JESD204C receiver	0	R/W
	0	JRX_204C_CRC_IRQ_ENABLE	1 = enable the CRC-12 mismatch interrupt	0	R/W
0x0562	[7:0]	JRX_DL_204C_LANE_SKEW[7:0]	Relative lane skew in UI. Compare lanes for accurate skew.	0x0	R
0x056B	7	JRX_DL_204C_LANE_SKEW[8]	Relative lane skew in UI. Compare lanes for accurate skew.	0x0	R
	[3:0]	JRX_DL_204C_MB_ERR_CNT	Count of multiblock alignment errors	0x0	R
0x0574	[5:0]	JRX_DL_204C_SH_ERR_CNT	Count of block alignment errors	0x0	R
0x057C	[7:4]	JRX_DL_204C_EMB_ERR_CNT	Count of EMB alignment errors	0x0	R
0x057E	[4:0]	JRX_E_CFG	Number of MB in EMB (minus 1), (256 * E) %F = 0, E = LCM (F, 256) / 256	0x0	R/W
0x0584-0x058B	[7:0]	JRX_DL_204C_CRC_ERR_CNT[0:7]	Per lane count of CRC parity errors 0x0584 is lane0 CRC error count 0x0585 is lane1 CRC error count, etc.	0x0	R

DAC Path Deterministic Latency

The JESD204B/C systems contain various clock domains distributed throughout. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B/C link. These ambiguities lead to nonrepeatable latencies across the link from power cycle to power cycle with each new link establishment. The JESD204C specification addresses the issue of deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

Subclass 0 defines normal device operation where deterministic latency is not needed and a nonrepeatable latency across the link is acceptable.

The device supports JESD204B/C Subclass 0 and Subclass 1 operation. The JRX_SUBCLASSV_CFG bit field (Register 0x04AE, Bits[7:5]) sets the subclass mode for the device and the default is set for Subclass 0 operating mode (Register 0x04AE, Bits[7:5] = 0). If deterministic latency is not a system requirement, Subclass 0 operation is recommended and the SYSREF signal is not required to establish a link. Note that, even in subclass 0 mode, some internal synchronization is still required using a one shot sync as described in the SYSREF Modes section and SYSREF Setup/Sync Procedure section. In Subclass 0 mode, the one shot sync pulse is provided internally instead of an external SYSREF, based on the arbitrary phase of the LMFC/LEMC.

Subclass 0

Subclass 0 mode provides deterministic latency to within several JRX_SAMPLE_CLK cycles. This mode does not require any signal on the SYSREF± pins, which can be left disconnected. The JRX_SAMPLE_CLK value is the rate at which digital samples are processed through the JESD204B/C receiver and is equal to F_{DAC}/(interpolation×NS). F_{DAC} is the rate at which the DAC samples data. NS is the number of samples processed per F_{DAC} in the datapath and its value depends on the interpolation rate with some exceptions, as described in Table 88.

Subclass 0 requires that all lanes arrive within the same LMFC/LEMC cycle so that all of the DACs are synchronized to each other.

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Table 88. JESD204B/C Receiver NS Value vs. Interpolation Mode Rule

Interpolation			
Main (Coarse)	Channel(Fine)	NS	Exceptions
1	1	32	204C Mode 12, Mode 17, and Mode 35: NS = 16 204C Mode 33: NS = 8 204B Mode 18: NS = 16 204B Mode 63: NS = 8
1	>1	8	204C Mode 36: NS = 32 204C Mode 13, Mode 18, Mode 34,and Mode 35: NS = 16 204C Mode 2, Mode 4, Mode 5, Mode 8, Mode 9, Mode 21, and Mode 25: NS = 4
>1	*[1]	2	2x3, 3x2, 3x6, 6x3: NS = 4 204B Mode 6, Mode 10, Mode 15, Mode 17, and Mode 62: Nx1: NS = 4 204B Mode 12, Mode 18, and Mode 63: Nx1: NS = 8

[1] * = any value.

Subclass 1

Subclass 1 mode provides deterministic latency and allows the link to be synchronized to within ±1 DAC clock period (or less) when the SYSREF calibration procedure described in the SYSREF Setup/Sync Procedure section is implemented. This latency requires an external, low jitter SYSREF± signal that is accurately phase aligned to the DAC clock.

Link Delay

The link delay of a JESD204B/C system is the sum of the fixed and variable delays from the transmitter, channel, and receiver, as shown in Figure 65.

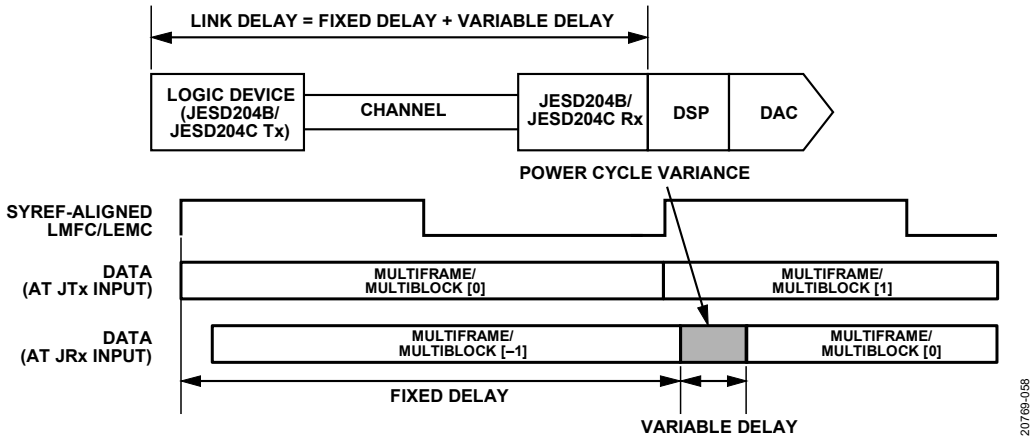

Figure 65. JESD204B Link Delay = Fixed Delay + Variable Delay

Deterministic Latency Requirements

The following key factors are required for achieving deterministic latency in a JESD204B/C Subclass 1 system:

- The SYSREF± signal distribution skew within the system must be less than the desired uncertainty.
- SYSREF setup and hold time requirements must be met for each device in the system. When the device is in averaged SYSREF mode, there are no setup or hold time requirements for the externally applied SYSREF signal because the internal LMFC/LEMC is aligned to an edge derived from the average of multiple sampled SYSREF edges References to SYSREF setup and hold times are only in the context of the sampled SYSREF mode.
- The JESD204B/C receiver receive buffer is a finite resource. The total latency variation across all lanes, links, and devices must be less than the LMFC period (if in JESD204B mode) or the smaller of the two values (32×F) and ((K×S)/NS) in JRX_SAMPLE_CLK periods (if in

JESD204C mode). This value includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system.

To enable deterministic latency, the JESD204B/C receiver has a receive buffer implemented using a FIFO with a read timing referenced to the SYSREF aligned LMFC/LEMC. The received data LMFC/LEMC boundary, as decoded from the incoming data, can be located significantly far away from the next occurring SYSREF aligned LMFC/LEMC. In this case, the receive buffer may not be deep enough to hold all the data. For this reason, adjust the read pointer using the JRX_TPL_PHASE_ADJUST[15:0] register (MSBs at Register 0x04A4, Bits[7:0] and LSBs at Register 0x04A3, Bits[7:0]) so that the buffer releases data sufficiently close to, but after, the received data LMFC/LEMC. The received data LMFC/LEMC can also arrive too close to the SYSREF aligned LMFC/LEMC. Arriving too close means the total link latency in the system is near an integer multiple of the LMFC/LEMC period so that, from one power cycle to the next, the data arrival time of the incoming LMFC/LEMC boundary at the receive buffer can straddle the JESD204B/C receiver local LMFC/LEMC boundary. In this case, use the JRX_TPL_PHASE_ ADJUST register to move the buffer read pointer so that the received LMFC/LEMC of all lanes, across all power cycles, and all links arrive at least two JRX_SAMPLE_CLK cycles prior to the buffer release time.

In the Figure 66 and Figure 67 examples, the link delay is approximately an integer multiple of an LMFC/LEMC period, and the power-cycle variation occurs across an LMFC/LEMC boundary in the JESD204B/C receiver. Use the JRX_TPL_PHASE_ ADJUST register to move the read pointer beyond the last arriving data. The step size for this adjustment is in JRX_ SAMPLE_CLK cycles, where JRX_SAMPLE_CLK = f_{DAC}/(INTERPOLATION×NS).

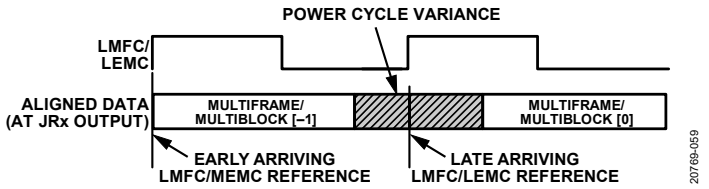

Figure 66. Link Delay > LMFC/LEMC Period Example

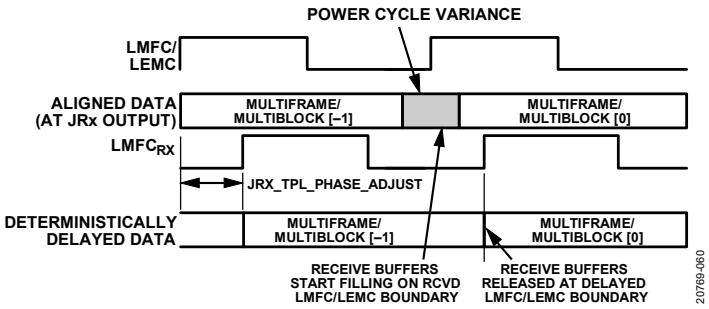

Figure 67. JRX_TPL_PHASE_ADJUST to Ensure Deterministic Latency

The method to select the appropriate value for JRX_TPL_PHASE_ ADJUST register is described in the LMFC/LEMC Delay Setup Example section.

Setting the JRX_TPL_PHASE_ADJUST appropriately ensures that the receive buffer absorbs all link delay variation. This write ensures that all data samples arrived before reading. Set these values to fixed values across runs and devices, to achieve deterministic latency.

LMFC/LEMC Delay Setup Example

The device JESD204B/C receiver reads back the phase difference between the local LMFC/LEMC boundary and the LMFC/LEMC boundary of the arriving data using the JRX_TPL_PHASE_DIFF, Bits[7:0] register (Register 0x04A5, Bits[7:0]). This information is used to calculate the appropriate JRX_TPL_PHASE_ADJUST register setting.

JRX_TPL_PHASE_DIFF is a read only register that reflects the time difference between the JESD204B/C receiver LMFC/LEMC boundary and the received data's LMFC/LEMC boundary in JRX_SAMPLE_CLK cycles.

To determine the JRX_TPL_ PHASE_ADJUST register setting, take the following steps:

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1. Cycle the link power at least 20 times using the process described in the JESD204B/C Receive Mode Tables section to determine the latest possible arriving time of the incoming data LMFC/LEMC boundary across all power cycles.
2. After each power-on cycle, read the JRX_TPL_PHASE_ DIFF register and record the value.
3. The latest possible arriving time is equal to the largest value recorded in Step 1. The count values range from 0 to ((K×S)/NS) – 1 (the number of JRX_SAMPLE_CLK cycles in the LMFC/LEMC. If the range of values recorded span the terminal count value of the JRX_SAMPLE_CLK counter, the latest possible arriving time value could be from 0 to 3 (see the example in Figure 69).
4. To ensure appropriate margin, add 2 to the latest possible arriving time and program this value into the JRX_TPL_PHASE_ADJUST register.

Figure 69 shows an example using JESD204B Mode 63 (1×1 interpolation). Step 1 through Step 3 in this example reveal that there are only two possible values recorded in Step 2, that is, 7 and 0. Accounting for the counter roll-over from 7 to 0, 0 is the latest arriving time (from Step 2). Therefore, a value of 2 is programmed into the JRX_TPL_PHASE_ADJUST register (0 + 2, as described in Step 3). The data read out of the read buffer is deterministically delayed and output on the delayed LMFC/LEMC boundary (read pointer).

Figure 68 shows an example using JESD204C Mode 22 (2×4 interpolation). In this example, the receive buffer depth is 32×F JRX_SAMPLE_CLK deep, which is 96. The LEMC contains 256 JRX_SAMPLE_CLK worth of data. Therefore, the receive buffer cannot store an entire LEMC worth of data. To avoid data errors, perform Step 1 through Step 3 for this example, which results in four possible values recorded in Step 2 (127, 128, 129, and 130). If no adjustment is made to the JRX_TPL_ PHASE_ ADJUST register, the buffer must have a depth of 255 – 127 (128) to avoid data errors. However, because the latest arrival time of the received data was determined to be at a count of 130 (as described in Step 2), a value of 132 is programmed into the JRX_TPL_PHASE_ADJUST register (130 + 2, as described in Step 3). The data read out of the read buffer is deterministically delayed and output on the delayed LMFC/LEMC boundary (read pointer). Note that this method ensures the minimum latency through the DAC.

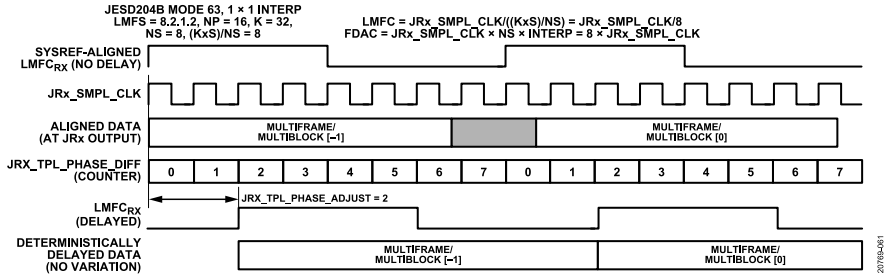

Figure 68. Example 2, Setting LMFC/LEMC Delay for Deterministic Latency (Derived from JRX_TPL_PHASE_DIFF)

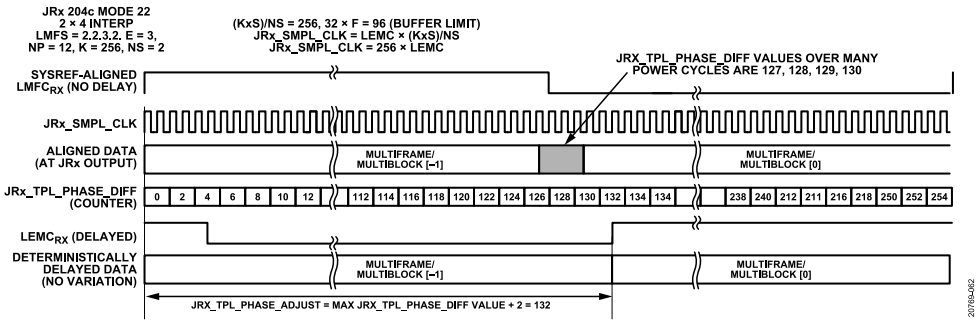

Figure 69. Example 1, Setting LMFC/LEMC Delay for Deterministic Latency (Derived from JRX_TPL_PHASE_DIFF)

JESD204B/C Receiver Multichip Synchronization

Adjustments to determine the JRX_TPL_PHASE_ADJUST register settings for each device in a multilink or multichip system (similar to determining the deterministic latency for a single link), take the following steps:

1. Cycle the link power for all links and devices at least 20 times using the process described in the JESD204B/C Receive Mode Tables section to determine the latest possible arriving time of the incoming data LMFC/LEMC boundary across all power cycles, links, and devices.

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2. When each power-on cycle is complete, read the JRX_TPL_PHASE_DIFF register for all links and devices in the system and record the values. The latest possible arriving time across all links and devices is equal to the largest value recorded in Step1.
3. To ensure appropriate margin, add 2 to the latest possible arriving time and program this value into the JRX_TPL_PHASE_ADJUST register of all links and devices in the system.

Figure 70 shows an example using JESD204C Mode 17. Step 1 through Step 3 for this example reveal that there are eight possible values across all power cycles, links, and devices recorded in Step 1. These values range from 47 to 54. 54 is the latest arriving time (as described in Step 2). Therefore, a value of 56 is programmed into the JRX_TPL_PHASE_ADJUST register (54 + 2, as described in Step 3). The data coming out of the read buffer is deterministically delayed and output on the delayed LMFC/LEMC boundary.

JESD204B/C Receiver Multichip Synchronization API Functions

The adjustment of the LMFC/LEMC phase in the JESD204B/C receiver is implemented in the adi_ad9xxx_jesd_rx_lmfc_ delay_set() API function that is included in the adi_ad9xxx_jesd.c code. This low level API is called as part of the adi_ad9xxx_jesd_ rx_link_config_set() function which is called in the top level adi_ad9081_device_startup_tx() API function.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

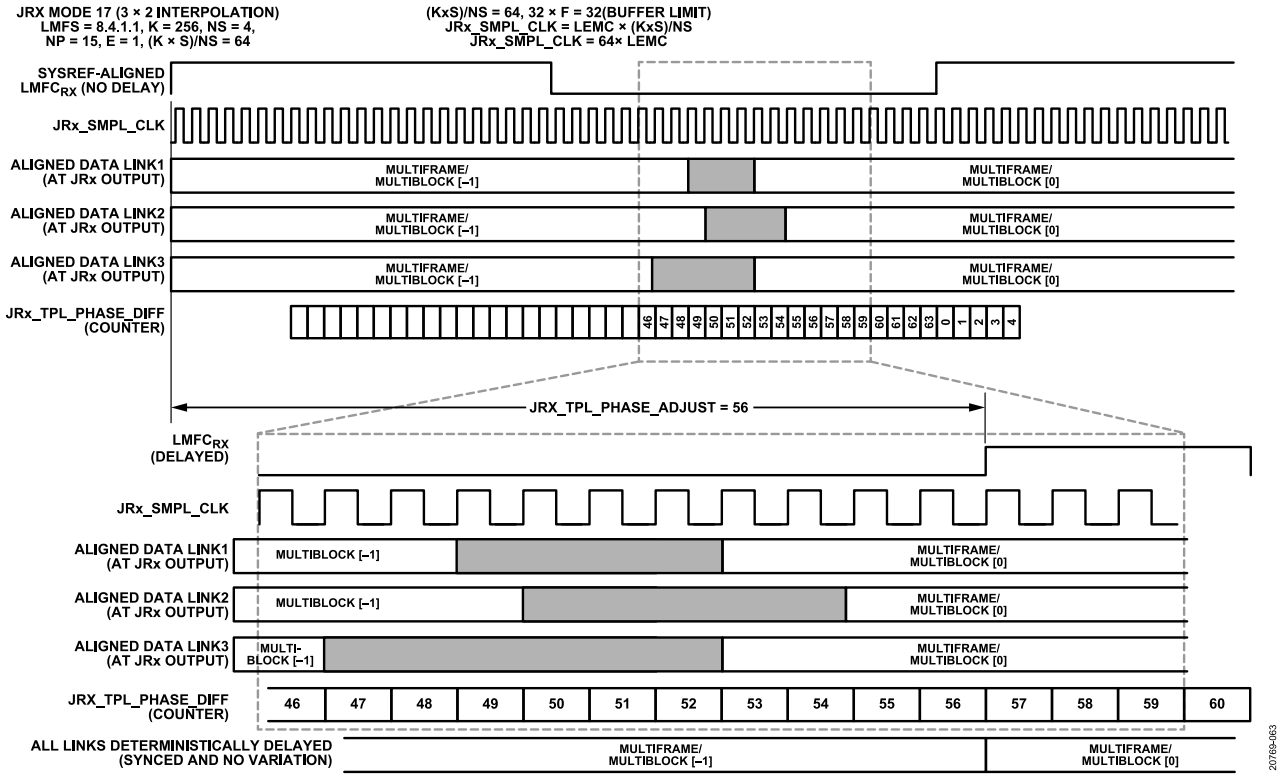

Figure 70. Setting LMFC/LEMC Delay for Multilink or Multichip Synchronization

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Table 89. JESD204B/C Receiver Deterministic Latency SPI Registers

Address	Bits	Bit Name	Description	Reset	Access
0x04AE	[7:5]	JRX_SUBCLASSV_CFG [2:0]	Set the Subclass Operation for the JESD204B/C receiver. 000 = Subclass 0 001 = Subclass 1 010 to 111 = invalid	0x00	R/W
0x00B0	[4:0]	SYNC_LMFC_DELAY_SET_FRM	SYSREF to LMFC/LEMC Coarse Delay (in Frame Units).	0x0	R/W
0x00B1	[7:0]	SYNC_LMFC_DELAY_SET	SYSREF to LMFC/LEMC Fine Delay (in DAC Clock Units).	0x0	R/W
0x04A4	[7:0]	JRX_TPL_PHASE_ADJUST[15:8]	Bits[15:8] of the JRX_TPL_PHASE_ADJUST value. JRX_TPL_PHASE_ADJUST is used to delay the transport layer LMFC/LEMC relative to the device local LMFC/LEMC in JRX_SAMPLE_CLOCK cycles	0x00	R/W
0x04A3	[7:0]	JRX_TPL_PHASE_ADJUST[7:0]	Bits[7:0] of the JRX_TPL_PHASE_ADJUST value.	0x00	R/W
0x04A5	[7:0]	JRX_TPL_PHASE_DIFF[7:0]	Difference between the local LMFC/LEMC boundary and the arriving data's LMFC/LEMC boundary in JRX_SAMPLE_CLOCK cycles	0x00	R

JESD204B/C Receiver Transport Layer

The transport layer receives the descrambled JESD204B/C frames and converts them to DAC samples based on the programmed JESD204B/C parameters shown in Table 90. The device parameters are defined in Table 91.

Certain combinations of these parameters are supported by the device. See Figure 69 and Figure 68 for a list of supported JESD204B/C modes.

Table 90. JESD204B/C Transport Layer Parameters

Parameter	Description
E	Number of multiblocks in an extended multiblock (204C mode only)
F	Number of octets per frame per lane: 1, 2, 3, 4 or 8.
K	Number of frames per multiframe: K = 32.
L	Number of lanes per converter device (per link): 1, 2, 3, 4 or 8.
M	Number of converters per device (per link): For real data modes, M is the number of real data converters (if total interpolation is 1×). For complex data modes, M is the number of complex data subchannels, I or Q.
S	Number of samples per converter, per frame: 1, 2, 4 or 8.

Table 91. JESD204B/C Device Parameters

Parameter	Description
CF	Number of control words per device clock per link. Not supported, must be 0.
CS	Number of control bits per conversion sample. Not supported, must be 0.
HD	Reflects the status of the JESD204 high density (HD) mode (indicates when converter samples are split across multiple lanes).
N	Converter resolution.
N' (or NP)	Total number of bits per sample.

JESD204B/C Receive Mode Tables

The device DAC path supports many JESD204B/C modes, as described in JESD204B/C Receiver Multichip Synchronization API Functions and Table 93. The JESD204B/JESD204C mode is set automatically based on the setting in the configuration of the JESD_MODE register as well as the settings in the link layer selection registers, JRX_DL_204B_ENABLE and JRX_DL_ 204C_ENABLE. See Table 94 for details on each of these registers.

To assist the user in selecting the appropriate mode for their application, the JESD204B/C Mode Selector Tool is available. The tool can be used to narrow down the number of modes to only include those modes that support the user's specific application use case. The tool guides the user through the mode selection process as described in the JESD204B/C Mode Selector Tool and Transmitter Mode Tables section.

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Table 92. DAC Path Supported JESD204B Modes

JESD204B Mode	L	M	F	S	K	N	NP	Dual Link	Interpolation Modes (Coarse×Fine)	JESD_MODE (Register 0x01FE, Bits[5:0])
4	2	8	6	1	32	12	12	Yes	4×6, 6×4, 6×6, 6×8, 8×3, 8×4, 8×6, 8×8, 12×2, 12×3, 12×4	0x04
5	2	4	4	1	32	16	16	Yes	2×8, 4×4, 4×6, 4×8, 6×4, 6×6, 6×8, 8×2, 8×3, 8×4, 8×6, 12×2, 12×3, 12×4	0x05
6	2	2	2	1	32	16	16	Yes	2×3, 2×4, 2×6, 2×8, 4×2, 4×3, 4×4, 4×6, 4×8, 6×2, 6×3, 6×4, 8×1, 8×2, 8×3, 8×4, 12×1, 12×2	0x06
8	3	6	4	1	32	16	16	Yes	2×8, 4×4, 4×6, 4×8, 6×4, 6×6, 6×8, 8×2, 8×3, 8×4, 8×6, 12×1, 12×2, 12×3, 12×4	0x08
9	4	8	4	1	32	16	16	Yes	2×8, 4×4, 4×6, 4×8, 6×4, 6×6, 6×8, 8×2, 8×3, 8×4, 8×6, 12×1, 12×2, 12×3, 12×4	0x09
10	4	4	2	1	32	16	16	Yes	2×3, 2×4, 2×6, 2×8, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x0A
12	4	2	2	2	32	16	16	Yes	2×1, 2×2, 2×3, 2×4, 4×1, 4×2, 6×1, 8×1	0x0C
14	6	12	4	1	32	16	16	No	2×8, 4×4, 4×6, 4×8, 6×4, 6×6, 6×8, 8×2, 8×3, 8×4, 8×6, 12×2, 12×3, 12×4	0x0E
15	8	8	2	1	32	16	16	No	2×3, 2×4, 2×6, 2×8, 4×2, 4×3, 4×4, 4×6, 4×8, 6×2, 6×3, 6×4, 8×1, 8×2, 8×3, 8×4, 12×1, 12×2	0x0F
16	8	16	4	1	32	16	16	No	2×8, 4×4, 4×6, 4×8, 6×4, 6×6, 6×8, 8×2, 8×3, 8×4, 8×6, 12×2, 12×3, 12×4	0x10
17	8	4	1	1	32	16	16	No	2×1, 2×2, 2×3, 2×4, 2×6, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x11
18	8	2	2	4	32	16	16	No	1×1, 2×1, 2×2, 2×3, 2×4, 4×1, 4×2, 6×1, 8×1	0x12
62	4	2	1	1	32	16	16	Yes	2×1, 2×2, 2×3, 2×4, 2×6, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x3E
63	8	2	1	2	32	16	16	No	1×1, 2×1, 2×2, 2×3, 2×4, 4×1, 4×2, 6×1, 8×1	0x3F

Table 93. DAC Path Supported JESD204C Modes

JESD204C Mode	L	M	F	S	K	E	N	NP	Dual link	Interpolation Modes (Coarse×Fine)	JESD_MODE (Register 0×01FE, Bits[5:0])
0	1	8	12	1	64	3	12	12	No	4×6, 6×4, 6×8, 8×3, 8×4, 8×6, 8×8, 12×2, 12×4	0x00
1	1	4	8	1	32	1	16	16	Yes	2×8, 4×4, 4×6, 4×8, 6×4, 6×6, 6×8, 8×2, 8×3, 8×4, 8×6, 12×2, 12×3, 12×4	0x01
2	1	2	4	1	64	1	16	16	Yes	2×3, 2×4, 2×6, 2×8, 4×2, 4×3, 4×4, 4×6, 4×8, 6×2, 6×3, 6×4, 8×1, 8×2, 8×3, 8×4, 12×1, 12×2	0x02
3	2	8	8	1	32	1	16	16	Yes	2×8, 4×4, 4×6, 4×8, 6×4, 6×6, 6×8, 8×2, 8×3, 8×4, 8×6, 12×2, 12×3, 12×4	0x03
4	2	8	6	1	128	3	12	12	Yes	2×6, 2×8, 4×3, 4×4, 4×6, 4×8, 6×2, 6×3, 6×4, 8×2, 8×3, 8×4, 8×8, 12×1, 12×2	0x04
5	2	4	4	1	64	1	16	16	Yes	2×3, 2×4, 2×6, 2×8, 4×2, 4×3, 4×4, 4×6, 4×8, 6×2, 6×3, 6×4, 8×1, 8×2, 8×3, 8×4, 12×1, 12×2	0x05
6	2	2	2	1	128	1	16	16		2×1, 2×2, 2×3, 2×4, 2×6, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x06
7	3	12	8	1	32	1	16	16	No	2×8, 4×4, 4×6, 6×4, 6×6, 6×8, 8×2, 8×3, 8×4, 8×6, 12×2, 12×3, 12×4	0x07
8	3	6	4	1	64	1	16	16	Yes	2×3, 2×4, 2×6, 2×8, 4×2, 4×3, 4×4, 4×6, 4×8, 6×2, 6×3, 6×4, 8×1, 8×2, 8×3, 8×4, 12×1, 12×2	0x08
9	4	8	4	1	64	1	16	16	Yes	2×3, 2×4, 2×6, 2×8, 4×2, 4×3, 4×4, 4×6, 4×8, 6×2, 6×3, 6×4, 8×1, 8×2, 8×3, 8×4, 12×1, 12×2	0x09
10	4	4	2	1	128	1	16	16	Yes	2×1, 2×2, 2×3, 2×4, 2×6, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x0A
11	4	16	8	1	32	1	16	16	No	2×8, 4×4, 4×6, 4×8, 6×4, 6×6, 6×8, 8×2, 8×3, 8×4, 8×6, 12×2, 12×3, 12×4	0x0B
12	4	2	1	1	256	1	16	16	Yes	1×1, 2×1, 2×2, 2×3, 2×4, 4×1, 4×2, 6×1, 8×1	0x0C
13	4	2	3	4	256	3	12	12	Yes	1×1, 2×1, 4×1	0x0D
14	6	12	4	1	64	1	16	16	No	2×3, 2×4, 2×6, 2×8, 4×2, 4×3, 4×4, 4×6, 4×8, 6×2, 6×3, 6×4, 8×2, 8×3, 8×4, 12×2	0x0E

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Table 93. DAC Path Supported JESD204C Modes (Continued)

JESD204C Mode	L	M	F	S	K	E	N	NP	Dual link	Interpolation Modes (Coarse×Fine)	JESD_MODE (Register 0×01FE, Bits[5:0])
15	8	8	2	1	128	1	16	16	No	2×1, 2×2, 2×3, 2×4, 2×6, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x0F
16	8	16	4	1	64	1	16	16	No	2×3, 2×4, 2×6, 2×8, 4×2, 4×3, 4×4, 4×6, 4×8, 6×2, 6×3, 6×4, 8×2, 8×3, 8×4, 12×2	0x10
17	8	4	1	1	256	1	16	16	No	1×1, 2×1, 2×2, 2×3, 2×4, 4×1, 4×2, 6×1, 8×1	0x11
18	8	2	1	2	256	1	16	16	No	1×1, 2×1, 2×2, 4×1	0x12
19	8	2	1	4	256	1	8	8	No	1×1	0x13
20	8	1	1	4	256	1	16	16	No	1×1	0x14
21	4	8	8	2	32	1	16	16	No	2×3, 2×4, 2×6, 2×8, 4×2, 4×3, 4×4, 4×6, 4×8, 6×2, 6×3, 6×4, 8×1, 8×2, 8×3, 8×4, 12×1, 12×2	0x15
22	2	2	3	2	256	3	12	12	Yes	2×1, 2×2, 2×3, 2×4, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x16
23	4	4	3	2	256	3	12	12	Yes	2×1, 2×2, 2×3, 2×4, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x17
24	8	8	3	2	256	3	12	12	No	2×1, 2×2, 2×3, 2×4, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x18
25	1	4	6	1	128	3	12	12	Yes	2×6, 2×8, 4×3, 4×4, 4×6, 4×8, 6×2, 6×3, 6×4, 8×2, 8×3, 8×4, 12×1, 12×2	0x19
26	2	4	6	2	128	3	12	12	yes	2×1, 2×2, 2×3, 2×4, 2×6, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x1A
27	2	4	3	1	256	3	12	12	yes	2×1, 2×2, 2×3, 2×4, 2×6, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x1B
28	4	8	6	2	128	3	12	12	no	2×1, 2×2, 2×3, 2×4, 2×6, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x1C
29	4	8	3	1	256	3	12	12	no	2×1, 2×2, 2×3, 2×4, 2×6, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x1D
30	4	4	4	2	64	1	16	16	yes	2×1, 2×2, 2×3, 2×4, 2×6, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x1E
31	4	4	8	4	32	1	16	16	yes	2×1, 2×2, 2×3, 2×4, 2×6, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x1F
32	4	4	6	4	128	3	12	12	yes	2×1, 2×2, 2×3, 4×1, 4×2, 4×3, 6×1, 6×2, 8×1, 12×1	0x20
33	4	2	8	8	32	1	16	16	Yes	1×1, 2×1, 2×2, 2×3, 2×4, 4×1, 4×2, 6×1, 8×1	0x21
34	4	2	6	8	128	3	12	12	Yes	1×1, 2×1, 4×1	0x22
35	8	4	3	4	256	3	12	12	No	1×1, 2×1, 4×1	0x23
36	8	2	3	8	256	3	12	12	No	1×1, 2×1	024

Table 94. DAC Path Supported JESD204B Mode Selection Registers

Address	Bits	Bit Name	Description	Reset	Access
0x01FE	[5:0]	JESD_MODE	Quick configuration setting for JESD204B/C parameters according to JESD204B/C Receiver Multichip Synchronization API Functions or Table 93, respectively.	0	R/W
0x04C0	5	JRX_DL_204B_ENABLE	Set to 0b'1 to select 8-bit/10-bit link layer (204B mode).	0	R/W
0x055E	7	JRX_DL_204C_ENABLE	Set to 0b'1 to select 64-bit/66-bit link layer (204C mode).	0	R/W

CONFIGURING THE JESD204B/C RECEIVER

High Level Configuration Process

The process in Table 95 provides a general process specifically aimed at bringing up the JESD204B/C receiver that may prove to be useful when reconfiguring or re-starting the JESD204B/C link. This process assumes that the PLL is already configured per the procedure described in the SERDES PLL and Configuration section. Users must consider the start-up within the context of their entire system however and can refer to the device API for this context.

For dual link operation, the configuration for each link must be identical. If using a dual link configuration (JRX_LINK_MODE, Register 0x0596, Bit 3 = 1) repeat Step 7 (disable scrambling) and Step 10 (Subclass 1 enable) in Table 95 for each link because the registers are paged parameters. Otherwise, perform the configuration only once using Link Page 0.

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JESD204B/C Receiver Configuration API

The bulk of the JESD204B/C receiver configuration is performed in the adi_ad9xxx_jesd_rx_link_config_set() API function, which is called by the higher level API function adi_adxxxx_ device_startup_tx_or_nco_test (). Many lower level APIs are called as part of this startup sequence, some of which are identified in Table 95.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 95. JESD204B/C Receiver High Level Configuration Process

Step	Action	Description	Lower API Functions
1	Disable link	Set JRX_LINK_EN (Register 0x0596, Bits[1:0]) = 2b'00	adi_ad9xxx_jesd_tx_link_enable_set
2	Select link page	Set JRX_LINK_MSK (Register 0x001D, Bits[1:0]) appropriately. 2b'01 selects Link 0. 2b'10 selects Link 1 (only needed when in dual link mode).	adi_ad9xxx_jesd_rx_lane_xbar_set
3	Configure the PHY lane crossbar if necessary	JRX_SRC_LANEx registers, Bits[4:0] of Register 0x058D to Register 0x0594.	adi_ad9xxx_hal_bf_set
4	Enable the appropriate data link layer.	Set the JRX_dl_204b_enable register (Register 0x04C0, Bit 5) and JRX_dl_204c_enable (Register 0x055E, Bit 7) as follows: If using 8-bit/10-bit encoding (JESD204B mode): JRX_DL_204B_ENABLE = 1, JRX_DL_204C_ENABLE = 0 If using 64-bit/66-bit encoding (204C mode): JRX_DL_204B_ENABLE = 0, JRX_DL_204C_ENABLE = 1	adi_ad9xxx_hal_bf_set
5	Set JESD mode	Set JESD_MODE (Register 0x01FE) See JESD204B/C Receiver Multichip Synchronization API Functions and Table 93. Set Register 0x04A1, Bit 6 = 0 Power down unused lanes PD_MASTER_RC (Register 0x0400, Bit 0) = 0 PHY_PD register (Register 0x0401) to disable power-down on appropriate lanes	adi_ad9xxx_hal_bf_set
6	Set chip interpolation mode	Refer to the Main Datapath CDUC section	adi_adxxxx_dac_interpolation_set
7	Enable scrambling (required for JESD204C)	JRX_DSCR_CFG (Register 0x04A9, Bit 7) = 1	adi_ad9xxx_jesd_rx_descrambler_set
8	Enable subclass 1 operation and configure SYSREF if operating in subclass 1 mode.	JRX_SUBCLASSV_CFG (Register 0x04AE, Bits[7:5]) = 3b'001. Set JRX_SYSREF_FOR_STARTUP (Register 0x058C, Bit 6). If set to 1, the device waits for the first SYSREF edge to arrive before bringing the link up instead of immediately locking to the incoming data stream. Set SYSREF_MODE (Register 0x00B8). Enable one shot mode or continuous mode (Bit 1) and check the SYSREF status (Bits[5:4]) Link bring up is delayed until SYSREF alignment is achieved.	adi_ad9xxx_jesd_oneshot_sync adi_ad9xxx_device_nco_sync_sysref_mode_set
9	Optimize deserializer settings.	See the JESD204B/C Receiver PHY Register Writes for Proper Operation section.	See Table 81
10	Physical Layer adjustments as needed	See Table 78 and Table 79 in the Equalizer (CTLE and DFE) section.	See Table 81
11	Enable link	JRX_LINK_EN (Register 0x0596, Bits[1:0]) = 1 (or 3 if LINK_SEPERATE_EN (Register 0x0596, Bit 2) = 1 for dual link independent enable operation)	adi_ad9xxx_jesd_rx_link_enable_set()

Transmit Path and JESD204B/C Receiver API Functions

The device API has application layer and low level device drivers to assist in setting up the device, including the transmit path and JESD204B/C receiver.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Figure 71 shows the application layer API used to configure the transmit path with the JESD204B/C receiver portions highlighted in red boxes. The application layer API shown implements the JESD204B/C receiver setup procedure outlined in Table 95.

For descriptions of the low level driver code, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

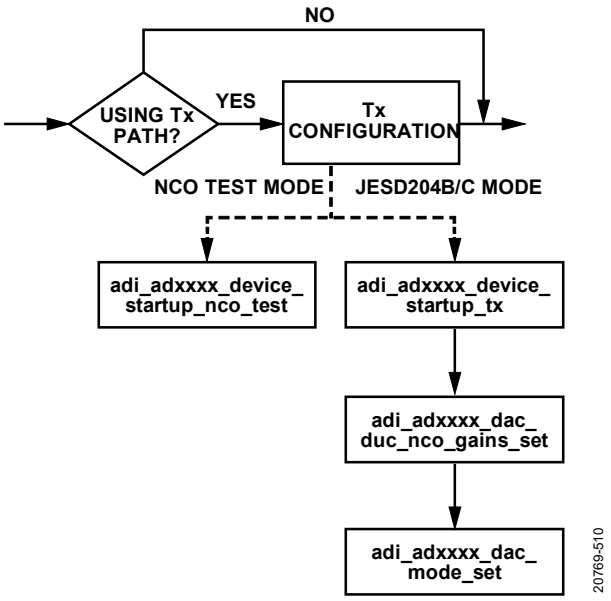

Figure 71. Transmit Path and JESD204B/C Receiver Application Layer API Configuration Flow

Table 96. DAC Path JESD204B/C Start-up Registers

Address	Bits	Bit Name	Description	Reset	Access
0x0400	0	PD_MASTER_RC	Master power-down for the JESD deserializers. Set this bit to 0 to unmask individual PHY_PD bits.	0x1	R/W
0x0401	[7:0]	PHY_PD	PHY power-down. Bit per lane applies. For example, a setting of 0xF0 powers down Physical Lane 7 to Physical Lane 4.	0xEE	R/W
0x04A1	6	JRX_TPL_BIT FIELD	This bit must be set to 0.	1	R/W
0x058C	6	JRX_SYSREF_FOR_STARTUP	Lane data is masked until an incoming SYSREF phase has been established after reset. This prevents link operation without deterministic latency.	0x0	R/W
0x0596	[1:0]	JRX_LINK_EN	Bit 0 = Link 0, 0 = disable Link 0, 1 = enable Link 0 Bit 1 = Link 1, 0 = disable Link 1, 1 = enable Link 1 Bit 1 is only enabled if JRX_LINK_SEPARATE_EN (Register 0x0596, Bit 2) = 1.		R/W
	2	JRX_LINK_SEPARATE_EN	0 = both links controlled by Bit 0 of JRX_LINK_EN (Register 0x0596, Bit 0). 1 = Link 0 and Link 1 controlled independently by Bit 0 and Bit 1 of JRX_LINK_EN (Register 0x0596, Bits[1:0]), respectively.		R/W
	3	JRX_LINK_MODE	0 = single link. 1 = dual link.		R/W
	5	JRX_LINK0_SYNCB_COMB_EN	0 = normal operation.		R/W
			1 = combine Link 0 and Link 1 synchronization signals as Link 0 synchronization output		
	6	JRX_LINK1_SYNCB_COMB_EN	0 = normal operation 1 = combine Link 0 and Link 1 synchronization signals as Link 1 synchronization output.		R/W
0x001D	[1:0]	JRX_LINK_MSK	Selects which deframer is being written to (only needed when in dual link mode).	2'b11	R/W

TRANSMIT DIGITAL DATAPATH AND OUTPUT

Table 96. DAC Path JESD204B/C Start-up Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
			2b'01 = select Link 0. 2b'10 = select Link 1. 2b'11 = select Link 0 and Link 1.		
0x058D-0x0594	6	JRX_LINK_LANE_INVERSE[0:7]	Per lane control for inverting data from each physical lane.		R/W
	[4:0]	JRX_SRC_LANE[0:7]	Per lane control for setting the logical lane source (Logical Lane 0 through Logical Lane 7) for each physical lane. (little endian: 0x061B assigns logical lane for PHY Lane 0)		R/W
0x04A9	7	JRX_DSCR_CFG	JESD204B/C receiver descrambler control. 0 = descrambling disabled. 1 = descrambling enabled (mandatory if using 64-bit/66-bit link layer.		
0x04C0	5	JRX_DL_204B_ENABLE	0 = disable 8-bit/10-bit link layer (204B mode) 1 = enable 8-bit/10-bit link layer (204B mode)		R/W
0x055E	7	JRX_DL_204C_ENABLE	0 = disable 64-bit/66-bit link layer (204C mode) 1 = enable 64-bit/66-bit link layer (204C mode)		R/W
0x055E	[6:4]	JRX_dl_204c_state	JESD204C RECEIVER state machine status 000 = reset. 010 = synchronization header alignment complete. 011 = extended multiblock synchronization complete. 100 = extended multiblock alignment complete. 110 = link is up and running.	0	R
0x00B8	5	INIT_SYNC_DONE	Initial sync done flag (after initial power-up).	0x0	R
	4	ONESHOT_SYNC_DONE	One shot sync done flag	0x0	R
0x00B8	1	SYSREF_MODE_ONESHOT	Enable one shot synchronization rotation mode.	0x0	R/W

TRANSMIT DIGITAL DATAPATH OVERVIEW

The complete transmit digital datapath is shown in Figure 72. On a high level, the transmit digital datapath is like the receive digital datapath but in reverse and consists of a bypassable channelizer path with eight fine digital quadrature upconverters (FDUC) and a main datapath with four coarse digital upconverters (CDUC). Note that the main path is bypassable on the device, which allows full bandwidth (or bypass) operation of the device, where the output of the JESD204B/C block is fed directly to a DAC core without passing through the datapath first. A 8 × 8 crossbar multiplexer maps any FDUC output to any coarse digital quadrature upconverters (CDUC) input across a summation block that allows up to eight channels to be summed together. When the channels and their FDUC are bypassed, a 4 × 4 crossbar multiplexer is available to map any I/Q input data pair to any CDUC, or any real data input to any DAC core if both the channelizer and main datapaths are bypassed.

The CDUC and FDUC share a common architecture that includes a gain scaling block that precedes an upsampling filter stage with selectable interpolation factors, as well as a bypassable quadrature upconverter for frequency translation. The 48-bit complex NCOs support integer-N or dual modulus operation, supports FFH, and may be configured to produce a single-tone output with adjustable amplitude and phase. The channelizer path is capable of delaying samples (skew adjust) ahead of the 8 x 8 crossbar mux at each FDUC output to allow coarse timing skew calibration.

During a SPI write cycle, similar blocks may be paged individually or as a group. Table 97 shows the different paging registers for the common blocks. This approach allows maximum flexibility when programming the device, especially when most settings are common to two or more datapath blocks while some custom settings are maintained. In this case, the common settings may be configured simultaneously using a single SPI write cycle.

The transmit digital path can be configured to support one or two JESD204B/C links. due to internal clocking and the phase alignment requirements between the datapaths, both links and the corresponding datapath interpolation factors must be configured identically. Generally, a single JESD204B/C link configuration is recommended unless a particular application requires supporting two identical links with independent synchronization. In most applications, the internal mux stages may be configured so that a single JESD204B/C link may be used.

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Table 97. Transmit Paging Register Bit Field Description

Address	Register Name	Register Description
0x001B	DACPAGE_MSK	Select which main datapath and DAC is paged during subsequent SPI read/write cycles
0x001C	DACCHAN_MSK	Select which channelizer is paged during subsequent SPI read/write cycles.
0x001D	MODS_MSK	DAC modulation mode select

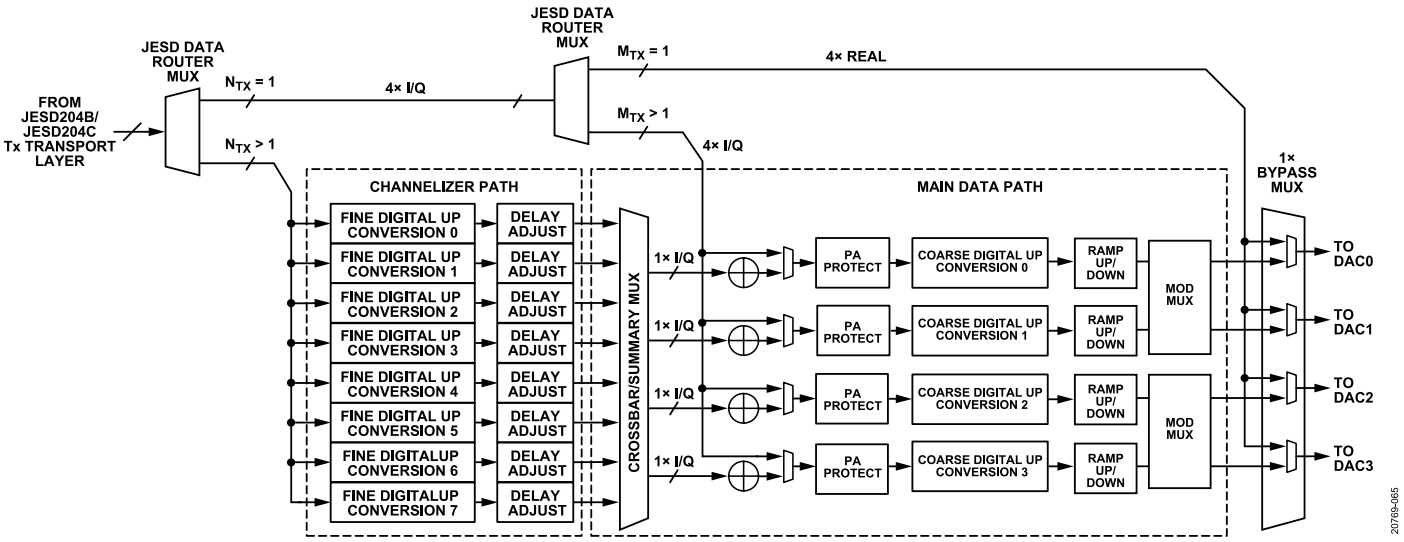

Figure 72. Complete Transmit Digital Datapath

Total Datapath Interpolation

The total interpolation factor is the product of the main path, M_{TX}, and channelizer, N_{TX} interpolation factor settings, as defined in the following equation:

$$Total\ Interpolation = M_{TX} \times N_{TX}$$

M_{TX} can be set to 1, 2, 4, 6, 8, or 12 and N_{TX} can be set to 1, 2, 3, 4, 6, or 8. A setting of 1 corresponds to bypass of the main data path or the channelizer path. Some JESD204B/C modes of operation limit the interpolation factor combinations that are available. The interpolation factors are set in 4-bit COARSE_ INTERP_SEL and FINE_INTERP_SEL bit fields in Register 0x01FF, as shown in Table 98.

If the total interpolation is equal to 1, all the datapaths and interpolation filter stages are bypassed. If processing I/Q data across a single JESD204B/C link, the total interpolation must be more than 1. If processing I/Q with an interpolation factor equal to 1, separate JESD204B/C links are used for I and Q.

The equation below shows the relationship between the DAC update rate (f_{DAC}), the I/Q input data rate (f_{IQ_IN}) and the total interpolation factor.

$$f_{DAC} = (Total\ Interpolation) \times f_{IQ\_IN}$$

Table 98. Interpolation Factor Settings in Register 0x01FF

Interpolation Factor	COARSE_INTERP_SEL, Bits[7:4], M_{TX}	FINE_INTERP_SEL, Bits[3:0], N_{TX}
1×	0x1	0x1
2×	0x2	0x2
3×	Not applicable	0x3
4×	0x4	0x4
6×	0x6	0x6
8×	0x8	0x8
12×	0xC	Not applicable

When determining the optimum M_{TX} and N_{TX} values, consider the following:

TRANSMIT DIGITAL DATAPATH AND OUTPUT

- Paging is not used because the M_{TX} and N_{TX} values are common to all datapaths regardless of JESD204 single or dual link operation.
- The I/Q input data rate (f_{IQ_IN}) required to represent the signal bandwidth of interest must exceed the bandwidth by at least a factor of 1.25, such that the signal falls within the interpolation filter bandwidth of the first interpolation stage. For example, if the desired signal bandwidth was a 100 MHz, with 80% I/Q interpolation filter bandwidth, the minimum f_{IQ_IN} must be no less than 125 MSPS.
- Operating at higher f_{DAC} (equivalent to increasing total interpolation for a given data rate) improves output power while simplifying filtering requirements external to the DAC output of the device. Filtering is used to suppress images (as predicted by sampling theory for an ideal DAC response) as well as other harmonic and non-harmonic spurious associated with a non-ideal DAC. Higher f_{DAC} pushes spurious that are folded from f_{DAC} to higher frequencies, which leads to a smaller filter with a higher cut off frequency and wider transition band. For example, LTCC filters allow a broad selection of high frequencies in a small package, as an alternative to designing discrete LC filters on a PCB. As a tradeoff, a lower f_{DAC} that still meets the overall system requirements may be preferred because operating the device DSP blocks at a lower f_{DAC} also leads to lower power consumption.
- For a multiband application, consider using individual channelizers to generate RF bands that can be summed in the main datapath, especially when such a configuration leads to a 2× or greater reduction in JESD204B/C link throughput and data rate. Using a separate channelizer for each band allows to transmit all the bands at baseband, without the need to transmit the white space between the bands. Note that transmit applications that employ digital predistortion do not typically benefit from this arrangement, because the reconstructed bandwidth is typically 3× or greater than the bandwidth of the RF band, and remains similar whether the signal is transmitted across a single channel or is split into its baseband signals across the channelizers.
- The maximum data rate output of the channelizer datapath is limited to 1500 MSPS. This restricts the minimum value of M_{TX} when using the channelizers, such that $M_{TX} > f_{DAC}/1500$, where f_{DAC} is specified in MHz. In a multiband application, this also restricts the maximum separation between the outer most RF bands to 1200 MHz because the pass band response of the interpolation filter inside the FDUC is limited to 80% of the input data rate, which in effect limits the useable frequency range of its NCO.

Total Datapath Interpolation API

The API supports total datapath interpolation with the adi_ ad9081_dac_duc_nco_set and adi_ad9081_dac_xbar_set functions, which are contained in the **adi_adxxxx_dac.c** file, and the adi_ad9081_jesd_rx_bit_rate_get function, which is contained in the **adi_adxxxx_jesd.c** file.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

DATA ROUTER MULTIPLEXERS AND DEFAULT MAPPING

The transmit path channels are enabled and the virtual converter data samples are routed from the JESD204B/C transport layer to the channelizer datapath, the main datapath, or the DAC inputs automatically, depending on the interpolation settings, NTX, and MTX. Note that the API function *adi_ad9xxx_dac_interpolation_set* sets the interpolation factors for the main and channelizer data paths, as well as determines the virtual converter routing, depending on the channelizer interpolation setting. If N_{TX} is >1, the data samples are routed to the channelizer datapath. If the channelizer datapath is bypassed with N_{TX} = 1 and M_{TX} >1, the data samples are routed to the main datapath. In the case of the AD9081 and AD9082, which support bypass mode (or N_{TX} = M_{TX} = 1), the samples are routed to the DACs. An optional 4 × 4 crossbar multiplexer can be used to change the default mapping of either the I/Q data pairs to CDUCs or the virtual converter samples to specific DACs in the case of complete datapath bypass, as shown in Figure 72.

When the channelizer and/or main datapaths are enabled, each I/Q sample is routed to a pair of virtual converters, each corresponding to an I data stream and a Q data stream. If the channelizer datapath is enabled, the data mapping to the FDUCs is sequential, such that the I/Q samples corresponding to Virtual Converter 0 and Virtual Converter 1 are mapped to FDUC0, the next pair of I/Q samples corresponding to Virtual Converter 2 and Virtual Converter 3 are mapped to FDUC1, and so on. When using two JESD204B/C links (dual link), the samples from the 1st link are mapped to FDUC 0 through FDUC 3 whereas the samples from the 2nd link are always mapped to FDUC 4 through FDUC 7. The 8 × 8 crossbar multiplexer in the main datapath allows the FDUC outputs to be mapped to any CDUC input.

Similarly, if the channelizers are bypassed and the main datapath is enabled, the default mapping for a single JESD204B/C link is with the first pair of samples mapped to CDUC 0 and subsequent pairs (presumably when M = 4, 6 or 8) are mapped in sequential order to CDUC1, CDUC2, and CDUC3. When using two JESD204B/C links (dual link), the samples from the 1st link are mapped to CDUC 0 through CDUC 1 where as the samples from the 2nd link are always mapped to CDUC 2 through CDUC 3.

The default mapping of the CDUC outputs to the DAC cores is sequential, with the complex CDUC 0 output mapped to DAC0, CDUC 1 to DAC1, and so on. For other mapping options, such as routing the real CDUC 0 output to DAC0 and the imaginary CDUC 0 output to DAC1, see the Modulator Multiplexer (Mod Mux) section.

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If the datapath is completely bypassed, the default mapping of virtual converters to the DAC cores for single link JESD204B/C is also sequential starting with the first sample mapped to DAC0 with M = 1 and ending with the fourth sample (if M = 4) mapped to DAC3. Although a dual link configuration is possible, there is no practical reason to select this mode of operation when operating with datapaths that are completely bypassed, because all datapaths are accessible using a single JESD204B/C link.

Note while the digital datapath is intended to support the complex I/Q data format (common in communication applications), the data samples are not required to be in quadrature for proper device operation and the user may elect to map any data to the virtual converters across the JESD204B/C link, in effect utilizing the I/Q datapath for two parallel data streams. This particularly useful if the complex NCOs of the channelizer and main datapaths are bypassed, so that samples pertaining to each virtual converter are not mixed inside the DUC and only undergo interpolation, thus retaining the original signal representation. The two data streams may be then split to two DAC cores using the mode mux, or one of the streams may be discarded in cases where real data is transmitted into the I/Q datapath. The usable interpolation filter bandwidth when processing a single stream of real data across the I/Q datapath is 40% of the input data rate, as opposed to the 80% bandwidth when processing complex (IQ) data.

4 × 4 Crossbar

Although the default API-based mapping from the JESD204B/C block to the main datapath is adequate for most applications, sometimes remapping the samples offers added flexibility. For instance, it may be desirable to map the I/Q data to a specific CDUC and its associated DAC to achieve maximum isolation when only two DACs are required in the application. The 4 × 4 crossbar allows remapping the I/Q data pairs routed to the main datapath or the real data routed directly to the DAC. Using the DACPAGE_MSK, the DAC cores can be configured to accept data from any JEAD204B/C data stream, whether as a dedicated stream mapped to each output individually or as a single data stream mapped simultaneously to multiple CDUCs or DACs.

To change the default settings of the 4 × 4 crossbar, take the following steps:

1. Determine the CDUC (or DAC) inputs that benefit from a different mapping.
2. Set the bit field in the DACPAGE_MSK register corresponding to the CDUC (or DAC) input that requires a modification. For example, if the input data source for CDUC3 requires a modification, set 0x001B = 0x08.
3. Set Bit 7 of the register MAINDP_DAC_1XXX_ENABLES (Register 0x01C8) to enable crossbar remapping for the input.
4. In the same register, select the input data source. To select the source, set only one of the bit assignments in Bits[3:0] to 1 and set the other three bit assignments to 0. Note that the Bit 0 assignment corresponds to the first data pair if the main datapath is used or the first virtual converter sample if the main datapath is bypassed. For example, to map the second pair of I/Q data to CDUC3, set Register 0x01C8 to 0x82.
5. Repeat Step 1 through Step 4 for other CDUC (or DAC) inputs that may require remapping.
6. Disable any unused digital datapaths and DACs to save power.

4 × 4 Crossbar API

The lower level APIs called adi_ad9xxx_dac_xbar_set and adi_ad9xxx_dac_select_set are used to configure the 4x4 crossbar.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

CHANNELIZER DATAPATH

The channelizer datapath shown in Figure 73 consists of eight identical complex upconversion stages. Each stage includes an FDUC and a gain and sample skew delay block. The FDUC consists of a selectable N-factor interpolation filter and a complex quadrature upconverter driven by a complex NCO. Note that the interpolation setting, N_{TX}, is share among all stages. The maximum output data rate of the channelizer datapath is 1.5 GSPS, with the interpolation filters providing 80% of useable pass band response relative to the input complex I/Q data rate (or 40% pass band response if the data is treated as real data). This leads to a maximum frequency spacing between channels of 1200 MHz, as measured between the outer most band edges of the channel. Table 99 provides the maximum usable complex and real bandwidths for different interpolation settings when the channelizer is operated at 1.5 GSPS.

The gain, skew delay and the NCO settings can be individually configured for each channelizer using the DACCHAN_MSK bit field (Register 0x001C), where each bit assignment directly maps to the channelizer number (for example, Bit 0 corresponds to Channelizer 0). Updates to all the NCO settings can trigger synchronously in response to an internal SYNC signal aligned either to a sampled SYSREF edge or a SPI write to register DDSC_FTW_UPDATE.

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To bypass the channelizer stage, set the interpolation factor to 1 and disable the complex NCOs of all the channelizers.

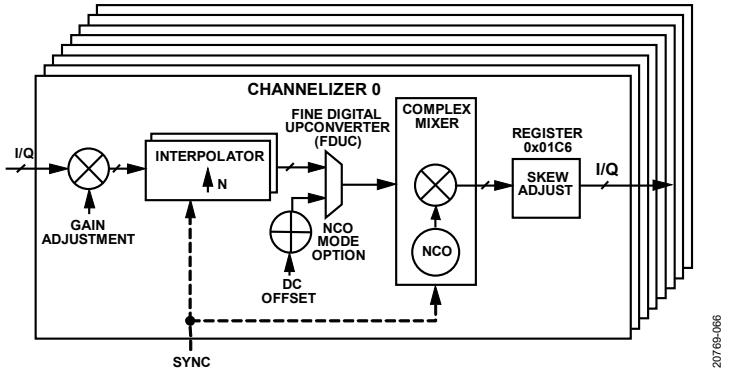

Figure 73. Channelizer Datapath, Eight Upconversion Paths with Independent Gain, Skew, and NCO Settings.

Table 99. Maximum Usable Input Complex or Real Signal Bandwidth for the Channelizer Interpolation Stage

N_{TX}	Maximum Usable Complex I/Q Signal Bandwidth (MHz)	Maximum Usable Real Signal Bandwidth (MHz)	Maximum Input Data Rate (MSPS)
2	600	300	750
3	400	200	500
4	300	150	375
6	250	100	250
8	150	75	187.5

Digital Gain

The data passing through each channelizer stage can be rescaled prior to summation and additional processing. This feature is useful in multiband applications to prevent digital clipping when the outputs of two or more channelizer stages are summed ahead of the main datapath to produce a multiband band signal. The 12-bit gain code, CHNL_GAIN, is set in Register 0x01B8 and Register 0x01B9.

To calculate the gain or gain code, use the following formulas:

$Gain\ Code = 2048 \times Gain = 2^{11} \times 10^{(dBGain/20)}$

$Gain = Gain\ Code \times (1/2048)$

$0 \le Gain \le (2^{12} - 1)/2^{11}$

$dB\ Gain = 20 \times log_{10}(Gain)$

$-\infty\ dB < dBGain \le +6.018$ dB

The digital gain scaling operation is a multiplication operation performed directly on the digital samples. As a result, the change is near instantaneous and takes effect as soon as the request propagates through the SPI logic. The gain scaling does not result in any measurable glitches or settling at the analog output.

Channelizer Digital Gain API

The API supports channelizer digital gain with the adi_ad9081_ dac_duc_nco_gain_set function. Note this API is not called by the main datapath configuration API adi_ad9xxx_device_ startup_tx and must be called in user application after adi_ad9xxx_ device_startup_tx.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Skew Adjust

The channel skew adjust feature allows different delay offsets between the individual channelizer stages with the unit delay relative to the output data rate of the channelizer. The unit delay corresponds to 667 ps at an output data rate of 1500 MSPS. A discrete unit delay step between −4 and +4 can be set for each channel using the CHNL_SKEW_ADJ bit field in Register 0x01C6, Bits[3:0], where bit 3 indicates a negative delay.

The unit delay resolution can also be referenced to the complex input data rate, as shown in the following equation:

$$Unit\ Delay = 1/(N_{TX} \times f_{IQ\_IN})$$

where:

N_{TX} is the channelizer interpolation rate, equal to 2, 3, 4, 6, or 8.

Transmit Channelizer Skew Adjust API

The API supports transmit channelizer skew adjust with the adi_ad9081_dac_duc_chan_skew_set function. Note this API is not called by the main datapath configuration API adi_ad9xxx_ device_startup_tx and must be called in user application after adi_ad9xxx_device_startup_tx.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Channelizer Interpolation Stage

The channelizer interpolation filter stage shown in Figure 74 consists of three half-band, low-pass filters (HB0, HB1, and HB2) that provide 2× interpolation, as well as a 3× interpolation filter (TB0). The individual filters selected in the cascaded lineup depend on the desired interpolation factor, N_{TX}. The cascaded response has a linear phase response with < 0.001 dB ripple over a complex passband region of 80% relative to the input data rate, f_{IQ_IN}. The stopband rejection in the alias or image regions exceeds 85 dB. FINE_INTERP_SEL field in Register 0x01FF, Bits[3:0], sets the interpolation factor.

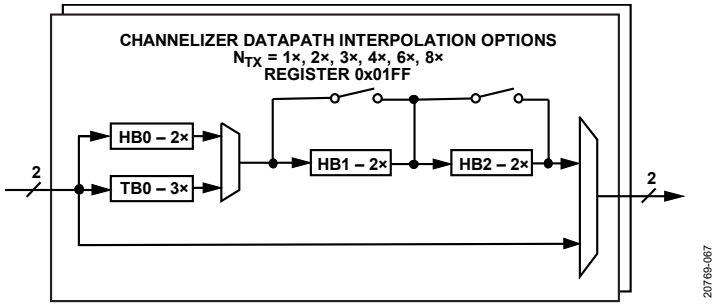

Figure 74. Channelizer Interpolation Filter Lineup

Transmit Channelizer Interpolation Stage API

The API supports transmit channelizer interpolation stage with the high level adi_ad9xxx_device_startup_tx API. It is a 4 × 4 crossbar configuration and the channelizer interpolation based on the ch_interp and dac_chan parameters. Note the API uses these configured settings for JESD lane rate calculation.

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Channelizer FDUC

Frequency translation is accomplished with a complex NCO and a digital quadrature mixer, as shown in Figure 75, where the complex input data after the interpolation filter is multiplied by the NCO complex exponential frequency ($e^{-j\omega ct}$) data output, such that the input spectrum (represented by the input data) is shifted and centered around the desired carrier frequency (f_c). The f_c is generated by the NCO according to the specified FTW. The NCO clock rate, f_{NCO}, operates at the channelizer output data rate, $f_{IQ\_OUT\_CH}$ where

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$f_{NCO} = f_{IQ\_OUT\_CH} = N_{TX} \times f_{IQ\_IN}$

As a result, the tuning range for the FDUC NCO is between $-f_{NCO}/2$ and $+f_{NCO}/2$, although from a practical perspective, the usable frequency tuning range is 80% of this span due to the pass band response of the main datapath interpolation filter downstream.

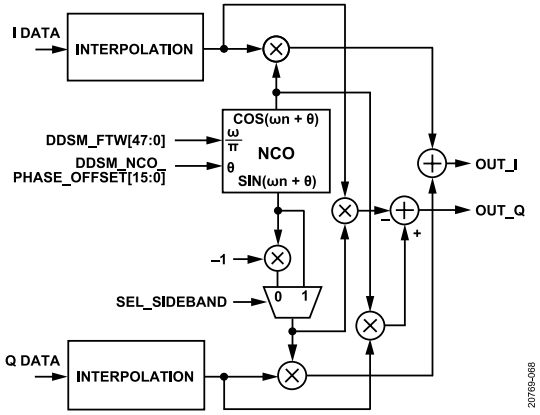

Figure 75. FDUC Block Diagram

Table 100 lists the bit field names associated with the DDSC_ DATAPATH_CFG register (Register 0x01A0) that configure the FDUC. Set the DDSC_SEL_SIDEBAND bit to 1 to flip the polarity of the NCO carrier frequency, which is akin to swapping I data and Q data at the input of the NCO. The DDSC_MODULUS_ EN bit allows the NCO to operate in dual modulus mode, as described in the FDUC Dual Modulus NCO Mode section.

Table 100. FDUC Configuration Register (Register 0x01A0)

Bit	Bit Name	Description
6	DDSC_NCO_EN	Enable channel NCO
2	DDSC_MODULUS_EN	Enable dual modulus NCO
1	DDSC_SEL_SIDEBAND	Enable lower sideband (spectral inversion)
0	TEST_TONE_EN	Enable test tone generation

The FDUC can be configured to accommodate the following modes of operation:

- Variable IF: the NCO and mixers are enabled to allow frequency translation of the interpolated I/Q input data spectrum. To enable this mode, set the DDSC_NCO_EN bit to 1.
- Zero IF (ZIF): The I/Q input data is interpolated but the NCO is disabled, and no frequency translation occurs. To bypass the NCO and mixers, set the DDSC_NCO_EN bit to 0.
- NCO only: The I/Q input data into the FDUC is internally generated in the form of DC samples, instead of the interpolated I/Q input data from a JESD204B/C link. This results in a CW tone output whose peak amplitude is proportional to the level of the DC samples. To enable this mode, set the TEST_TONE_EN bit and the DDSC_NCO_EN bit to 1.

Internal to the FDUC block, the 48-bit complex NCO supports the following modes of operation (see Table 101 for a list of registers that configure these modes):

- Integer-N mode: the twos complement, 48-bit frequency tuning word and the 16-bit initial phase offset word are set by the DDSC_FTW and DDSC_NCO_PHASE_OFFSET.
- Dual modulus mode: enabled by DDSC_MODULUS_EN in register 0x01A0, this mode allows a higher frequency resolution to generate precision NCO frequencies that otherwise cannot be generated using the Integer-N mode. The fractional frequency step is set using the two 48-bit DDSC_ACC_DELTA and DDSC_ACC_MODULUS words.

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Table 101. Channelizer FDUC NCO Registers

Address	Register Name	Description
0x01A1	DDSC_FTW_UPDATE	Synchronous NCO update via SYSREF or SPI
0x01A7 to 0x1A2	DDSC_FTW[47:0]	48-bit frequency tuning word
0x01A9 and 0x01A8	DDSC_NCO_PHASE_OFFSET[15:0]	16-bit phase offset word
0x01AF to 0x01AA	DDSC_ACC_MODULUS[47:0]	48-bit modulus denominator
0x01B5 to 0x1B0	DDSC_ACC_DELTA[47:0]	48-bit modulus numerator
0x0204	CHNL_NCO_RST_EN[7:0]	Enables SYSREF for NCO update per channelizer

Transmit Channelizer FDUC API

The channelizer FDC configuration is handled by the high level API adi_ad9xxx_device_startup_tx. The API also provides block level transmit channelizer FDUC with the following functions:

- adi_ad9081_dac_duc_nco_enable_set
- adi_ad9081_dac_duc_nco_ftw_set
- adi_ad9081_dac_dc_test_tone_en_set
- adi_ad9081_dac_duc_nco_phase_offset_set
- adi_ad9081_dac_duc_nco_reset_set

These functions are also exposed via the **adi_adxxx.h** file.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

FDUC NCO Synchronization and Reset

Unlike other registers, the DDSC_FTW, DDSC_ACC_DELTA and DDSC_ACC_MODULUS registers are not updated immediately when the write operation is complete. Instead, the user has the option to trigger the update of one or more NCOs simultaneously in response to an internal synchronization signal or an external SYSREF signal (synchronization to an external event, as needed for multichip synchronization or phase coherency relative to the arriving SYSREF edge). The default method is to reset the NCOs relative to an internal synchronization signal, where the rising edge of the DDSC_FTW_LOAD_REQ bit (Register 0x01A1, Bit 0) triggers an update on the next rising edge of the internal synchronization signal. Alternatively, reset the NCOs relative to a sampled SYSREF signal, where the rising edge of the ALIGN_ARM bit (Register 0x0205, Bit 2) triggers an update on the next sampled rising edge of an external SYSREF signal. For best results, perform a one shot sync prior to using SYSREF to reset the NCOs. For more information, refer to the System Multichip Synchronization section.

Resetting the NCO is useful when determining the start time and phase of the NCO output.

FDUC NCO Synchronization and Reset API

The API supports FDUC NCO sycnchronization and reset with the adi_ad9081_dac_duc_nco_reset_set and adi_ad9081_dac_duc_nco_ftw_set functions.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

FDUC Dual Modulus NCO Mode

This mode operates in fractional N mode to provide a tuning accuracy resolution of >48 bits. To enable this mode, set the DDSC_MODULUS_EN bit (Register 0x01A0 Bit2) to 1. An example of a rational frequency synthesis that requires >48 bits of accuracy is a carrier frequency of 1/10 of the sample rate, a ratio that an integer-N NCO cannot generate because it is not a power of two submultiple of the sample rate.

When a frequency accuracy of ≤48 bits is acceptable, integer-N mode is more suitable. The following equations can be used calculate the DDSC_FTW, DDSC_ACC_DELTA, and DDSC_ ACC_MODULUS words (for more information on the programable modulus feature, see the AN-953 Application Note, *Direct Digital Synthesis (DDS) with a Programmable Modulus.*):

$$\frac{\mathrm{mod}(f_C, f_{NCO})}{f_{NCO}} = \frac{RN}{RD} = \frac{X + (A/B)}{2^{48}} \quad (1)$$

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$$DDSC\_FTW = X = floor(2^{48}\frac{\text{mod}(f_C, f_{NCO})}{f_{NCO}}) \quad (2)$$

DDSC_ACC_DELTA =*A* = mod(2^{48} × *RN*, *RD*) (3)

DDSC_ACC_MODULUS = *B* = *RD* (4)

where:

RN is the integer representing the rational numerator of the frequency ratio.

RD is the integer representing the rational denominator of the frequency ratio.

The following example highlights a case where dual modulus mode is required to realize the exact desired NCO frequency. For example, if f_{NCO} = 1500 MHz and the desired value of f_c is 150 MHz, the output frequency is not a power of two submultiple of the sample rate, namely f_c = (1/10) f_{NCO}, which is not possible with a typical accumulator based DDS. The frequency ratio, f_c/f_{NCO}, is proportional to the M/N ratio, where M and N are derived by reducing the fraction (150,000,000/1,500,000,000) to the lowest terms, that is,

M/*N* = 150,000,000/1,500,000,000 = 1/10

where *M* = 1 and *N* = 10.

Using the above equations to solve for X, A, and B results in X = 28,147,497,671,065, A = 6, and B = 10. When these values are programmed into the registers for X, A, and B, the NCO produces an output frequency of exactly 150 MHz given a 1500 MHz sampling clock.

FDUC Dual Modulus NCO Mode API

The API supports FDUC dual modulus NCO mode with the adi_ad9081_dac_duc_nco_ftw_set function, which is contained in the **adi_adxxxx_dac.c** file.

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

FDUC Integer NCO Mode and Phase Offset

Integer-N mode is the default mode with the DDSC_MODULUS_EN bit (Register 0x01A0 Bit2) set to 0 by default. The frequency tuning word, DDSC_FTW, is calculated by using the following formula:

$$DDSC\_FTW = round(2^{48}\frac{\text{mod}(f_C, f_{NCO})}{f_{NCO}}) \quad (9)$$

The phase offset is set with a 16-bit, twos complement value using the DDSC_NCO_PHASE_OFFSET word.

To calculate the phase offset word, use the following equations:

−180° ≤ Degrees Offset ≤ +180°

DDSC_NCO_PHASE_OFFSET = *Degrees Offset*/180° × 2^{15}

The NCO synchronization is still maintained when the phase offset word is loaded, even though the writes to update the word are inherently asynchronous. For example, it is possible to make a series of writes to adjust the phase in one direction and follow with a series of writes in the other direction to arrive at the initial phase offset before any adjustments were made.

FDUC Integer NCO Mode and Phase Offset API

The API supports FDUC integer NCO mode and phase offset with the adi_ad9081_dac_duc_nco_ftw_set and adi_ad9081_dac_duc_nco_phase_offset_set functions, which are contained in the **adi_adxxxx_dac.c** file.

For more information, refer to the transmit path NCOs section in the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Channelizer NCO Only Mode

This mode can be configured to provide a complex, CW output. To enable this mode, use the TEST_TONE_EN bit listed in Table 100. The tone is generated using a programmable internal DC amplitude offset level (DC offset in Figure 73) that is injected into the complex modulator input to generate an unmodulated single tone, as shown in Figure 73. The DC amplitude level is controlled by the 16-bit DC_OFFSET word loaded into Register 0x01B6 and Register 0x01B7 where a setting of 0x5A82 corresponds to the peak amplitude of the tone. This mode operates the NCO as a DDS, for applications that require multiple single-tone signals of a varying frequency and amplitude. Applications that only require a single tone must consider using the CDUC NCO instead. See the Main Path NCO Only Mode section for more details.

When channelizer NCO only mode is enabled, the data source of the digital datapath is the DC offset word. Note that even when the JESD204B/C link is set up and data is properly transferred to the device over the link, this data is not presented to the NCO until this mode is disabled.

Channelizer NCO Only Mode API

The API supports channelizer NCO only mode with the adi_ad9081_dac_dc_test_tone_en_set and adi_ad9081_dac_ dc_test_tone_offset_set functions, which are contained in the **adi_adxxxx_dac.c** file.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

8 × 8 CROSSBAR MULTIPLEXER

This crossbar multiplexer routes the data samples from the channelizer datapath to the main datapath. The multiplexer allows up to eight channelizer outputs to be directed to any or all of the four main datapath summation nodes. From an implementation perspective, the multiplexer selects which channelizer outputs are directed to the summation node of each main datapath, as shown in Figure 76. The API function called adi_ad9081_dac_xbar_set is used to program this block. However, it is recommended that the user use the high level adi_ad9xxx_device_startup_tx and the dac_chan parameter API functions to configure the desired datapath.

The DACPAGE_MSK bit field in Register 0x001B selects the main datapath(s) for which the inputs to the summation node is configured. The CHAN_ENABLES register (Register 0x01BA) selects which channelizers are routed to the summation block(s). Note that the bit location corresponds to the channelizer number. For example, Bit 0 corresponds to Channelizer 0.

The summation of any number of channels being used must not exceed the $\pm 2^{15}$ value range to avoid data signal clipping at the output of the summation block and the input into the main datapath. The amount of digital gain scaling (back off) required depends on the number of channels being summed and the probability distribution characteristics of the waveform (the probability that the summed data samples exceeds $\pm 2^{15}$ for waveforms of a known peak-to-average ratio). Adjust each channelizer gain accordingly to prevent digital clipping.

The maximum data rate for each channel when the channel interpolation is >1× is limited by the summing node junction maximum speed of 1.5 GSPS. If the channel datapaths are bypassed (channel interpolation is 1×), the summing node block from the channelizers is also bypassed, as shown in Figure 76.

MAIN DIGITAL DATAPATH

The main datapath shown in Figure 76 consists of four identical complex upconversion stages. The input signal consists of one or more channelizer outputs or a wideband complex signal from the JESD data router multiplexer when the channelizer path is bypassed. The main datapath is functionally identical to the channelizer path, with the addition of an input summation block for multicarrier signal generation through the channelizer datapath, a power amplifier protection block with capability to softly ramp up/ramp down the output to the DAC cores, and an extra 32-bit calibration NCO in the CDUC. The input select multiplexer (input select mux in Figure 77) is automatically configured based on the interpolation factor setting of the FDCU block (N_{TX}), located upstream from the main datapath. The channelizer is bypassed when $N_{TX} = 1$.

The interpolation factor of the main datapath (M_{TX}) is common among all stages and cannot be independently controlled in each CDUC block. To independently control the gain, PA protection and NCO settings are paged using the DACPAGE_MSK bit field (Register 0x001B) to mask which main datapath is configured (for example, Bit 0 enables controlling Main Datapath 0). Unused datapaths can be disabled via the MAINDP_ENABLE register (Register 0x01F0, Bits[7:4]) where Bit 4 corresponds to Main Datapath 0. The main digital datapath is bypassed when $M_{TX} = 1$.

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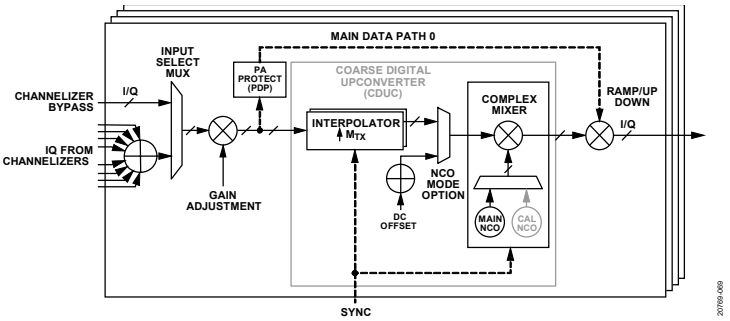

Figure 76. Main Digital Datapath per Main DAC Output Block Diagram

Digital Gain Scaling

The input data can be attenuated prior to additional processing. DP_GAIN is a 12-bit gain loaded into Register 0x20D4, Bits[11:8], and Register 0x20D3, Bits[7:0], to set the attenuation level. The GAIN_LOAD_STROBE bit field (Register 0x20D4, Bit 7) applies the value to the datapath when it is toggled from 0 to 1.

To calculate the DP_GAIN code, use the following formulas:

$0 \le Gain \le (2^{12} - 1)/2^{12}$

$-\infty\ dB < dBGain \le 0\ dB$

$Gain = Gain\ Code / 2^{12}$

$dB\ Gain = 20 \times log10\ (Gain)$

$DP\_GAIN\ code = 4096 \times Gain = 2^{12} \times 10^{(dBGain/20)}$

Digital Gain Scaling API

The API supports digital gain scaling with the adi_ad9081_dac_ duc_main_dsa_set and adi_ad9081_dac_duc_main_dsa_enable_ set functions which are exposed to the user in the **adi_adxxx.h** file.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Main Datapath Interpolation Stage

The interpolation stage consists of three half-band, low-pass filters (HB3, HB4, HB5) that provide 2× interpolation and a 3× interpolation filter (TB1), as shown in Figure 77. The individual filters are enabled in a cascaded fashion so that the total interpolation through the interpolation stage is equal to the assigned interpolation factor M_{TX}. The COARSE_INTERP_SEL bit field in Register 0x01FF, Bits[7:4], sets the interpolation factor M_{TX}.

The interpolation stage is designed to support the widest possible bandwidth while trading off filter performance against reasonable power consumption. When $M_{TX} > 1$, the HB3 filter is always enabled, and it thus sets the total maximum bandwidth of the filter bank; HB4, TB1, and HB5 are designed for a slightly wider bandwidth than HB3 (once normalized to a common datarate to account for the rate conversion following each filter), and do not limit the bandwidth.

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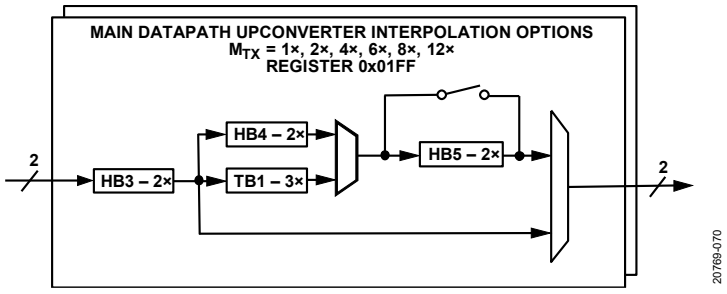

Figure 77. Main Datapath Interpolation Filter Lineup

In its default configuration, the HB3 filter has a maximum input datarate of 4GSPS and it provides a complex pass band bandwidth equivalent to 80% of its input datarate, f_{IQ_IN}, along with a linear phase response, ripple of < 0.001 dB, and a stop-band rejection of 85 dB.

The HB3 in Main Datapath 0 supports f_{IQ_IN} of up to 6GSPS, to support single-channel / wideband operation that requires running the JESD204B/C link near its maximum throughput.

Additionally, the HB3 in Main Datapath 0 and Main Datapath 2 can be reconfigured to support 90% f_{IQ_IN} bandwidth with a 70 dB stopband rejection and a maximum input datarate of 4GSPS. To use this topology, set the HB3_90BW_EN bit fields in Register 0x01F0, where Bit 1 corresponds to Main Datapath 0 and Bit 2 corresponds to Main Datapath 2.

When using the 90% bandwidth topology, consider the following:

- The 90% HB3 filter is only available in Main Datapath 2 and Main Datapath 0; however, the HB3 in the other main datapaths can still be used in its 80% bandwidth topology.
- The maximum input data rate into the 90% HB3 filter is 4 GSPS; when M_{TX} = 2 and f_{DAC} > 8GSPS , the 4 GSPS limit is exceeded: $f_{DAC} = M_{TX} \times 4GSPS = 8GSPS$. So for f_{DAC} > 8GSPS, the 80% bandwidth topology provides the widest possible bandwidth, while the 90% HB3 topology requires setting M_{TX} = 4, with a maximum input data rate $f_{IQ\_IN} = 12GSPS / M_{TX} = 3GSPS$.

Table 102 shows the available complex or real reconstruction bandwidths relative to the DAC clock and the input data rate to the interpolation block, when HB3 is configured for 80% bandwidth.

Table 102. Signal Bandwidth for f_{DAC} = 6 GSPS, 9 GSPS, and 12 GSPS DAC Clock Rates for M_{TX} Interpolation Factors

	DAC CLOCK = 6 GSPS		DAC CLOCK = 9 GSPS		DAC CLOCK = 12 GSPS	
M Factor	Usable Complex / Real Signal Bandwidth (GHz)[1]	Input Data Rate (GSPS)	Usable Complex I/Q/Real Signal Bandwidth (GHz)	Input Data Rate (GSPS)	Usable Complex I/Q/Real Signal Bandwidth (GHz)	Input Data Rate (GSPS)
2	2.4/1.2	3	3.6/1.8	4.5	4.8/2.4	6
4	1.2/0.6	1.5	1.8/0.9	2.25	2.4/1.2	3
6	0.8/0.4	1	1.2/0.6	1.5	1.6/0.8	2
8	0.6/0.3	0.75	0.9/0.45	1.13	1.2/0.6	1.5
12	0.4/0.2	0.5	0.6/0.3	0.75	0.8/0.4	1

[1] Quoted with HB3 configured for 80% f_{IQ_IN} bandwidth.

Main Datapath Interpolation Stage API

The high level API adi_ad9xxx_device_startup_tx supports the transmit datapath main DUC interpolation configuration using the main_interp parameter.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Main Datapath CDUC

The main datapath CDUC upconverts (or modulates) the input signal to a specified RF output prior to signal reconstruction by the DAC(s). Because the CDUC shares the same design features as the channelizer FDUC shown in Figure 75, an abbreviated description of the CDUC functionality is provided in this section. Table 103 lists the bit fields associated with the DDSM_DATAPATH_CFG register (Register 0x01C9)

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that is used to configure the CDUC. Like the FDUC, the DDSM_SEL_SIDEBAND bits and DDSM_ MODULUS_EN bits are used for sideband selection and NCO dual modulus mode operation, respectively.

The CDUC differs from the FDUC in the following notable ways:

- The CDUC provides the option for either real (default setting) or complex modulated output data. For complex data, set the EN_CMPLX_MODULATION bit to 1.
- The CDUC operates at f_{DAC}. For real data output, this operation rate provides a tuning range from 0 to $+f_{DAC}/2$. For complex output data, the tuning range is extended to $-f_{DAC}/2$ to $+f_{DAC}/2$.

Table 103. CDUC Configuration Register (Register 0x01C9)

Bit	Bit Name	Description
6	EN_CMPLX_MODULATION	Enables complex modulation. Enables an I and Q output from the CDUC and to the Mod Multiplexer
3	DDSM_NCO_EN	Enable DDSM NCO
2	DDSM_MODULUS_EN	Enable the DDSM modulus
1	DDSM_SEL_SIDEBAND	Enable lower sideband (spectral inversion)

The CDUC can be configured for the following modes of operation (see Table 103):

- Variable IF with real output. To configure the CDUC for this mode, take the following steps:
  - Set the DDSM_NCO_EN bit to 1 to enable the NCO and the mixers.
  - Set the EN_CMPLX_MODULATION bit to 0 for real output only.
- Variable IF with complex output. To configure the CDUC for this mode, take the following steps:
  - Set the DDSM_NCO_EN bit to 1.
  - Set the EN_CMPLX_MODULATION bit to 1.
- Zero IF (ZIF). To configure the CDUC for this mode, take the following steps:
  - Set the DDSM_NCO_EN bit to 0.
  - Set the EN_CMPLX_MODULATION bit to 0.
- NCO only. To configure the CDUC for this mode, take the following steps:
  - Set the DDSM_EN_CAL_DC_INPUT bit to 1 (Register 0x01E9, Bit 1).
  - Use the EN_CMPLX_MODULATION bit to select a real or complex data output.
  - Disable unused datapaths.

The 48-bit complex NCO supports the following modes of operation (see Table 101 for the associated registers used for configuration):

- Integer-N mode where the twos complement, 48-bit frequency tuning and 16-bit initial phase offset words are set by the DDSM_FTW register and the DDSM_NCO_ PHASE_OFFSET register.
- Dual modulus mode for higher frequency resolution where the modulus is set by the 48-bit DDSM_ACC_ DELTA and DDSM_ACC_MODULUS words.

Table 104. Main Data Path CDUC NCO Registers

Address	Register Name	Description
0x01CA	DDSM_FTW_UPDATE	Synchronous NCO update via SYSREF or SPI
0x01D0 through 0x1CB	DDSM_FTW[47:0]	48-bit frequency tuning word
0x01D1 and 0x01D2	DDSM_NCO_PHASE_OFFSET[15:0]	16-bit phase offset word
0x01D3 through 0x01D8	DDSM_ACC_MODULUS[47:0]	48-bit denominator of modulus
0x01D9 through 0x1DE	DDSM_ACC_DELTA[47:0]	48-bit numerator of modulus
0x0203	MAIN_NCO_RST_EN[3:0]	Enables SYSREF for NCO update per channelizer

Main Datapath CDUC API

The high level API adi_ad9xxx_device_startup_tx for datapath configuration configures the main NCO per the desired frequency shift specified by the main_shift parameter.

In addition, the API provides block level the main datapath CDUC support with the following functions:

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- adi_ad9081_dac_duc_nco_ftw_set
- adi_ad9081_dac_duc_nco_ftw0_set
- adi_ad9081_dac_complex_modulation_enable_set
- adi_ad9081_dac_duc_nco_enable_set
- adi_ad9081_dac_duc_main_dc_test_tone_en_set
- adi_ad9081_dac_duc_nco_phase_offset_set
- adi_ad9081_dac_duc_nco_reset_set

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

CDUC NCO Synchronization and Reset

Unlike other registers, the DDSM_FTW, DDSM_ACC_DELTA and DDSM_ACC_MODULUS registers are not updated immediately when the write operation is complete. Instead, the user has the option to trigger the update of one or more NCOs simultaneously in response to an internal synchronization signal or an external SYSREF signal (synchronization to an external event, as needed for multichip synchronization or phase coherency relative to the arriving SYSREF edge). The default method is to reset the NCOs relative to an internal synchronization signal, where the rising edge of the DDSM_FTW_LOAD_REQ bit (Register 0x01CA, Bit 0) triggers an update on the next rising edge of the internal synchronization signal. Alternatively, reset the NCOs relative to a sampled SYSREF signal, where the rising edge of the ALIGN_ARM bit (Register 0x0205, Bit 2) triggers an update on the next sampled rising edge of an external SYSREF signal. For best results, perform a one shot sync prior to using SYSREF to reset the NCOs. For more information, refer to the System Multichip Synchronization section.

Resetting the NCO is useful when determining the start time and phase of the NCO output.

CDUC NCO Synchronization and Reset API

The API supports CDUC NCO synchronization and reset with the adi_ad9081_dac_duc_nco_reset_set function and adi_ad9081_dac_duc_nco_ftw_set function which is exposed via the **adi_ad9xxx.h** header file.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

CDUC Dual-Modulus NCO Mode

This mode operates in fractional N mode to provide a tuning accuracy resolution of >48 bits. To enable this mode, set the DDSM_MODULUS_EN bit (Register 0x01C9)to 1. The following equations can be used calculate the DDSM_FTW, DDSM_ACC_DELTA, and DDSM_ACC_MODULUS words (note that f_c is referenced to f_{DAC}):

$$\frac{\mathrm{mod}(f_C, f_{DAC})}{f_{DAC}} = \frac{M}{N} = \frac{X + (A/B)}{2^{48}} \quad (1)$$

$$DDSM\_FTW = X = floor(2^{48}\frac{\mathrm{mod}(f_C, f_{DAC})}{f_{DAC}}) \quad (2)$$

$DDSM\_ACC\_DELTA = A = \mathrm{mod}(2^{48} \times M, N)$ (3)

$DDSM\_ACC\_MODULUS = B = N$ (4)

CDUC Dual Modulus NCO Mode API

The API supports CDUC dual modulus NCO mode with the adi_ad9081_dac_duc_nco_ftw_set function, which is contained in the **adi_adxxxx_dac.c** file.

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

CDUC Integer NCO Mode and Phase Offset

Integer-N mode is the start-up mode with the DDSM_ MODULUS_EN bit set to 0 by default. The frequency tuning word, DDSM_FTW, is calculated using the following formula:

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$$DDSM\_FTW = round(2^{48}\frac{\text{mod}(f_C, f_{DAC})}{f_{DAC}}) \quad (10)$$

The phase offset is set with a 16-bit, twos complement value using the DDSM_NCO_PHASE_OFFSET word.

To calculate the phase offset word, use the following equations:

−180° ≤ Degrees Offset ≤ +180°

DDSM_NCO_PHASE_OFFSET = Degrees Offset/180° × 2^{15}

Note that NCO synchronization is still maintained when the phase offset word is asynchronously loaded.

CDUC Integer NCO Mode and Phase Offset API

The API supports CDUC integer NCO mode and phase offset with the adi_ad9081_dac_duc_nco_ftw_set and adi_ad9081_dac_duc_nco_phase_offset_set functions, which are contained in the **adi_adxxxx_dac.c** file.

For more information, refer to the AD9081/AD9082/AD9986/ AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Main Path NCO Only Mode

Similar to the channelizer FDUC, any CDUCs can be independently configured (using the DACPAGE_MSK) to generate a complex, single tone output of varying amplitude, as shown in Figure 76. Consider this mode if only a single tone output is desired as an output signal. Multitone generation must use the channelizer FDUCs to allow summation of multiple tones. To enable this mode, set the DDSM_EN_CAL_DC_INPUT bit to 1 (Register 0x01E9, Bit 1). The DC amplitude level is controlled using the 16-bit MAIN_DC_OFFSET bit field in Register 0x01E0 and Register 0x01E1 where a setting of 0x5A82 corresponds to a full-scale tone.

When main path NCO only mode is enabled, the data source of the digital datapath is the DC offset word. Note that the JESD204B/C link can be brought up and data can be properly transferred to the device over the link, however it is not presented to the DAC until this mode is disabled.

Optional Calibration NCO

An additional, optional 32-bit calibration integer-N NCO block can be used as part of any initial system calibration to avoid reprograming the 48-bit NCO of the CDUC. The calibration NCO is selected using the DDSM_EN_CAL_FREQ_TUNE bit (Register 0x01E9, Bit 0). To enable this feature, take the following steps:

- Use the following formula to program the 32-bit frequency tuning word in the DDSM_CAL_FTW bit field (Register 0x01E5 through Register 0x01E8):

$$DDSM\_CAL\_FTW = round(2^{32}\frac{\text{mod}(f_C, f_{DAC})}{f_{DAC}}) \quad (11)$$

- Set the DDSM_EN_CAL_ACC bit in Register 0x01E9 (Bit 2) to enable the NCO accumulator clock.
- Toggle the DDSM_FTW_LOAD_REQ bit (Register 0x01CA, Bit 0) from 0 to 1 to load the value.
- Set the DDSM_EN_CAL_FREQ_TUNE bit (Register 0x01E9, Bit 0) to 1 to switch the multiplexer state such that the calibration NCO is used.

Modulator Multiplexer (Mod Mux)

A pair of modulator multiplexers, Mod Mux 0 and Mod Mux 1, determine how the CDUC outputs are connected to the DAC core input. To support the various configurations between a pair of CDUCs and DACs, two identical multiplexers are used. Mod Mux 0 is situated between CDUC0, CDUC1 and DAC0, DAC1 whereas Mod Mux 1 is situated between CDUC2, CDUC3 and DAC2, DAC3 as shown in figure 78. Each mod mux may receive its input from one or two CDUCs and deliver an output into the DAC core(s) that may be real or complex.

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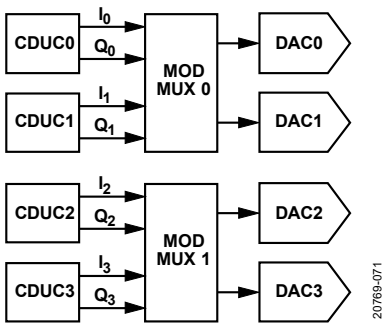

Figure 78. Mod Multiplexer Connections Between the CDUC Blocks and the DAC Cores

To configure one or both mod mux blocks, page to the desired mod mux(s) using the MODS_MSK bit field (Register 0x001D, Bits[3:2]), where Bit 2 selects Mod Mux 0 and Bit 3 selects Mod Mux 1. The DDSM_DATAPATH_CFG register (Register 0x01C9) selects one of six possible mod mux configurations, as described in Table 105.

The mod mux configuration is dictated by the end application. Consider configuration 0 or 3 if the reconstructed signal requires no additional upconversion stages externally, or if the upconversion is performed by a double sideband or image reject mixer. Consider config 1, 2, 3A, 3B, or 3C for zero-IF or complex-IF applications, where the reconstructed I and Q signals are routed to two DAC outputs that drive the inputs to a I/Q modulator for upconversion. Configurations 3A, 3B, and 3C allow using the CDUC NCOs as intermediate upconversion stages.

Consider summing two CDUC outputs in cases where each CDUC is operated as a wideband channel (band) in a multiband application. In the case when two CDUCs are summed, the outputs are rescaled by a factor of ½ to prevent digital clipping after the samples are summed into the DAC(s).

The mod mux configurations may be useful for non-IQ signals, where the two virtual converter streams from the JESD204B/C transport layer are treated as separate data streams and the I/Q datapath is only used to process and interpolate the signal(s).

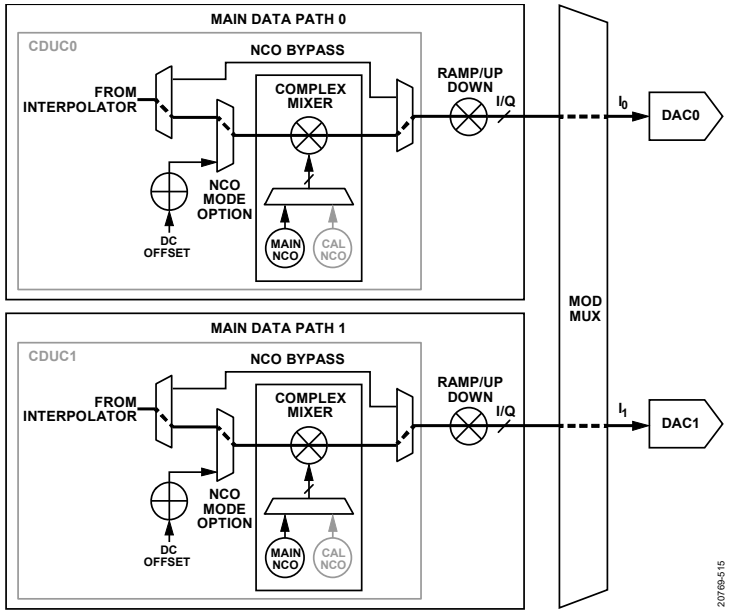

Figure 79. Mod Mux Configuration 0—DAC0 = I_0, DAC1 = I_1

TRANSMIT DIGITAL DATAPATH AND OUTPUT

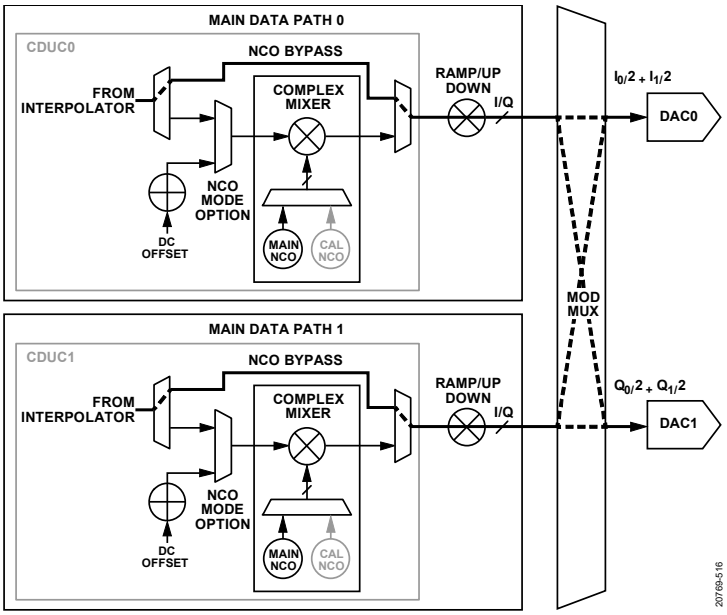

Figure 80. Mod Mux Configuration 1—DAC0 = $(I_0 + I_1)/2$, DAC1 = $(Q_0 + Q_1)/2$

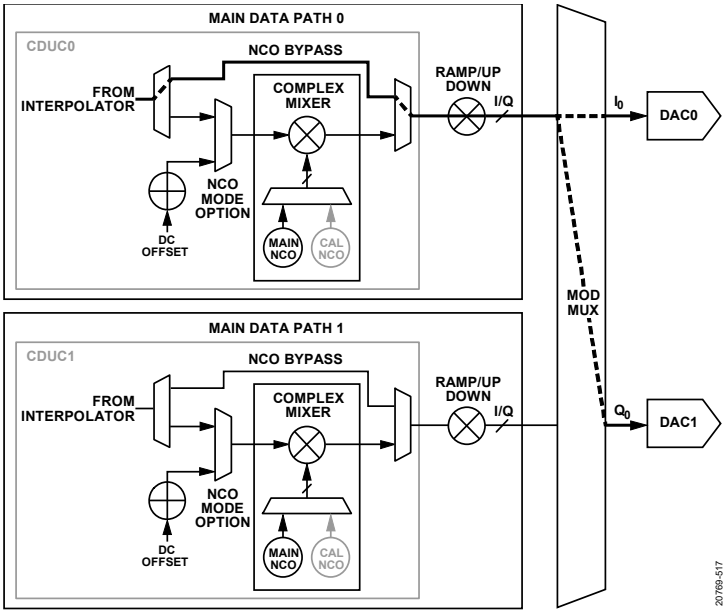

Figure 81. Mod Mux Configuration 2—DAC0 = I_0, DAC1 = Q_0

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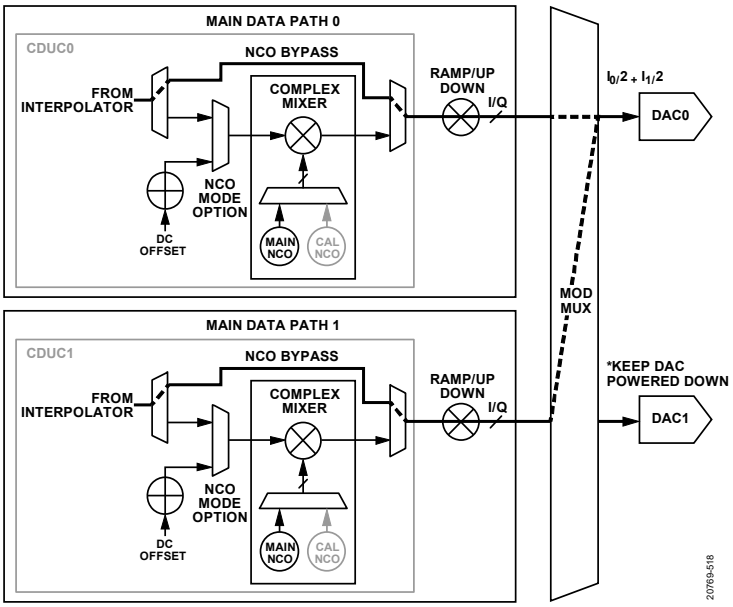

Figure 82. Mod Mux Configuration 3, DAC0 = (I_0 + I_1)/2, DAC1 = Invalid (Keep DAC Core Powered Down)

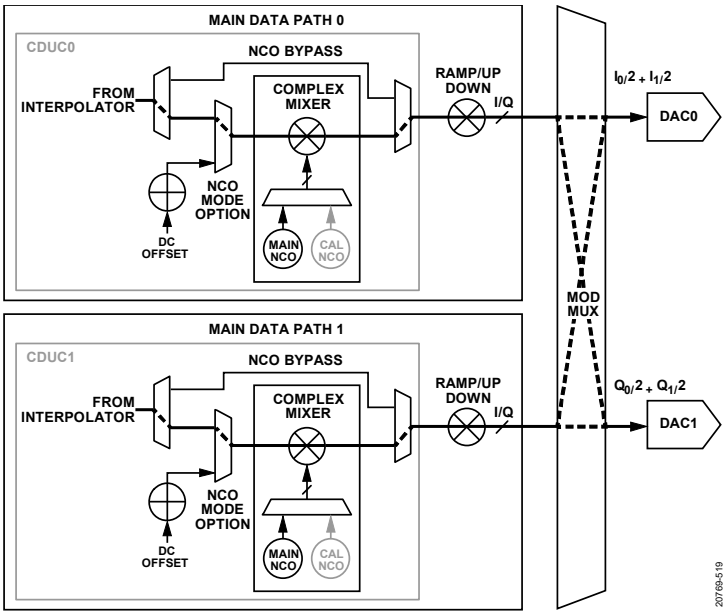

Figure 83. Mod Mux Configuration 3A, EN_CMPLX_MOD = 1, all NCOs Enabled—DAC0 = (I_0 + I_1)/2, DAC1 = (Q_0 + Q_1)/2

TRANSMIT DIGITAL DATAPATH AND OUTPUT

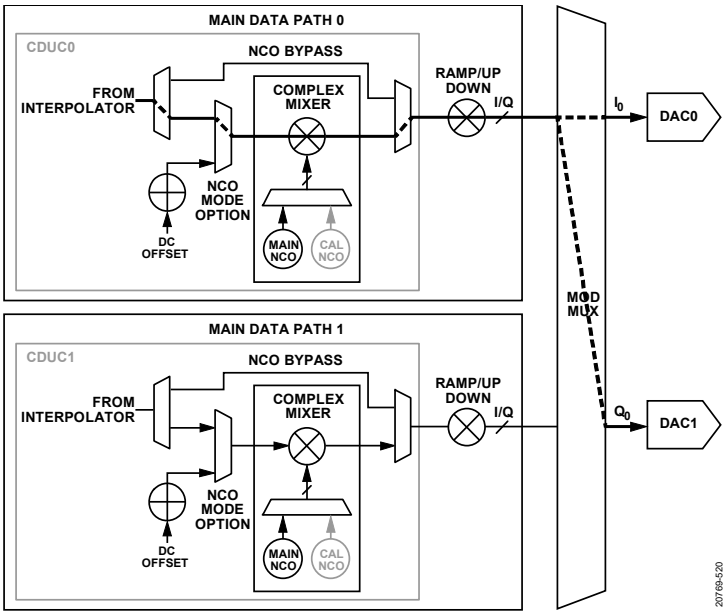

Figure 84. Mod Mux Configuration 3B, EN_CMPLX_MOD = 1, NCO of CDUC1 Disabled—DAC0 = I_0, DAC1 = Q_0

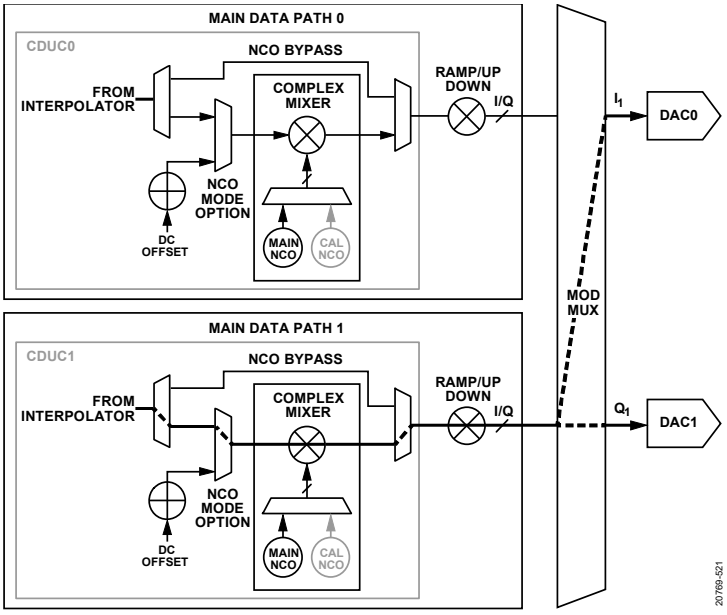

Figure 85. Mod Mux Configuration 3C, EN_CMPLX_MOD = 1, NCO of CDUC0 Disabled—DAC0 = I_1, DAC1 = Q_1

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Table 105. DAC0 and DAC1 Outputs for Different Mod Mux Settings, Mod Mux 0 or Mod Mux 1

Configuration	Register 0x01C9, Bit 6 (EN_COMPLEX_MOD)	Register 0x01C9, Bits[5:4] (DDSM_MODE)	Register 0x01C9, Bit 3	
			NCO0[1] Enable	NCO1[2] Enable
Configuration 0	0	0	1	1
Configuration 1	0	1	0	0
Configuration 2	0	2	0	0
Configuration 3	0	3	1	1
Configuration 3A	1	3	1	1
Configuration 3B	1	3	1	0
Configuration 3C	1	3	0	1

[1] NCO0 is internal to the CDUC0 block and it is connected to Mod Mux 0. When configuring Mod Mux 1, page to configure NCO2 instead.

[2] NCO1 is internal to the CDUC1 block and it is connected to Mod Mux 0. When configuring Mod Mux 1, page to configure NCO3 instead.

Mod Multiplexer API

The API supports the mod multiplexer with the adi_ad9081_dac_ mode_set and adi_ad9081_dac_mode_switch_group_select_set functions, which are exposed via the **adi_ad9xxx.h** header file.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

DAC OUTPUTS

The four DACs each provide complementary current outputs, DACxP and DACxN, where x = 0, 1, 2, or 3. Figure 86 shows an equivalent output circuit for the DAC. The DAC outputs feature two internal, 50 Ω termination resistors (R_{INT}). To achieve optimal performance for ac-coupled applications, use a balun that provides a DC bias path to analog ground. This allows placing the balun as close as possible to the DAC output on the PCB. Alternatively, the DAC output may be biased with a pair of choke inductors to analog ground, as shown in Figure 87. This may be an adequate solution for applications where the balun of choice does not provide a DC bias path to analog ground.

To eliminate aging effects on the output stage over device life, the active MSB current sources must be slowly rotated. The rate of rotation is slower than when MSB shuffle is enabled. See the MSB Shuffle section for more details.

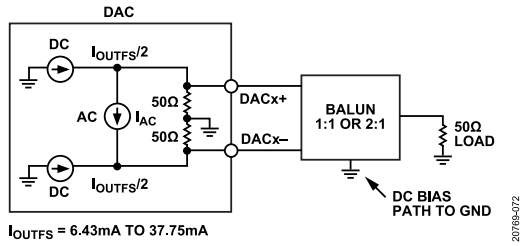

Figure 86. Equivalent DAC Output Circuit and Recommended DAC Output Network

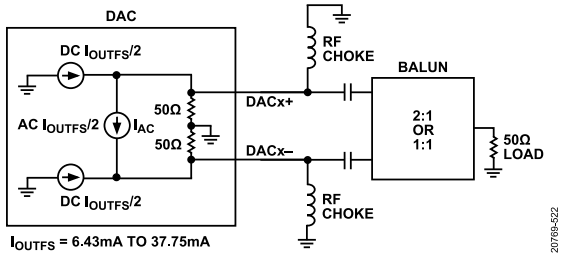

Figure 87. Equivalent DAC Output Circuit and Optional DAC Output Network

I_{OUTFS} is the full-scale current of each of the four DAC outputs. I_{OUTFS} has a nominal default setting of 26 mA but can be set over a range of 6.43 mA to 37.75 mA using the 4-bit FSC_MIN_CTRL bit field and 10-bit FSC_CTRL bit field. The DACPAGE_MSK bit field selects the desired

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DAC(s) to be programmed. FSC_MIN_ CTRL sets an offset current and FSC_CTRL sets the full-scale level above this offset. The following equations show the relationship between I_{OUTFS} and these bit field settings:

I_{FSC_MIN} = (FSC_MIN_CTRL/16) × 25

$I_{OUTFS} = I_{FSC\_MIN}$+ (FSC_CTRL/1024) × 25

For an I_{OUTFS} of 37.75 mA, set Register 0x117 = 0xA and Register 0x118 = 0xFF. Note that the maximum FSC_MIN_ CTRL setting is limited to 0xA (or decimal 10).

The DAC output can be modeled as a pair of DC sources that source half of the I_{OUTFS} current to each output and a differential ac current source that has a peak level of $I_{OUTFS}/2$ (see Figure 86). The value of this AC source (I_{AC}) depends on the DAC code data, DACCODE, which represents the signal sample that is latched into the DAC core following each DAC clock cycle.

This relationship is shown in the following equation:

$I_{AC} = (DACCODE-32768)/65535 \times I_{OUTFS}/2$

where:

DACCODE = 0 to 65535 (decimal).

I_{AC} is typically defined in mA and assumes positive and negative values.

This ideal equivalent model of the DAC output does not account for the parasitic capacitances and inductances of the DAC output stage. Refer to the DAC Output Impedance Characteristics section for more details. Table 106 lists the SPI bit fields used to control the DAC analog output setting, including the power down of individual DAC cores.

Table 106. Bit Fields Used to Configure DAC

Address	Bits	Bit Name
0x001B	[3:0]	DACPAGE_MSK
0x0090	[7:4]	DAC_POWERDOWN
0x0117	[7:4]	FSC_MIN_CTRL
0x0117	[1:0]	FSC_CTRL[1:0]
0x0118	[7:0]	FSC_CTRL[9:2]
0x0143	5	MSB_ROTATION_EN
	[4:0]	MSB_ROTATION_SPD
0x0140	4	MSB_MODE

DAC Outputs API

The following API functions support control of the DAC outputs: ad9081_dac_select_set, adi_ad9081_dac_fsc_set, and adi_ad9081_dac_power_up_set functions. For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is a part of the API release package, Revision 1.1.0 or later.

DAC Output Impedance Characteristics

Because of parasitic capacitances and inductances at the output stage, a constant 100 Ω termination impedance cannot be maintained across the full operating frequency range of the DAC output. Whereas Figure 86 represents an ideal DAC output model, Figure 88 shows the typical differential S11 characteristics of the DAC outputs. Note that DAC0 and DAC3 differential trace inside the package laminate that is 2.3 mm longer than the DAC1 and DAC2 differential traces, which explains the differences in S11 characteristics between the DAC cores at higher frequencies. If symmetrical frequency responses among all DACs is desired, add 2.3 mm of trace length to the DAC1 and DAC2 traces leading to the first component on the PCB, such as the choke inductors or the balun.

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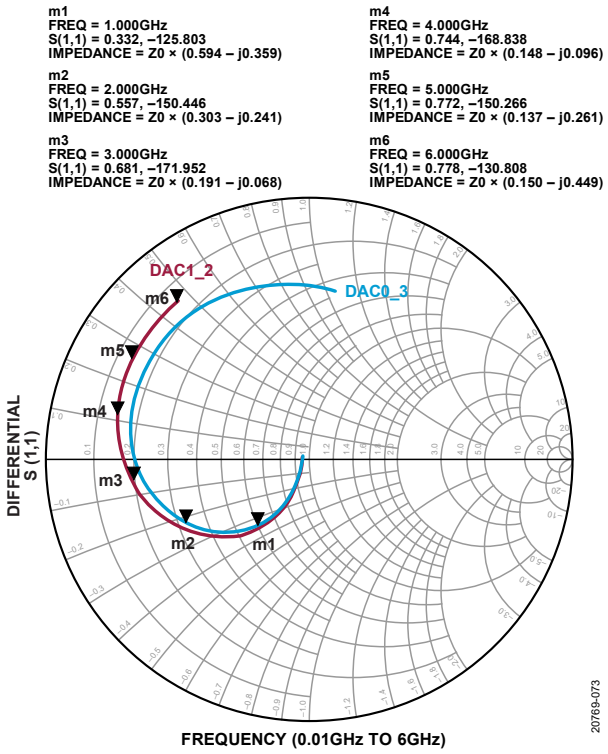

Figure 88. Smith Chart with Differential S11 of DAC Outputs Normalized to 100 Ω

Figure 89 shows the equivalent parallel resistance of the DAC, as derived from S11. The resistance can vary considerably over frequency. When matching the DAC differential output to a single-ended 50 Ω load, use the following guidelines:

- For best RF performance, use an AC analysis model when optimizing the frequency response to an external component (such as a balun), along with an extracted PCB layout model. Keysight ADS models are available from ADI, which include an AC analysis model and the S-parameters of the DAC output.
- A 1:1 balun is recommended when operating below 4.2 GHz. Balun example include the Marki Microwave BALH-0009 and the Mini-Circuits TCM1-83X, although the balun choice is typically dictated by the application.
- A 2:1 balun is recommended when operating above 3.4 GHz. Balun examples include the Murata LDB184G6BAAEA048 LTCC balun, although the balun choice is typically dictated by the application.
- Place the balun as close as possible to the DAC output pins using a tightly coupled, 50 Ω differential traces. This ensures the lowest pass-band ripple and highest output bandwidth.
- Consider the amplitude and phase balance of the balun over the frequency region of interest, especially when a frequency region can be limited by an aliased even order harmonic such as the 2nd harmonic.

TRANSMIT DIGITAL DATAPATH AND OUTPUT

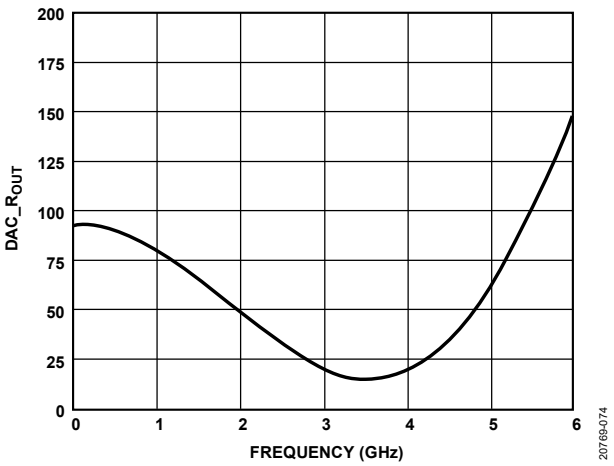

Figure 89. DAC1 and DAC2 Equivalent Parallel DAC Differential Output Resistance vs. Frequency

Because the output impedance of the DAC is complex, comprised of a resistive and a reactive component, the actual rms power delivered across a balun to a 50 Ω nominal load depends on the operating frequency. The rms power delivered to the load is influenced by the following factors:

- Proper PCB layout, balun selection, and balun placement on the PCB, which together impact the quality of the match between the 50 Ω load and DAC output impedance.
- The DAC sinc response due to signal reconstruction using a finite DAC sampling rate.
- The I_{OUTFS} setting. Doubling the I_{OUTFS} setting results in a 6 dB increase in output power.
- The digital gain setting relative to the full-scale digital output of 0 dBFS
- The characteristics of the reconstructed waveform defined by its crest factor or peak-to-average power ratio (PAPR). A signal with a high PAPR results in a lower rms power.

Figure 90 shows the frequency response of the BALH-009 measured on the FMCA evaluation board and the TCM1-83X and LDB184G6BAAEA048 measured on the FMCB evaluation board with the DAC operating at 12 GSPS and I_{OUTFS} of 26 mA.

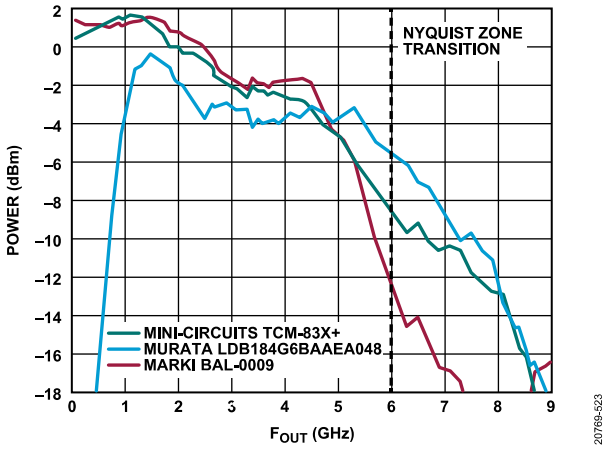

Figure 90. DAC Frequency Response with 12 GSPS Update Rate for Different Baluns with Optimized PCB Layouts

DC-Coupled Operation

DC coupling is often required in applications interfacing to quadrature modulators (or an upconverter). In these applications, keep the common-mode voltage near 0V and no greater than 300 mV. Note that the third-order nonlinearity of the DAC degrades as the common-mode voltage increases from 0 V to 300 mV. Figure 91 shows an example interface where the quadrature modulator allows 25 Ω external resistors to set the differential and common-mode input resistance. In this example, the DAC I_{OUTFS} is set to 20 mA, which results in a V_{CM} = 0.3 V.

TRANSMIT DIGITAL DATAPATH AND OUTPUT

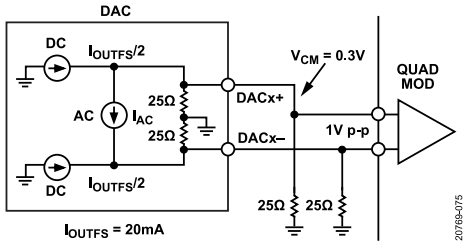

Figure 91. DC Coupling to RF Quadrature Modulator Example

MSB Shuffle

The number of DAC MSB current sources used to reconstruct a digital waveform depends on its digital full-scale level. The amount of switching activity per current source segment depends on the histogram characteristics of the waveform. Depending on these waveform characteristics, some DAC MSB current sources can remain static (unused) or seldom used. Any mismatch errors specific to the few dynamic MSBs used for signal reconstruction can appear as a degradation in spurious free dynamic range (SFDR) performance of the analog outputs, particularly at lower signal levels when only a few MSB sources are active.

Typically, SFDR performance improves when the active MSBs are continuously remapped (or shuffled) and randomly selected from the total number of MSBs available to reconstruct the signal. MSB shuffling is a form of error averaging because the cumulative errors are pseudorandom as a result. The improved SFDR performance comes at the expense of higher noise spectral density. MSB shuffling becomes more effective as more static MSBs are available so that these MSBs can be randomly switched in. The effectiveness diminishes as the signal level increases and the number of dynamic MSBs increases as a result. To enable MSB shuffling, set the MSB_MODE bit field to 1 (Register 0x0140, Bit 4).

MSB Rotation

Whenever MSB_MODE = 0 (MSB shuffle disabled), enable an automatic MSB rotation by setting MSB_ROTATION_EN = 1 (Register 0x0143 bit 5). This bit slowly rotates the pattern of MSBs to ensure equal aging and consistent performance over device life. MSB_ROTATION_EN may remain set whether shuffle is enabled or disabled.

MSB Shuffle API

The MSB shuffle feature is enabled by default by the API during the transmit datapath configuration process using the adi_ad9xxx_device_startup_tx.

AUXILIARY FEATURES

RECEIVE AGC ASSIST FUNCTIONS

Receiver applications require a mechanism available to reliably determine when the ADC full-scale input is about to be exceeded because clipping can lead to severe degradation of a receiver blocker performance. The standard overrange bit in the JESD204B/ JESD204C output data stream provides information on the state of the analog input, but has significant latency associated with the complete digital datapath to allow the receiver to react to input signals that have significant slew rates or envelope responses.

A fast detect circuitry for each ADC (or ADCn where n = 0, 1, 2, or 3) monitors if the input signal falls above or below an upper and lower threshold, upon which a logic indicator bit is triggered and transitions from 0 to 1. The logic indicator bit can be directed to the JESD204B/C transport layer to be inserted as a control bit or to the external ADCx_FD0 pin and ADCx_FD1 pin to be monitored by a host processor for the lowest possible latency. The latency in ADC clock cycles from when the input signal passes a threshold to when these external pins transition high is 102 cycles for the AD9081 and 106 cycles for the AD9082. The ADCn_FD1 is an optional additional indicator bit with associated threshold and dwell time.

The fast detector circuitry is highly configurable using SPI registers. Table 107 and Table 109 list the bit fields used to configure this block and the corresponding register and bit assignments. Note that some of these bit field names span across two registers with the suffix of MSB and LSB used to delineate the upper and lower bit fields.

The settings for each ADC can be set independently using the ADCx_PAGE bits. The FD_FINE_EN_GPIO bit determines whether the detector is enabled by the FD_FINE_EN bit or by an external signal applied to a GPIOx pin. Consider using an external enable signal for AGC implementations that require the AGC operation to be gated. For continuous operation, set the FD_FINE_EN bit to 1 and the FD_FINE_EN_GPIO to 0. Note that the ADCn_FD pins are pulled low and the fast detector circuitry disables.

Table 107. AGC Fast Detect Assist Registers

Address	Bits	Bit Name
0x018	[3:0]	ADCx_PAGE
0x330	6	FD_GPIO2_THRESH2
	5	FD_FINE_EN_GPIO
	2	FD_FINE_EN
0x331	[7:0]	FD_UP_THRESH_LSB
0x332	[2:0]	FD_UP_THRESH_MSB
0x333	[7:0]	FD_LOW_THRESH_LSB
0x334	[2:0]	FD_LOW_THRESH_MSB
0x335	[7:0]	FD_DWELL_THRESH_LSB
0x336	[7:0]	FD_DWELL_THRESH_MSB
0x337	[7:0]	FD_DWELL_THRESH2_LSB
0x338	[7:0]	FD_DWELL_THRESH2_MSB
0x339	[7:0]	FD_DWELL_THRESH_UP_LSB
0x33A	[7:0]	FD_DWELL_THRESH_UP_MSB
0x33B	[7:0]	FD_LOW_THRESH2_LSB
0x33C	[2:0]	FD_LOW_THRESH2_MSB
0x33D	[7:0]	FD_UP_THRESH2_LSB
0x33E	[2:0]	FD_UP_THRESH2_MSB
0x352	4	FD0_FUNC_SEL
	[3:2]	FD_1_SEL
	[1:0]	FD_0_SEL

The ADCx_FD0 supports additional threshold shown in Figure 94. Table 108 shows the bit field value to enable the upper threshold.

Table 108. ADCx_FDC0 functions

Bit Name	Value	Internal ADCn_FD Signal Route to External Pin
FD0_FUNC_SEL	00	ADCx_FD0 uses both the upper and lower threshold
	01	ADCx_FD0 uses only the upper threshold

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The default setting has the respective ADCx_FD0 and ADCx_FD1 indicator signals mapped to the respective pin assignment that shares the same name. In the unlikely event that the default mapping must be modified, the FD_1_SEL and FD_0_SEL bits. Table 109 shows the bit field values required to remap indicator signals to different pins

Table 109. Remapping of FD0 and FD1 Internal Signals to External Pins Using FD_0_SEL and FD_1_SEL

Bit Name	Value	Internal ADCn_FD Signal Route to External Pin
FD_0_SEL	00	Route to ADC0_FD0
	01	Route to ADC1_FD0
	10	Route to ADC2_FD0
	11	Route to ADC3_FD0
FD_1_SEL	00	Route to ADC0_FD1
	01	Route to ADC1_FD1
	10	Route to ADC2_FD1
	11	Route to ADC3_FD1

The indicator bit for the ADCx_FD0 pin (and ADCx_FD1 pin, if used) immediately sets whenever the absolute value of the input signal exceeds the programmable upper threshold level, which is defined by an 11-bit value. The upper three bits of this value pertain to the FD_UP_THRESH_MSB bit field and the lower eight bits correspond to the FD_UP_THRESH_LSB bit field For ADCx_FD1 indicator bit, the corresponding bit fields are FD_UP_THRESH2_MSB and FD_UP_THRESH2_LSB The indicator bit only clears when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. Note that the FD_LOW_THRESH_ MSB and FD_LOW_THRESH_LSB bit fields pertain to the lower 11-bit threshold level of the ADCn_FD0 pin and the ADCn_FD1 lower threshold is set with the FD_LOW_THRESH2_MSB and FD_LOW_THRESH2_LSB bit fields. This lower threshold feature provides hysteresis and prevents the indicator bits from excessive toggling.

The approximate upper threshold magnitude (measured in dBFS) is defined by the following equation:

$$Upper\ Threshold\ Magnitude = 20 \times \log(Threshold\ Magnitude/2^{11})$$

The lower threshold magnitude (also measured in dBFS) is defined by the following equation:

$$Lower\ Threshold\ Magnitude = 20 \times \log(Threshold\ Magnitude/2^{11})$$

For example, to set an upper threshold of −6 dBFS, write 0x3FF to the FD_UP_THRESH bit field. To set a lower threshold of −10 dBFS, write 0x288 to the FD_LOW_THRESH bit field.

To program the dwell time to be from 1 to 65535 sample clock cycles, load the desired 16-bit dwell time value in FD_DWELL_ THRESH_MSB and FD_DWELL_THRESH_LSB.

The dwell counter can start its count when the input signal falls below the lower or upper threshold using the FD0_FUNC_SEL bit. Set this bit to 0 for the lower threshold or 1 for the upper threshold. For the ADCx_FD1, the FD_GPIO2_THRESH2 bit field provides the same start counter configuration options as the FD0_FUNC_SEL bit field. If the dwell time is programmed as zero, the lower threshold is disabled. For example, the ADCn_FD1 and ADCn_FD0 indicator outputs go low immediately when the samples fall below the upper threshold.

Fast Detect Mode Configuration Examples

The first example shown in Figure 92 uses the ADCn_FD0 pin and the dwell counter starts when the input signal falls below the lower threshold that is defined by the FD_LOW_THRESH_MSB and FD_LOW_THRESH _LSB bit fields. This example operates as follows:

- The ADCn_FD0 output immediately sets when the absolute value of the input signal exceeds the programmable upper threshold level.
- The dwell time counter starts when the ADCn_FD0 output is high and the input signal falls below the lower threshold.
- The dwell time counter resets if the samples go beyond the lower threshold.
- If the samples remain below the lower threshold for the duration the dwell time counter takes to reach the programmed dwell time, the ADCn_FD0 output is pulled low.

The second example shown in Figure 93 uses the ADCn_FD1 pin with an external active high signal (FD_EN) to allow the fast detect circuitry to be gated by the host processor. Note that the ADCn_FD0 pin is also gated by FD_EN had this pin been selected as well, which is also the case in the first example.

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The FD_EN input signal is connected to a user selectable GPIOx pin (refer to

Table 126 for the pin assignment). When this external signal is low, the ADCn_FD1 (and ADCn_FD0) outputs remain low. This example operates as follows:

- The ADCn_FD1 output immediately sets when the absolute value of the input signal exceeds the programmable upper threshold level.
- The dwell time counter resets when the input signal falls below the upper threshold.
- The dwell time counter resets if the sample values cross over the upper threshold and starts counting again when the signal falls below the upper threshold.
- If the samples remain below the upper threshold for the duration the dwell time counter takes to reach the programmed dwell time, the ADCn_FD1 output is pulled low.

The third example shown in Figure 94 uses both the ADCn_FD0 and ADCn_FD1 indicators with the respective dwell counters set to 0. In this case, only the upper threshold setting is used for each indicator. The ADCn_FD0 indicator is set to go high when the upper threshold is exceeded and low when the signal falls below this threshold. The ADCn_FD1 indicator is set to go high when the input signal falls below the upper threshold and high when the signal exceeds this threshold.

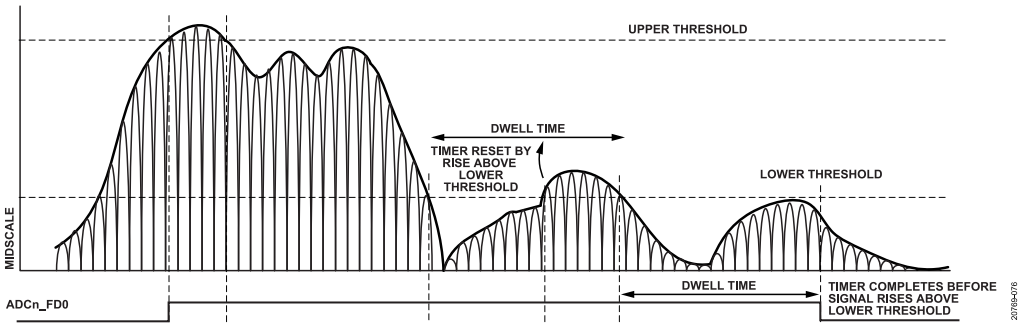

Figure 92. Example 1, Dwell Counter Starts when Input Signal Falls Below the Lower Threshold

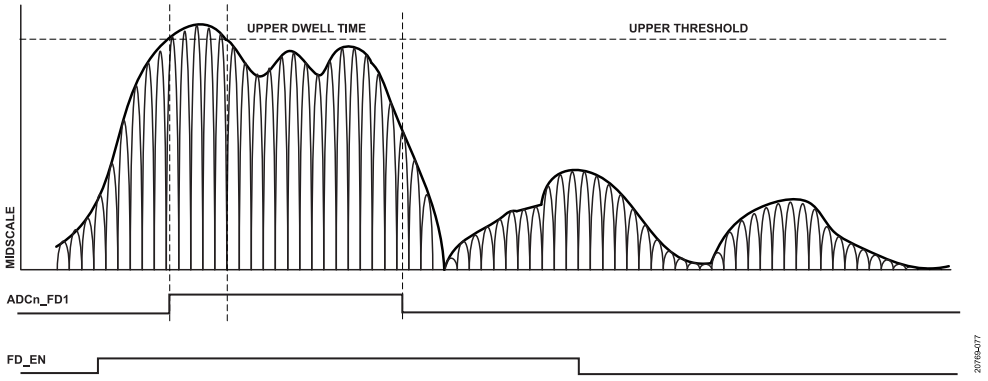

Figure 93. Example 2, Gated FD_EN Input Signal and Dwell Counter Start when Input Signal Falls Below the Upper Threshold

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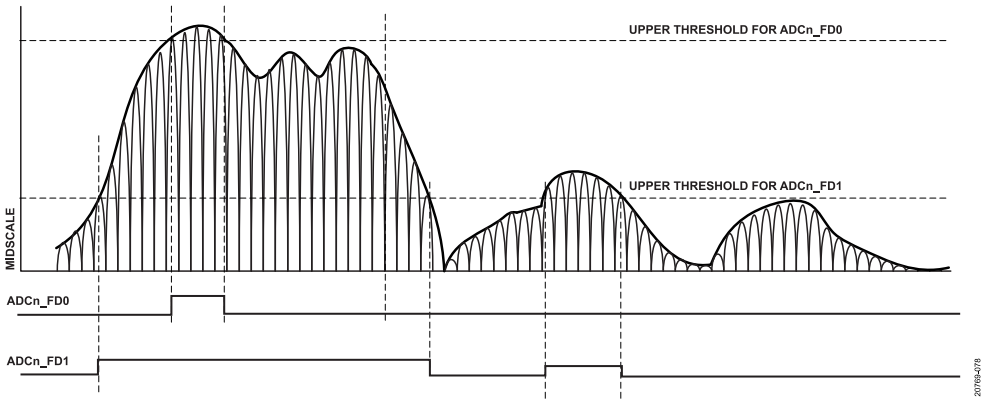

Figure 94. Example 3, ADCn_FD0 and ADCn_FD1 Indicators Enabled and Dwell Counter Set to 0

Signal Monitor Block

The signal monitor block provides additional statistical information on the signal that is digitized by the ADC and can be used as an additional input for AGC implementations. The signal monitor computes the peak magnitude of the digitized signal over a defined period of time and transfers this value to the host via the JESD204B/C interface as separate control bits. Like the fast detection block, the signal monitor also provides an option to set lower and upper thresholds that cause an indicator signal to be triggered when the value is exceeded and sent to an external pin that is monitored by the host processor.

Table 110 lists the names of the bit fields used to configure this block and the corresponding register and bit assignments. Like the fast detect threshold block, each ADC can be set independently using the ADCn_PAGE bit field. Note that some of the bit field names span across multiple registers and the highest number embedded in the bit field name signifies the MSB. For instance, the SMON_PERIOD bit field consists of a 32-bit word with the upper 8 MSBs loaded into the SMON_PERIOD3 bit field and the lower 8 LSBs loaded into the SMON_PERIOD0 bit field.

Figure 95 shows a simplified block diagram of the signal monitor block. The peak detector captures the largest signal within the 32-bit observation period set in the SMON_PERIOD bit field. Note the signal monitor block must only be enabled after the observation period is set by setting the SMON_PEAK_EN bit field. The detector only observes the magnitude of the signal. The resolution of the peak detector is an 11-bit value. To calculate the peak magnitude (measured in dBFS), use the following equation:

$$Peak\ Magnitude = 20 \times \log(Peak\ Detector\ Value/2^{11})$$

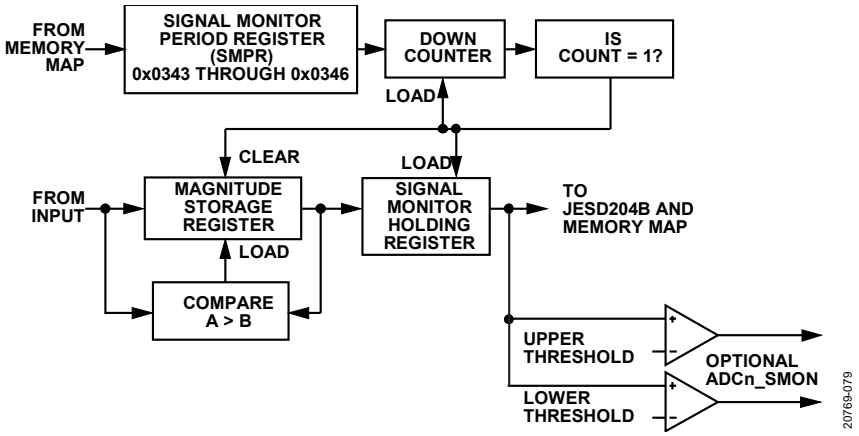

Figure 95. Signal Monitoring Block

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Table 110. AGC Signal Monitoring Registers

Address	Bits	Bit Name
0x341	[2:1]	SMON_SFRAMER_MODE
	0	SMON_CLK_EN
0x342	[7:0]	SMON_STATUS_FCNT
0x343	[7:0]	SMON_PERIOD_0
0x344	[7:0]	SMON_PERIOD_1
0x345	[7:0]	SMON_PERIOD_2
0x346	[7:0]	SMON_PERIOD_3
0x347	6	SMON_GPIO_EN
	5	SMON_JLINK_SEL
	4	SMON_PEAK_EN
	[3:1]	SMON_STATUS_RDSEL
	0	SMON_STATUS_UPDATE
0x348	[7:2]	SMON_SFRAMER_INSEL
	1	SMON_SFRAMER_MODE
	0	SMON_SFRAMER_EN
0x349	1	SMON_SYNC_NEXT
	0	SMON_SYNC_EN
0x34A	[7:0]	SMON_STATUS
0x34D	[7:0]	SMON_THRESH_LOW0[7:0]
0x34E	[2:0]	SMON_THRESH_LOW1[10:8]
0x34F	[7:0]	SMON_THRESH_HIGH0[7:0]
0x350	[2:0]	SMON_THRESH_HIGH1[10:8]
0x37DA	0	Enable ADCx_SMONx pin

When peak detection mode is enabled, the SMON_PERIOD value is loaded into a monitor period timer that decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user) and the greater of the two values is updated as the current peak level. Note that the initial value of the internal magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 11-bit peak level value is transferred to the signal monitor holding register shown in Figure 95, which can be read through the memory map or transferred over the JESD204B/C interface. The monitor period timer is reloaded with the SMON_PERIOD value and the countdown restarts. In addition, the magnitude of the first input sample is updated in the magnitude storage register and the comparison and update procedure continues.

Similar to the fast threshold detect block, the user can also compare the held peak value with user specified, upper and lower, 11-bit threshold values loaded into the SMON_THRESH_HIGH and the SMON_THRESH_LOW. To direct the indicator signals from the comparator outputs to external pins, set the SMON_GPIO bit. The indicator signal is routed to the ADCn_SMON1 pin and ADCn_SMON0 pin for the AD9082 or substituted for the fast detector indicator and sent to the ADCn_FD1 pin and ADCn_FD0 pin for the AD9081. Figure 96 shows an example of how these signals react to a slow varying envelope response with a short monitoring period. Register 0x37DA, Bit 0 must be set to enable the SMON signal to be output to the corresponding pin.

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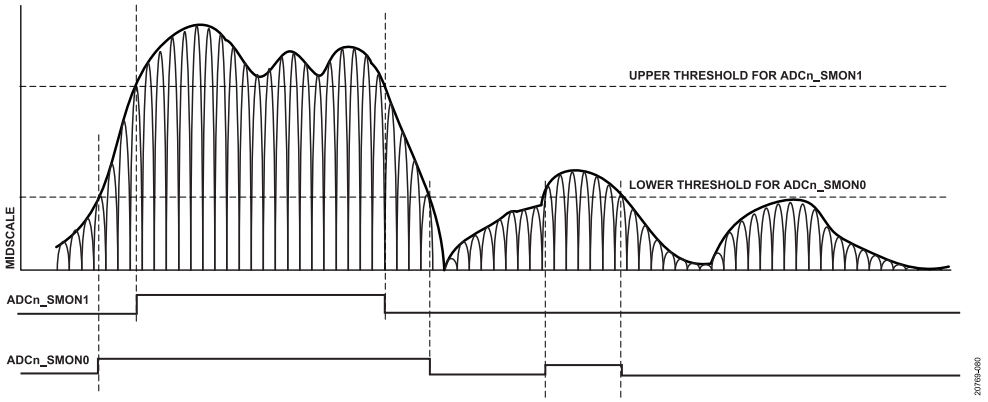

Figure 96. ADCn_SMON Signals Reaction to Crossing User Defined Upper and Lower Thresholds

Signal Monitoring Data Over JESD204B

The signal monitor data can be serialized and sent over the JESD204B/C interface as control bits. The SMON_JLINK_SEL bit specifies what link the data is transferred over. These control bits must be deserialized from the samples to reconstruct the statistical data. To enable the signal control monitor function, set the SMON_ SFRAMER_EN and SMON_SFRAMER_MODE bits. Figure 98 shows two different example configurations for the signal monitor control bit locations inside the JESD204B/C samples.

A maximum of three control bits can be inserted into the JESD204B/C samples, but only one control bit is required for the signal monitor. Control bits are inserted from the MSB to the LSB. If only one control bit is to be inserted (CS = 1), only the most significant control bit is used (see Example Configuration 1 and Example Configuration 2 in Figure 98). Figure 97 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 99 shows the embedded data over the JESD204B signal monitor data with a monitor period timer set to 80 samples.

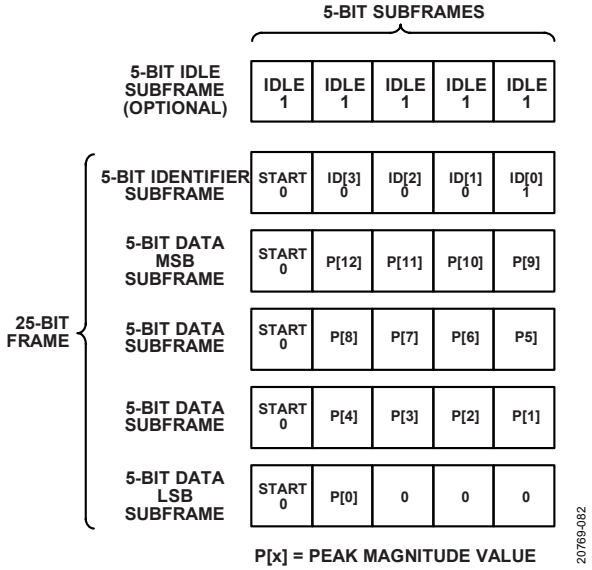

Figure 97. JESD204B or JESD204C Signal Monitor Frame Data

PROGRAMMABLE FILTER (PFILT)

The programmable PFILT filter is an optional signal processing block that enables the user to provide customized FIR digital filtering directly to the wideband signal content represented at the ADC output(s). This block avoids the need to perform the same function in an ASIC or FPGA, which allows the user to take full advantage of the digital filtering capability in the receive datapath. The net result of using this filter is that

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considerable power and cost savings (reduced MOPS and FPGA processing overhead) can be realized on an FPGA or ASIC. Table 111 lists the bit fields used to configure this block and the corresponding register and bit assignments.

Both the AD9081 and AD9082 support the PFILT block with the same number of coefficients. The PFILT implementation in the AD9082 supports a maximum sample rate of 6 GSPS, and the implementation in the AD9081 supports a maximum sample rate of 4 GSPS.

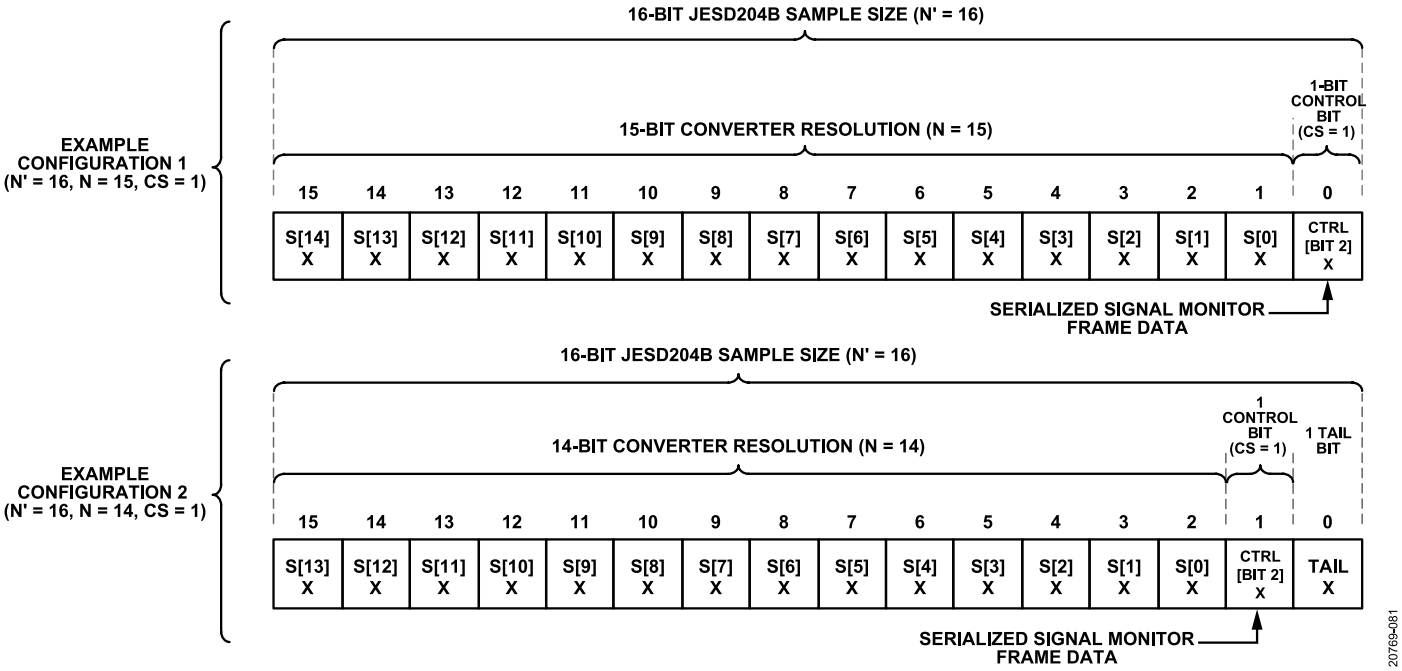

Figure 98. Signal Monitor Control Bit Locations

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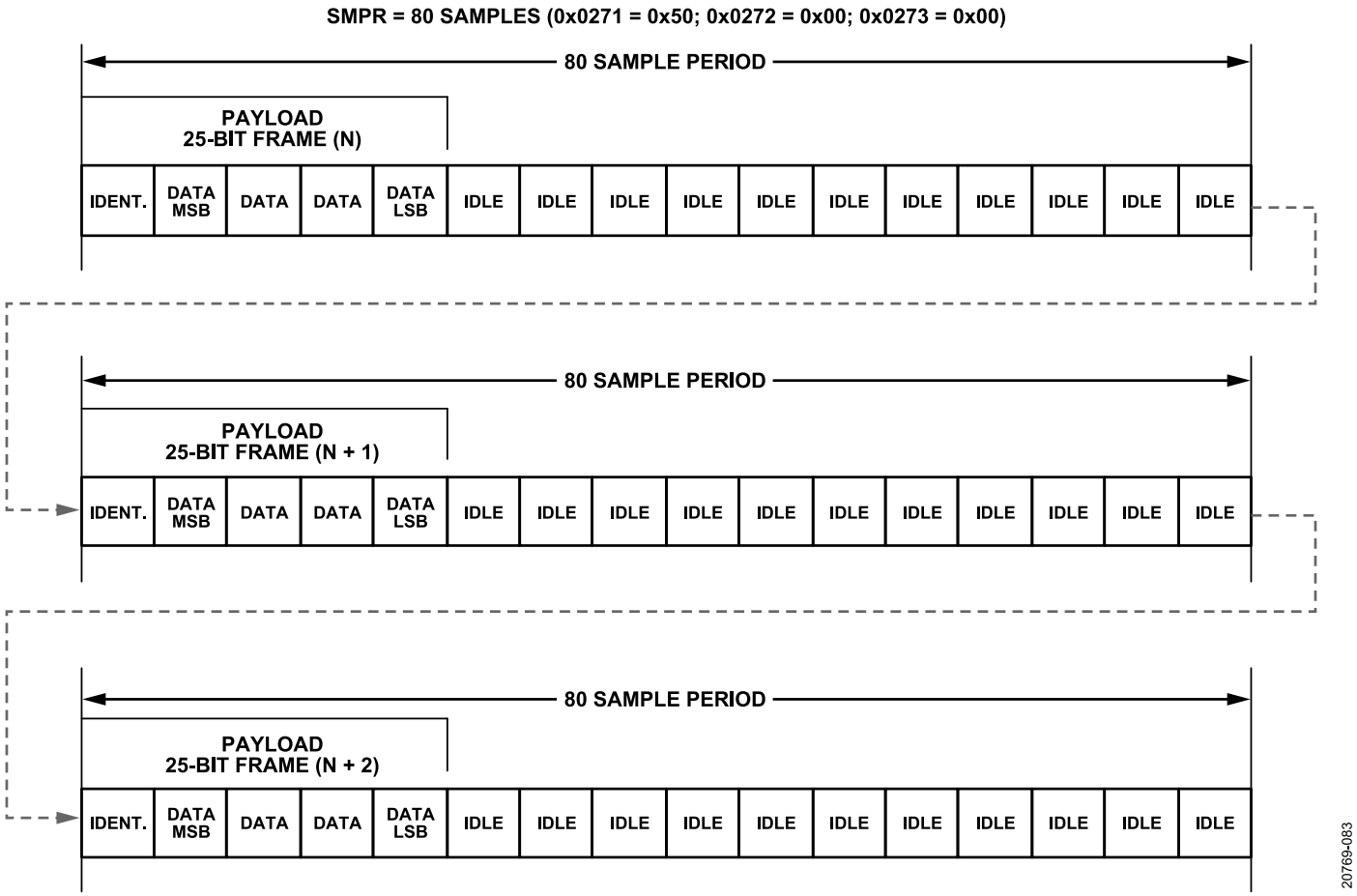

Figure 99. JESD204B or JESD204C Signal Monitor Example with 80-Sample Period

Table 111. Programmable FIR Filter Control Registers

Address	Bits	Bit Name	Description
0x01E	1	PFILT_ADC_PAIR1_PAGE	Paging Bit for PFILT corresponding to ADC Pair 1 and ADC Pair 0.
	0	PFILT_ADC_PAIR0_PAGE	
0x01F	3	PFILT_COEFF_PAGE3	Paging Bits for PFILT Coefficient Bank 3 through Coefficient Bank 0.
	2	PFILT_COEFF_PAGE2	
	1	PFILT_COEFF_PAGE1	
	0	PFILT_COEFF_PAGE0	
0xC0C	7	Reserved	
	[6:4] [2:0]	PFILT_Q_MODE PFILT_I_MODE	The PFILT_Q_MODE and PFILT_I_MODE bit fields select the filter mode for the I and Q filters, as described in the Supported Modes in the AD9082 section and the Supported Modes in the AD9081 section. 000: disabled (filters bypassed). 001: real N/4 tap filter for I channel. 010: real N/ I channel. 011: reserved. 100: N/4 tap Matrix mode of operation (pfilt_q_mode must also be set to 100) 101: N/3 tap Full Complex Filter (pfilt_q_mode must also be set to 101) 110: Half Complex Filter using N/2-Tap Filters for the Q channel + N/2 Tap Programmable Delay Line for the I Channel.(pfilt_q_mode must also be set to 010) 111: Real N Tap Filter for the I (pfilt_q_mode must be set to 000)
0xC0D	[5:3]	PFILT_B_GAIN	PFILT I/Q Gain Scaling (twos complement).

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Table 111. Programmable FIR Filter Control Registers (Continued)

Address	Bits	Bit Name	Description
	[2:0]	PFILT_A_GAIN	110: −12 dB loss.
0xC0F	[5:3]	PFILT_D_GAIN	111: −6 dB loss.
	[2:0]	PFILT_C_GAIN	000: 0 dB gain. 001: 6 dB gain. 010: 12 dB gain. 0x100 to 101 and 011: undefined.
0xC11	[7:0]	DELAY_SETTING	Delay Setting for Half Complex Mode.
0xC17	0	PFILT_COEFF_TRANSFER	Coefficient Transfer Signal. 0 to 1 transition transfers all coefficients from the main registers to the subordinate registers.
0xC1A	[6:0]	HC_PROG_DELAY	Programmable delay for group delay balancing the bypassed channel with filtered channel in half complex mode
0xC1C	0	QUAD_MODE	0: AD9082
			1: AD9081
0xC1D	7	GPIO_CONFIG1	Main Coefficient Bank Selection via GPIOx Pins when Enabled. Otherwise, controlled via the RD_COEFF_PAGE_SEL bit field (Register 0xC1E, Bits[1:0]).
	6	VLE_COEFF	Input Coefficients VLE Encoded.
	5	COEFF_CLEAR	Clears the currently selected main coefficient bank.
	4	COMPLEX_LOAD	Set these bits according to the type of coefficients being streamed via SPI.
	3	REAL_CROSS_Q_LOAD	
	2	REAL_CROSS_I_LOAD	
	1	REAL_Q_LOAD	
	0	REAL_I_LOAD	
0xC1E	[1:0]	RD_COEFF_PAGE_SEL	Selects the coefficient page for PFILT.

Supported Modes in the AD9082

The following modes of operation, where N = up to 192 taps, are supported (note that the asterisk symbol (*) denotes convolution)

Real N/2-tap filter for each I/Q channel (see Figure 100).

- DOUT_I[n] = DIN_I[n] × A[n]
- DOUT_Q[n] = DIN_Q[n] × D[n]

Single Real N-tap filter for either the I or the Q channel (see Figure 101).

- DOUT_I[n] = DIN_I[n] × A[n]
- or DOUT_Q[n] = DIN_Q[n] × D[n

Half complex filter using two real N/2-tap filters for the I/Q channels (see Figure 102).

- DOUT_I[n] = DIN_I[n]
- DOUT_Q[n] = DIN_Q[n] × D[n]] + DIN_I[n] × B[n]

N/3-tap complex filter for the I/Q channels (see Figure 103).

- DOUT_I[n] = DIN_I[n] × B[n]- DIN_I[n] × A[n]+ DIN_Q[n] × B[n]]
- DOUT_Q[n] = DIN_I[n] × B[n]] + DIN_Q[n] × B[n]- DIN_Q[n] × C[n]

Full complex filter using four real N/4-tap filters for the I/Q channels (see Figure 104).

- DOUT_I[n] = DIN_I[n] × A[n] + DIN_Q[n] × C[n]
- DOUT_Q[n] = DIN_I[n] × B[n] + DIN_Q[n] × D[n]

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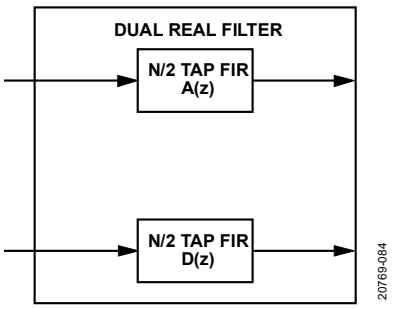

Figure 100. Two Real N/2-Tap Filters

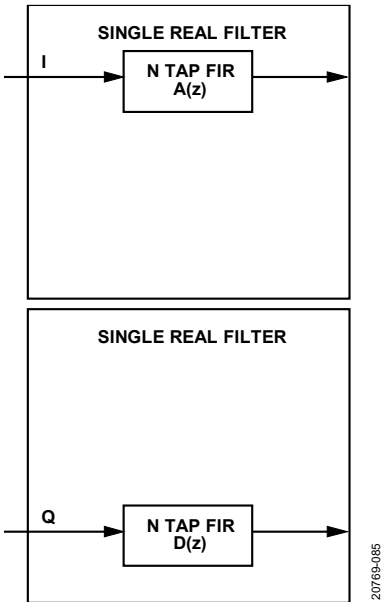

Figure 101. Single Real Coefficient FIR Filter on the I or the Q channel

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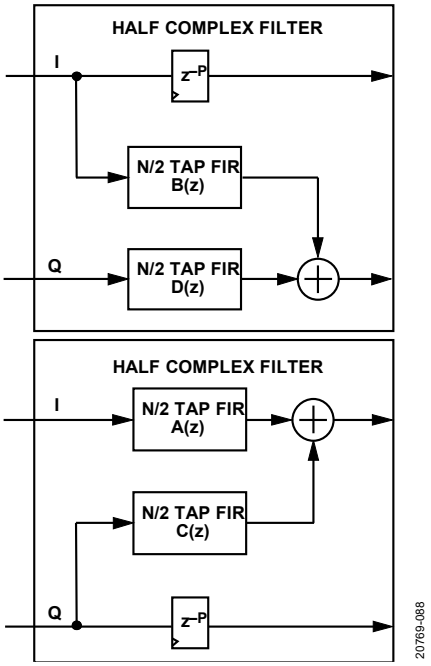

Figure 102. 96-Tap Half Complex Filter

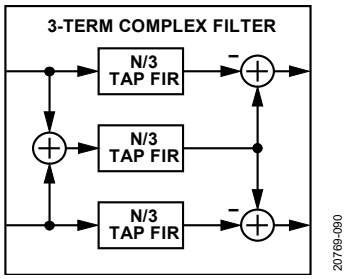

Figure 103. N/3-Tap Complex Filter

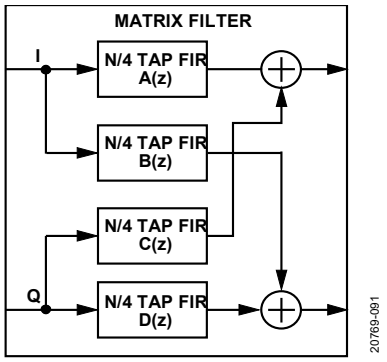

Figure 104. Full Matrix Filter with N/4-Taps per FIR

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Supported Modes in the AD9081

In the AD9081, the PFILT takes in data from two ADC pairs (or two sets of I/Q channels) and performs the filtering. To enable this mode, set the QUAD_MODE bit (Register 0x0C1C, Bit 0).

The same total number of coefficients are available for the AD9081.

The two ADC pairs can be configured to be in different modes. For example, one ADC pair can be in complex mode and the other can be in real mode, as shown in Figure 105.

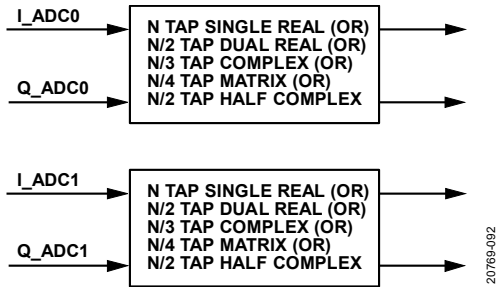

Figure 105. Supported PFILT Modes in the AD9081 Filter Modes, ADC Mapping, and Input Rates

Table 112 and Table 113 show the different supported filter modes for the AD9081 and AD9082, respectively.

Table 112. PFILT Operating Modes Supported on the AD9081

Filter Mode	Support
Full Complex Filter	Two 64-tap full complex filter, one for each I/Q pair.
Matrix Mode	Two 48-tap matrix filter, one for each I/Q pair, 48 taps for each filter (A, B, C, and D), as shown in Figure 104.
Half Complex	Two 96-tap half complex filter, one for each I/Q pair, 96 taps for each for cross term and direct term.
48-Tap Real Filter Mode	Four 48-tap real filters, one for each ADC.
96-Tap Real Filter Mode	Four 96-tap real filters, one for each ADC.
192-Tap Real Filter Mode	Two 192-tap real filters on two ADCs. Full chip multiplexing can determine if the filters can be on any two ADCs or if there are any restrictions.

Table 113. PFILT Operating Modes Supported on the AD9082

Filter Mode	Support
Full Complex Filter	Single 64-tap full complex filter.
Matrix Mode	Single 48-tap matrix filter, 48 taps for each filter (A, B, C, and D), as shown in Figure 104.
Half Complex	Single 96-tap half complex filter, 96 taps for each for cross term and direct term.
48-Tap Real Filter Mode	Two 48-tap real filters, one for each ADC.
96-Tap Real Filter Mode	Two 96-tap real filters, one for each ADC.
192-Tap Real Filter Mode	One 192-tap real filter, only on one ADC.

Use Case Scenarios to Filter Modes Mapping

The optimum filter configuration depends on the usage case. Possible usage cases for the different PFILT configurations include the following:

- Equalization of analog impairments: the PFILT can be used to compensate for gain and/or phase impairments vs. frequency. This usage case can either be for real signals or for complex signals. For real sampling applications one FIR filter is used for each converter. This usage case either uses the single channel real filter when only one converter channel is used or uses the dual real filter mode when two converters are used. In the Dual Channel (not I/Q) Equalization case the channels each use separate real filters to perform compensation over some percentage of the Nyquist band. The PFILT is used in dual real filter mode if this is the only requirement. When the signal that is processed is a complex signal with I/Q components, use either complex filter mode or matrix filter mode. If equalization is all that is desired, complex filter mode (shown in Figure 103) provides more taps for this case.
- Channel-to-channel crosstalk correction mode: the PFILT views the converters as pairs that can be either two real signals or a complex I/Q pair. If the channels are separate real signals, the matrix filter shown in Figure 104 can be used for crosstalk cancelation. In the matrix filter

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configuration, the filters B(z), and C(z) can be used to model the coupling transfer function between the channels and subtract an estimate of the cross talk from the other channel. The A(z) and D(z) filters are programmed with a single nonzero coefficient of decimal 32767 (1 LSB less than full scale) at the appropriate coefficient to compensate for group delay of the cross-term filter. Typically, this coefficient is placed on Tap 0 of the A(z), and D(z) filters.

- Equalization with crosstalk correction: this case is a combination of equalization of analog impairments and channel-to-channel crosstalk correction mode where the matrix mode can again be used. For this the single coefficient of A(z) and D(z) is replaced by a filter transfer function to perform the equalization and C(z) and D(z) perform the crosstalk correction.
- Quadrature error correction: when a complex signal is sampled, then imperfections in the amplitude and phase imbalance of the I/Q signal can be corrected. The most common method for error correction is to use the half complex filter of Figure 102 using the B(z), and D(z) filters. Half complex filter can be used if there is no frequency asymmetry involved and full complex filter if there is frequency asymmetry..

Programmable Gain Scaling

A programmable scalar at the output of each FIR filter can be used to apply a gain or loss in 6 dB steps to account for the gain of the filter coefficients themselves. This is shown in Figure 106. To program the gain or loss information, use the PFILT_I_GAIN and PFILT_Q_GAIN register settings. Table 114 defines the use of these scaling factors for the different filter modes. The coefficients are all 1.15 numbers (signed, 16-bit numbers). The largest coefficient must range from −32768 to +32767. The gain of each FIR filter (A, B, C, and D) can be up to 12 dB and uses the −12 dB scale to normalize.

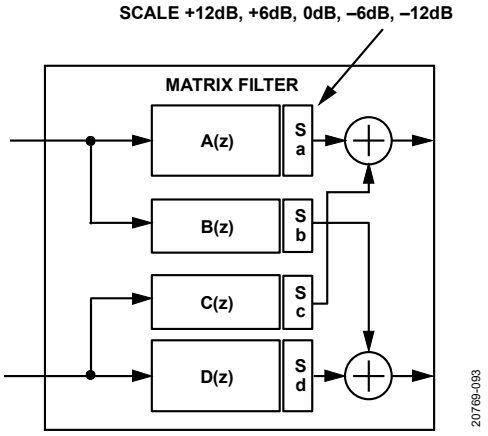

Figure 106. Optional 6 dB/12 dB Scalar Following Each Filter Can Apply a Gain or Loss of 6 dB or 12 dB

Table 114. Use of Gain Scaling Factor

Filter Mode	Scale Factor Usage
Half-Complex	Two independent scale factors, either A/C or B/D.
Matrix	Four independent scale factors for the A, B, C, and D filters.
Dual-Real	Only gains for the A and D filters are used.
Complex	The A and D filters must have the same programming.

Coefficient Bank Description and Fast Updating Between Coefficient Banks

The coefficient table in PFILT uses main/subordinate registers that consist of four sets of main registers and one set of subordinate registers, as shown in Figure 107.

This implementation enables a user to switch between different coefficient sets that may have been configured or optimized for different applications or physical channel impairments. Select the desired coefficient set with either the assigned GPIOx pins (for the fastest update) or the SPI. If using the SPI for selection, use the RD_COEFF_PAGE_SEL control to select the coefficient set and toggle the PFILT_COEFF_TRANSFER bits in Register 0xC17 to transfer the set to the subordinate register.

If using the GPIOx pins for selection, refer to the GPIOx Pin Operation section for more information on the pin assignment as the two internal control signals called I_EQ_Frac0 and I_EQ_Frac1 can be mapped to these GPIO pins. The subordinate register is loaded

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whenever the assigned GPIO pins are toggled. If the assigned GPIOx pins are already at the required value, write explicitly to the PFILT_COEFF_TRANSFER register (Register 0xC17) to update the subordinate coefficient registers from the main registers.

When a coefficient set is selected, a transfer pulse transfers all coefficients together to the subordinate registers, which is the working copy used by the PFILT engine. Having a separate transfer bit ensures that all coefficients used by the filters in the PFILT are changed simultaneously when changing from one set of coefficients to another. Refer to Table 115 and Table 116 for more information.

One of the four sets of coefficients is used by the hardware at a time, and the other three sets are offline and can be updated through the SPI port. Expect a normal filter transient during the coefficient switch. In addition to the normal transient from switching coefficients, invalid data can propagate for a few cycles after the switch. Switching times are provided in Table 117 for different modes.

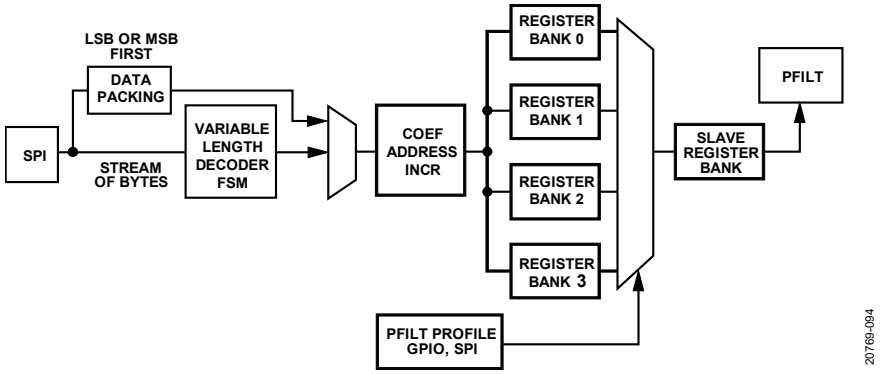

Figure 107. PFILT Streaming Load Options

Table 115. Supported Configurations for the AD9082

Config.	Control Signals	Single Real, Complex, Matrix, or Half-Complex Filter	Two Real Filters
0	I_EQ_Frac0, I_EQ_Frac1	Switching between four set of coefficients	Switching between four sets of coefficients for all filters
1	I_EQ_Frac0	Switching between coefficient Set 1 and Set 0	Switching between coefficient Set 1 and Set 0 for the I filter
	I_EQ_Frac1	Not applicable	Switching between coefficient Set 2 and Set 3 for the Q filter

Table 116. Supported Configurations for the AD9081

Config.	Control Signals	Filter Setup
0	I_EQ_Frac0 and I_EQ_Frac1	Switching between four sets of coefficients for all filters
1	I_EQ_Frac0	Switching between the first I/Q pair
	I_EQ_Frac1	Switching between the second I/Q pair

Table 117. Coefficient Switching Time

Mode	AD9082 Number of Samples/Time (ns)	AD9081 Number of Samples/Time (ns)
Dual-Real Filter (96 Taps)	144/19.92	120/30
Single-Real Filter (192 Taps)	240/35.86	216/48
Half Complex Filter (96 Taps)	144/19.92	120/30
Complex Filter (64 Taps)	120/18.592	96/24
Matrix Filter (48 Taps)	104/17.264	80/20

Coefficient Size Optimizations

The PFILT hardware implementation takes advantage of the fact that not all coefficients must span a full 16-bit range. In most applications, the coefficients get smaller towards the ends of the filter impulse responses, which is especially true when the implementation involves correcting for very small errors in the analog response. As a result, not every coefficient requires a full 16-bit multiplier. Therefore, the multipliers use different coefficient bit widths that change how these are used in the structure and which taps these represent.

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In the PFILT implementation, the coefficients are separated into three groups where some are 16-bit coefficients, some are 12-bit coefficients, and the remaining are 6-bit coefficients. The coefficient LSBs are aligned such that all coefficients can be thought of as having 16-bit coefficient precision with the three different sets of coefficients that have different weights or ranges. The coefficients can be thought of as being LSB justified Table 118 shows the number of coefficients of various sizes that are allowed for different PFILT operating modes.

Table 118. Coefficient Sizes for PFILT Operating Modes

Mode	16-Bit Coefficient	12-Bit Coefficient	6-Bit Coefficient	Total Coefficient
Single Real	48	48	96	192 in single FIR
2N Real	24	24	48	96 per FIR
Matrix	12	12	24	48 per A, B, C, and D FIR filter
Complex	16	16	32	64 complex taps
Half Complex	24	24	48	

Figure 108 shows usage examples of the taps of the filter being moved around in multiples of four taps. The 12-bit coefficients must be adjacent to the 16-bit coefficients. However, each group of coefficients can be moved through the filter impulse response in multiples of four taps.

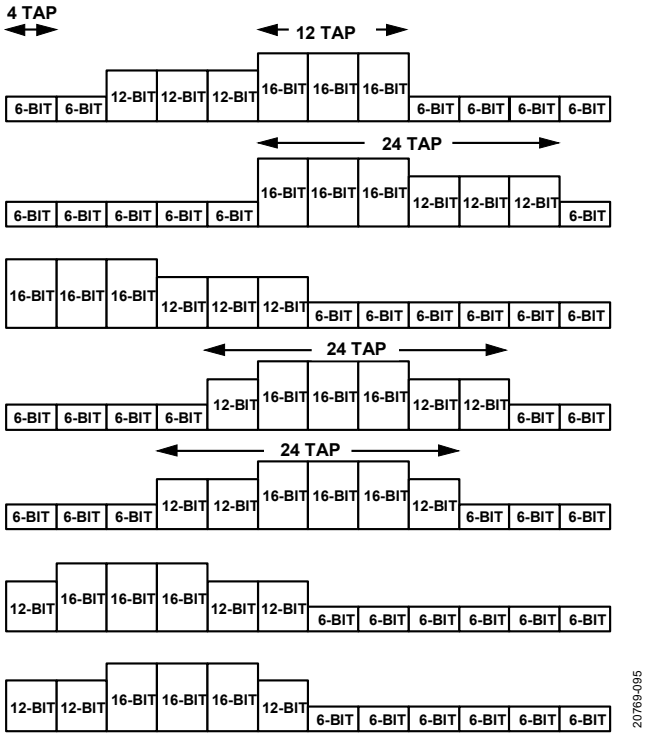

Figure 108. PFILT Coefficient Size Examples

SPI Programming of Coefficients

The PFILT filter coefficients are SPI programmable. Table 119 provides the I and Q coefficient tables, respectively. To reduce the write time, a streaming mode is used to avoid setting the address for each data byte. Coefficients are written as blocks with an internal address that autoincrements. All coefficients must be written except for the zero value coefficients on the end of the impulse response. The coefficients must be represented in twos complement format. Set the COEFF_CLEAR bit to 1 to clear the coefficients that are currently programmed into the structure. When cleared, all coefficient bits are set to 0. Depending on the filter mode, the COMPLEX_LOAD, REAL_CROSS_Q_LOAD, REAL_CROSS_I_LOAD, REAL_I_LOAD, and REAL_Q_LOAD bits must be set to signify the type of coefficients streamed. Use a multibyte or variable length encoded data mode to stream the coefficient data via the SPI, as shown in Figure 107.

In multibyte mode, each coefficient is written byte wise. The number of bytes for each coefficient is considered 16-bit words and the coefficients are twos complement. If the coefficients are less than 16-bits (12-bit or 6-bit coefficients), the coefficients must be sign extended to 16-bits.

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A state machine determines which coefficients require 16-/12-/6-bit multipliers to be used and optimizes the PFILT hardware implementation accordingly.

The alternative mode uses a variable length encoding (VLE) compression algorithm to provide up to 75% data compression, which further reduces the SPI programming time as well as the memory required to store one or more coefficient data sets. Compression is achieved by representing the twos complement coefficients with 7 bits or less as a single byte. Like the multibyte mode, a state machine optimizes the hardware configuration. To enable this mode, set the VLE_COEFF bit.

For VLE encoding, the 7 LSBs of a coefficient are set as the LSBs of a byte of data. If these 7 LSBs represent the entire coefficient, the MSB of the encoded byte is set to 0. If there are other MSBs, the MSB is set to 1 to indicate that the next byte written belongs to the same coefficient and a new byte is generated in the same manner. For every byte, 7 bits are real data bits of the coefficient and the encoded MSB determines whether the next byte is a continuation of the same coefficient or the start of a new coefficient. Note that coefficients that have 7 bits to 12 bits of data require two-byte representation and 13-bit to 16-bit coefficients require three bytes.

Table 119. Coefficient Table

Address	48-Tap Filter (I /Q Mode [2:0] = 0x1)	96-Tap Filter (I/Q Mode [2:0] = 0x2)	48-Tap Matrix Filter (I Mode [2:0] = 0x4, Q Mode [2:0] = 0x4)	64-Tap Full Complex Filter (I Mode [2:0] = 0x5, Q Mode [2:0] = 0x5)	96-Tap Half Complex Filter (I Mode [2:0] = 0x6, Q Mode [2:0] = 0x2)	96-Tap Half Complex Filter (I Mode [2:0] = 0x2, Q Mode [2:0] = 0x6)	192-Tap Feal Filter (I Mode [2:0] = 0x7, Q Mode [2:0] = 0x0 or Q Mode [2:0] = 0x7, I Mode [2:0] = 0x0)
0x1900	A C0 [7:0]	A C0 [7:0]	A C0 [7:0]	Real C0 [7:0]	B C0 [7:0]	A C0 [7:0]	A or D C0 [7:0]
0x1901	A C0 [15:8]	A C0 [15:8]	A C0 [15:8]	Real C0 [15:8]	B C0 [15:8]	A C0 [15:8]	A or D C0 [15:8]
0x1902	A C1 [7:0]	A C1 [7:0]	A C1 [7:0]	Real C1 [7:0]	B C1 [7:0]	A C1 [7:0]	A or D C1 [7:0]
0x1903	A C1 [15:8]	A C1 [15:8]	A C1 [15:8]	Real C1 [15:8]	B C1 [15:8]	A C1 [15:8]	A or D C1 [15:8]
…	…	…	…	…	…	…	…
0x195E	A C47 [7:0]	A C47 [7:0]	A C47 [7:0]	Real C47 [7:0]	B C47 [7:0]	A C47 [7:0]	A or D C47 [7:0]
0x195F	A C47 [15:0]	A C47 [15:0]	A C47 [15:0]	Real C47 [15:8]	B C47 [15:0]	A C47 [15:0]	A or D C47 [15:0]
0x1960	Unused	A C48 [7:0]	B C0 [7:0]	Real C48 [7:0]	B C48 [7:0]	A C48 [7:0]	A or D C48 [7:0]
0x1961	Unused	A C48 [15:0]	B C0 [15:8]	Real C48 [15:8]	B C48 [15:0]	A C48 [15:0]	A or D C48 [15:0]
…	Unused	…	…	..	…	…	…
0x197E	Unused	A C63 [7:0]	…	Real C63 [7:0]	B C63 [7:0]	A C63 [7:0]	A or D C63 [7:0]
0x197F	Unused	A C63 [15:0]	…	Real C63 [15:8]	B C63 [15:0]	A C63 [15:0]	A or D C63 [15:0]
…	Unused	…	…	Unused	…	…	…
0x19BE	Unused	A C95 [7:0]	B C47 [7:0]	Unused	B C95 [7:0]	A C95 [7:0]	A or D C95 [7:0]
0x19BF	Unused	A C95 [15:0]	B C47 [15:0]	Unused	B C95 [15:0]	A C95 [15:0]	A or D C95 [15:0]
0x19C0	D C0 [7:0]	D C0 [7:0]	D C0 [7:0]	image C0 [7:0]	D C0 [7:0]	C C0 [7:0]	A or D C96 [7:0]
0x19C1	D C0 [15:8]	D C0 [15:8]	D C0 [15:8]	image C0 [15:8]	D C0 [15:8]	C C0 [15:8]	A or D C96 [15:0]
…	…	…	…	…	…	…	…
0x1A1E	D C47 [7:0]	D C47 [7:0]	D C47 [7:0]	…	D C47 [7:0]	C C47 [7:0]	…
0x1A1F	D C47 [15:8]	D C47 [15:8]	D C47 [15:8]	…	D C47 [15:8]	C C47 [15:8]	…
0x1A20	Unused	D C48 [7:0]	C C0 [7:0]	…	D C48 [7:0]	C C48 [7:0]	…
0x1A21	Unused	D C48 [15:8]	C C0 [15:8]	…	D C48 [15:8]	C C48 [15:8]	…
…	Unused	…	…	…	…	…	…
0x1A3E	Unused	D C63 [7:0]	…	image C63 [7:0]	D C63 [7:0]	C C63 [7:0]	…
0x1A3F	Unused	D C63 [15:0]	…	image C63 [15:8]	D C63 [15:0]	C C63 [15:0]	…
…	Unused	…	…	Unused	…	…	…
0x1A7F	Unused	D C95 [7:0]	C C47 [7:0]	Unused	D C95 [7:0]	C C95 [7:0]	A or D C191 [7:0]
0x1A7F	Unused	D C95 [15:0]	C C47 [15:8]	Unused	D C95 [15:0]	C C95 [15:0]	A or D C191 [15:0]

TRANSMIT DOWNSTREAM POWER AMPLIFIER PROTECTION

Corrupted data content can result in severe transients at the DAC outputs which can potentially damage a downstream power amplifier. To prevent such an event from occurring, each main transmit datapath shown in Figure 72 has the capability to monitor and detect several different error sources where data corruption can occur. A flag is generated from these sources when an error is detected. This flag can trigger a ramp-down of the DAC output signal at a user defined rate and/or be routed to the IRQB_x pins to initiate the power-down of other external

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components. When the error condition is cleared, the DAC output is restored and ramps up to the previous output power level. Note that signal monitoring occurs at the input to the transmit main datapath whereas the ramp up/down function occurs at the end of this datapath, which allows more time for the DAC output to be turned off in advance of receiving the transient because of the added delay through the main datapath. Table 120 shows the register and bit location of all applicable SPI control bits for this protection feature. All control names ending in _MSB and _LSB are called by the functional name for simplicity and those control values require two SPI register write operations.

To enable this protection feature, set the BE_SOFT_OFF_GAIN_ EN bit. For baseband I/Q applications where I/Q data are directed to separate DACs, also set the NEW_GAIN_CONTRL_EN.

The DAC output can be triggered to turn on and off via a ramping signal upon receipt of any of the following signals shown in Figure 109:

- PDP_PROTECT signal: asserts when the calculated digital vector power exceeds a programmable threshold.
- INTERFACE_PROTECT signal: asserts when certain JESD204B/C errors occur.
- SPI_PROTECT signal: asserts when the user enables the SPI_SOFT_ON_EN and SPI_SOFT_OFF_EN SPI trigger bits listed in Table 120.
- BSM_PROTECT signal: asserts when a blanking state machine (BSM) module flushes the transmit datapath on the rising edge of either the TXEN0 signal or the TXEN1 signal applied to the respective pin names. This flushing feature is particularly useful in time duplex applications where the transmit datapath must be cleared between bursts. Note that both GPIO4 and GPIO5 pins can also be assigned as TXEN inputs, allowing for individual control of each DAC output.

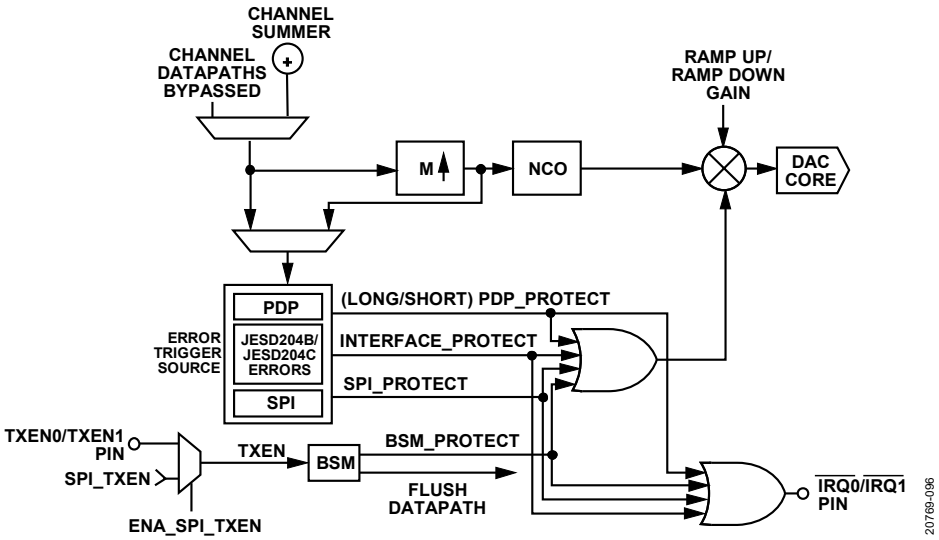

Figure 109. Downstream Protection Triggers Block Diagram

Table 120. PDP Threshold and Power Calculation Controls

Address	Bits	Bit Name
0x00B9	[1:0]	ROTATION_MODE
0x001B	[3:0]	DACPAGE_MSK
0x0300	3	NEW_GAIN_CONTRL_EN
	[2:0]	BE_GAIN_RAMP_RATE
0x0301	3	ENA_JESD_ERR_SOFTOFF
	2	ROTATE_SOFT_OFF_EN
	0	SPI_SOFT_OFF_EN
0x0303	7	SPI_SOFT_ON_EN
	6	LONG_LEVEL_SOFTON_EN
	4	HI_LO_RECV_SOFT_ON_EN
0x304	2	SOFT_OFF_GAIN_ALL_ENABLE
	1	LONG_PA_ALL_ENABLE
	0	SHORT_PA_ALL_ENABLE

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Table 120. PDP Threshold and Power Calculation Controls (Continued)

Address	Bits	Bit Name
0x305	[7:0]	LONG_PA_THRESHOLD_LSB
0x306	[4:0]	LONG_PA_THRESHOLD_MSB]
0x307	7	LONG_PA_ENABLE
	[3:0]	LONG_PA_AVG_TIME
0x308	[7:0]	LONG_PA_POWER_LSB
0x309	[4:0]	LONG_PA_POWER_MSB
0x30A	[7:0]	SHORT_PA_THRESHOLD_LSB
0x30B	[4:0]	SHORT_PA_THRESHOLD_MSB
0x30C	7	SHORT_PA_ENABLE
	[3:0]	SHORT_PA_AVG_TIME
0x30D	[7:0]	SHORT_PA_POWER_LSB
0x30E	[4:0]	SHORT_PA_POWER_MSB

Power Detection and Protection (PDP) Block

The PDP block detects the average power of the DAC input signal and prevents overrange signals from passing through the DAC output, which protects power sensitive devices like power amplifiers.

The protection function provides a signal, PDP_PROTECT, that can shut down the DAC outputs or be routed externally to shut down a power amplifier. The maximum input data rate to the PDP block is limited to 1.5 GSPS.

The PDP block uses a separate path with a shorter latency than the datapath to ensure that the ramp down is triggered before the overrange signal reaches the analog DAC cores (except when the total interpolation is 1×).

The sum of the I^2 and Q^2 signals are calculated as a representation of the input signal power (only the top six MSBs of data samples are used). The calculated sample power numbers are accumulated through a moving average filter with an output that is the average of the input signal power in a certain number of samples.

There are two types of average filters with different lengths, as shown in Figure 110. The short averaging filter path detects short pulses as low as 3 ns with high power that can exceed the breakdown voltage of a power amplifier.

The long averaging filter path detects signals that can cause thermal breakdowns. These signals are typically high power, wideband signals and can cause power amplifier damage when the signals last longer than the power amplifier thermal constant (~100 µs).

To enable these filters, set the SHORT_PA_ENABLE and LONG_ PA_ENABLE. When the output of the short or long averaging filter exceeds the specified threshold, the internal PDP_PROTECT signal goes high and causes the DAC output to ramp down and triggers an optional IRQ flag.

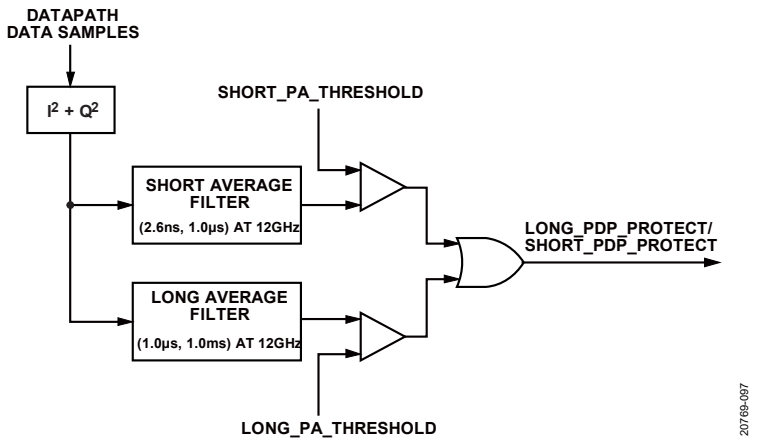

Figure 110. PDP Block Diagram

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The long averaging time and short averaging time are configured using the LONG_PA_AVG_TIME bits and SHORT_PA_AVG_ TIME bits, respectively, and the LONG_PA_ENABLE bits and SHORT_PA_ENABLE bits to enable each filter block. Use the following calculations to determine the average window size times:

Length of Long Average Window = $2^{LONG\_AP\_AVG\_TIME + 9}$

Length of Short Average Window = $2^{SHORT\_PA\_AVG\_TIME}$

When the average calculation value exceeds the specified threshold set by the LONG_PA_THRESHOLD and SHORT_PA_THRESHOLD, the ramp-down signal is triggered to ramp down the output.

The SHORT_PA_AVG_TIME and LONG_PA_AVG_TIME set the dwell time duration for the average power calculation to remain below the threshold before a ramp-up event can occur to restore the full-scale signal to the power amplifier. Read back the long and short average power calculations via the SHORT_PA_ POWER and LONG_PA_POWER.

Each DAC acts as an individual, associated PDP block to monitor the individual datapath and link. However, the user can also cause a ramp down on all DAC outputs if the fault condition is only impacting one of the DACs.

Set the following bits to enable the respective block to send a SOFT_OFF signal to all DACs and links to initiate a ramp down. The SOFT_OFF_GAIN_ALL_ENABLE bit enables the soft off gain blocks, and the SHORT_PA_ALL_ENABLE and LONG_PA_ALL_ENABLE bits enable the short and long power amplifier protect blocks. Note that a ramp up is also issued to all DACs.

JESD Interface and Synchronization Error Protection

A data transfer error that results in a transient can be incurred during a synchronization event where internal clocks are rotated for phase alignment purposes. For applications that require synchronization, the following bit fields must be set: ROTATE_SOFT_OFF_EN, ENA_JESD_ERR_SOFTOFF, and ROTATION_MODE. When these bits are set, the synchronization logic rotation triggers the DAC ramp-down block, rotates the digital clocks, and ramps back up. Similarly, a ramp-down and ramp-up event can be initiated if a JESD204B/C error is detected. In this case, set the ROTATE_SOFT_OFF_EN to 0 and leave the ENA_JESD_ERR_SOFTOFF and ROTATION_MODE set to 1.

Ramp-Up and Ramp-Down Gain

Various trigger signals can be configured in the power amplifier protection block to trigger a gain ramp down and mute the data transmitted out of the DAC, as shown in. This process is referred to as a soft off event because the event corresponds to a gradual ramp down in the signal with a programmable soft delay. In normal operation (assuming the LONG_LEVEL_SOFTON_EN is set), a ramp-down event is followed by a ramp-up event (or soft on event) to protect the downstream power amplifier from any transient as the DAC output signal is brought back to level prior to the soft off event.

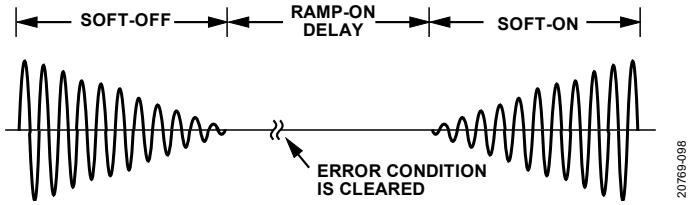

Figure 111. Soft Off and Soft On Ramping Characteristics

A linear ramp profile consists of a sequence of unsigned, 6-bit samples that are multiplied with the DAC datapath sample to ramp up or to ramp down the DAC output samples. A value of 32 corresponds to 0 dB or no input signal attenuation. By default, the ramp sample is updated once every eight DAC clock cycles (or $2^3/f_{DAC}$), which corresponds to the fastest ramp-up/ramp-down rate. The ramp-up/ramp-down rate of the digital gain is set by BE_GAIN_RAMP_RATE and can be decreased by up to a factor of 128 or 2^7. For example, a DAC that operates with an f_{DAC} = 12 GSPS update rate can have the ramp rate set from 21.3 ns out to 2.7 µsec. Individual control of each DAC ramp rate can be realized using the DACPAGE_MSK (Register 0x001B). To calculate the ramp time in DAC cycles (or $1/f_{DAC}$), use the following equation:

Ramp Time = $32 \times 2^3 \times 2^{(BE\_GAIN\_RAMP\_RATE)}$

When the data is ramped down, the data can be ramped back up directly by toggling the SPI_SOFT_OFF_EN bit, or the ramp up automatically performs if the LONG_LEVEL_SOFTON_EN bit is set to 1. In the latter case, a ramp-on delay counter starts to count when the JESD204B/C

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link is ready and the TXEN signal remains high. To calculate the delay in DAC cycles between when the error condition is cleared to when the ramp on begins when the interpolation filters are enabled, use the following equation:

$$Ramp\ On\ Delay = (8 \times M_{TX} \times (2^{(BE\_GAIN\_RAMP\_RATE + 5)} + 10)) - 2^{(BE\_GAIN\_RAMP\_RATE + 8)}$$

In the case where the interpolation filter is bypassed (N = 1), use the following equation:

$$Ramp\ On\ Delay = (32 \times (2^{(BE\_GAIN\_RAMP\_RATE + 5)} + 10)) - 2^{(BE\_GAIN\_RAMP\_RATE + 8)}$$

Note that if the digital signal exceeds the short or long threshold settings or a JESD204B/C link error reoccurs while the TXEN signal remains high, a ramp-down signal request is reasserted.

TRANSMIT POWER CONTROL

Transmit power control is also supported using the main datapath digital scaling block in tandem with the DAC analog full-scale current to control the transmit signal power level over a 47 dB span with 0.2 dB resolution, as shown in Figure 112. To enable this feature, set the EN_DSA_CTRL bit high. DSA_CTRL is an 8-bit word used to set the attenuation level over a 47 dB range in 0.2 dB increments. To realize initial attenuation, reduce the DAC full-scale current setting, I_{OUTFS}, from the default setting of 26 mA down to a level as low as 7 mA, which results in 11.4 dB of attenuation control.

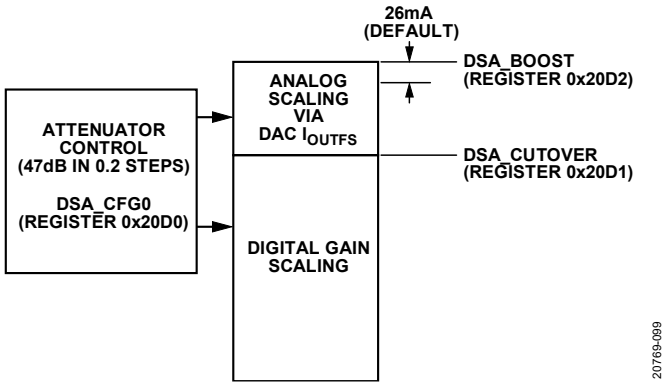

Figure 112. DAC I_{OUTFS} and Digital Gain Controlled by Look Up Table

DSA_BOOST can be used to extend this range by increasing the I_{OUTFS} level to 40 mA, which extends the analog range control by an additional 3.8 dB if programmed with a decimal value of 19. The resulting I_{OUTFS} with DSA_BOOST applied represents the maximum transmit power level that corresponds to the 0 dBFS reference level with DSA_CTRL representing the amount of attenuation from this upper limit. The DSA_CUTOVER specifies the transition point in 0.2 dB increments where additional attenuation is performed by digital scaling and is relative to the 0 dBFS level. In practice, the decimal value into this 8-bit register must not exceed 75 because this value corresponds to a 15 dB I_{OUTFS} attenuation range (or 40 mA to 7 mA) if DSA_BOOST is also set to 19. Note that the power level seen at the output of the DAC will immediately change after modifying the DSA_CTRL value and as a result, it is not possible to simultaneously update all DAC outputs with different DSA_CTRL values since no gain strobe option exists.

Table 121. Transmit Power Control Registers

Address	Bit Name	Description
0x20D0	DSA_CTRL	8-bit attenuation setting (LSB = 0.2 dB attenuation)
0x20D1	DSA_CUTOVER	8-bit analog to digital transition level. (LSB = 0.2 dB attenuation)
0x20D2	EN_DSA_CTRL	Set Bit 7 high to enable DSA control feature
	DSA_BOOST	5-bit setting, Bits[4:0] sets I_{OUTFS} boost level above default 26 mA (LSB = 0.2 dB boost)

The DAC current source array is calibrated at device initialization for the I_{OUTFS} setting used in the initialization process. The DAC linearity performance can begin to degrade as the I_{OUTFS} deviates from this setting. For this reason, evaluate the DAC AC performance for the particular usage case to ensure that the DAC meets the target systems performance requirements.

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IRQ

Two interrupt request output signals, IRQB_0 and IRQB_1, are available and can be sent to external pins having the same name. These optional signals can be used to notify an external host processor when an internal device event occurs. The IRQB_x pins are open-drain, active low outputs when used with an external load resistor. These pins can be tied to the interrupt pins of other devices with open-drain outputs to wire create a wired OR gate function. This IRQ feature is not required to configure or operate the device.

There are six groups of SPI registers allocated for interrupt request operation. Each group consists of the following registers (with x designating the group number): IRQ_ENABLE_x, IRQ_STATUS_x, and IRQ_OUTPUT_MUX_x. These groups cover a wide span of possible interrupt event flags, but only the flags pertaining to SYSREF input clock jitter monitoring and the power amplifier protection block are of possible use in a system application. The remaining flag options are for IC debug purposes only.

Table 122 lists the interrupt events that are available to use in an application. The SYSREF_IRQ flag monitors if the external SYSREF input signal falls outside a specified window because of excessive jitter. The PAERR_n and SRER_n flags are part of the transmit path power amplifier protection block that monitors the digital waveform for violations in the user specified average value and the maximum envelope slew rate of the input signal seen at the summing junction of the main datapath. Note that n signifies which main datapath the power amplifier protection block resides in.

Each interrupt event flag has three separate bit field assignments to enable the flag, monitor status, and direct flag signal to the IRQB_0 pin or IRQB_1 pin. The bit field in the IRQ_ENABLE_x register enables the designated interrupt event flag. The bit field in the IRQ_STATUS_x register shows the state of the designated interrupt event flag where a 1 indicates that an event has occurred. The bit field in the IRQ_OUTPUT_MUX_x register directs the signal flag to the external IRQB_0 or IRQB_1 pin. Note that for any particular interrupt flag name, the same bit field location is used in all three registers. For example, SYSREF_IRQ uses Bit 2 in all three SPI registers, Register 0x0020, Register 0x0026 and Register 0x002C.

Table 122. IRQ Register Block Details

IRQ Name	IRQ_ENABLE_x Register and Bit	IRQ_STATUS_x Register and Bit	IRQ_OUTPUT_MUX_x Register and Bit
SYSREF_IRQ	0x0020, Bit 2	0x0026, Bit 2	0x002C, Bit 2
PAERR_0	0x0021, Bit 3	0x0027, Bit 3	0x002D, Bit 3
PAERR_1	0x0021, Bit 7	0x0027, Bit 7	0x002D, Bit 7
PAERR_2	0x0022, Bit 3	0x0028, Bit 3	0x002E, Bit 3
PAERR_3	0x0022, Bit 7	0x0028, Bit 7	0x002E, Bit 7
SRER_0	0x0025, Bit 0	0x002B, Bit 0	0x0031, Bit 0
SRER_1	0x0025, Bit 1	0x002B, Bit 1	0x0031, Bit 1
SRER_2	0x0025, Bit 2	0x002B, Bit 2	0x0031, Bit 2
SRER_3	0x0025, Bit 3	0x002B, Bit 3	0x0031, Bit 3

Interrupt Service Routine

To start interrupt request management, select the set of event flags that require host intervention or monitoring. To enable the desired event flags, set the designated bit field in the IRQ_ENALBE_x with both the register address and bit field assignment provided in Table 122 and selecting the desired IRQB_x output pin the flag appears in (using the designated bit field in its associated IRQ_OUTPUT_MUX_x register). For events that require host intervention upon $\overline{IRQ}$ activation, take the following steps to clear an interrupt request:

1. Read the status of the event flag bits that are monitored.
2. Write 0 to the designated bit in the IRQ_ENABLE_x register to disable the interrupt.
3. Read the event source.
4. Perform any actions required to clear the cause of the event. Typically, no specific actions are required.
5. Verify that the event source is functioning as expected.
6. Write 1 to the designated bit in the IRQ_STATUS_x register to clear the interrupt.
7. Write 1 to the designated bit in the IRQ_ENABLE_x registers to reenable the interrupt.

GPIOX PIN OPERATION

The GPIOx pins support various transmit and receive digital blocks that can benefit from a faster data interface than the SPI port. These digital blocks support the following optional system level features:

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- FFH for transmit and receive path. The SYNC1OUTB+ and SYNC1OUTB− pins as well as the SYNC1INB+ and SYNC1INB− pins can be repurposed for paging purposes for individual control of transmit and receive NCO hopping.
- Power reduction of transmit and/or receive circuity in time duplex where designated blocks are placed in standby state during the off portion of the burst.
- Transmit power amplifier protection to send an external flag signal to an upstream device for further protection.
- Fast multiplexing between receive equalization and fractional delay settings in support of transmit digital predistortion applications where an ADC can be used to observe multiple transmitter outputs with feedback paths that have different group delays and RF pass band characteristics
- Receive AGC applications where the threshold detection flags must be gated by an external control signal.

For transmit features, the GPIO0 through GPIO5 pins and the SYNC1OUTB+ and SYNC1OUTB− pins may be configured to route internal signals to or from the pin. Note that all these pins can be configured as an input or output using Register 0x0035 through Register 0x0038. Note that to use the SYNC1OUTB+ pin and SYNC1OUTB− pin as GPIOs, there may be an additional write needed to bit SEL_SYNCB_MODE_RC in Register 0x042A. If any of the pins are configured as an input, the bit fields located in the GPIO_STATUS (Register 0x0033 and Register 0x0034), can be read to find out the state of each GPIOx pin. Table 123 lists the different transmit features, the pin assignments, and the SPI register values to map the functional name to the corresponding external pin assignments.

Table 123. GPIO and SYNC1_OUTB Pin Functions vs. Transmit Feature

Feature	Function Name	Input/ Output	Pin Assignments	Description
Power Control	TXEN1	Input	GPIO4	Enable or disable the output from DAC1 and DAC3. Configure register 0x0037: GPIO4_CFG=0x1 for TXEN1 and GPIO5_CFG=0x1 for TXEN3. All or some of the pins may be used.
	TXEN3		GPIO5	Also, pins can be reassigned to different DACs by setting the en_txen_flexible_route bit (Reg 0x01F2, bit 4) to enable reconfiguration through the TXEN_ROUTE_CTRL register (0x01F1, bit[7:0]).
Power Amplifier Protection	PA0_EN	Output	GPIO0	Routes the internal PDP_PROTECT signal to a GPIOx pin to control an external power amplifier on/off state. In registers 0x0035 and 0x0036, set bit fields GPIO0_CFG=0x1, GPIO1_CFG=0x1, GPIO2_CFG=0x1, GPIO3_CFG=0x2. The signal is triggered form the corresponding datapath: for example PA3_EN arrives from the PA protection block in the Main Datapath 3. All or some of the pins may be used.
	PA1_EN		GPIO1	
	PA2_EN		GPIO2	
	PA3_EN		GPIO3	
Transmit FFH[1]	DAC_NCO_FFH0	Input	SYNC1OUTB+	Paging address to page the correct CDUC and FFH NCOs: NCO0, NCO1, NCO2, NCO3. Set Register 0x0038 to value of 0x013. 0b00 – NCO0 0b01 – NCO1 0b10 – NCO2 0b11 – NCO3
	DAC_NCO_FFH1		SYNC1OUTB−	
	DAC_NCO_FFH2		GPIO0	5-bit control word to select one of 32 FTWs that are pre-configured as part of the FFH engine inside the coarse NCOs. DAC_NCO_FFH6 is the MSB and DAC_NCO_FFH2 is the LSB. Set Register 0x0035 and 0x00036 to value of 0x33. Set Register 0x0037, Bits[3:0] to value of 0x2.
	DAC_NCO_FFH3		GPIO1	
	DAC_NCO_FFH4		GPIO2	
	DAC_NCO_FFH5		GPIO3	
	DAC_NCO_FFH6		GPIO4	
	DAC_NCO_FFH_STROBE		GPIO5	Strobe signal to latch the 5-bit control word input on GPIO0 through GPIO4, and thus hop to a new FTW. Set Register Address 0x0037, Bits[7:4] to value of 0x2
Main-Subordinate Synchronization	MS_SYNC0	Input or Output	GPIO0	A method for clock and NCO synchronization across multiple devices. On each device in the system, configure just one GPIOx pin to either transmit a trigger signal to multiple devices (output, main) or receive a signal from a main device to begin resynchronization (subordinate, input). Select either one of available GPIOx pins to perform this function. Detailed explanation is available in the System Multichip Synchronization section.
	MS_SYNC1		GPIO1	
	MS_SYNC2		GPIO2	
	MS_SYNC3		GPIO3	
	MS_SYNC4		GPIO4	
	MS_SYNC5		GPIO5	

[1] All the GPIO pins listed for FFH control are required to control the FFH function.

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In support of the receive features, the GPIO6 pin through GPIO11 pin are used as well as the SYNC1INB+ and SYNC1INB− pins. The different receive features along with the corresponding function name and description are listed in Table 126.

Unlike the implementation used for transmit features, the receive feature implementation includes a crossbar multiplexer, as shown in Figure 113, that provides a greater degree of mapping between functional signals and device pins. Therefore, the function names in Table 126 are instead associated with a net name to the multiplexer input that corresponds to the register name used in turn to map an input to an output. The relevant peripheral input control, or PERI_I_SELx registers, occupy the SPI address space between Register 0x37DC and Register 0x37D7.

Table 124 shows the register values required to map the selected PERI_I_SELx input to a pin. For example, Table 125 lists the functional names and their associated PERI_I_SELx registers used to receive fast frequency hopping control. The table also lists the SPI address and value required to map each of these functions to the desired external pin. Note that the user can refer to Table 124 to modify the register values for a different function to pin external mapping.

Table 124. Net to Pin Mapping Profile Performed by GPIO Pin Crossbar Multiplexer (Register 0x37CC to Register 0x37D8)

Register Name	Pin Assignment	Register Value
PERI_I_SELx where x = 12 to 17 and 20 to 24	GPIO6	0x02
	GPIO7	0x03
	GPIO8	0x04
	GPIO9	0x05
	GPIO10	0x06
	SYNCINB1+	0x07
	SYNCINB1−	0x08

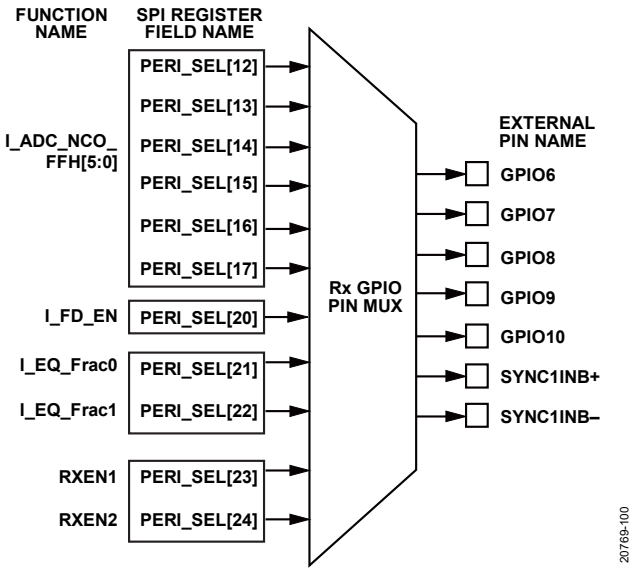

Figure 113. Receive GPIO Pin Crossbar Multiplexer Functional Diagram

Table 125. Example Mapping for Receive Fast Frequency Hopping

Function Name	Multiplexer Register Name	External Pin Name	Register Address	Register Value
I_ADC_NCO_FFH0	PERI_I_SEL17]	SYNC1INB−	0x37D1	0x08
I_ADC_NCO_FFH1	PERI_I_SEL[16]	SYNC1INB+	0x37D0	0x07
I_ADC_NCO_FFH2	PERI_I_SEL[12]	GPIO6	0x37CC	0x05
I_ADC_NCO_FFH3	PERI_I_SEL[13]	GPIO7	0x37CD	0x04
I_ADC_NCO_FFH4	PERI_I_SEL[14]	GPIO8	0x37CE	0x03
I_ADC_NCO_FFH5	PERI_I_SEL[15]	GPIO9	0x37CF	0x02

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Table 126. GPIOx and SYNC1_INB Pin Functions vs. Receive Feature

Feature	Function Name	Multiplexer Register Name	Register Address	Description
Receive FFH	I_ADC_NCO_FFH0	PERI_IN[17]	0x37D1	Main Datapath NCOx Paging for FFH
	I_ADC_NCO_FFH1	PERI_IN[16]	0x37D0	
				0: NCO0
				1: NCO1
				2: NCO2
				3: NCO3
	I_ADC_NCO_FFH2	PERI_IN[12]	0x37CC	4-bit control word selecting receive fast FTW with FFH5 being the MSB.
	I_ADC_NCO_FFH3	PERI_IN[13]	0x37CD	
	I_ADC_NCO_FFH4	PERI_IN[14]	0x37CE	
	I_ADC_NCO_FFH5	PERI_IN[15]	0x37CF	
Fast Detect	I_FD_EN	PERI_IN[20]	0x37D4	Enable update of fast detect output signals (ADCx_FDx) for time gated AGC application
Equalization/Fractional Delay Profile	I_EQ_Frac0	PERI_IN[21]	0x37D5	Allows four different PFILT coefficient and fractional delay settings to be selected under external pin control.
	I_EQ_Frac1	PERI_IN[22]	0x37D6	
Power Control	RXEN1	PERI_IN[23]	0x37D7	Turn ADC1 and ADC3 on and off
	RXEN3	PERI_IN[24]	0x37D8	

TEMPERATURE MONITORING UNIT (TMU)

The device contains a TMU that functions as a digital thermometer. The TMU comprises four sensors placed at different chip locations. The on-die temperature value is measured and digitized through an ADC. Table 127 shows the relevant API function calls used to configure the TMU and readback minimum and maximum die temperatures across the chip. Note that adi_txfe_device_startupTMU is a lower level API that is automatically called upon during the device initialization process.

At any given time, the 16-bit value from the sensor with the highest temperature is stored as LSB and MSB words in Register 0x2107 and Register 0x2108. Similarly, the 16-bit value from the sensor with the lowest temperature is stored as LSB and MSB words in Register 0x210B and Register 0x210C. The nine MSBs of each 16-bit temperature word are the integer portion of the die temperature in twos complement and the seven LSBs represent the fractional portion of the temperature, that is, the digits to the right of the decimal place. For example, the most significant of the seven LSBs represents 2^{-1} and the next bit to the right is 2^{-2}.

The following procedure is an example of obtaining the value of the sensor that produces the highest temperature reading. The same procedure applies to reading the minimum temperature and Register 0x210B and Register 0x210C are read back instead. To obtain the maximum temperature, read Register 0x2108 and Register 0x2107 to obtain the MSB and LSB 16-bit value.

For example,

Register 0x2108 = 0x1A = 00011010b

Register 0x2107 = 0xD2 = 11010010b

Concatenate the MSBs to the LSBs to give the following 16-bit word,

0001101011010010b

The nine MSBs of this word represent the twos complement integer value of the temperature in °C,

000110101 (twos complement) = 53 (decimal).

The seven LSBs of the 16-bit word are the fractional portion where the most significant (left most) bit value is 2^{-1}, the next is $2^{-2,}$ and so on. Using this convention,

1010010 = 0.640625 (decimal).

Therefore, the die temperature reported by the highest reading sensor is 53°C + 0.640625°C = 53.640625°C. Due to the accuracy constraints of an uncalibrated TMU, the fractional portion of the temperature value has limited significance and can be omitted, such that only Bit 7 of the

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LSB word is used if resolution to 1°C is desired. Note that if 2°C of resolution is acceptable, only the MSB word need be used. Therefore, the junction temperature is equal to 2 × Register 0x2108, Bits[7:0]).

Table 127. TMU API Functions

Function Call	<C file>	Description
adi_txfe_device_startupTMU	**adi_ad9081_device_c**	Function to configure the TMU for readback
adi_txfe_device_get_temperature	**adi_ad9081_device_c**	Reads back min and max temperature

AD9081/AD9082/AD9177 ONLY FEATURES

The following sections focus on AD9081 and AD9082, yet the information equally applies to the AD9177. The distinguishing features of the three variants are listed in Table 1. The AD9177, a DAC only variant of the AD9081 and AD9082, has the ADC cores and the JESD204B/C transmitter disabled, while allowing access to the receive path NCOs and other DSP and synchronization features as described in the Receive Main Digital Datapath section and Receive Channelizer Digital Datapath section.

TRANSMIT AND RECEIVE BYPASS MODE

Bypass mode of operation allows the transmit and/or receive digital datapath to be bypassed completely to allow direct data access to the DAC data input or ADC logical outputs. The JESD204B/C receiver and/or the JESD204B/C transmitter virtual converter link setting, M, is equal to the number of DACs and/or ADCs required with the unused converters powered down. If the transmit and receive paths are both configured for bypass mode, set Register 0x180 to Register 0x00 to set the ADC clock divider to 1. It is possible to configure two JESD204B/C transmitter links for ADCs where one link supports bypass mode and the other link supports usage of the receive digital datapath.

Bypass mode of operation results in the highest throughput rate for the JESD204B/C transmitter and JESD204B/C receiver links. To achieve a 25% reduction in throughput rate, select a JESD204B/C NP setting of 12 (vs. 16). No loss in dynamic range occurs in the receive path because the ADC core resolution is also 12 bits. For the transmit path, negligible loss in dynamic range often results by truncating the data to 12 bits because the quantization noise incurred from truncation is spread over the Nyquist bandwidth approaching the thermal (and jitter) induced noise floor.

To configure the DAC datapath for bypass mode operation, take the following steps:

1. Select the JESD204B/C receiver link parameters to accommodate the number of DACs and data link throughput rate. Consider using the JESD204B/C mode to improve the payload efficiency, which reduces the required lanes or lane rate.
2. Set the main and channelizer interpolation factors via Register 0x01FB to 1.
3. Set the DDSM_DATAPATH_CFG registers (Address 0x1C9 to Address 0x20) such that the real data samples are directed to the DACs.
4. Power down unused DACs.

To configure the ADC datapath for Bypass mode operation, take the following steps:

1. Select the physical ADCs to enable while powering down unused ADCs.
2. Map the physical ADCs to the corresponding logical ADCs using Crossbar Mux0 based on the settings for the AD9081 and AD9082, respectively.
3. Configure the PFIR_MODE and CDELAY in Register 0x0C0C and Register 0x0B14, respectively, if used. If the PFILT filter and coarse delay features are unused, set these registers to 0x00 and use PFILT_CTL_PAGE, Register 0x001E, to independently configured a pair of ADCs.
4. Configure the data format block to select the desired logical ADCs using the FBW_SEL registers (Address 0x2AB and Address 0x02AC) such that the desired logical ADC is routed to the corresponding output.
5. Configure the JESD204B/C crossbar Mux4 to map the output of the data format block to a virtual converter using the JTX_PAGE registers (Register 0x001A and Register 0x0600 through Register 0x060F).
6. Select the JESD204B/C transmitter link parameters to accommodate the number of ADCs operating in bypass mode and the throughput rate. Consider using JESD204C to improve the payload efficiency and reduce the required lanes or lane rate.

FFH MODE

The complex NCOs used in both the transmit and receive datapaths support FFH mode. In the transmit datapath, each main datapath NCO consists of a bank of 31 NCOs. In the receive main and channelizer datapaths, each NCO consists of a bank of 16 NCOs. Paging is used to set unique FFH frequency tuning words (FTW) associated with each bank of NCOs. The transmit and receive hop sequence can be independently controlled via GPIOx pins or the SPI register. Asynchronous trigger hop mode is an additional mode only supported on the receive path.

Transmit Main Path FFH NCO Mode

The FFH NCO associated with each main datapath is implemented as a main 48-bit NCO with additional 31 NCOs, each with a 32-bit resolution. Each of the 31 NCOs can be configured with a unique FTW (DDSM_HOPF_FTWx) where x is a value between 1 and 31. These FTWs can be preloaded into the hopping frequency register bank. Table 128 lists the various registers and control field names associated with the transmit FFH NCO feature.

To program the channel registers, take the following steps:

AD9081/AD9082/AD9177 ONLY FEATURES

1. Set the DACPAGE_MSK that corresponds to the main datapath NCOs to be programmed with the same register values.
2. Program the desired 32-bit FTW into the appropriate DDSM_HOPF_FTWx.

Repeat Step 1 and Step 2 for any other NCO channels.

Table 128. Transmit Main Path FFH Control Fields

Address	Bits	Bit Name
0x001B	[3:0]	DACPAGE_MSK
0x01C9	3	DDSM_NCO_EN
0x0800	[7:6]	DDSM_HOPF_MODE
	5	HOPF_GPIO_SEL_NONGLITCH_EN
	[4:0]	DDSM_HOPF_SEL
0x0801	0	GPIO_HOP_EN
0x0806 through 0x0809	[31:0]	DDSM_HOPF_FTW1
0x080A through 0x080D	[31:0]	DDSM_HOPF_FTW2
0x080E through 0x087D	[31:0]	DDSM_HOPF_FTWx, where x =3 to 30
0x87E through 0x881	[31:0]	DDSM_HOPF_FTW31

Select the preloaded FTW under SPI control using DDSM_ HOPF_SEL and DACPAGE_MSK or the GPIOx pins if the GPIO_HOP_EN bit is set. GPIOx pin mapping is described in Table 123 with a strobe signal applied to the GPIO5 pin and a page selection performed by the SYNC+ pin and SYNC− pin. The delay between the rising edge of strobe and frequency transition at the DAC output is approximately 100 ns. Note that this GPIOx selection option does not allow all main datapath NCOs to be paged simultaneously and the user is required to select each preloaded FTW sequentially using the SYNC+ pin and SYNC− pin. The HOPF_GPIO_SEL_NONGLITCH_EN bit can be set if potential glitching is noticed between frequency transitions.

The phase transition between frequency hops is controlled by the 2-bit control field, DDSM_HOPF_MODE. The three options and the associated bit field settings are as follows:

- Phase continuous with 0b00 setting
- Phase discontinuous with 0b01 setting
- Phase coherent with 0b10 setting

In phase discontinuous mode, the NCO FTW updates and the phase accumulator resets, which results in an abrupt phase change each time the NCO hops to a new frequency. The discontinuous phase can result in a glitch at the transition point. Alternatively, in phase continuous switching, the frequency tuning word of the NCO updates and the main phase accumulator maintains count throughout the update, which results in a smooth phase transition between carrier frequencies.

In phase coherent mode, a bank of 31 additional phase accumulators is enabled that maintains count regardless of which accumulator value is applied to the main accumulator. In this mode, the phase of all 32 FTWs is always known for each carrier frequency, thus allowing phase coherency between hops relative to Time 0 (the time when the NCO was last reset). Because this mode requires the NCO phase accumulators to start at the same time, all FTWs must be preloaded before selecting the phase coherent switch mode

Not all registers must be written to if fewer than 31 FTWs are required. To conserve power, the 31 additional NCOs are enabled only when the corresponding FTW is programmed to a value other than 0x0. All NCO FTWs have a default value of 0x0. Note that the main phase accumulator (corresponding to the 48-bit FTW, namely FTW0), is concurrently enabled using the DDSM_ NCO_EN bit.

Each 32-bit NCO can be powered down as needed. If a 32-bit NCO is initially powered up, first program the FTW to 0x0001 to flush the accumulator from any residual values, and then program the FTW to 0x0000 to power down the NCO output only (not the accumulator). This method avoids the possibility of any residual spurious tones appearing at the output of adjacent NCOs during power-down.

Hop Time Delay

The hop time delay, when using GPIO pins to trigger a hop, can be estimated. The delay ($T_{HOP, DELAY}$) can be measured between the time when a strobe signal arrives at the GPIO pins and the moment when the phase of the NCO-generated signal fully settles at the DAC output. The delay depends on the chosen phase transition mode (selected using the bitfield DDSM_HOPF_MODE), and is summarized as follows:

- Phase continuous or phase in-continuous: 2 nS + 50 cycles of $F_{CLK}/8$ + 285 cycles of F_{CLK}

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- Phase Coherent: 2 nS + 50 cycles of $F_{CLK}/8$ + 225 cycles of F_{CLK}

For example, if F_{CLK} = 12 GHz, which results in an NCO clock rate of 12 GSPS, has a cycle period of 1/12 GHz or 83.3 pS. For Phase Coherent mode, the delay is calculated as follows:

$T_{HOP, DELAY}$ = 2 nS + 50 x (83.3 pS x 8) + 225 x (83.3 pS) = 54.06 nS

A similar calculation can be performed for the Phase Continuous or Phase In-Continuous modes.

As the GPIO pins are sampled asynchronously inside the device, some variance may exist when correlating the calculation to a measurement taken in a particular setup. The variance is typically within 2 nS.

Using an SPI command to trigger a hop incurs a larger variance and $T_{HOP, DELAY}$, when compared to using the GPIO pins for hopping.

Receive Main and Channelizer Path FFH NCO Mode

Coherent FFH is supported in the main datapath coarse NCO as well as the channelizer fine NCOs, but most applications perform hopping using the coarse NCOs only. As are result, the functional description that follows calls out SPI registers that pertain to the coarse NCOs for simplicity. Note that the fine NCO share the same name corresponding to the control field names with the exception that COARSE is replaced by FINE. For example, an equivalent control field name for COARSE_ DDC0_NCO_REGMAP_CHAN_SEL exists for the fine NCO called FINE_DDC0_NCO_REGMAP_CHAN_SEL. Table 129 and Table 130 list the various registers and control field names associated with the main and channelizer datapaths, respectively, that are referenced in the following sections.

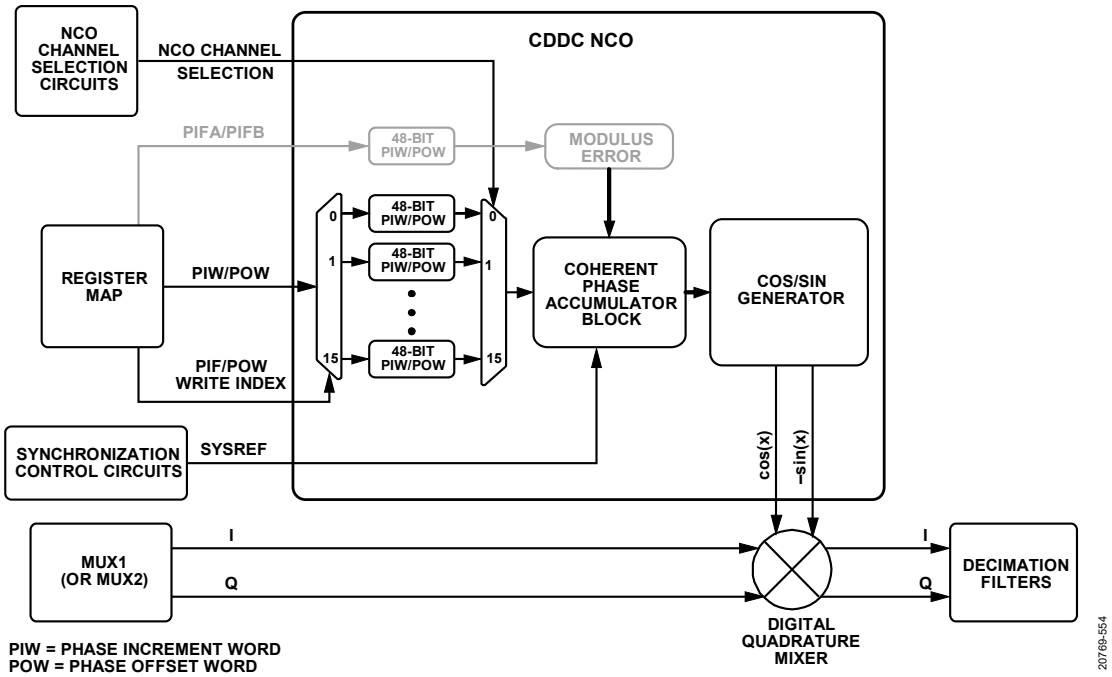

Figure 114. Coherent FFH NCO in CDDC (and FDDC)

Table 129. Receive Main Path FFH Control Fields

Address	Bits	Bit Name
0x18	[7:4]	COARSE_DDC_PAGE
0x28A	0	COMMON_HOP_EN
0xA00	4	COARSE_DDC_SOFT_RESET
0xA03	[7:4]	COARSE_DDC0_NCO_CHAN_SEL_MODE
	[3:0]	COARSE_DDC0_NCO_REGMAP_CHAN_SEL
0xA04	7	COARSE_DDC0_PROFILE_UPDATE_MODE

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Table 129. Receive Main Path FFH Control Fields (Continued)

Address	Bits	Bit Name
	6	COARSE_DDC0_GPIO_CHIP_TRANSFER_MODE
	[3:0]	COARSE_DDC0_PROFILE_UPDATE_INDEX
0xA05 through 0xA0A	[7:0]	COARSE_DDC_PHASE_INCx, where x = 0 to 5
0xA0B through 0xA10	[7:0]	COARSE_DDC0_PHASE_OFFSE_TRANSMIT, where x = 0 to 5
0xA1F	0	COARSE_DDC0_CHIP_TRANSFER
0xA20 through 0xA25	[7:0]	COARSE_DDC0_PSWx, where x = 0 to 5
0xA26 through 0xA2B	[7:0]	COARSE_DDC0_ACTIVE_PHASE_INCx, where x = 0 to 5
0xA2C through 0xA31	[7:0]	COARSE_DDC0_ACTIVE_PHASE_OFFx, where x = 0 to 5
0xA39 through 0x0A3E	[47:0]	COARSE_COUNTER_LOAD_REG

Table 130. Receive Channelizer Path FFH Control Fields

Address	Bits	Bit Name
0x19	[7:4]	FINE_DDC_PAGE
0xA80	4	FINE_DDC_SOFT_RESET
0xA83	[7:4]	FINE_DDC0_NCO_CHAN_SEL_MODE
	[3:0]	FINE_DDC0_NCO_REGMAP_CHAN_SEL
0xA84	7	FINE_DDC0_PROFILE_UPDATE_MODE
	6	FINE_DDC0_GPIO_CHIP_TRANSFER_MODE
	[3:0]	FINE_DDC0_PROFILE_UPDATE_INDEX
0xA85 through 0xA8A	[7:0]	FINE_DDC_PHASE_INCx, where x = 0 to 5
0xA9B through 0xA90	[7:0]	FINE_DDC0_PHASE_OFFSE_TRANSMIT, where x = 0 to 5
0xA9D	0	FINE_DDC0_CHIP_TRANSFER
0xAA0 through 0x AA5	[7:0]	FINE_DDC0_PSWx, where x = 0 to 5
0xAA6 through 0xAAB	[7:0]	FINE_DDC0_ACTIVE_PHASE_INCx, where x = 0 to 5
0xAAC through 0xAB1	[7:0]	FINE_DDC0_ACTIVE_PHASE_OFFx, where x = 0 to 5
0xAB9 through 0xABE	[47:0]	FINE_COUNTER_LOAD_REG

The NCO contains 16 channel registers, as shown in Figure 114, that can be programmed with unique PIW and POW register values as described in Table 30. These registers are implemented as main/subordinate types to allow all registers to be updated simultaneously. An indexing scheme programs each shadow register where the COARSE_DDC0_PROFILE_UPDATE_ INDEX selects the shadow channel register number associated with the coarse NCO. The COARSE_DDC_PAGE selects which main datapath NCO(s) to program.

To program the channel registers, take the following steps:

- Set the bits in ADC_COARSE_PAGE bit field that corresponds to the NCOs to program with the same register values.
- Set the COARSE_DDC0_NCO_REGMAP_CHAN_SEL index bit field with the desired channel register number.
- Program the required 48-bit PIW and optional POW settings for this channel register number, the COARSE_DDC_PHASE_INC and the COARSE_DDC0_PHASE_OFFSET bit fields.
- Repeat Step 1 through Step 3 for any other NCO channels.

The COARSE_DDC0_PROFILE_UPDATE_MODE bit determines if the register values update immediately when set to 0 or synchronously when set to 1. The latter option allows all new values to be programmed into the main SPI register before simultaneously transferring the values into subordinate registers. The COARSE_DDC0_GPIO_CHIP_TRANSFER_MODE bit determines if the transfer command is generated via SPI or a GPIOx pin when set to 0 or 1, respectively. For the SPI transfer option, transfer occurs when the COARSE_DDC0_GPIO_CHIP_ TRANSFER bit is set from 0 to 1. Note that this bit must be cleared before performing another transfer. For the GPIOx pin option, a low to high transition on the GPIO10 pin results in a transfer.

The NCO channel selection circuit shown in Figure 115 determines which register is loaded into the NCOs phase accumulator. The following four control modes of operation are supported: GPIO level , GPIO edge, profile select timer, and register map. Set the COMMON_HOP_EN bit to hop all main datapath NCOs simultaneously

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The phase accumulator block contains the logic that allows an infinite number of coherent frequency hops and is allowed to return to any unique shadow register setting while maintaining phase coherency at the instance of return. In other words, the NCO phase returns to the same the same value at that instance of time as if no prior frequency hopping had occurred.

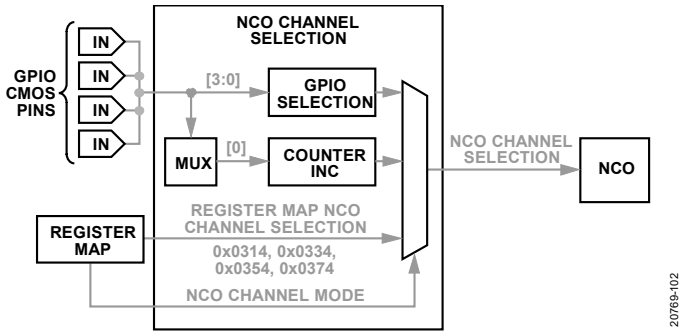

Figure 115. NCO Channel Selection Block

GPIO Level Control

In this mode, four GPIOx pins are available to select the desired NCO channel and two GPIOx pins are used for paging purposes if independent hopping between main datapaths is required. The number of GPIOx pins for channel selection depends on the number of shadow channel registers used and the COARSE_ DDC0_NCO_CHAN_SEL_MODE bit field (Register 0xA03, Bits[7:4]) determines the number of assigned logical profile pins. See Table 126 for more information on the assignment of logical pins to GPIOx pins. Note that this mode of operation is not supported for the channelizer path fine NCOs.

To configure the device for this mode of operation, take the following steps:

1. Use the COARSE_DDC0_NCO_CHAN_SEL_MODE bits to configure one or more GPIOx pins as NCO channel selection inputs. This register refers to the pins as logical profile pins. To assign the logical profile pins to a GPIOx pin, refer to Table 126.
2. Select the desired NCO channel and main datapath through the GPIOx pins.

GPIO Edge Control

In this mode, a single GPIOx pin is used to update a counter on a low to high transition. When the counter reaches the wraparound value programmed into the COARSE_DDC0_ NCO_REGMAP_CHAN_SEL, the count returns to 0. The internal channel selection counter can be reset by either an external SYSREF signal or by a DDC soft reset.

To configure for this mode of operation, take the following steps:

1. Set the COARSE_DDC0_NCO_CHAN_SEL_MODE bit to 1. Refer to Table 126 to map the logical pin to a GPIOx pin.
2. Set the wraparound count value in the COARSE_DDC0_SW.
3. Apply an external SYSREF signal or set the COARSE_DDC_SOFT_RESET bit (Register 0xA00, Bit 4) to reset the internal counter.
4. Issue a low to high transition on the designated GPIOx pin to increment the counter.

Profile Select Time Mode

This mode is similar to the GPIO edge control mode with the exception that the internal channel selection counter is updated by a 32-bit profile select timer (PST) that operates at the same clock rate as the NCO, and the COARSE_DDC0_PSWx bit field specifies the number of sample clock cycles between frequency hops. The NCO channel increments when the PST expires and the PST resets after each channel increment. A 48-bit wraparound value can also be programmed into the COARSE_COUTNER_ LOAD_REG bit field such that the channel counter resets to 0 when the programmed value is reached. The channel selection counter is reset by a DDC soft reset.

To configure for this mode of operation, take the following steps:

- Set the COARSE__DDC0_NCO_CHAN_SEL_MODE bit.
- Configure the COARSE_COUNTER_LOAD bit field. Note that the profile select timer operates at the NCO clock rate.
- Set the wraparound count value in the COARSE_DDC0_PSWx bit field.

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Register Map Control Mode

In this mode, the NCO channel selected is determined directly through the register map where the DDC0_NCO_REGMAP_ CHAN_SEL bit field is used to select the shadow channel register number. Set the COARSE_DDC0_NCO_CHAN_SEL_MODE bit to 0 when using this mode.

RECEIVE TO TRANSMIT ANALOG LOOPBACK

The AD9081 and AD9082 support two methods to loop back the samples from the receive path to the transmit path, as shown in Figure 116.

The direct loopback path loops the ADC output data directly back into a specified DAC without any signal processing, which provides the shortest path latency but no ability to delay or modify the received signal before retransmitting through the DAC cores. Only ADC0 and ADC1 loopback is supported for the AD9081, although it is possible to designate any two of the four physical ADC outputs as ADC0 and ADC1 using Mux0. See the Mux0 section for details on controlling this mux.

The indirect loopback path loops the ADC outputs through the receive and transmit datapaths to take advantage of the signal processing capability at the expense of higher latency. The data loopback occurs between the lane FIFO blocks of the JESD204B/C transmitter and JESD204B/C receiver.

A unique feature of the AD9177, the DAC-only version of the MxFE, is that the receive path may be configured to operate the CDDC and FDDC NCOs as a DDS to generate CW tones and utilize the FFH feature. The output samples are then looped back to the transmit datapath for further processing. Table 131 shows the applicable control fields and register assignments to configure each loopback mode whereas Table 132 lists the loopback API functions.

To enable the direct loopback mode, set the DIRECT_ LOOPBACK_MODE. The ADC and DAC clock rates must be equal and keep the ADCDIVN_DIVRATIO_SPI at the default setting of divide-by-1 because the output data of ADC0 or ADC1 is fed directly back into one of the DACs. The LOOPBACK_CB_ CTRL controls the crossbar multiplexer and allows the output of ADC0 or ADC1 to be looped back to each DAC input. Register control is such that Bits[1:0] correspond to DAC0 where a 0 or 1 corresponds to ADC0 or ADC1, respectively, and Bit [3:2}, Bit [5:4], and Bit [7:6] correspond to the control of DAC1, DAC2, and DAC3, respectively.

To reduce digital datapath power, disable the clocks with both the TXCLK_EN and RXCLK_EN set to 0. Note that the ADC output data can be also directed to the JESD204B/C transmitter directly or via the receive digital datapath. In this case, set RXCLK_EN to 1 and configure the JESD204B/C transmitter setting to support the receive digital datapath throughput requirements. The direct loopback mode latency is 183 clock cycles for the AD9081 and 187 clock cycles for the AD9082. For the AD9082, which operates at 6 GSPS, the loopback latency is 20.8 ns.

To enable indirect loopback mode, set the TXFE_LOOPBACK_ MODE (with direct loopback disabled). Because loopback occurs after the JESD204B/C transmitter FIFO, the link parameters for the JESD204B/C receiver must match that of the JESD204B/C transmitter with only the single link JESD204B/C transmitter and JESD204B/C receiver supported. The physical to logical lane mapping for both links must also match and must be kept at the default settings. Like direct loopback mode, the host processor has access to the JESD204B/C transmitter data. Also, if the JESD204B protocol is used, the external SYNC0OUTB signal must be routed back to the SYNC0INB input of the device. For this reason, use of the JESD204C protocol may be preferred.

The receive and transmit digital datapaths must be configured such that I/Q data rates into and out of the JESD204B/C transport layer are matched. The interpolation factor on the transmit datapath can be set higher than the decimation factor on the receive datapath based on the ADC clock divide settings in the ADCDIVN_DIVRATIO_SPI bit field. The loopback latency can vary considerably because the latency depends on the datapath interpolation and decimation factors as well as the JESD204B/C transmitter and JESD204B/C receiver link configuration.

Because this mode enables the complete receive and transmit datapaths, the user can vary the received input waveform delay, frequency, amplitude, or pass band frequency characteristics (see Figure 117 and Figure 118). Additionally, the GPIO based profile hopping option allows preloaded profiles to be quickly switched between time slots, as described in the FFH Mode section. In the receive datapath, the receive PFILT has four profiles that can be switched using a pair of GPIOx pins and different integer or fractional settings between time slots, as shown in Figure 119.

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Table 131. Loopback Control Fields

Address	Bits	Bit Name
0x00C0	4	DIRECT_LOOPBACK_MODE
	1	TXCLK_EN
	0	RXCLK_EN
0x0180	[1:0]	ADCDIVN_DIVRATIO_SPI
0x00C2	[7:0]	LOOPBACK_CB_CTRL
0x0941	0	TXFE_LOOPBACK MODE

Table 132. Loopback API Functions

Function Call	<C file>	Description
adi_9xxx_device_direct_loopback_set	**adi_ad9081_device_c**	Function to configure device for direct loopback option with DAC mapping to ADC0 or ADC1
adi_ad9081_jesd_loopback_mode_set()	**adi_ad9081_jesd_c**	Function to configure device for indirect loopback via JTx to JRx FIFO

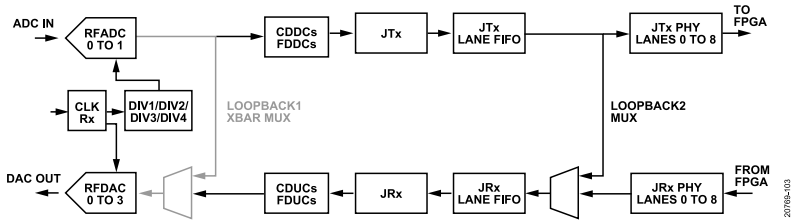

Figure 116. Direct and Indirect Analog Loopback Modes

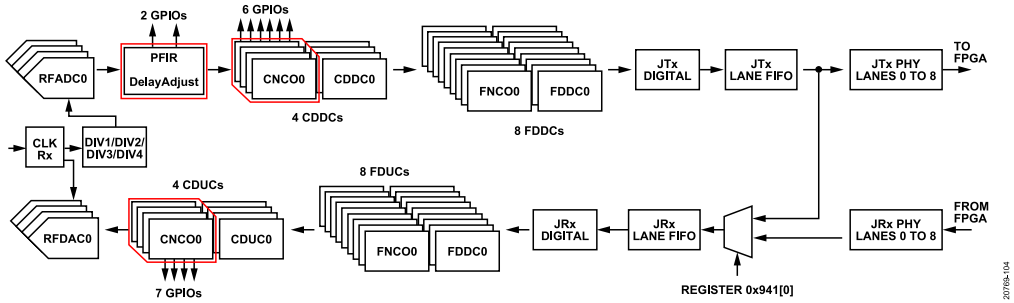

Figure 117. GPIO Based Profile and NCO Hopping

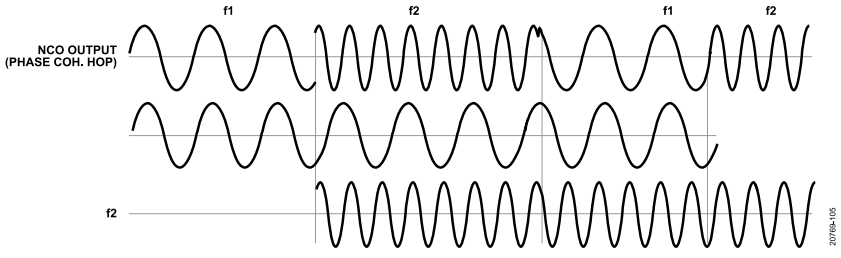

Figure 118. Transmit/Receive NCO FFH

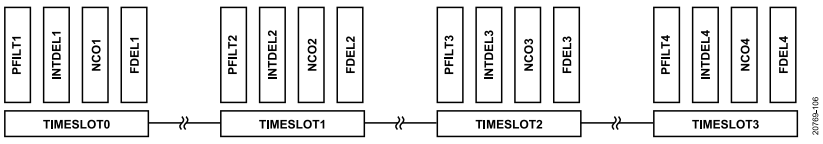

Figure 119. Receive PFILT/Delay Adjust Fast Profile Hopping

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DEVICE LATENCY

Receive Path End to End Total Latency

Total latency of the receive path in the device is dependent on the ADC pipeline latency, configurations of the digital processing blocks, and the JESD204B/C configurations. For any given combination of these parameters, the latency is deterministic. However, the value of this deterministic latency must be calculated using the AD9081_82 latency calculator spreadsheet.

The latency of each block is described as in Table 133, Table 134, and Table 135:

Table 133. ADC

Mode	Latency (Clock Cycles)
Dual	109
Quad	105

Table 134. PFILT

Mode	Latency (Clock Cycles)
Bypassed	8
Dual, Single Real	120
Dual, 2^N Real	136
Dual, Full Complex	113
Dual, Matrix	89
Quad, Single Real	95
Quad, 2^N Real	77
Quad, Full Complex	105
Quad, Matrix	61

Table 135. Integer Delay

Mode	Latency (Clock Cycles)
Bypass	0
Enabled	+ programmed delay

For the Datapath (CNCO + Fractional Delay + FNCO) and JESD204B/C blocks (Transport Layer + Link Layer + Serdes), see the latency calculator.

To determine the total latency of the receive path, add the latency contributed by each of the block along the pipeline (see Figure 1). Example calculations are provided in the Example Latency Calculations section.

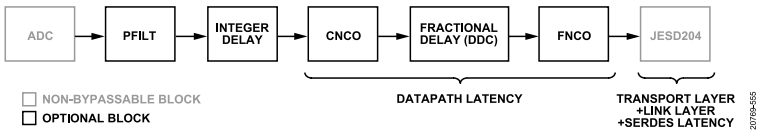

Figure 120. Latency Block Diagram

Example Latency Calculations

Example 1:

Configuration 1 is as follows:

- ADC: Dual
- Integer Delay: Bypassed
- PFILT: Bypassed
- Coarse DDC: Bypassed
- Fine DDC: Bypassed
- JESD204B/C configurations:

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- 204C
- C2R=0
- Async Mode=0
- LMF = 1,8,16
- S=1
- NP=16

Latency (in encode clock cycles):

- ADC = 109
- Integer Delay = 0
- PFILT = 0
- Datapath (Coarse DDC + Fine DDC) = 16
- Transport Layer = 88.5
- Link Layer = 1
- Serdes = 1.78 (minimum) to 2.86 (maximum)

Total Latency = 216.28 (minimum) to 217.36 (maximum)

Example 2:

Configuration 2 is as follows:

- ADC: Quad
- Integer Delay: Bypassed
- PFILT: Single Real Filter
- Coarse DDC: Variable IF, decimate by 2
- Fine DDC: Variable IF, decimate by 1
- DDC C2R: disabled
- DDC Fractional Delay: Bypassed
- JESD204B/C configurations:
- 204C
- C2R=0
- Async Mode=0
- LMF = 1,4,8
- S=1
- NP=16

Latency (in clock cycles):

- ADC = 105
- Integer Delay = 0
- PFILT = 95
- Datapath (Coarse DDC + Fine DDC) = 321
- Transport Layer = 178
- Link Layer = 4
- Serdes = 7.12 (minimum) to 11.44 (maximum)

Total Latency = 710.12 (minimum) to 714.44 (maximum)

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LMFC Referenced Latency

Some FPGA vendors may require the end user to know LMFC-referenced latency to make appropriate deterministic latency adjustments. If they are required, the total latency values of ADC + integer delay + PFILT + datapath can be used for the analog in to LMFC latency value. The total latency values of transport layer + link layer + SERDES can be used for the LMFC to data out latency values.

SYSTEM MULTICHIP SYNCHRONIZATION

As described in previous sections, the device contains DSP blocks on-silicon to allow channel-to-channel digital phase and/or amplitude calibration techniques to be implemented as part, or the entirety, of the system level calibration. Some of these phase adjustments occur at the NCOs residing in the four coarse DUC/DDCs and eight fine DUC/DDCs. Additionally, on the receive path, on-silicon PFILT blocks allow equalization of both phase and amplitude for all receive channels in the system. Each of these DSP blocks must be synchronized when dealing with multiple devices in a system.

Multichip synchronization using the device is achieved with the help of two distinct features:

- One shot sync helps to align baseband data and some internal clocks
- NCO main-subordinate sync helps to align the multiple NCOs spanning across all the chips on the platform

There are multiple signals on the platform which are used to achieve multichip synchronization:

- SYSREF signals to each device are used to help achieve One shot Sync.
- GPIO signals are used to implement NCO Main-Subordinate Sync.
- SPI control of the PLL phases to each device in the system are used to compensate for changes in thermal gradients across the system.

Note that multichip synchronization applications desiring to use the on-chip PLL must be aware that the DAC clock rate must be selected such that it exceeds 5.8 GSPS to avoid potential phase ambiguity between devices that may occur when the D divider of the PLL is set to values other than 1 (refer to the Clock Multiplier section for more details on the device PLL setup). Because the D divider cannot be reset (via SYSREF signal), its output phase can assume 2 or more states (depending on divider setting) thus making it possible for phase variation in the sampling clocks (DACCLK and ADCCLK) among different devices regardless if a SYSREF signal is applied. This situation can be avoided when the D divider is set to 1 thus forcing the DAC clock rate to equal the PLL VCO frequency which has range of 5.8 GHz to 12 GHz. Additionally, for the receive path only (or when using the AD9207 or AD9209) applications requiring multichip synchronization, the D divider must be set to 1 whereas the L divider (having reset capability) is set such that $L \times f_{ADC}$ falls within the VCO frequency range of 5.8 to 12 GHz.

Quad MxFE Reference Design

Analog Devices developed the quad MxFE that is part of a full stack reference design that implements the complete system level multichip synchronization described within this section. The HDL code, device driver and application code for the reference design can be found on the quad MxFE wiki page. The goals for multichip synchronization for systems that require it are:

- Achieve phase determinism for both the receive and transmit paths. That is, the input RF phases to each ADC channel and the output RF phases from each DAC channel are identical so that full dynamic range and phase noise system level benefits can be realized/
- Simplification of the system level calibration routine. If the front end is attached, it allows for the use of a look-up table (LUT) to be loaded at system boot that aligns all receive channels and all transmit channels.

Figure 121 shows the high level multichip sync platform architecture. The following sections refer to this design to describe how the synchronization functions can be implemented.

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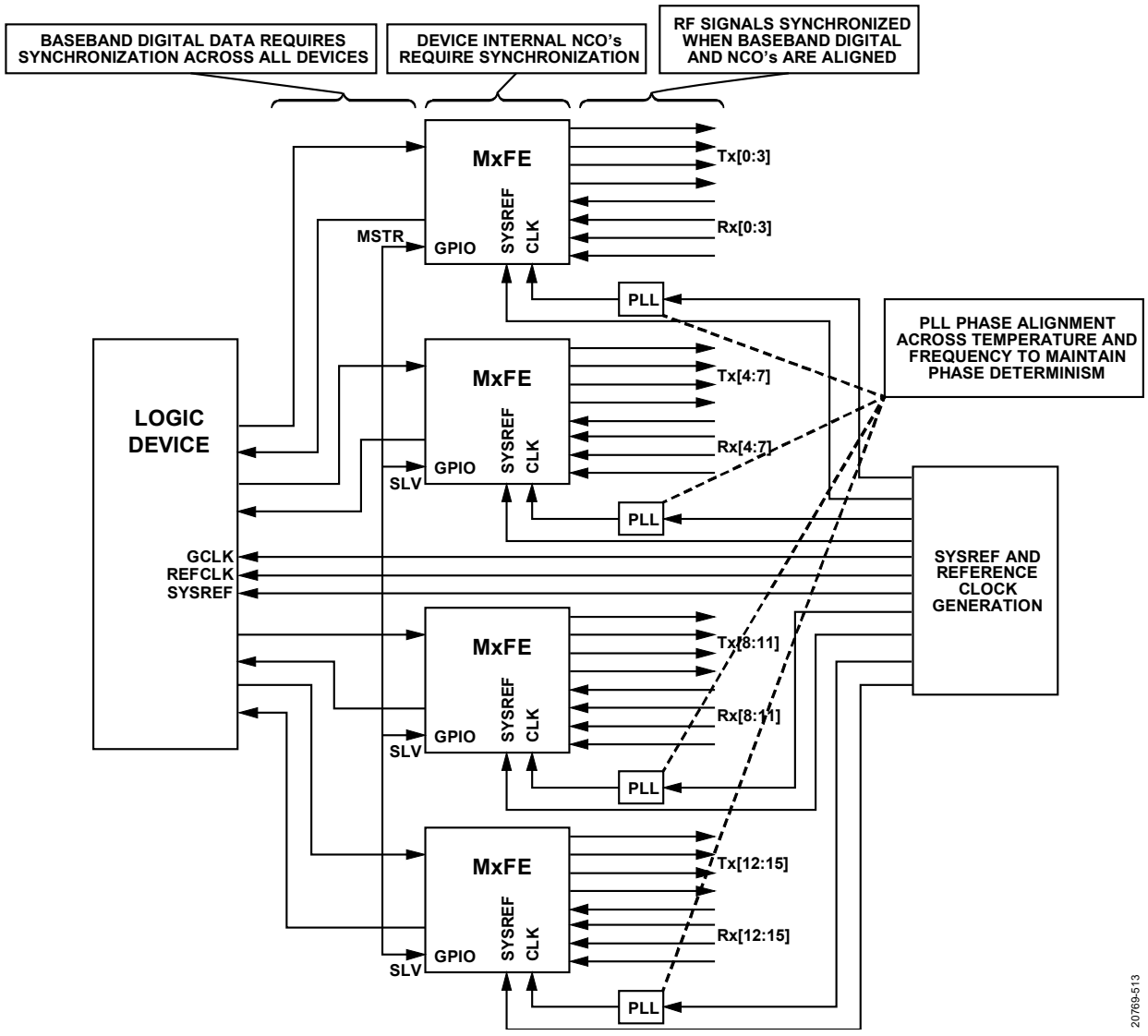

Figure 121. Quad MxFE Reference Design Block Diagram

One Shot Sync

Baseband digital data synchronization is achieved using the one shot sync feature. This feature requires that the user define the JESD204B/C link parameters (such as L, M, F) and then configure the synchronization logic for any desired SYSREF averaging (if using continuous SYSREF pulses). Additionally, desired LEMC delays can be used to force the LEMC to be generated at a certain delay after the SYSREF edge. After this is completed, the user then enables the one shot sync bit within each digitizer IC and then requests that SYSREF pulses be sent to each IC within the same clock cycle. One shot sync can be accomplished using the API function adi_ad9xxx_jesd_oneshot_sync which is called when executing the adi_ad9xxx_device_startup_tx_or_nco_test API function. Refer to the SYSREF and Subclass 1 Operation section for more details on the SYSREF function.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

For the quad MxFE Platform, analog fine delays have been introduced within the HMC7043 clock buffer IC to allow synchronous SYSREFs to all digitizer ICs. A subsequent check can be executed to verify the one shot sync process performed successfully by querying registers within

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each IC which provide information about the phase relationship between the SYSREF signal and the LEMC boundary of each link of the IC. Once a stable phase is measured (that is, once the SYSREF-LEMC phase register reads 0), the user then knows that the LEMCs of all the digitizer ICs are aligned and the user can then proceed to the NCO main-subordinate sync process. Refer to the JESD204B/C Transmitter Multichip Synchronization section for details on making appropriate adjustments for the transmit path multichip synchronization. For the receive path, refer to the JESD204B/C Receiver Multichip Synchronization section or the user guide for the logic devices JESD204B/C receiver IP that is being used. The subtasks described for the one shot sync are contained within API provided for the device.

NCO Main-Subordinate Sync

The NCO main-subordinate sync feature first assigns one of the AD9081 within the subarray to act as a main chip, as shown in Figure 121. All other digitizers are then deemed subordinate ICs. The main IC is setup such that the GPIO0 pin of this device is configured as an output and routed to the GPIO0 nets of the three subordinate digitizer ICs. The subordinate GPIO0 nets are configured as inputs. The user can then choose to trigger on either the SYSREF pulse, the LEMC rising edge, or the LEMC falling edge. The LEMC rising edge is used as the NCO main-subordinate sync trigger source as default for the base control code provided with the platform, and the GPIO nets are routed through the HDL instead of locally on the subarray. Next, the DDC synchronization bits are toggled low and then high to arm the ADC-side NCO synchronization algorithm. Likewise, the microprocessor align bit is toggled low and then high to arm the DAC-side NCO synchronization algorithm. When this trigger is requested, at the next LEMC rising edge the main digitizer IC asserts high a main out signal through its GPIO0 net. This signal propagates to the GPIO0 inputs of each of the subordinate devices. At the next LEMC edge, all digitizer ICs experience a NCO reset algorithm. After this any LEMC pulses are ignored with regards to the NCO main-subordinate sync algorithm. As with the one shot sync, these NCO main-subordinate sync subtasks are contained within API functions for user ease-of-use. The high level application code can be found on the quad MxFE wiki page. This code uses the following API functions, which are described in the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later:

- adi_ad9xxx_jesd_oneshot_sync()
- adi_ad9xxx_device_nco_sync_pre()
- adi_ad9xxx_adc_nco_main_subordinate_sync()
- adi_ad9xxx_device_nco_sync_post()

PLL Synthesizer Phase Adjustments

The ADF4371 PLL synthesizers allow relative sample clock phase adjustments injected into each digitizer IC. Thermal drift, and the resulting PLL phase drift between the sample clock and the SYSREF of each IC, is compensated by creating a feedback mechanism which ensures that the first transmit channel of each AD9081 is phase aligned to the first transmit channel of first AD9081 IC, as shown in Figure 121. To achieve this feedback loop, the first transmit channel of each MxFE outputs a signal which differentiates itself from the other transmit channels. These four signals are combined and sent into a common receiver, which for this system is labeled Rx0.

A receiver data capture is obtained which then allows the user to apply cross-correlation techniques to determine the complex phase offsets between these four transmit channels, $\varphi_{TxOffset}$. The ADF4371 PLL synthesizer ICs contain a VCO which is operating at a frequency f_{VCO_PLL}. The measured phase offsets $\varphi_{TxOffset}$ are then related to the required PLL phase adjustment φ_{PLL_Adj} and the RF frequency $f_{CARRIER}$ such that:

$$\phi_{PLLadj} = \left[\frac{f_{VCOPLL}}{f_{CARRIER}}\right]\phi_{TxOffset} \quad (12)$$

Using this formula, the ADF4371 PLL synthesizer phases can be adjusted by a new known amount to establish a common transmit baseline between all digitizer ICs for all power cycles. The calibrated transmit phase offsets for the first (and second) channelizers of all AD9081s are phase aligned. The second channelizer of each digitizer IC is aligned in this instance as well because two channelizers are used for each DAC in the system.

Note that the PLL synthesizer phase adjustments described in this section are specific to the clocking architecture for this reference design. Other clocking architectures can be employed that may minimize or altogether eliminate the need for these adjustments. However, this example provides a useful illustration of system level adjustments that may be necessary to ensure accurate multichip synchronization.

Quad MxFE System Level API

The system level API that implements multichip synchronization on the quad MxFE platform is executed in three stages and utilizes the device level API as described in the One Shot Sync section and NCO Main-Subordinate Sync section. The API of each stage can be found through the following linked text:

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- Stage 1: one shot sync
- Stage 2: main/subordinate NCO sync
- Stage 3: NCO sync sustain

Each of these stages is executed in parallel for each MxFE device in the system before moving on to the next stage.

PCB LAYOUT AND DESIGN CONSIDERATIONS

CAD Symbol, Package Pinout and Unused Balls

The CAD symbols and package pinout are available for each device on their respective product page in the design resources section. The package pinout is also included in their respective datasheets. Note, leave any ball that is labeled as DNC open and leave any ball labeled as NC open or connected to a surrounding GND pin

PCB Material and Stack Up Selection

The evaluation board PCB stack up shown in Figure 122 consists of 12-layers. All critical RF analog and JESD204B/C SERDES input and output signals are microstrip traces located on the top or bottom side of the PCB. For high speed SERDES lane rates that exceed 16+ GBPS, as well as having extended trace length lengths (+6 inches), consider a laminate material such as Tachyon100G or Rodgers 4003 for the laminate material for the top and bottom layers of the PCB. A via-in-pad approach is used to simplify access to inner layers on the evaluation board and enable decoupling capacitors on the back side of the PCB (under the device). A via-outside-pad approach can also be considered in instances where many of the digital and SERDES pins remain unused. In most cases, the required board artwork stack up is different than the evaluation board stack up. As a result, further optimization of RF transmission lines specific to the desired board environment is essential to the design and layout process.

CUSTOM INFO	TYPE	LYR	IMAGE	FOIL	GROUP	THK (MIL)	ER
TOP01 / PLP02	SIGNAL POWER / GROUND	TOP01 PLP02		0.5oz 0.5oz	TACHYON_100G TACHYON 5.0 CORE... 370HR 106 370HR 2113	5 5.832	2.98 3.54 3.86
SIG03 / PLP04	MIXED POWER / GROUND	SIG03 PLP04		0.5oz 0.5oz	370HR 4.0 CORE H/H 370HR 106 370HR 106	4.3 4.323	3.80 3.54 3.54
PWR05 / PLP06	POWER / GROUND POWER / GROUND	PWR05 PLP06		1oz 1oz	HIPER V R–1755V 2.0 CORE 1/1 370HR 106 370HR 106	2 4.444	3.75 3.54 3.54
PWR07 / PLP08	POWER / GROUND POWER / GROUND	PWR07 PLP08		1oz 1oz	HIPER V R–1755V 2.0 CORE 1/1 370HR 106 370HR 106	2 4.404	3.75 3.54 3.54
PWR09 / SIG10	POWER / GROUND MIXED	PWR09 SIG10		0.5oz 0.5oz	370HR 4.0 CORE H/H 370HR 2113 370HR 106	4.3 5.754	3.80 3.86 3.54
PLP11 / BOT12	POWER / GROUND SIGNAL	PLP11 BOT12		0.5oz 0.5oz	TACHYON_100G TACHYON 5.0 CORE...	5	2.98

20769-514

Figure 122. Evaluation Board PCB Stack Up

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Component Placement and Routing Priorities

Signals with Highest Routing Priority

Figure 123 shows the top and bottom side of the PCB layout used on the AD9081-FMCA-EBZ and AD9082-FMCA-EBZ evaluation boards, where RF and high speed digital signals have the highest priority. To achieve the highest isolation, adjacent ADC and DAC channels are placed on opposite side of the PCB. Note that the footprint of the Mark BALH-0009 balun used for both ADC and DAC interfaces also makes it difficult to support all RF analog traces on the top side if isolation is of a lower priority. The BALH-0009 has excellent amplitude and phase balance characteristics over a wide bandwidth such that any residual degradation in even order harmonic performance can be attributed to the ADC or DAC.

Other wideband baluns with smaller footprints such as the Mini-circuits TCM1-83X or Murata LTCC baluns (like the LDB183G0BAADA042 or LDB184G6BAAEA048) allow all adjacent ADC and DAC channels to be placed on the same side of PCB. However, these lower cost baluns do not maintain the same level of amplitude/phase balance over a broad frequency range. As a result, degraded even order harmonic performance may exist in frequency regions where the amplitude/phase balance is poor.

RF baluns are typically used to interface single-ended signals to the differential analog ADC input and DAC output ports. In general, the highest achievable analog bandwidth for the selected balun is achieved with the balun situated within a few mm to the ADC and DAC pins (as allowed by PCB design rules). The exception to this rule can be the broadband balun used for clock input in support of direct RF clock frequencies in the 6 GHz to 12 GHz range where the distance from the CLKINP pin and CLKINN pin can have significant impact on the clock signal level delivered to the IC internal clock input. S parameters, Keysight ADS models of the DAC outputs, and ADC and clock inputs are available to assist in the optimization of the interface network. Consider optimization of trace impedance per balun type. The FMCA-EBZ uses single-ended, 25 Ω and 50 Ω traces to realize 50 Ω and 100 Ω differential impedances for the DAC and ADC, respectively.

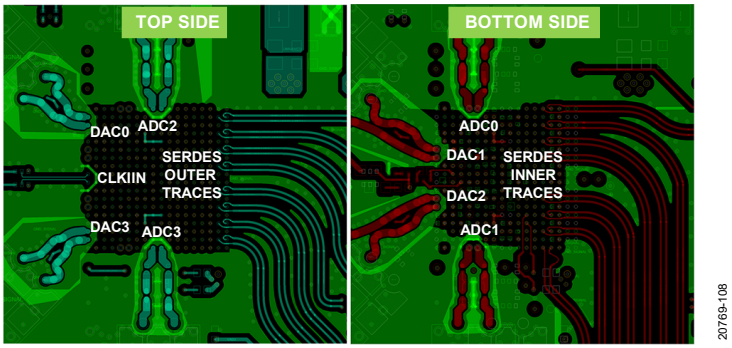

Figure 123. Routing Direction of Critical RF Analog and SERDES Signals

Use the top side of the PCB for applications requiring only four transmit and receive SERDES lanes and select the outermost balls in Column 17 and Column 18 on the package ball assignments. For applications that require more SERDES lanes, route the traces associated with the balls on Column 14 and Column 15 on the back side of the PCB. Refer to the RF and JESD204B/C SERDES Transmission Line Layout section for specific guidelines on trace layout.

The device CLKIN input is sensitive to any additive noise or signal coupling that can degrade the jitter and phase noise performance of the device. The CLKIN input signal can be a high frequency when equal to the DAC update rated up to 12 GHz or a lower frequency input that serves as a reference to the on-chip PLL clock multiplier which allows less than 3 GHz frequency. Because the additive jitter from the on-chip clock receiver is sensitive to the slew rate of the clock input signal, either wideband matching (when interfacing to the PECL or CML clock driver outputs) or tuned matching must be maintained when interfacing to RF synthesizers that produce a CW output. If the clock input signal serves as a reference to the on-chip PLL, this trace can be laid out in an inner layer as a microstrip, loosely coupled, 100 Ω trace. Otherwise, the trace must be laid out on the top side of the PCB. For a single-ended source using an LTCC balun (such as the Mini-circuits NCR2-123+), simulation using Keysight ADS models can be used to optimize the balun placement vs. bandwidth. Place 100 pF DC blocking capacitors after the balun differential pads.

The SYSREF signal is an optional input control signal used to configure the device for JESD204 Class 1 operation enabling deterministic latency and/or multichip phase alignment. This signal typically originates from a clock distribution IC that provides an LVDS or PECL signal type that interfaces to the devise SYSREFP pin and SYSREFN pin, which provides a 100 Ω on-chip termination. Use loosely coupled, 100 Ω strip

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line traces for this signal that can be routed on the inner layer. For dc-coupled PECL applications, a pair of 150 Ω resistors to ground must be added for DC biasing of the PECL output stage.

The ADCDRVN output is an optional, high speed, differential clock output that can be used by another ADC device. This output must be ac-coupled. Run this signal on an inner signal layer to provide isolation from the sensitive DAC and ADC traces.

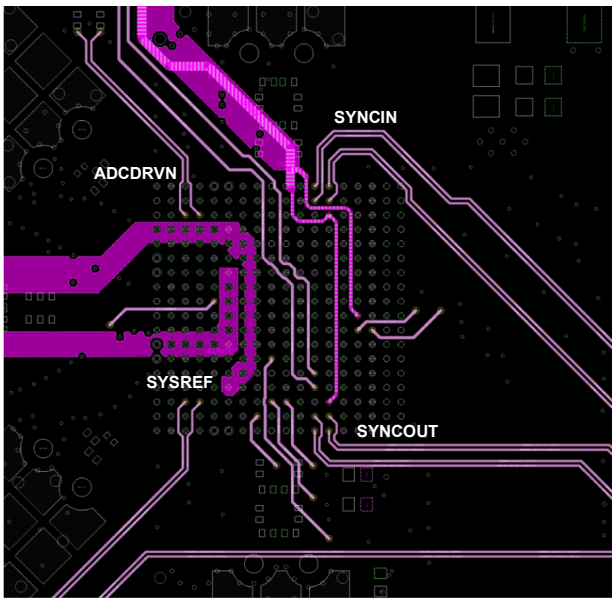

Figure 124. Digital Signal Routing of Priority SYSREF and ADCDRVN with Second Priority Signals, SYNCIN and SYNCOUT

Signals with Second Routing Priority

The on-chip clock multiplier of the device requires an external loop filter if used as well as decoupling capacitors for the on-chip regulator. The fine loop filter consists of the R1 resistor and the C1 and C2 capacitors, the component location of which is on backside of the PCB just beyond the outline of the package, as shown in Figure 125.

Place the C3 coarse capacitor across the VCO_COARSE and VCO_VCM balls on the back side of the PCB with the VCO_REG decoupling capacitors. This layout keeps the trace and loop inductance of filter components to a minimum to reduce noise coupling and ensures the PLL stability that results from the effective series inductance of long traces.

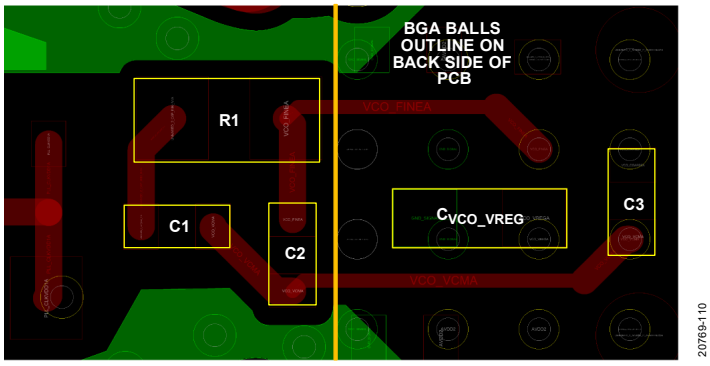

Figure 125. CLK PLL Filter Components Layout with VCO Regulator Bypass Capacitor

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Signals with Lowest Routing Priority

This section provides information on the signals that are of the lowest signal routing priority. These signals can only be routed when all critical signal routes are complete to ensure that these signals do not interfere with the critical component placement and routing.

The SYNCINB and SYNCOUTB control signals are used for JESD204B/C link establishment. Like the SYSREF signal, these signals can be configured for a 100 Ω differential interface or a single-ended CMOS interface. When configured for a differential 100 Ω interface, use loosely coupled 100 Ω strip line traces to the host processor. When configuring for a single-ended interface, use the positive polarity pin and leave the negative polarity pin floating. Route all CMOS input and output signals such as those supporting the SPI interface, as well as optional GPIO and control and status flag signals on the inner PCB layers. Route these signals away from the analog section.

The DAC full-scale current is set using an external 4.99 kΩ 1% standard resistor connected to the ISET pin and referenced to the adjacent ground pin. A 0201 or 402 sized resistor can be placed on the back side of PCB that connects to the ISET and ground vias.

The ADCs include on-chip buffers that include internal, high frequency switching regulators to generate negative and positive supply domains for internal biasing. Place ceramic, 0.1 µF bypass capacitors at the NVG1_OUT, VNN1, BVNN2, and BVDD3 pins. Place these capacitors as close as possible to the device with the ground side of the bypass capacitor placed such that ground currents flow away from other power balls and the corresponding bypass capacitors, if possible.

RF AND JESD204B/C SERDES TRANSMISSION LINE LAYOUT

The layout recommendations in this section are intended for high frequency signals.

Acceptable PCB designs include the following:

- Match the evaluation board design as close as possible to the board design files available on the product page.
- Be attentive to power distribution and power ground return methodology to avoid coupling onto signal traces or the ground reference plane. In general, do not run high speed digital lines near DC power distribution routes or RF line routes.
- Use microstrip or coplanar waveguides (CPWG) on the top side of the PCB for transmission lines whenever possible. These structures do not require via structures that cause additional impedance discontinuities that vary across frequency. However, isolation between RF analog inputs/ outputs and space constraints associated with using all JESD204B/C lanes require using the back side of the PCB.

Design the RF line systems between the device ball pad reference plane and the balun/filter reference plane for a differential impedance (Z_{DIFF}) of 50 Ω for the DAC output and 100 Ω ADC input. Differential lines from the balun to the ADC and DAC input/output balls must be as short as possible. This design is a compromise impedance with respect to frequency and an optimal starting point for design. The SERDES lanes are microstrip lines designed for a Z_{DIFF} of 100 Ω.

In most cases, the required board artwork stack up is different than the evaluation board stack up. Optimization of RF transmission lines specific to the desired board environment is essential to the design and layout process.

JESD204B/C SERDES Trace Routing Recommendations

The SERDES lanes are split into four rows, two rows for transmit and two rows for receive. Routing is not symmetric because each differential pair is placed on a separate column. When deciding on the layout of these traces, consider the following guidelines:

- The positive and negative traces must be of equal length to avoid mismatch between the driver and receiver.
- All SERDES lane traces must be impedance controlled to achieve 50 Ω to ground. Ensure that the differential pair is coplanar and loosely coupled with a maximized trace width.
- As stated in the JESD204C Receiver DFE Operation Above 16 Gbps section, the JESD204B/C receiver PHY calibration relies on a minimal amount of slewing of the input signal to detect the eye shape, and make CTLE and DFE adjustments accordingly. Therefore, the best practice is to design the JESD204C receiver pcb channels with at least 3 dB of insertion loss when operating the link above 16 Gbps.
- Route the differential pairs on a single plane and use a solid ground plane as a reference on the layers above and/or below the traces. Ensure that reference planes for impedance controlled signals are not segmented or broken for the entire length of a trace.
- Traces can become marginally thinner to escape ballout.
- Place coupling capacitors close to one end of the SERDES lanes to lessen reflections.
- Minimize the pad area for all connector and passive component choices as much as possible to avoid a capacitive plate effect that can lead to issues with signal integrity.
- Route the inner transmit lanes to the inner or bottom layers.

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- The internal JESD204B/C crossbar multiplexer can be used to alleviate routing when not all SERDES lanes are utilized.
- Ground shielding or fencing is recommended between lanes as space allows.
- To ensure optimal performance of the interface, place the device close enough to the baseband processor to keep the insertion loss of the pcb channel within the limits of the feed-back equalizer (DFE) (for the JESD204B/C receiver) and the feed-forward equalizer (FFE) (for the JESD204B/C transmitter) capabilities, and route the traces as directly as possible between the devices.
- Use a PCB material with a low dielectric constant (<4) to minimize loss.
- For distances greater than 6 inches, use a premium PCB material such as Rogers 4003C or Tachyon100G.

Stripline vs. Microstrip

When routing the PCB layout for SERDES data lines, the user must decide to route the signals using either stripline traces or microstrip traces. There are positive and negative aspects of both trace types that must be carefully considered before choosing one or the other.

The use of stripline traces has less loss and emits less electromagnetic interference (EMI) than the use of microstrip lines, but stripline traces require the use of vias that add line inductance and can require more complex add line inductance control.

The use of microstrip traces is simpler to implement if the component placement and density allow routing on the top layer of the PCB, which simplifies impedance control.

If using the top layer of the PCB is problematic or if the advantages of using the stripline traces are needed, consider the following recommendations:

- Minimize the number of vias.
- Use blind vias wherever possible to eliminate via stub effects and use microvias to minimize via inductance.
- If using standard vias, use maximum via length to minimize the stub size. For example, on an 8-layer board, use Layer 7 for the stripline pair.
- Place a pair of ground vias near each via pair to minimize the impedance discontinuity.
- Route SERDES lanes on the top side of the PCB as a differential 100 Ω pair (microstrip) when possible. In cases where this method is not possible, the SERDES signals are routed on the inner layers of the PCB as differential 100 Ω pairs (stripline). To minimize potential coupling, these signals are placed on an inner PCB layer with a via embedded in the component footprint pad where the ball connects to the PCB. AC coupling capacitors (100 nF) on these signals are placed at the connector, away from the chip, to minimize coupling. The JESD204C interface can operate at frequencies up to 25 GHz. Take care to maintain signal integrity from the chip to the connector.

ISOLATION TECHNIQUES USED ON THE EVALUATION BOARD

The evaluation board uses a fencing technique to provide isolation between first priority RF analog input and output signals as well as between the SERDES lane pairs (see Figure 126). Ground vias placed around each JESD204B pair provide isolation and decrease crosstalk. Spacing between vias follows the rule provided in Equation 40.

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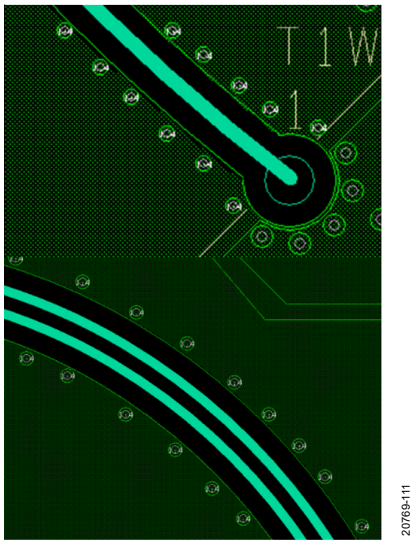

Figure 126. Fencing Technique on RF Analog (Top) and SERDES Lane Pairs (Bottom)

Through-hole vias that connect the top layer to the bottom layer and all layers in between are optimal. These vias steer return current to the ground planes near the apertures.

Use electromagnetic simulation software to develop accurate slot spacing and square aperture layout when designing the PCB. Ensure that spacing between apertures is not more than 1/10 of the shortest wavelength supported.

Calculate the wavelength with the following equation:

$$wavelength\ (\mathrm{m}) = \frac{300}{frequency\ (\mathrm{MHz}) \times \sqrt{\varepsilon_r}} \quad (40)$$

where:

ε_r is the dielectric constant of the isolator material.

For Roger 4003C material with a microstrip structure (and taking air as an insulator into account), the ε_r value is 3.55. For FR4-370 HR material with a stripline structure, the ε_r value is 4.6.

For example, a maximum RF signal frequency is 6 GHz. For Rogers 4003C material with microstrip structures and ε_r = 3.55, the minimum wavelength is approximately 26.5 mm. To fulfill the 1/10 of a wavelength rule, square aperture spacing must be at a distance of 2.65 mm or closer.

POWER CONSUMPTION

The device features a wide variety of modes to support various applications. Generally, the total power consumption depends on the following:

- Number of ADC (Rx) and DAC (Tx) channels used
- DAC and ADC clock rates
- The instantaneous bandwidth that needs to be processed
- DDC/DUC
- Programmable FIR
- JESD204B/C setup

The example use cases below show the device setup, and the typical and maximum power consumption for that particular use case. Note that additional power savings options may be available to minimize the power consumption for each use case example that follows. Refer to the Power Management Considerations section for more details.

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Example 1: 2D2A, 3 GSPS I/Q Mode

Table 136. 2D2A, 3 GSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (GSPS)	Output Data Rate from ADC (GSPS)
AD9082, AD9986	2	2	12	6	3 (I/Q)	3 (I/Q)

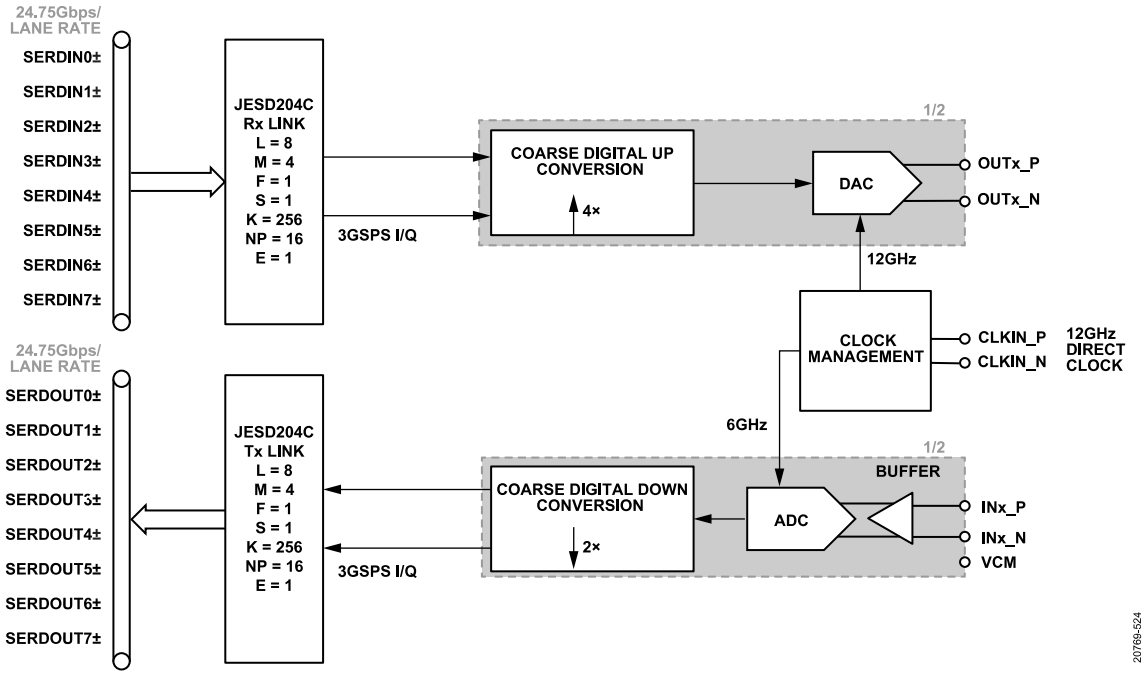

Figure 127. 2D2A, 3 GSPS I/Q Mode Block Diagram

Table 137. Typical and Maximum Power Consumption for 2D2A, 3GSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		102	107	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		0.874	1.004	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		620	795	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1710	2095	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		90	150	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	80	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		925	1130	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2540	3545	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		560	680	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1850	2500	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		8.635	11.36	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		9.5	12.4	W

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Example 2: 2D2A, DAC in 3 GSPS I/Q Mode, ADC in Full Bandwidth Mode

Table 138. 2D2A, DAC in 3 GSPS I/Q Mode, ADC in Full Bandwidth Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (GSPS)	Output Data Rate from ADC (GSPS)
AD9082	2	2	12	6	3 (I/Q)	6

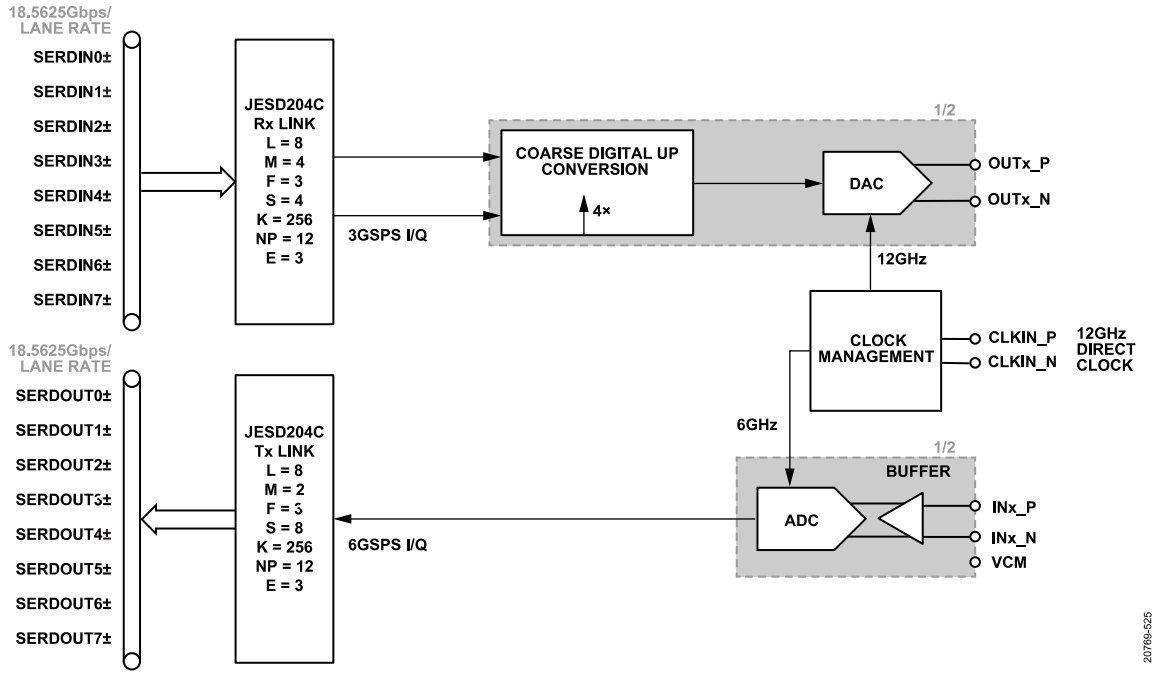

Figure 128. 2D2A, DAC in 3 GSPS I/Q Mode, ADC in Full Bandwidth Mode Block Diagram {Note to illustrator (DI): JTx LMFS should be 8.2.3.8 in diagram above, per Example 2 in https://jira.analog.com/browse/TDQ-646]

Table 139. Typical and Maximum Power Consumption for 2D2A, DAC in 3GSPS I/Q mode, ADC in Full Bandwidth Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		102	107	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		0.874	1.004	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		620	795	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1710	2095	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		90	150	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	80	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		925	1130	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2050	3035	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		560	680	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1500	2045	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		7.795	10.395	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		8.7	11.4	W

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Example 3: 2D2A Quad Band, DAC in 250 MSPS I/Q mode, ADC in 500MSPS I/Q Mode

Table 140. 2D2A Quad Band, DAC in 250 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9082, AD9986	2	2	6	6	250 (I/Q)	500 (I/Q)

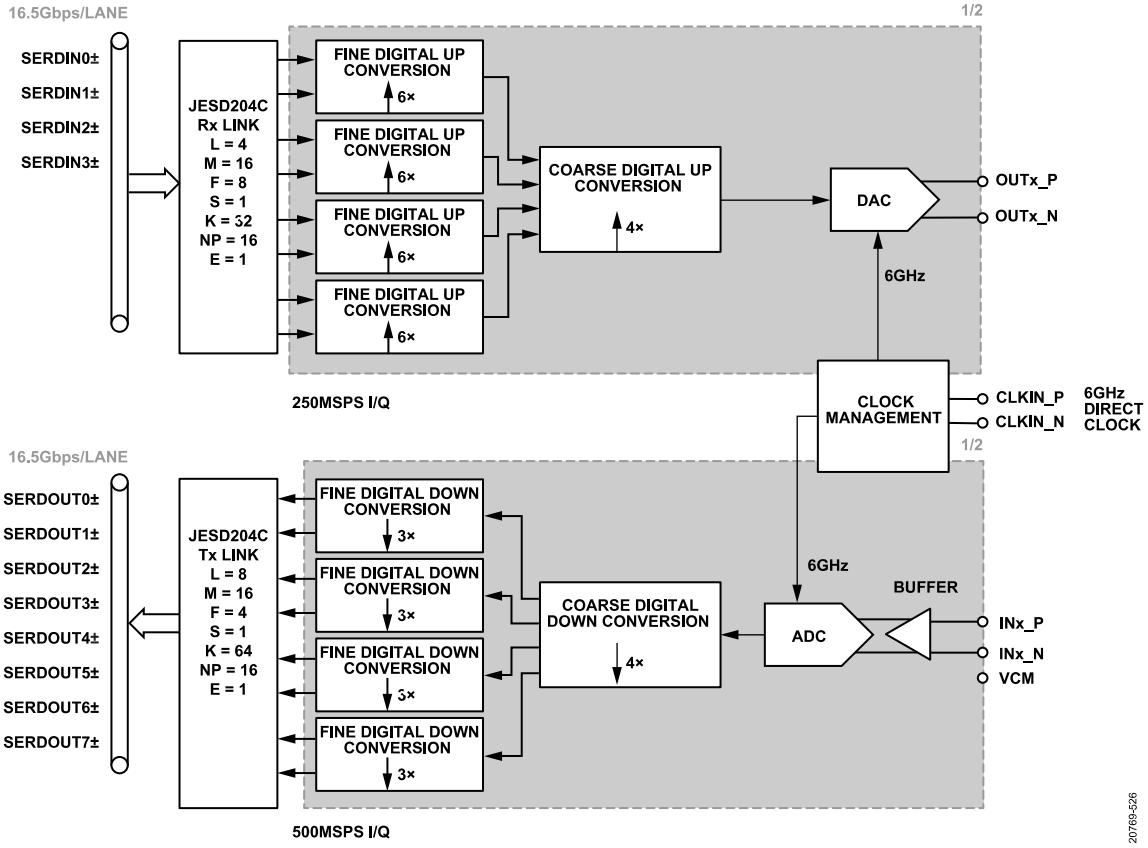

Figure 129. 2D2A Quad Band, DAC in 250 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode Block Diagram

Table 141. Typical and Maximum Power Consumption for 2D2A Quad Band, DAC in 250 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		102	107	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		0.874	1.004	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		360	465	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1710	2095	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		90	150	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	80	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		490	650	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2850	3860	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		530	640	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1100	1550	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		7.47	9.875	W

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Table 141. Typical and Maximum Power Consumption for 2D2A Quad Band, DAC in 250 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		8.4	10.9	W

Example 4: 4D2A Single Band Tx, Dual Band Rx, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Table 142. 4D2A Single Band Tx, Dual Band Rx, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9082, AD9986	4	2	12	6	500 (I/Q)	500 (I/Q)

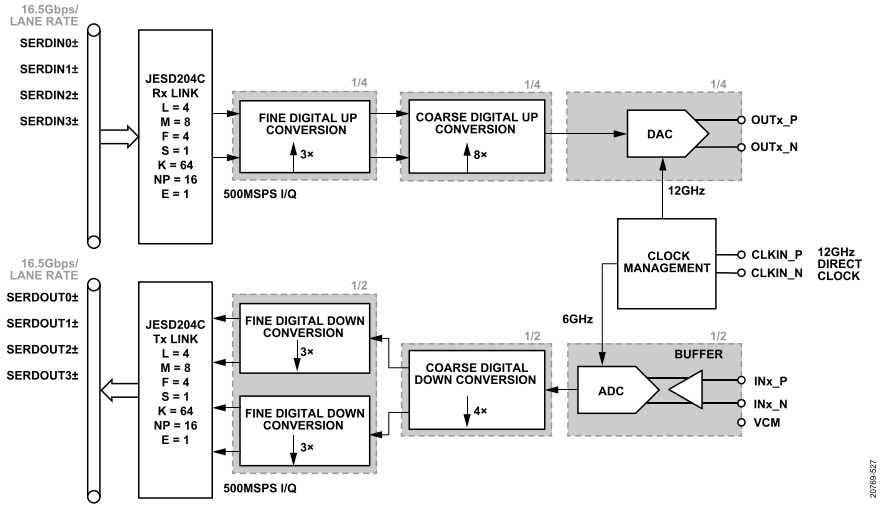

Figure 130. 4D2A Single Band Tx, Dual Band Rx, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode Block Diagram

Table 143. Typical and Maximum Power Consumption for 4D2A Single Band Tx, Dual Band Rx, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		195	204	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.198	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		975	1180	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1725	2100	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		90	150	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	80	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1575	1840	mA
DVDD1 (I_{DVDD1})	1.0 V supply		3240	4340	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		630	760	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		825	1220	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		9.4	12.055	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		10.5	13.3	W

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Example 5: 4D2A Single Band, DAC in 1 GSPS I/Q Mode, ADC in 1 GSPS I/Q Mode

Table 144. 4D2A Single Band, DAC in 1 GSPS I/Q Mode, ADC in 1 GSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (GSPS)	Output Data Rate from ADC (GSPS)
AD9082, AD9986	4	2	12	6	1 (I/Q)	1 (I/Q)

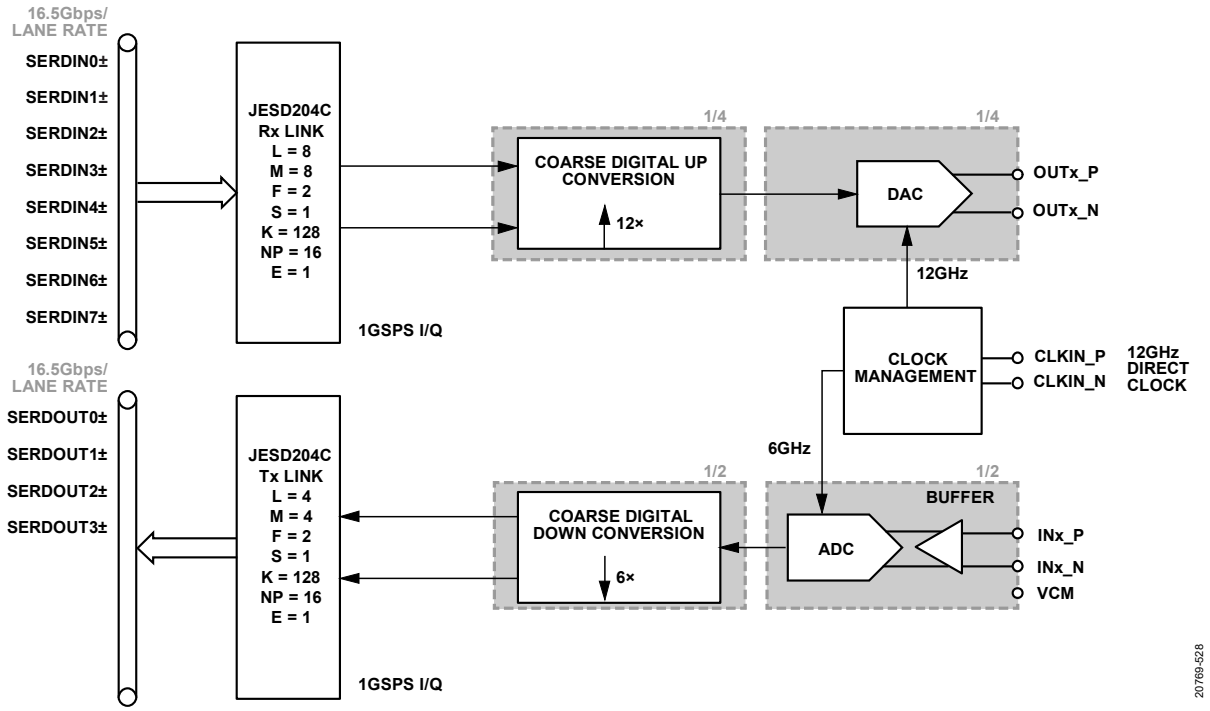

Figure 131. 4D2A Single Band, DAC in 1 GSPS I/Q mode, ADC in 1 GSPS I/Q Mode Block Diagram

Table 145. Typical and Maximum Power Consumption for 4D2A Single Band, DAC in 1 GSPS I/Q Mode, ADC in 1 GSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		195	204	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.198	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		975	1180	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1725	2100	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		90	150	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	80	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1575	1840	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2605	3600	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		630	760	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1100	1550	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		9.04	11.645	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		10.2	12.9	W

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Example 6: 4D2A Single Band, DAC in 750 MSPS I/Q Mode, ADC in 750 MSPS I/Q Mode

Table 146. 4D2A Single Band, DAC in 750 MSPS I/Q Mode, ADC in 750 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9082, AD9986	4	2	12	6	750 (I/Q)	750 (I/Q)

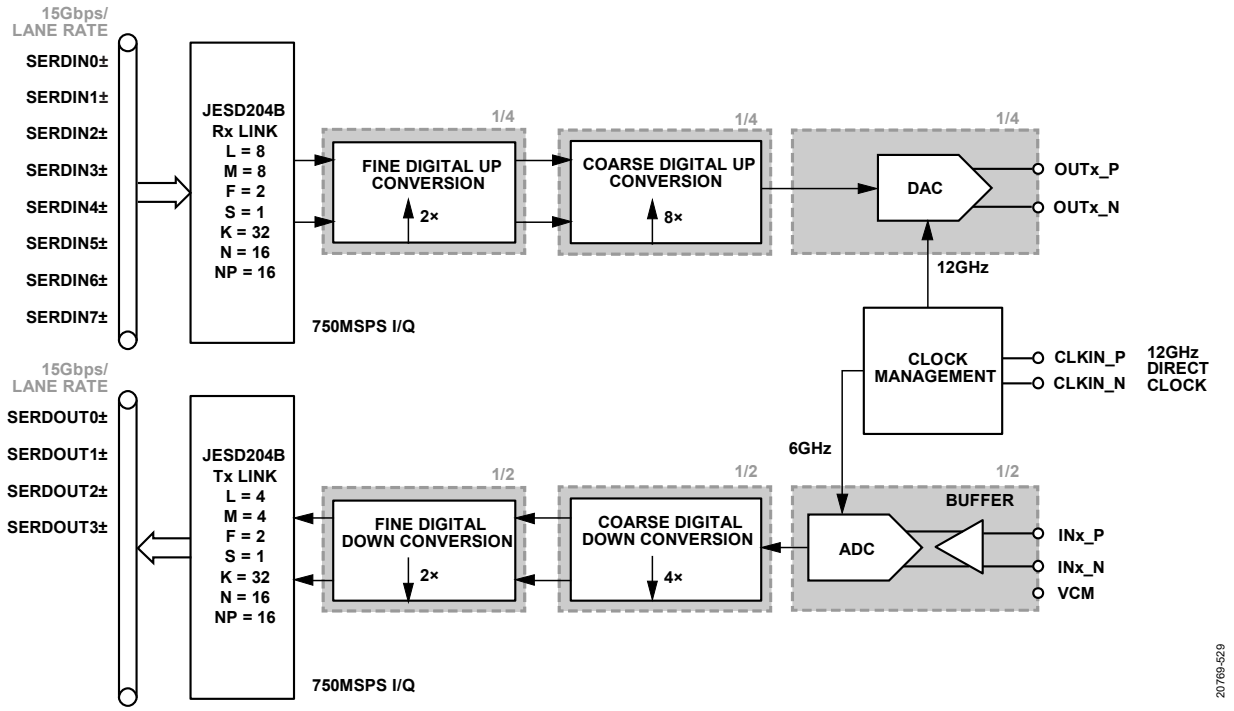

Figure 132. 4D2A Single band, DAC in 750 MSPS I/Q Mode, ADC in 750 MSPS I/Q Mode Block Diagram

Table 147. Typical and Maximum Power Consumption for 4D2A Single Band, DAC in 750 MSPS I/Q Mode, ADC in 750 MSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		195	204	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.198	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		975	1180	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1725	2100	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		90	150	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	80	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1575	1840	mA
DVDD1 (I_{DVDD1})	1.0 V supply		3185	4270	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		630	760	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1140	1620	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		9.66	12.385	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		10.7	13.6	W

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Example 7: 4D2A Single Band, DAC in 375 MSPS I/Q Mode, ADC in 375 MSPS I/Q Mode

Table 148. 4D2A Single Band, DAC in 375 MSPS I/Q Mode, ADC in 375 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9082, AD9986	4	2	12	6	375 (I/Q)	375 (I/Q)

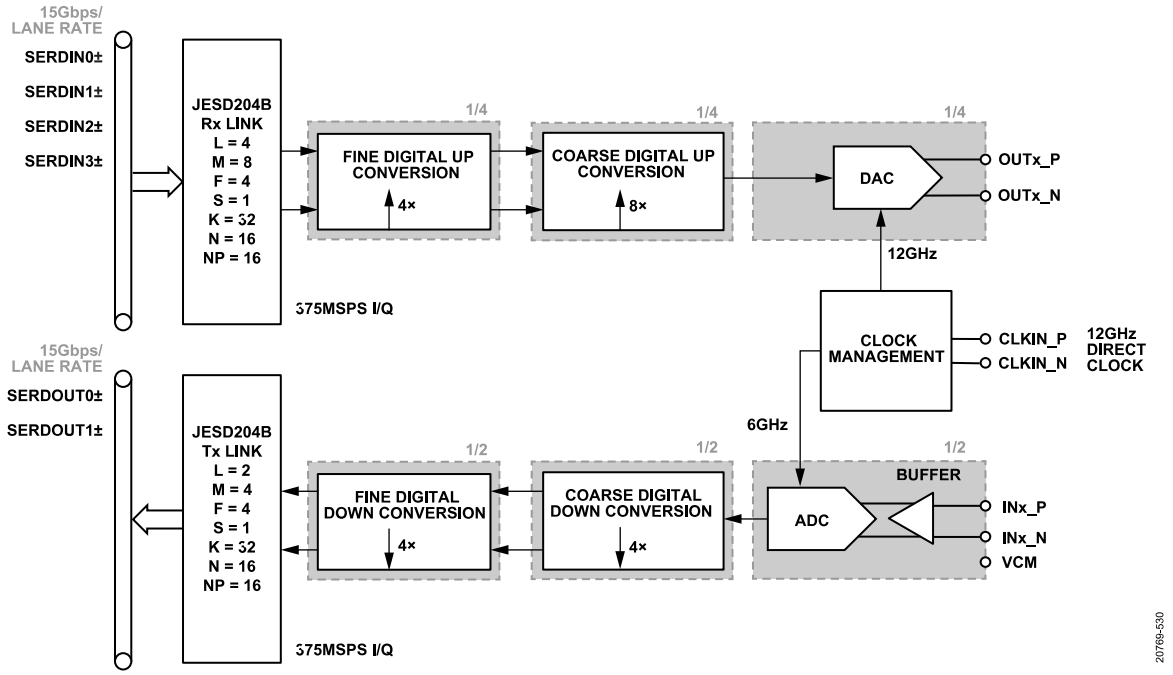

Figure 133. 4D2A Single Band, DAC in 375 MSPS I/Q mode, ADC in 375 MSPS I/Q Mode Block Diagram

Table 149. Typical and Maximum Power Consumption for 4D2A Single Band, DAC in 375 MSPS I/Q Mode, ADC in 375 MSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		195	204	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.198	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		975	1180	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1725	2100	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		90	150	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	80	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1575	1840	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2995	4045	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		630	760	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		745	1130	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		9.075	11.67	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		10.2	12.9	W

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Example 8: 4D2A Single Band, DAC in 375 MSPS I/Q Mode, ADC in 375 MSPS I/Q Mode with On-Chip PLL

Table 150. 4D2A Single Band, DAC in 375 MSPS I/Q Mode, ADC in 375 MSPS I/Q Mode with On-Chip PLL

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9082, AD9986	4	2	12	6	375 (I/Q)	375 (I/Q)

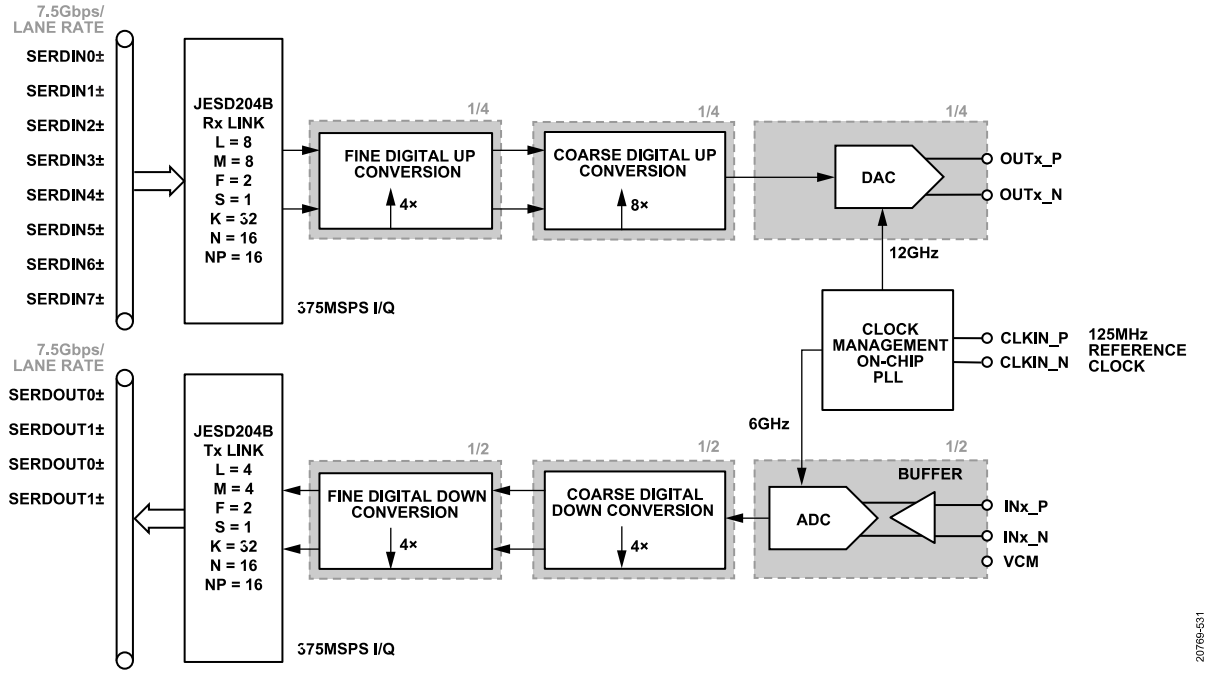

Figure 134. 4D2A Single Band, DAC in 375 MSPS I/Q mode, ADC in 375 MSPS I/Q Mode with On-Chip PLL Block Diagram

Table 151. Typical and Maximum Power Consumption for 4D2A Single Band, DAC in 375 MSPS I/Q Mode, ADC in 375 MSPS I/Q Mode with On-Chip PLL

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		195	204	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.198	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		975	1180	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1725	2100	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		90	150	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	80	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1575	1840	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2995	4045	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		630	860	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		930	1360	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		9.26	12	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		10.4	13.3	W

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Example 9: 4D2A Dual Band, Dual Link, DAC in 375 MSPS I/Q Mode, ADC in 187.5 MSPS I/Q Mode

Table 152. 4D2A Dual Band, Dual Link, DAC in 375 MSPS I/Q Mode, ADC in 187.5 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9081, AD9082, AD9986, AD9988	4	2	12	3	375 (I/Q)	187.5 (I/Q)

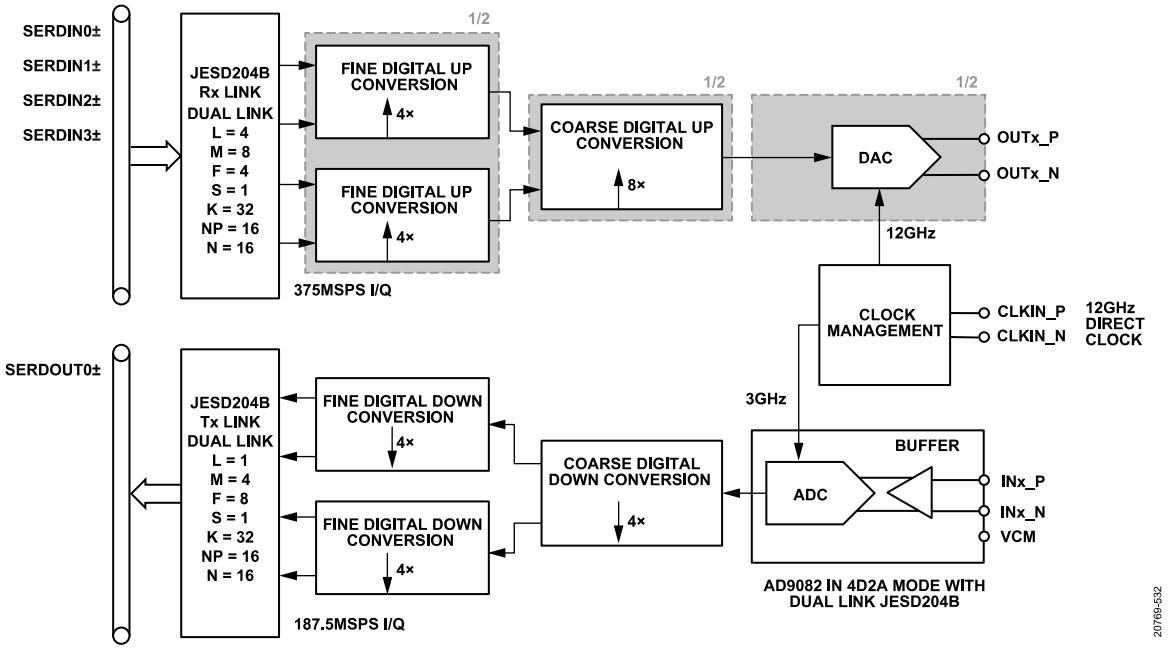

Figure 135. 4D2A Dual Band, Dual Link, DAC in 375 MSPS I/Q Mode, ADC in 187.5 MSPS I/Q Mode Block Diagram

Table 153. Typical and Maximum Power Consumption for 4D2A Dual Band, Dual Link, DAC in 375 MSPS I/Q Mode, ADC in 187.5 MSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		195	204	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.198	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		975	1180	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1330	1670	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		55	115	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	80	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1575	1840	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2340	3885	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		375	500	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1025	1460	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		8.015	11.115	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		9.1	12.3	W

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Example 10: 4D2A Dual Band, Dual Link, DAC in 375 MSPS I/Q Mode, ADC in 187.5 MSPS I/Q Mode with On-Chip PLL

Table 154. 4D2A Dual Band, Dual Link, DAC in 375 MSPS I/Q Mode, ADC in 187.5 MSPS I/Q Mode with On-Chip PLL

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9081, AD9082, AD9986, AD9988	4	2	12	3	375 (I/Q)	187.5 (I/Q)

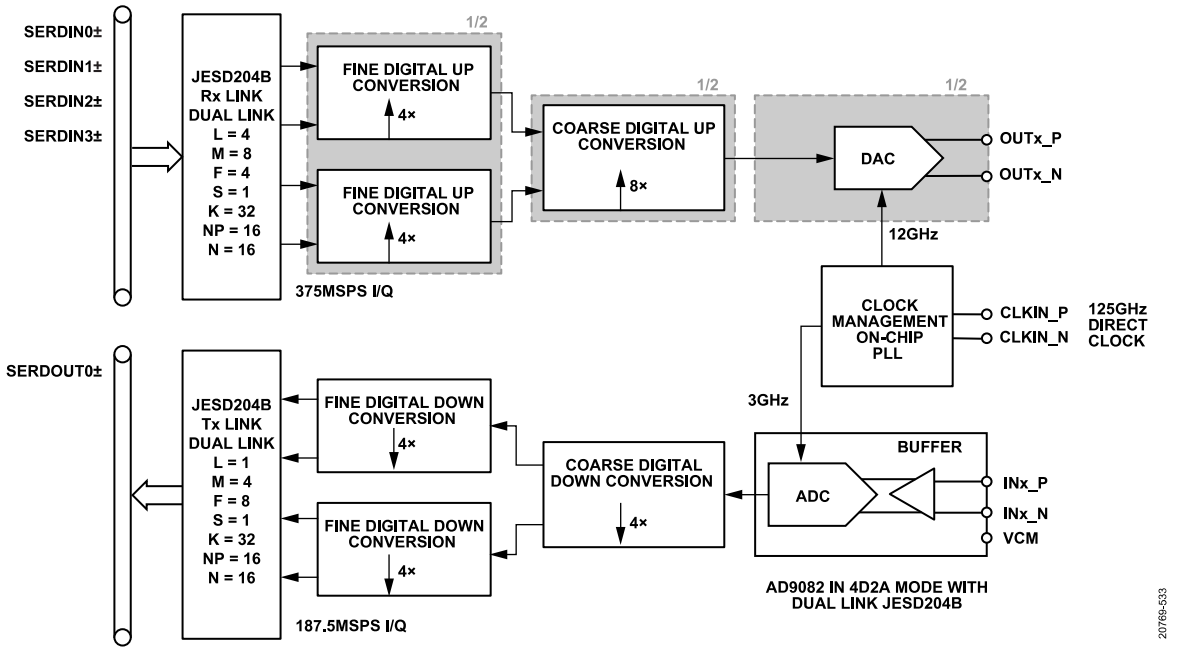

Figure 136. 4D2A Dual Band, Dual Link, DAC in 375MSPS I/Q Mode, ADC in 187.5 MSPS I/Q Mode with On-Chip PLL Block Diagram

Table 155. Typical and Maximum Power Consumption for 4D2A Dual Band, Dual Link, DAC in 375 MSPS I/Q Mode, ADC in 187.5 MSPS I/Q Mode with On-Chip PLL

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		195	204	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		80	100	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.13	1.288	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		20	30	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		975	1180	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1300	1855	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		55	115	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	80	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1575	1840	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2340	3885	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		375	500	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1025	1460	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		7.99	11.305	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		9.2	12.6	W

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Example 11: 2D2A, DAC in 6 GSPS Real Mode, ADC in 6 GSPS Full Bandwidth Mode

Table 156. 2D2A, DAC in 6 GSPS Real Mode, ADC in 6 GSPS Full Bandwidth Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (GSPS)	Output Data Rate from ADC (GSPS)
AD9082	2	2	6	6	6	6

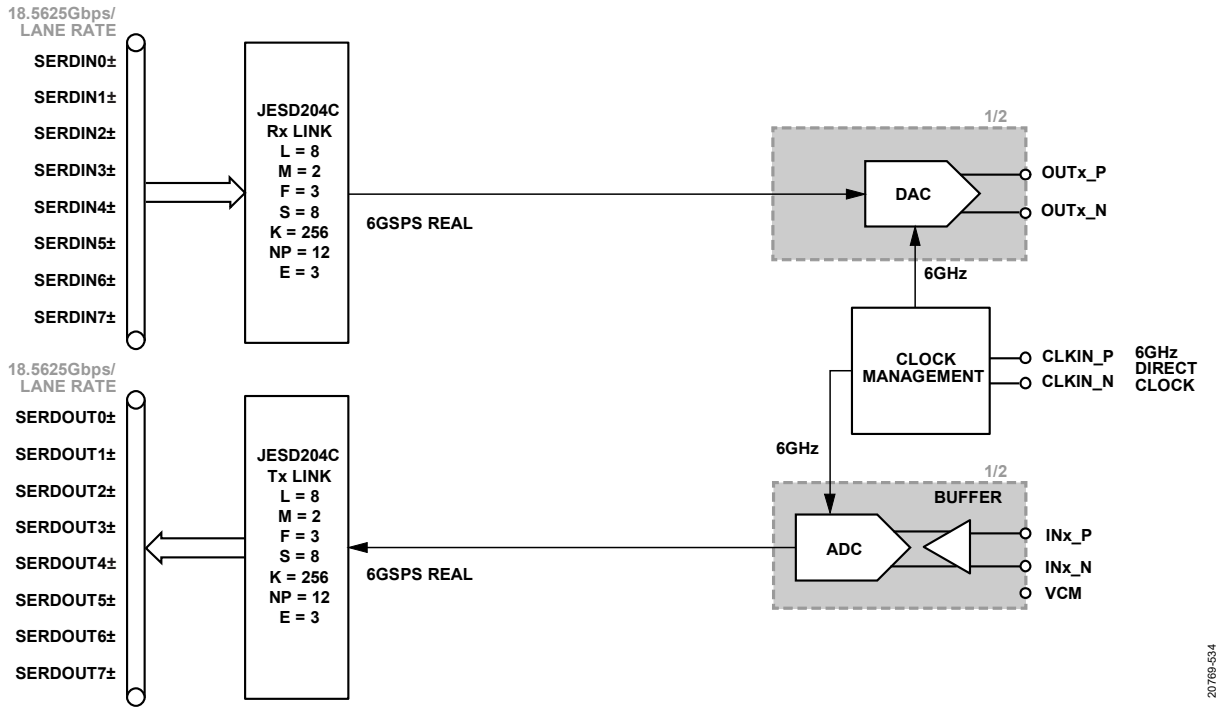

Figure 137. 2D2A, DAC in 6 GSPS Real Mode, ADC in 6 GSPS Full Bandwidth Mode Block Diagram

Table 157. Typical and Maximum Power Consumption for 2D2A, DAC in 6 GSPS Real Mode, ADC in 6 GSPS Full Bandwidth Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		103	107	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		0.876	1.004	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		8	15	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		350	450	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1725	2100	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		90	150	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	80	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		490	650	mA
DVDD1 (I_{DVDD1})	1.0 V supply		1425	2320	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		515	620	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1500	2040	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		6.428	8.785	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		7.4	9.8	W

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Example 12: 4D2A, Dual Band, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Table 158. 4D2A, Dual Band, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9081, AD9082, AD9986, AD9988	4	2	9	3	375 (I/Q)	187.5 (I/Q)

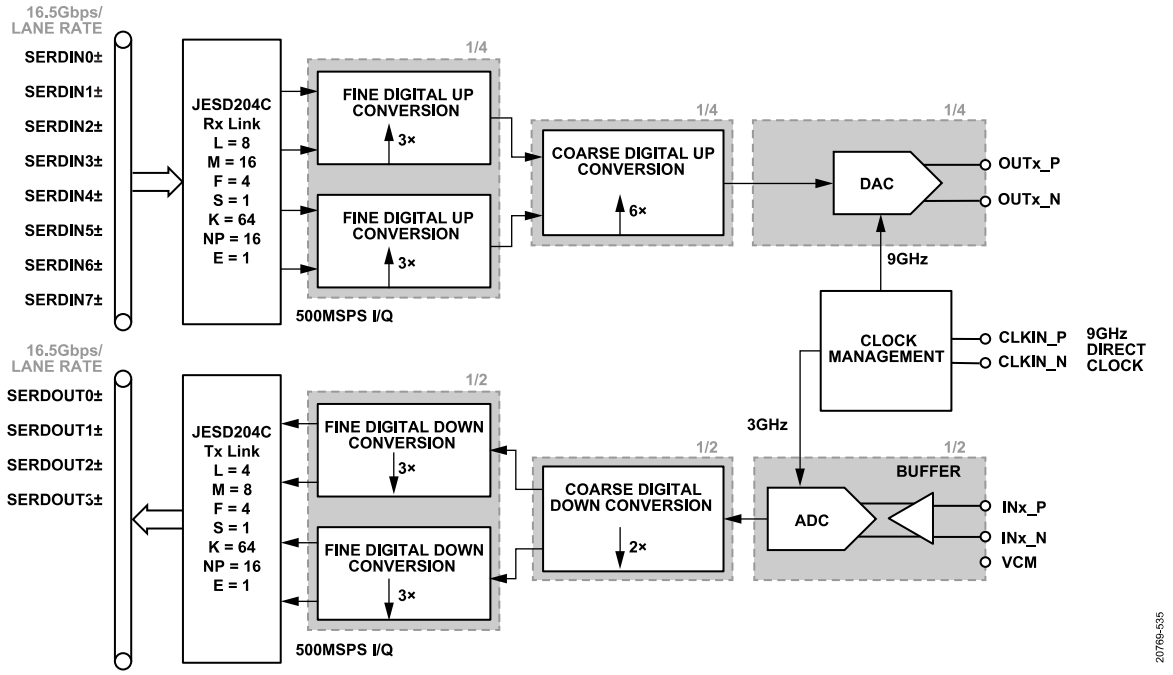

Figure 138. 4D2A, Dual Band, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode Block Diagram

Table 159. Typical and Maximum Power Consumption for 4D2A, Dual Band, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		195	204	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		290	340	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.198	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		10	20	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		750	930	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1325	1650	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		55	115	mA
FVDD1 (I_{FVDD1})	1.0 V supply		40	70	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	360	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1200	1430	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2850	3850	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		375	500	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1100	1550	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		7.985	10.475	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		9.1	11.7	W

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Example 13: 4D4A, DAC in 1.5 GSPS I/Q Mode, ADC in 3 GSPS Full Bandwidth Mode

Table 160. 4D4A, DAC in 1.5 GSPS I/Q Mode, ADC in 3 GSPS Full Bandwidth Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (GSPS)	Output Data Rate from ADC (GSPS)
AD9081	4	4	12	3	1.5 (I/Q)	3

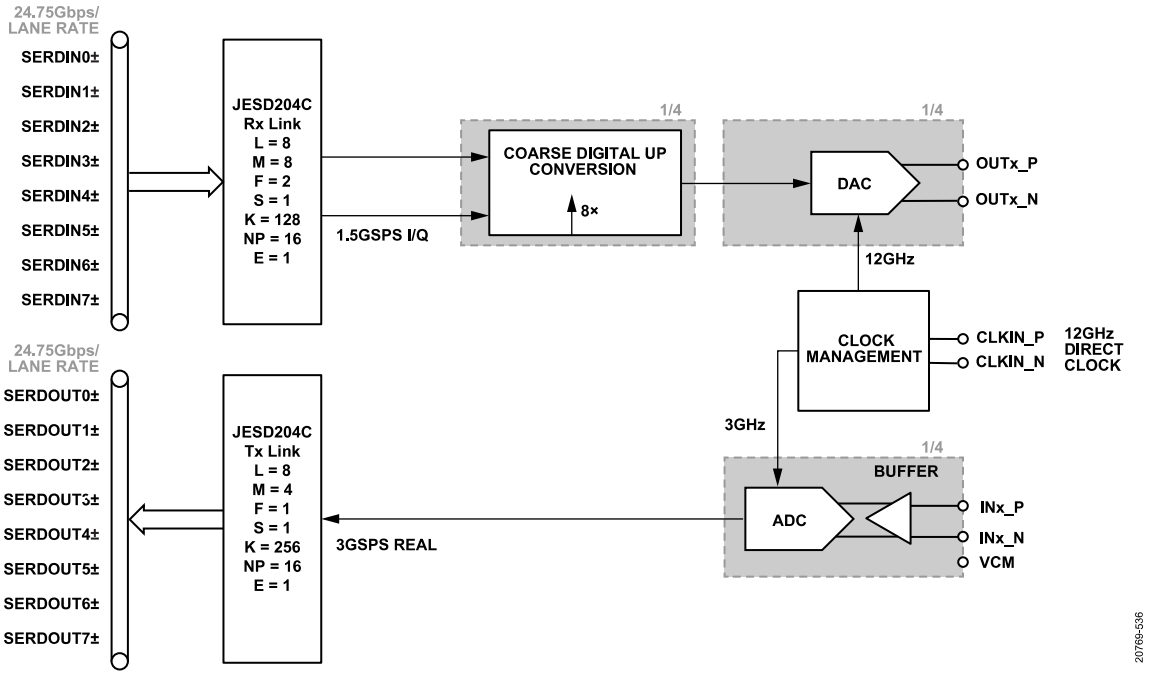

Figure 139. 4D4A, DAC in 1.5 GSPS I/Q Mode, ADC in 3GSPS Full Bandwidth Mode Block Diagram

Table 161. Typical and Maximum Power Consumption for 4D4A, DAC in 1.5 GSPS I/Q Mode, ADC in 3 GSPS Full Bandwidth Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		190	205	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		295	350	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.22	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		1000	1185	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1625	1910	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		60	110	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	65	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	345	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1600	1835	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2400	3400	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		570	700	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1920	2570	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		9.515	12.145	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		10.6	13.4	W

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Example 14: 4D4A, DAC in 1 GSPS I/Q Mode, ADC in 1 GSPS I/Q Mode

Table 162. 4D4A, DAC in 1 GSPS I/Q Mode, ADC in 1 GSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (GSPS)	Output Data Rate from ADC (GSPS)
AD9081, AD9988	4	4	12	4	1 (I/Q)	1 (I/Q)

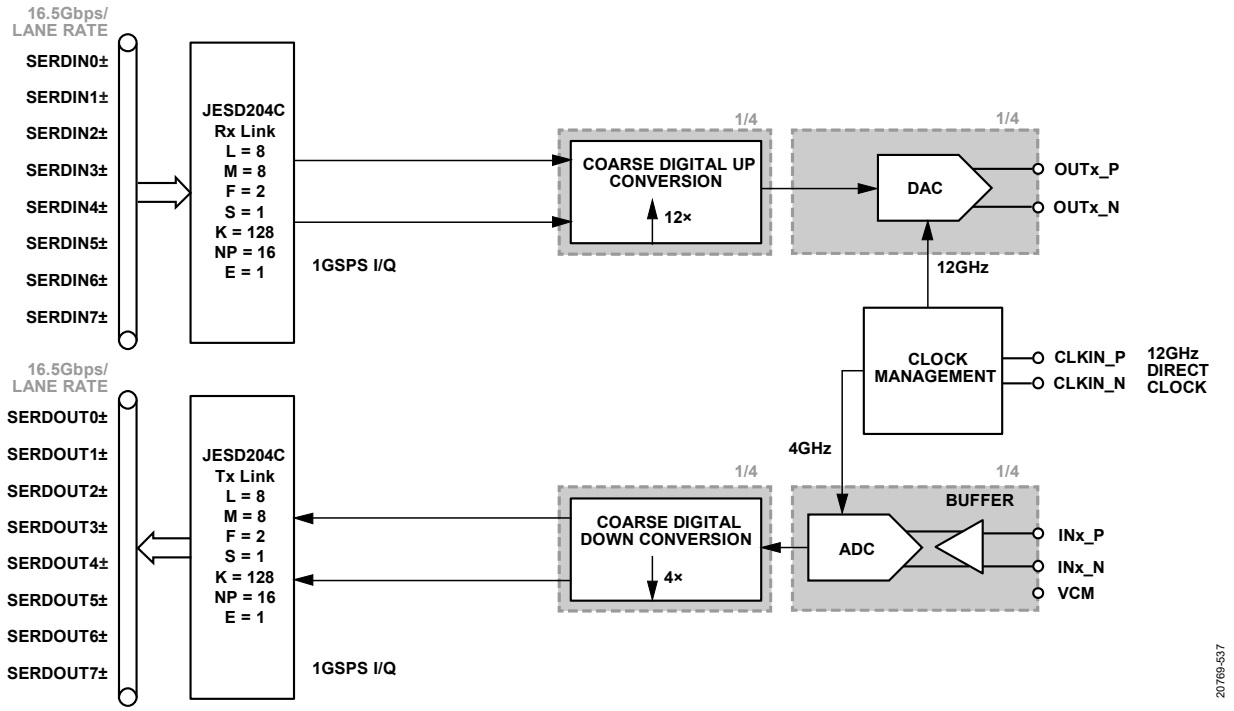

Figure 140. Block Diagram 4D4A, DAC in 1 GSPS I/Q Mode, ADC in 1 GSPS I/Q Mode

Table 163. Typical and Maximum Power Consumption for 4D4A, DAC in 1 GSPS I/Q Mode, ADC in 1 GSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		190	205	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		295	355	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.23	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		1000	1185	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1825	2155	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		70	125	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	70	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	345	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1600	1835	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2600	3585	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		720	840	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1420	1960	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		9.575	12.125	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		10.6	13.4	W

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Example 15: 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Table 164. 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9081, AD9988	4	4	12	4	500 (I/Q)	500 (I/Q)

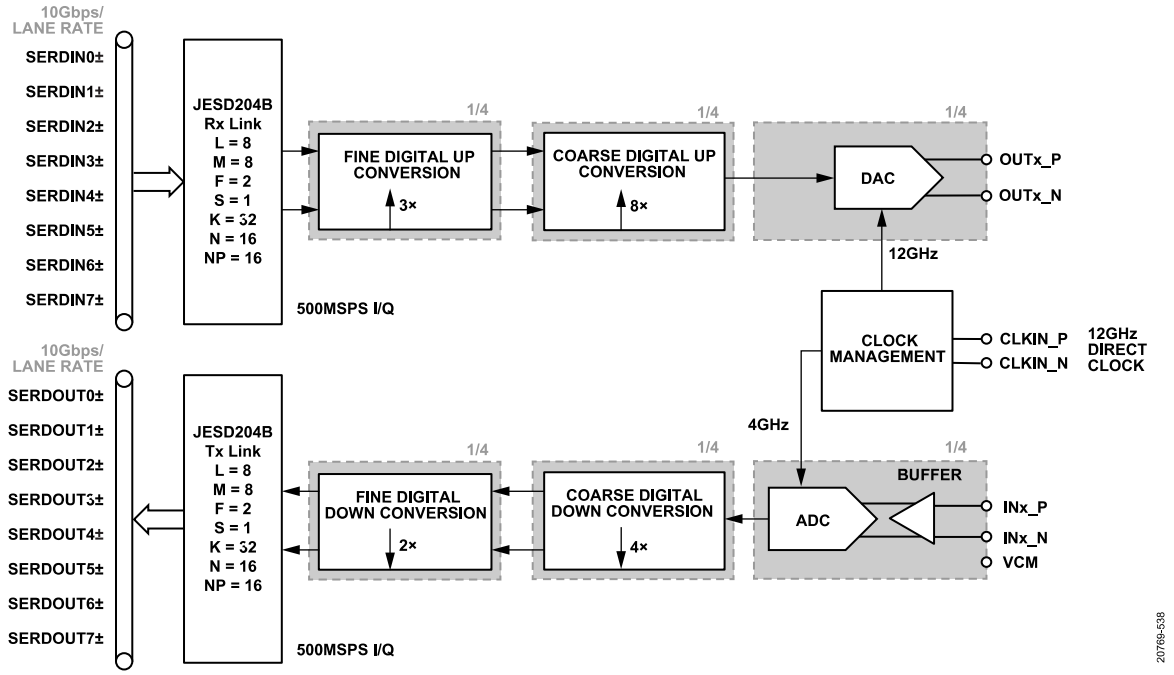

Figure 141. 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode Block Diagram

Table 165. Typical and Maximum Power Consumption for 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		190	205	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		295	355	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.23	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		1000	1200	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1830	2155	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		70	125	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	70	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	345	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1600	1835	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2850	3895	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		700	830	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1070	1530	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		9.46	12.01	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		10.5	13.3	W

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Example 16: 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Table 166. 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9081, AD9988	4	4	12	4	500 (I/Q)	500 (I/Q)

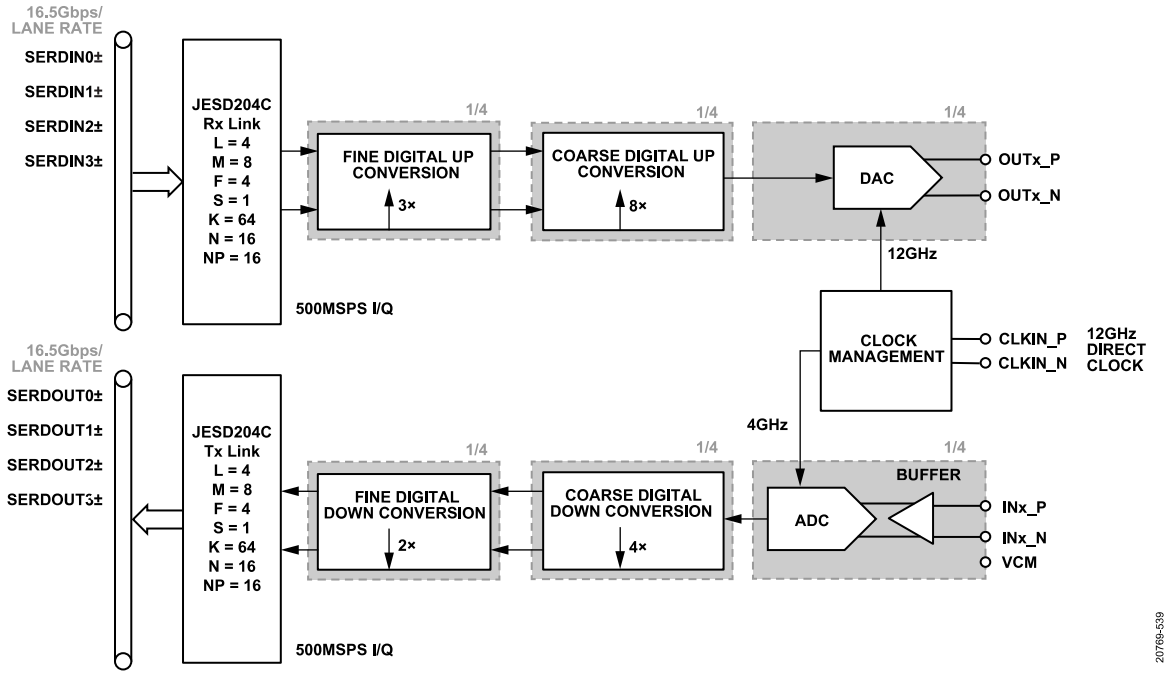

Figure 142. 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode Block Diagram

Table 167. Typical and Maximum Power Consumption for 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		190	205	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		295	355	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.23	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		1000	1200	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1825	2155	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		70	125	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	70	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	345	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1590	1835	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2650	3625	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		710	840	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		840	1270	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		9.025	11.49	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		10.1	12.7	W

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Example 17: 4D4A, DAC in 2 GSPS I/Q Mode, ADC in 2 GSPS I/Q Mode

Table 168. 4D4A, DAC in 2 GSPS I/Q Mode, ADC in 2 GSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (GSPS)	Output Data Rate from ADC (GSPS)
AD9081, AD9988	4	4	12	4	2 (I/Q)	2 (I/Q)

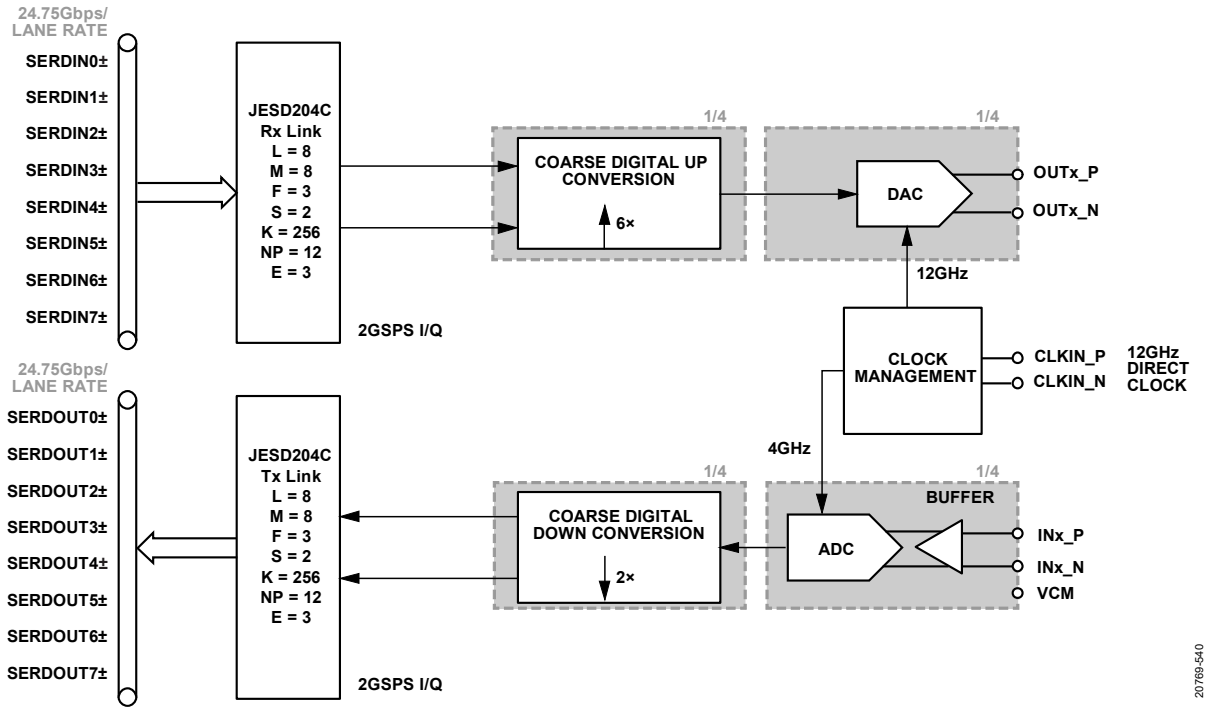

Figure 143. 4D4A, DAC in 2 GSPS I/Q Mode, ADC in 2 GSPS I/Q Mode Block Diagram

Table 169. Typical and Maximum Power Consumption for 4D4A, DAC in 2 GSPS I/Q Mode, ADC in 2 GSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		190	205	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		295	355	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.23	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		1000	1200	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1840	2155	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		70	125	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	70	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	340	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1600	1835	mA
DVDD1 (I_{DVDD1})	1.0 V supply		3175	4225	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		715	840	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1925	2570	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		10.665	13.385	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		11.7	14.6	W

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Example 18: 4D4A, DAC in 250 MSPS I/Q Mode, ADC in 250 MSPS I/Q Mode

Table 170. 4D4A, DAC in 250 MSPS I/Q Mode, ADC in 250 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9081, AD9988	4	4	12	4	250 (I/Q)	250 (I/Q)

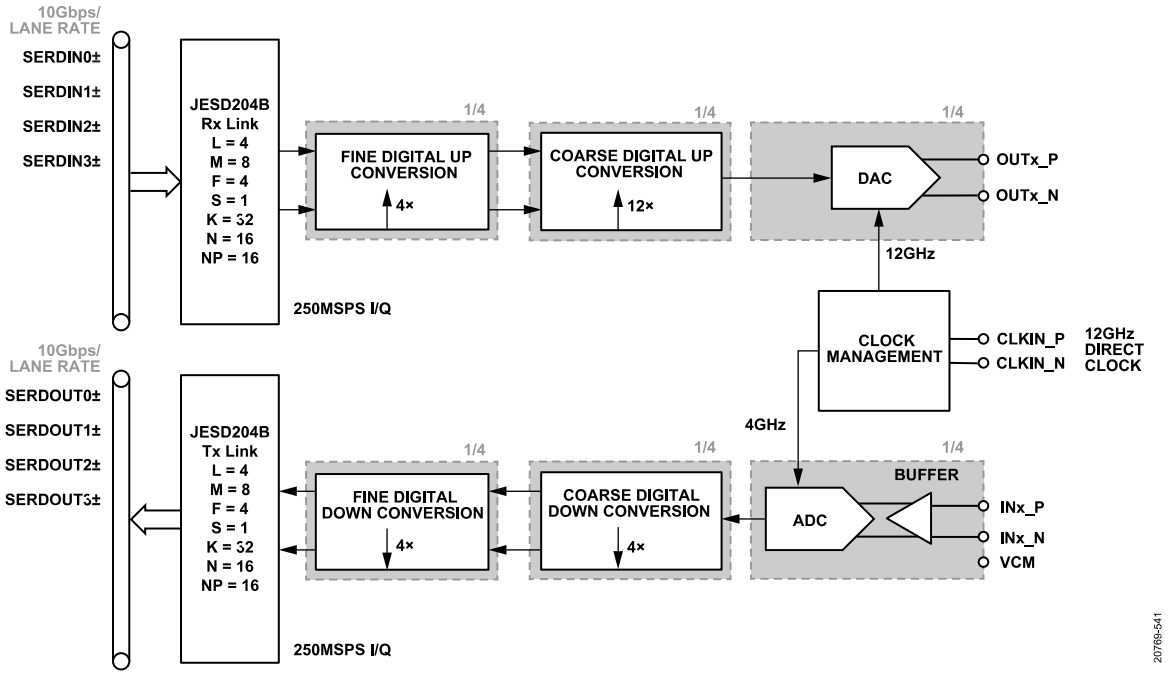

Figure 144. 4D4A, DAC in 250 MSPS I/Q Mode, ADC in 25 0MSPS I/Q Mode Block Diagram

Table 171. Typical and Maximum Power Consumption for 4D4A, DAC in 250 MSPS I/Q Mode, ADC in 250 MSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		190	205	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		295	355	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.23	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		1000	1200	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1840	2155	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		70	125	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	70	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	345	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1600	1835	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2500	3465	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		700	825	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		680	1065	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		8.73	11.11	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		9.8	12.4	W

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Example 19: 4D4A, DAC in 250 MSPS I/Q Mode, ADC in 250 MSPS I/Q Mode with On-Chip PLL

Table 172. 4D4A, DAC in 250 MSPS I/Q Mode, ADC in 250 MSPS I/Q Mode with On-Chip PLL

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9081, AD9988	4	4	12	4	250 (I/Q)	250 (I/Q)

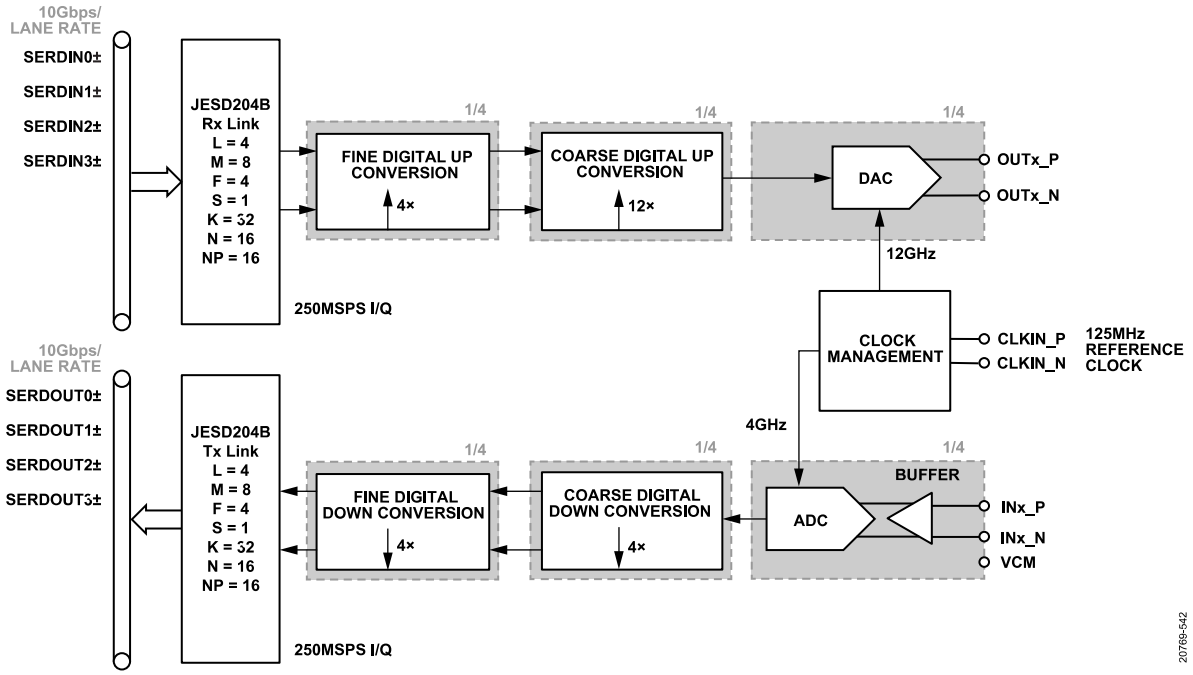

Figure 145. 4D4A, DAC in 250 MSPS I/Q Mode, ADC in 250 MSPS I/Q Mode with On-Chip PLL Block Diagram

Table 173. Typical and Maximum Power Consumption for 4D4A, DAC in 250 MSPS I/Q Mode, ADC in 250 MSPS I/Q Mode with On-Chip PLL

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		190	205	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		295	355	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		80	100	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.13	1.32	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		25	30	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		1000	1225	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1840	2155	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		70	125	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	70	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	345	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1560	1815	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2500	3465	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		700	825	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		680	1065	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		8.7	11.12	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		9.9	12.5	W

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Example 20: 4D4A, DAC in 750 MSPS I/Q Mode, ADC in 750 MSPS I/Q Mode

Table 174. 4D4A, DAC in 750 MSPS I/Q Mode, ADC in 750 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9081, AD9988	4	4	12	3	750 (I/Q)	750 (I/Q)

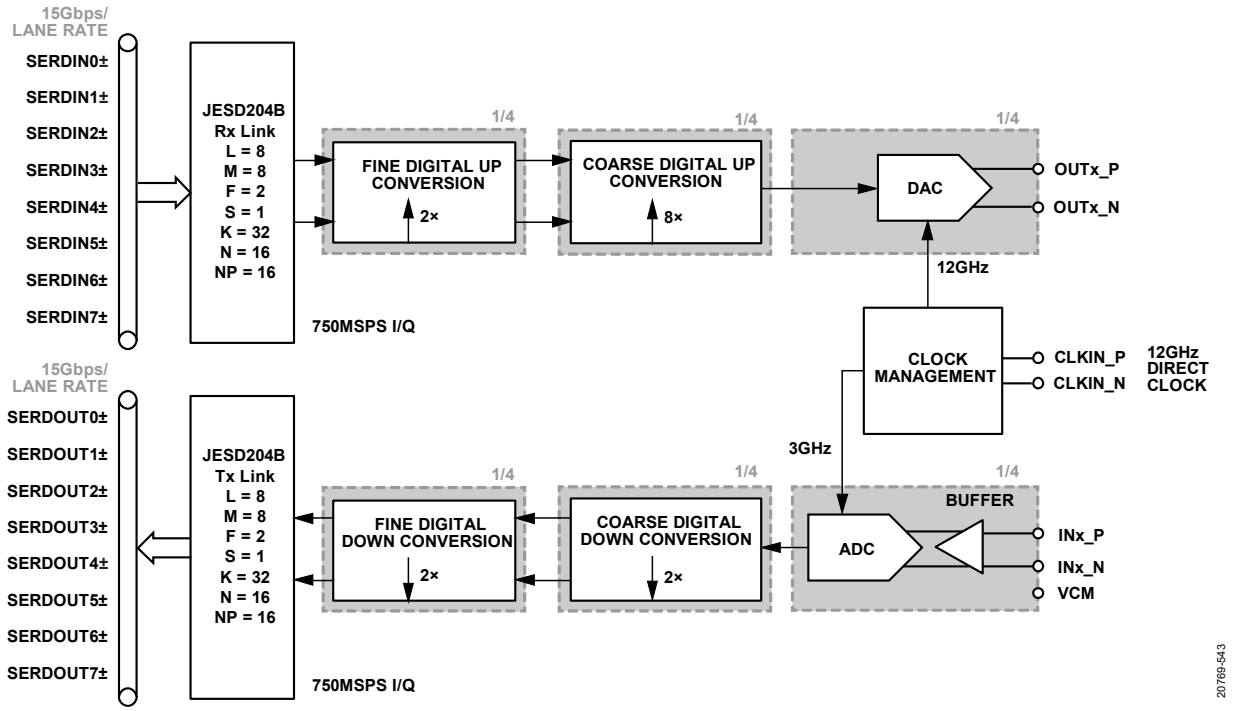

Figure 146. 4D4A, DAC in 750 MSPS I/Q Mode, ADC in 750 MSPS I/Q Mode Block Diagram

Table 175. Typical and Maximum Power Consumption for 4D4A, DAC in 750 MSPS I/Q Mode, ADC in 750 MSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		190	205	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		295	50	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	0.62	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		1000	1200	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1620	1900	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		60	110	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	65	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	345	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1580	1845	mA
DVDD1 (I_{DVDD1})	1.0 V supply		3260	4375	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		550	650	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1430	1990	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		9.84	12.505	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		10.9	13.1	W

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Example 21: 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Table 176. 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Applicable Devices	No. of Tx Channels	No. of Rx Channels	DAC Clock Rate (GHz)	ADC Clock Rate (GHz)	Input Data Rate to DAC (MSPS)	Output Data Rate from ADC (MSPS)
AD9081, AD9988	4	4	9	3	500 (I/Q)	500 (I/Q)

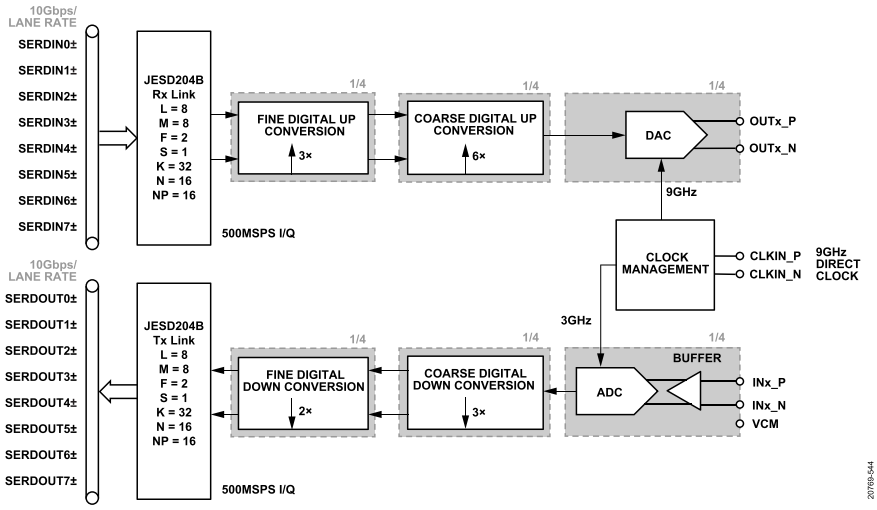

Figure 147. 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode Block Diagram

Table 177. Typical and Maximum Power Consumption for 4D4A, DAC in 500 MSPS I/Q Mode, ADC in 500 MSPS I/Q Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		190	205	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		295	350	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	55	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		1.06	1.22	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		12	25	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1($I_{DCLKVDD1}$)	1.0 V supply		775	940	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1620	1900	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		55	110	mA
FVDD1 (I_{FVDD1})	1.0 V supply		45	65	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		280	345	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1210	1430	mA
DVDD1 (I_{DVDD1})	1.0 V supply		2850	3885	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		515	650	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1075	1550	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		8.437	10.9	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		9.5	12.1	W

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POWER MANAGEMENT CONSIDERATIONS

The device has seventeen different power supply domains, as shown in Table 178, with maximum estimated current draw. The device requires a 2 V supply and a 1 V supply with a tolerance of ±5%.V. The digital supply for CMOS interfaces can operate over a 1.8 V to 2 V range.

Note the following:

- Table 78 lists the analog supply domain, on-chip regulators used to generate −2 V, −1 V, and +3 V supplies.
- Both the analog and digital supply domains operate from 2 V and 1 V supplies.
- The device requires no specific power supply sequencing order.
- The evaluation board uses a via-in-pad method with through-hole vias for all supply and ground pins, although a via adjacent to pad is also possible if many pins remain unused. An 0201, 0.1 µF decoupling capacitor is used on each via supply pin (unless otherwise noted).
- The AVDD2, BVDD2, RVDD2, AVDD1, AVDD1_ADC, and CLKVDD1 analog supply domains are sensitive to noise coupling. These supply domains are placed on the same layer where ground planes isolate the domains from digital supply domain layers.
- Ensure that the 0.1 µF decoupling capacitors for the AVDD1_ADC, CLKVDD1, and PLLCLVDD1 supply domains are initially considered as do not installs (DNI), as well as the 1 µF decoupling capacitor for CLKVDD1, which allows the option to install any capacitor required. Based on the evaluation board characterization for the ADC spurious performance, the addition of these capacitors results in higher levels of spurious levels attributed to digital noise coupling onto the internal sampling clock signal used by the ADC. Power distribution impedance plane modeling indicates that the addition of the 0.1 µF capacitors increases the impedance of the power distribution planes in a lower frequency region (<120 MHz) where digital clock noise can be present when operating the device with higher decimation factors. Because the power distribution network characteristics can vary between PCBs, these capacitors must have the option to be installed. Because of this option, the capacitors are listed as DNI.
- Ensure low power plane impedance to minimize DC voltage drop for domains with a high current load. Consider forming a capacitor with an adjacent ground reference plane to enlarge the power plane area and reduce the impedance at higher frequencies.

Table 178. Power Supply Requirements (±5%)

Pin	Mnemonic	Voltage (V)	Maximum Current (mA)	Description	Routing and Decoupling Notes
A2, E2, H2, L2, P2, V2, L3	AVDD2	2	260	Analog 2.0 V supply input for DAC and PLL.	0.1 µF per via under device, 1 µF in proximity to device
D7, E7, P7, R7, B11, U11	BVDD2+RVDD2	2	350	Analog 2.0 V supply input for ADC buffer.	0.1 µF per via under device, 1 µF in proximity to device
D2, R2, D3, E3, F3, N3, P3, R3, D4, R4,	AVDD1	1	1400	Analog 1.0 V supply input for DAC clock.	0.1 µF per via under device, 1 µF in proximity to device
G7, G8, M7, M8	AVDD1_ADC		2000	Analog 1.0 V supply input for ADC buffer and core.	Layout our for 0.1 µF per via under device and 1 µF in proximity to device but have 0.1 µF be DNI
G6, M6	CLKVDD1	1	20	Analog 1.0 V supply input for ADC clock.	Layout our for 0.1 µF per via under device and 1 µF in proximity to device but have 0.1 µF and 1 µF be DNI
J5	PLLCLKVDD1	1	40	Analog 1.0 V supply input for clock PLL.	Layout our for 0.1 µF per via under device and 1 µF in proximity to device but have 0.1 µF be DNI
D6, R6	FVDD1	1	56	Analog 1.0 V supply input for ADC reference.	0.1 µF per via under device, 1 µF in proximity to device
D10, R10	VDD1_NVG	1	340	Analog 1.0 V supply input for negative voltage generator (NVG) used to generate −1 V output.	0.1 µF per via under device, 1 µF in proximity to device
E5, F5, N5, P5	DAVDD1	1	1800	Digital Analog 1.0 V supply input.	0.1 µF per via under device, 1 µF in proximity to device
H9, J9, K9, L9, M9, F10, H11, J11, K11, L11	DVDD1	1	4000[1], 3000[2]	Digital 1.0 V supply input.	0.1 µF per via under device, 1 µF in proximity to device
J7, K7 (J6 and K6 also for AD9082, AD9986)	DVDD1_RT	1	860	Digital 1.0 supply input for retimer block.	0.1 µF per via under device, 1 µF in proximity to device
K5	DCLKVDD1	1	120	Digital 1.0 V clock generation supply.	0.1 µF per via under device, 1 µF in proximity to device

APPLICATIONS INFORMATION

Table 178. Power Supply Requirements (±5%) (Continued)

Pin	Mnemonic	Voltage (V)	Maximum Current (mA)	Description	Routing and Decoupling Notes
A16 to H16, M16 to V16	SVDD1	1	2570[3], 1220[4]	Digital 1.0 V supply input for SERDES deserializer and serializer.	0.1 µF per via under device, 1 µF in proximity to device
K15	SVDD2_PLL	2	50	Digital 2.0 V supply input for SERDES LDO regulator used by VCO.	0.1 µF per via under device, 1 µF in proximity to device
J16, K16	SVDD1_PLL	1	80	Digital 1.0 V supply input for SERDES clock generation and PLL.	0.1 µF per via under device, 1 µF in proximity to device
C13, F9, T13	DVDD1P8	1.8 to 2 V	4	Digital input/output interface and TMU supply input.	0.1 µF per via under device, 1 µF in proximity to device

[1] DAC Rate = 9 GSPS, ADC Rate = 3 GSPS.

[2] DAC Rate = 6 GSPS, ADC Rate = 3 GSPS.

[3] JESD204C eight lanes at 24.75 Gbps.

[4] JESD204C four lanes at 16.75 Gbps.

Table 179. On-Chip Power Supply Regulators Outputs and Associated Inputs

Pin Name	Pin	Voltage (V)	Description	Decoupling Requirements
NVG1_OUT	E9, P9	−1	Analog −1 V Supply Output from NVG.	0.1 µF per via under device
BVNN2	C9, T9	−2	Analog −2 V Supply Output for ADC Buffer.	0.1 µF per via under device
BVDD3	C10, T10	3	Analog 3 V Supply Output for ADC Buffer.	0.1 µF per via under device
BVNN1	D8, E8, P8, R8	−1	Analog −1V Supply Input for ADC Buffer.	Connect to neighboring NVG1_OUT pin
RVNN1	E10, P10	−1	Analog −1V Supply Input for ADC Reference.	Connect to neighboring NVG1_OUT pin

Power Delivery Network

A suggested power delivery network to accommodate many modes of operation for a single device is shown in Figure 148. Note that for modes having high SERDOUT lane count, consider moving the SVDD1 supply domain such that it is powered by same domain as DVDD1 to reduce the current loading on the ADP1765 which is limited to 5 A. Ferrite beads are used to isolate each supply domain. The ferrite beads are sized to limit the voltage drop across it such that the ±5% regulation specification is maintained. The DVDD1 supply does not use a ferrite bead because of the high current draw. Avoid connecting the DVDD1_RT to the DVDD1 domain because it may have large transient loads during the device initialization boot process that may momentarily drop the switcher output supply voltage below the rated minimum of 0.95 V. Typically, the system board has a universal 1.8 V supply.

THERMAL MANAGEMENT CONSIDERATIONS

The power consumption of the device is mode dependent and can exceed 9 W in many modes, especially when all ADC and DACs operate near their maximum sample rate. In such cases, thermal management must be considered such that the die temperature of the device does not exceeds the maximum operating temperature of 120°C. The thermal resistance of the device listed in the datasheet provides an indication of the heat transfer characteristics under specific conditions defined by JESD51-12. The θ_{JA} parameter can be used to establish a baseline in comparison to other devices (using similar test methodology listed in JESD51-12) but is highly dependent on the PCB design (such as size, thickness, and vias) and operating environment (such as air flow). As a result, thermal simulation of the PCB and the environment using specialized CAD tools and thermal device models (such as the Delphi compact model) is recommended to determine if additional thermal reduction methods are required.

For active cooling implementations, the device includes an on-chip TMU that can be read back to determine the die temperature. Refer to the AN-1432 Application Note for an overview of on-chip die temperature techniques and considerations. When reading back the TMU temperature as part of an active cooling control loop with temperature thresholds to activate cooling, the following two factors must also be considered. First, the TMU can report the highest temperature among the multiple temperature sensors situated around the die with the localized hot spots 2°C to 3°C being higher than what is reported as the maximum temperature. Second, an uncalibrated TMU has gain and offset error that results in an error.

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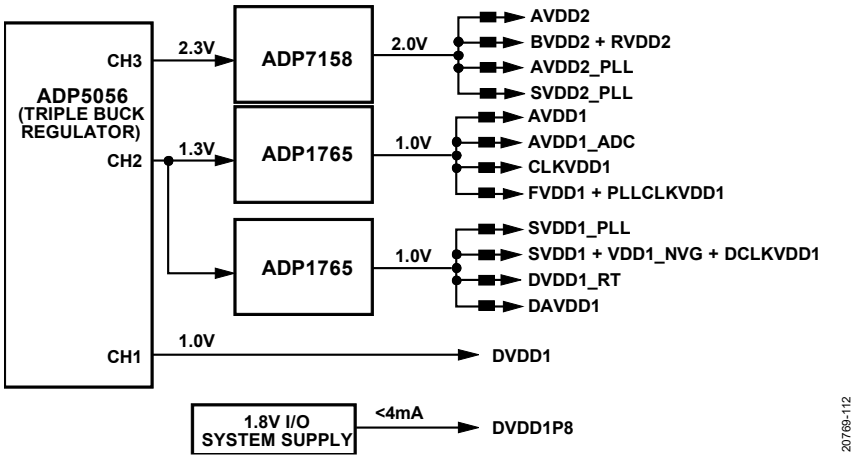

Figure 148. Suggested Power Delivery Network

DEVICE TEST MODES

ADC DATAPATH TEST MODES

ADC sample test pattern data can be inserted into the data formatter block of the receiver (ADC) datapath, as shown in Figure 149. To select the I-pattern data, use the TMODE_I_TYPE_SEL bits (Register 0x02B0, Bits[7:4]). The data can be routed to any even channel output of the DF_{OUT} block using DFORMAT_TMODE_SEL, Bits[15:0] (Register 0x02AD to Register 0x02AE). To select Q pattern data, use the TMODE_Q_TYPE_SEL bits (Register 0x02D4, Bits[7:4]). The data can be routed to any e odd channel output of the DF_{OUT} block using the DFORMAT_TMODE_SEL, Bits[15:0] bit field. (Register 0x02AC to Register 0x02AD). For more information, refer to the MUX3 (Data Format and Selection) section. The registers in Table 180 describe the various SPI controls for test pattern selection and test pattern insertion point selection.

JESD204B/C TRANSMITTER TEST MODES

The JESD204B/C transmitter data pattern generator has several test patterns that can be inserted before either of the JESD204B/C transmitter main functional blocks, as shown in Figure 149. The registers associated with these test modes are described in Table 180.

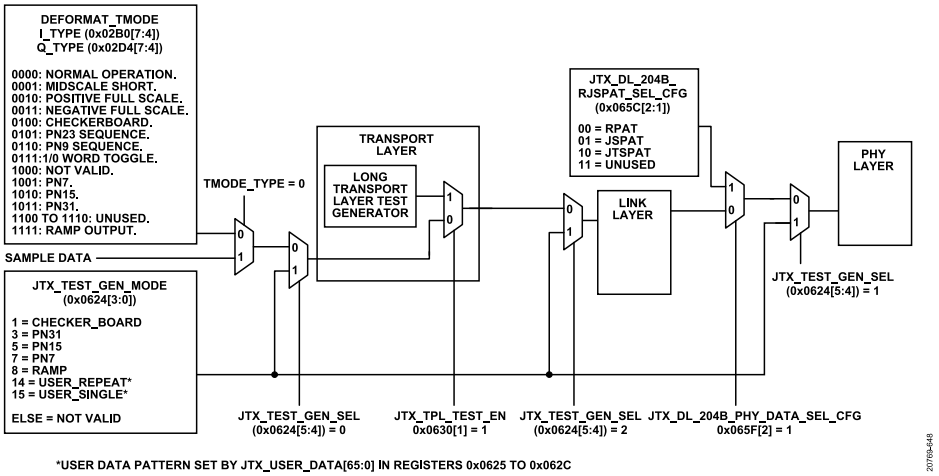

Figure 149. JESD204B/C Transmitter Test Mode Equivalent Block Diagram

JESD204B/C Transmitter PHY PRBS Test

Because the JESD204B/C transmitter pattern generator can insert a pattern at the input to the physical layer, it can be used to conduct PHY PRBS testing. This functionality enables bit error rate (BER) testing of each physical lane of the JESD204B link. The test generator sends the same pattern to each lane that is enabled. So, each lane has its own PRBSx pattern running and the FPGA PHY lanes must each be able self sync to the pattern. Even though this is a PHY test, the JESD204B/C transmitter must be configured for a valid (supported) mode even though the link does not need to be established. Therefore, it is recommended to set up the device for the mode of operation that it is intended to run when bringing up the link. These include settings for the JESD204B/C mode, decimation mode, and any crossbar mux settings. Refer to Table 43 to Table 54 for a list of valid modes. The procedure for implementing the test is as follows:

1. Make sure the clock to the FPGA is lane_rate/64 for JESD204C or lane_rate/20 for JESD204B.
2. Set appropriate clocking for the device.
3. Set link number (JTX_LINK_PAGE (Register 0x001A, Bits[1:0]), 0 is default so likely not needed).
4. Set the JESD204B/C parameters individually or using the JTX_MODEx registers as appropriate and described in Table 43 to Table 54.
5. Set the appropriate decimation registers for the mode of interest.
6. Set the crossbar (JRX_LINK_LANE_SEL) mux settings as appropriate for the hardware being tested.
7. Make sure SERDES PLL is locked by reading Register 0x0722, Bit 3)
8. Power up lanes to be tested using Register 0x0750 (bit per lane, 0 = lane enabled).
9. Set emphasis and V_{SWING} levels if needed using Register 0x0752 to Register 0x0755, Register 0x075A to Register 0x0761, and Register 0x0763 to Register 0x076A (first pass, leave at default).
10. Set test pattern (Register 0x0624, Bits[3:0]) and source (Register 0x0624, Bits[5:4] = 1).
11. Enable JRX PHY PRBS test in FPGA.
12. Wait.

DEVICE TEST MODES

13. Check PRBS error flags and counters in FPGA.

Table 180. ADC Datapath and JESD204B/C Transmitter Test Mode Registers

Address	Bits	Bit Name	Description	Reset	Access
0x02B0	[7:4]	TMODE_I_TYPE_SEL	Test Mode Generation Selection. The I-data pattern is routed to even numbered DF outputs, as DFORMAT_TMODE_SEL[15:0] enables. 0000: off, normal operation. 0001: midscale short. 0010: positive full scale. 0011: negative full scale. 0100: alternating checkerboard. 0101: PN23 sequence. 1010: PN15 sequence. 0111: 1/0 word toggle. 1000: user pattern test mode. 1001: PN7 sequence. 1011:PN31 sequence. 1100 to 1110: unused. 1111: ramp output.	0x0	R/W
0x02AD	[7:0]	DFORMAT_TMODE_SEL[7:0]	D-Formatter Test Mode Data Select (16-bits)	0x0	R/W
0x02AE	[7:0]	DFORMAT_TMODE_SEL[15:8]	Tmode Test Mode Output at Converter. Enumeration list: 16'0x00: no converters have Tmode data. 16'0x001: Tmode data at Converter 0. 16'0x002: Tmode data at Converter 1. 16'0x007: Tmode data at Converter 0, Converter 1, and Converter 2. 16'0xFFFF: Tmode data at all 16 converters.	0x0	R/W
0x02D4	[7:4]	TMODE_Q_TYPE_SEL	Test Mode Generation Selection. The Q-data pattern is routed to odd numbered DF_{OUT} outputs, as DFORMAT_TMODE_SEL, Bits[15:0] enables. 0000: off, normal operation. 0001: midscale short. 0010: positive full scale. 0011: negative full scale. 0100: alternating checkerboard. 0101: PN23 sequence. 0110: PN9 sequence. 0111: 1/0 word toggle. 1000: user pattern test mode (not currently valid). 1001: PN7. 1010:PN15. 1011:PN31. 1100 to 1110: unused. 1111: ramp output.	0x0	R/W
0x0624	[5:4]	JTX_TEST_GEN_SEL	Test Pattern Insertion Point Enable and Selection. 0: insert pattern before transport layer. 1: insert pattern before PHY layer. 2: insert pattern before link layer. 3: JESD204B/C transmitter test pattern generation is not enabled.	3	R/W
	[3:0]	JTX_TEST_GEN_MODE	Selects the data pattern to be generated. 1: CHECKER_BOARD 3:PN31.	0	R/W

DEVICE TEST MODES

Table 180. ADC Datapath and JESD204B/C Transmitter Test Mode Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
			5: PN15. 7: PN7. 8: ramp. 14: repeat the user data pattern, as programmed via the JTX_TEST_USER_DATA[65:0]. 15: transmits single occurrence of the user data pattern, as programmed via JTX_TEST_USER_DATA[65:0]. All other settings: not valid.		
0x0625	[7:0]	JTX_TEST_USER_DATA[7:0]	User programmable data pattern (up to 66 bits).	0	R/W
0x0626	[7:0]	JTX_TEST_USER_DATA[15:8]	User programmable data pattern (up to 66 bits).	0	R/W
0x0627	[7:0]	JTX_TEST_USER_DATA[23:16]	User programmable data pattern (up to 66 bits).	0	R/W
0x0628	[7:0]	JTX_TEST_USER_DATA[31:24]	User programmable data pattern (up to 66 bits).	0	R/W
0x0629	[7:0]	JTX_TEST_USER_DATA[39:32]	User programmable data pattern (up to 66 bits).	0	R/W
0x062A	[7:0]	JTX_TEST_USER_DATA[47:40]	User programmable data pattern (up to 66 bits).	0	R/W
0x062B	[7:0]	JTX_TEST_USER_DATA[55:48]	User programmable data pattern (up to 66 bits).	0	R/W
0x062C	[7:0]	JTX_TEST_USER_DATA[63:56]	User programmable data pattern (up to 66 bits).	0	R/W
0x062D	[1:0]	JTX_TEST_USER_DATA[65:64]	User programmable data pattern (up to 66 bits).	0	R/W
0x0630	1	JTX_TPL_TEST_EN	Long Transport Layer (LTPL) Data Pattern Enable. 0: LTPL disabled. 1: LTPL enabled.	0	R/W
0x0634	[7:0]	JTX_TPL_TEST_NUM_FRAMES[7:0]	Number of frames (minus 1) in the LTPL test pattern.	0	R/W
0x0635	[7:0]	JTX_TPL_TEST_NUM_FRAMES[15:8]	Number of frames (minus 1) in the LPL test pattern.	0	R/W
0x0659	[7:4]	JTX_DL_204B_ILAS_DELAY_CFG	Delays ILAS start by 0 to 15 LMFC periods. 0: transmit ILAS on the first LMFC after SYNCxINB± is deasserted. 1: transmit ILAS on the second LMFC after SYNCxINB± is deasserted. … 15: transmit ILAS on the sixteenth LMFC after SYNCxINB± is deasserted.	0x0	R/W
	3	JTX_DL_204B_BYP_ILAS_CFG	Bypass ILAS. 1 = ILAS.	0x0	R/W
	2	JTX_DL_204B_ILAS_TEST_EN_CFG	Enable ILAS Test Mode. 1 = the JESD204B/C transmitter sends a repeated ILAS pattern. If SYNCxINB± is not active (SYNCxINB± is logic 1), 16 CGS characters are sent prior to the repeated ILAS.	0x0	R/W
	1	JTX_DL_204B_BYP_8B10B_CFG	8-bit/10-bit Encoder Bypass. 1 = bypass the 8-bit/10-bit encoder for test purposes only.	0x0	R/W
	0	JTX_DL_204B_BYP_ACG_CFG	Alignment Character Generation Bypass. 1 = bypass alignment character generation (204B)	0x0	
0x065A	2	JTX_DL_204B_LSYNC_EN_CFG	Character Insertion for Lane Alignment Configuration. 0: insert K28.7 (/F/ for frame alignment) characters only. 1: insert K28.7 and K28.3 (/A/ for multiframe alignment) characters.	0x0	R/W
	1	JTX_DL_204B_DEL_SCR_CFG	Alternative Scrambler Enable (see JESD204B). 1: scrambling begins at Octet 2 of the user data 0: scrambling begins at Octet 0 of the user data This is the common usage.	0x0	R/W
	0	JTX_DL_204B_10B_MIRROR	Reverse the order of the 10-bit symbols from JESD204B link layer data.	0x0	R/W
0x065B	[7:0]	JTX_DL_204B_KF_ILAS_CFG	Number of multiframes to transmit during initialization sequence = 4 × (KF_ILAS_CFG + 1).	0x0	R/W
0x065C	7	JTX_DL_204B_CLEAR_SYNCXINB±E_COUNT	Clear SYNC~ Falling Edges Counter.	0x0	R/W
	6	JTX_DL_204B_TESTMODE_IGNORE_SYNCN_CFG	Ignore SYNCxINB± Input During D21.5 and RPAT Test Modes.	0x0	R/W
	5	JTX_DL_204B_SYNCXINB±	JESD204B/C Frame Synchronization. Active low. synchronous upon rising edge PCLK. 0: transmit code group synchronization (K characters).	0x0	R

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Table 180. ADC Datapath and JESD204B/C Transmitter Test Mode Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
			Subclass 1: internal LMFC is reset for 1 PCLK by falling edge of SYNCxINB±. Subclass 0: internal LMFC is held in reset by SYNCxINB± = 0.		
	[2:1]	JTX_DL_204B_RJSPAT_SEL_CFG	High Frequency Patterns Test Mode Configuration. 00: RPAT sequence. 01: JSPAT sequence. 10: JTSPAT sequence. 11:unused.	0x0	R/W
	0	JTX_DL_204B_RJSPAT_EN_CFG	Enable RPAT/JSPAT/JTSPAT Generator. 0: off. 1: on (must also set JTX_DL_204B_PHY_DATA_SEL_CFG, Register 0x065F, Bit 2 = 1).	0x0	R/W
0x065D	7	JTX_DL_204B_SYNCXINB±_FORCE_EN	1 = force SYNCxINB signal to the value specified in Register 0x065D, Bit 6.	0x0	R/W
	6	JTX_DL_204B_SYNCXINB±_FORCE_VAL	SYNCxINB logic if force enabled (Register 0x065D, Bit 7 = 1). 0 = force SYNCxINB to Logic 0. 1 = force SYNCxINB to Logic 1.	0x0	R/W
0x065F	2	JTX_DL_204B_PHY_DATA_SEL_CFG	JESD204C data to PHY on a lane boundary. 1 = RPAT/JSPAT/JTSPAT generator data. 0 = 8-bit/10-bit encoder output data.		

JESD204B/C RECEIVER TEST MODES

The device includes three pattern checking circuits that can be used to validate PHY performance and JESD204B/C receiver digital functionality (see Figure 150). The JESD204B/C receiver PHY pseudorandom bit sequence (PRBS) checker is located at the back end of the JESD204B/C receiver PHY and can be used to test for good signal integrity on the JESD204B/C link. A PRBS pattern checker for the datapath is located at the transport layer output. A short transport layer pattern checker is located at the transport layer output.

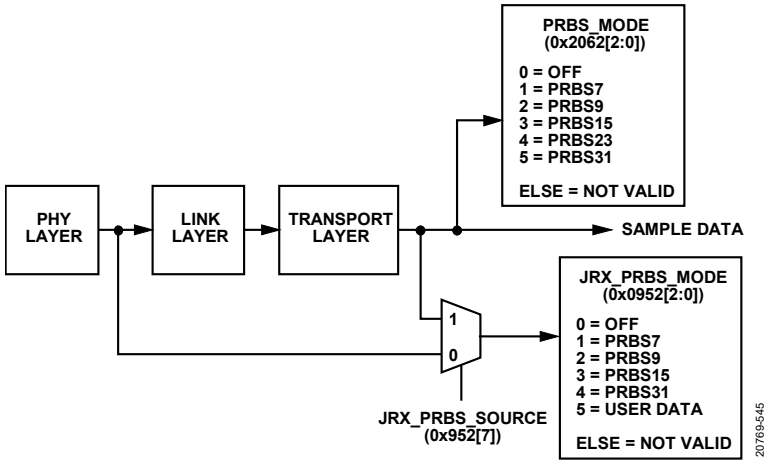

Figure 150. JESD204B/C Receiver Pattern Checking Equivalent Block Diagram

JESD204B/C Receiver PHY PRBS Testing

The JESD204B/C receiver on the device includes a PRBS pattern checker on the back end of the physical layer. This functionality enables BER testing of each physical lane of the JESD204B link.

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The PHY PRBS pattern checker does not require the JESD204B link is established, although a valid link configuration must be programmed into the part, and the link enabled. The pattern checker can synchronize with a PRBS7, PRBS9, PRBS15, or PRBS31 data pattern. PRBS pattern verification can be performed on multiple lanes at once. The error counts for failing lanes can be read back from registers.

To perform PRBS testing on the device, take the following steps:

1. Start sending a PRBS7, PRBS9, PRBS15, or PRBS31 pattern from the JESD204B transmitter. As there is no encoding on the data, set the logic device reference clock for LaneRate/64 for JESD204C or LaneRate/20 for JESD204B.
2. Write a 0 to Register 0x0952, Bit 7, to select the PHY PRBS checker.
3. Select and write the appropriate PRBS pattern to Register 0x0952, Bits[2:0], as shown in Table 181.
4. Configure the JESD204B/C receiver for a valid mode of operation from Table 92 or Table 93.
5. Set JRX_LINK_EN (0x0596. Bits 1:0). = 1.
6. If running at a lane rate >16 Gbps, execute the PHY calibration routine described in the JESD204C Receiver DFE Operation Above 16 Gbps section. Note that if the PHY calibration routine has already been executed prior to running the PHY PRBS test, bypass this step.
7. Write a 1 to Register 0x0950, Bit 0, to clear error counter.
8. Wait 500 ms.
9. Set back Register 0x0950, Bit 0, to 0.
10. Write a 1 to Register 0x0950, Bit 1, to update the error counter.
11. Wait as long as is desired.
12. Set back Register 0x0950, Bit 1, to 0.
13. Read the PRBS test results.

Each Bit 7 of Register 0x0953 to Register 0x095A corresponds to a SERDES lane (0 = pass, 1 = fail). Use this bit with Bit 6 of Register 0x0953 to Register 0x095a. If any Bit 6 from Register 0x0953 to Register 0x095a is 1, data on the corresponding lane to the PRBS receiver is always 0, which results in PRBS pass too. Only Bit 7 = 0 and Bit 6 = 0 result in PRBS pass.

The number of PRBS errors seen on each failing lane can be read from Register 0x095b to Register 0x0962, Register 0x0963 to Register 0x096a, and Register 0x096b to Register 0x0972. The first register group is the LSBs, Bits[7:0], the second is the middle 7 bits, and the third is the MSBs, Bits[7:0]. For example, Register 0x096b, Register 0x0963, and Register 0x095b correspond to the PRBS_LANE_0_ERROR_COUNT[23:16] PRBS_LANE_0_ ERROR_COUNT[15:8], and PRBS_LANE_0_ERROR_ COUNT[7:0]. If all bits are high, the maximum error count on the failing lane is exceeded.

JESD204B/C Receiver PHY PRBS API

The device API supports the PHY PRBS pattern checking in the **adi_adxxxx_jesd.c** file that is part of the device API package. The API function call is adi_adxxxx_jesd_rx_phy_PRBS_test(). For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Table 181. JESD204B/C Receiver PHY PRBS Test Registers

Address	Bits	Bit Name	Description	Reset	Access
0x0950	1	JRX_PRBS_LANE_UPDATE_ERROR_COUNT	Update Error Counters. Toggle this bit from 0 to 1 to update the error counters on all lanes.	0	
	0	JRX_PRBS_LANE_CLEAR_ERRORS	Clear Error Counters. Toggle this bit from 0 to 1 to clear the error counters on all lanes.		
0x0952	7	JRX_PRBS_SOURCE	Source for PRBS testing, 0: Lane data (independent checking per lane); 1: Sample data (M0 only, jrx_ns_cfg>0 not supported)	0	R/W
	[2:0]	JRX_PRBS_MODE	JESD204B/C Receiver PHY PRBS Test Mode.	0x0	R/W
			0 = pattern checker is off.		
			1 = PRBS7		
			2 = PRBS9		
			3 = PRBS15		
			4 = PRBS31		
			5 = user data (including short transport layer test pattern)		
			All other settings = not valid.		

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Table 181. JESD204B/C Receiver PHY PRBS Test Registers (Continued)

Address	Bits	Bit Name	Description	Reset	Access
0x0953 to 0x095A	7	JRX_PRBS_LANE_ERROR_FLAG	Error Counter Contains Nonzero Value. Clear the error counter to clear the error flag. Per lane register addressing applies (Register 0x0953 applies to Lane 0, Register 0x0954 applies to Lane 1, and so on).	0	R
	6	JRX_PRBS_LANE_INVALID_DATA_FLAG	Invalid PRBS Data.	0	R
			0 = data received by the PRBS checker is valid.		
			1 = data received by the PRBS checker is not valid (0s).		
	5	JRX_PRBS_LANE_INV	Inverted PRBS Data.	0	R
			0 = data received by PRBS checker is not inverted		
			1 = data received by PRBS checker is valid but inverted.		
0x095B to 0x0962	[7:0]	JRX_PRBS_LANE_ERROR_COUNT, Bits[7:0]	JESD204B/C Receiver PRBS Lane Error Counter. These registers contain the number of PRBS errors per lane. Per lane register addressing applies (Register 0x095B applies to Lane 0, Register 0x095C applies to Lane 1, and so on).	0	R
0x0963 to 0x096A	[7:0]	JRX_PRBS_LANE_ERROR_COUNT, Bits[15:8]		0	R
0x096B to 0x0972	[7:0]	JRX_PRBS_LANE_ERROR_COUNT,Bits [23:16]		0	R
0x0973	[7:0]	JRX_TEST_USER_DATA, Bits[7:0]	32-Bit User Data Pattern. If JRX_PRBS_MODE = 5, program the user data pattern to match the data sent by the logic device JESD204B/C transmitter.	0	R/W
0x0974	[7:0]	JRX_TEST_USER_DATA, Bits[15:8]		0	R/W
0x0975	[7:0]	JRX_TEST_USER_DATA, Bits[23:16]		0	R/W
0x0976	[7:0]	JRX_TEST_USER_DATA, Bits[31:24]		0	R/W

JESD204B/C Receiver PHY Eye Scan

The device has built in comparator circuits that enables the ability to reproduce an eye diagram estimate at the output of the CTLE circuit inside the JESD204B/C receiver core. This can be done while running the PHY PRBS test as described in the JESD204B/C Receiver PHY PRBS Testing section.

Horizontal Eye Scan

For lane data rates 8Gbps and above, the horizontal eye opening can be discerned by performing a horizontal sweep of the static phase offset (SPO) codes and checking for PRBS errors as described in the JESD204B/C Receiver PHY PRBS Testing section.

The bit fields for the SPO sweep are located in the JRX CBUS register map at address 0x000D. The SPO_LATCH bit field (bit 7) is used to latch in the new SPO value and the SPO_SETTING bit field (Bits[6:0]) controls the offset amount from phase 0 in twos complement format to support both positive and negative offsets.

When a SPO sweep is started, the SPO code must be at 0. When moving the SPO code the user must move it one code at a time. Taking large jumps in the SPO code could put the part in an unknown state. Since starting at phase 0 (middle of the eye), the sweep must be performed in both positive and negative directions. For half rate operation (lane rates between 8 Gbps and 16 Gbps), 64 SPO codes are in use. For quarter rate operation (lane rates between 16 Gbps and 24.75 Gbps), 32 SPO codes are in use. See the JESD204B/C Receiver Physical Layer API section for more details on appropriate settings for each of these modes.

To write to the CBUS, take the following steps:

- Write cbus_addr_JRX (Register 0x0406, Bits[7:0]) to the appropriate CBUS register address mentioned in Table 182.
- Write CBUS_WDATA_JRX (Register 0x0408, Bits[7:0]) to the appropriate value.
- Write CBUS_WRSTROBE_PHY (Register 0x0407, Bits[7:0]) to the appropriate value for the lane being scanned. (bit per lane, bit 0 for lane 0, and so on).

The per-lane process for determining the horizontal eye opening at the x-axis is as follows:

1. Verify that the lane under has no PRBS errors. See the JESD204B/C Receiver PHY PRBS Testing section.
2. Move SPO code one step to the left by writing to SPO_SETTING bit field. Make sure that SPO_LATCH bit is 0 when setting SPO code.
3. Set SPO_LATCH bit to 1 to latch in the new SPO code and then set it back to 0.
4. Perform a PRBS error check. See the JESD204B/C Receiver PHY PRBS Testing section.

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5. If there are no PRBS errors, keep moving SPO to the left and checking for PRBS errors by repeating Step 2 through Step 4.
6. If PRBS errors are detected, record this value. This is the number of good phases on the left side of the eye.
7. Move SPO back to the center, 0, one step at a time.
8. Move SPO code one step to the right by writing to SPO_SETTING bit field. Make sure that SPO_LATCH bit is 0 when setting SPO code.
9. Set SPO_LATCH bit to 1 to latch in the new SPO code and then set it back to 0.
10. Perform a PRBS error check. See JESD204B/C Receiver PHY PRBS Testing section.
11. If there are no PRBS errors keep moving SPO to the right and checking for PRBS errors by repeating Step 8 through Step 10.
12. If PRBS errors are detected, record this value. This is the number of good phases on the right side of the eye.
13. Move SPO back to the center, 0, one step at a time.

The horizontal eye scan is supported by the device API in the adi_ad9xxx_jesd_rx_spo_sweep() function.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

Vertical Eye Scan For 8 Gbps to 16 Gbps Lane Rates (Half Rate)

A vertical eye scan can be incorporated at each of the horizontal SPO sweep steps described above to provide the data needed to create a two-dimensional eye diagram. The procedure provide in this section applies to the half rate mode lane rates. For lane rates greater than 16 Gbps (quarter rate mode) see the 2D Eye Scan for Lane Rates > 16 Gbps (Quarter Rate) section. Because the horizontal eye scan is limited to 8Gsps and above, this means a complete 2D eye scan is limited to lane rates above 8 Gbps.

The vertical eye scan uses a 6-bit comparator available at each lane and checking PRBS errors. The bit fields used to control the comparator voltage and its sign are in the JRX CBUS register map. The comparator moves the center of the eye up and down in steps of 4mV by setting the COMP_SETTING bit field (Register 0x00CA, Bits[6:0]). The comparator voltage sign is controlled by S0_POLARITY_SWAP bit (Register 0x00D2, Bit 0). Writes to the serdes cbus register 0x00D2 should be a read, modify, write operation to maintain register setting from start-up, i.e., bits 7:4 should remain set to 4b'1111. For positive voltages use a value of 0 and for negative voltages use 1. This allows for comparator to sweep from −256 mV to +256 mV. Because the comparator voltage starts at 0 mV (middle of the eye), sweep must be performed in both negative and positive directions to get the lower and upper eye limits respectively.

To obtain a 2-dimensional eye diagram, perform a vertical eye scan at each SPO step in the horizontal eye scan. To perform this scan, insert the following steps between Step 4 and Step 5 and between Step 9 and Step 10.

1. Set S0_POLARITY_SWAP bit to 0 to sweep the comparator in the positive direction.
2. Move the comparator voltage one step by writing the voltage binary count to COMP_SETTING bit field.
3. Perform a PRBS error check. See the JESD204B/C Receiver PHY PRBS Testing section.
4. If there are no PRBS errors keep moving comparator voltage and checking for PRBS error by repeating Step 2 and Step 3.
5. If there are PRBS errors, record the current comparator voltage and the current SPO value. This is the upper limit of the eye at that specific SPO.
6. Reset the comparator voltage to the center by setting COMP_SETTING 0x00.
7. Set S0_POLARITY_SWAP bit to 1 to sweep the comparator in the negative direction.
8. Move the comparator voltage one step by writing the voltage count to COMP_SETTING bit field.
9. Perform a PRBS error check. See the JESD204B/C Receiver PHY PRBS Testing section.
10. If there are no PRBS errors keep moving comparator voltage and checking for PRBS error by repeating Step 8 and Step 9.
11. If there are PRBS errors, record the current comparator voltage and the current SPO value. This is the lower limit of the eye at that specific SPO.
12. Reset the comparator voltage to the center by setting COMP_SETTING bit field to 0x00 and S0_POLARITY_SWAP bit to 0.

The vertical eye scan is supported by the device API in the adi_ad9xxx_vertical_eye_scan() function.

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Creating the Half Rate Mode Eye Diagram

After running the horizontal and vertical eye scans, use the data recorded in Step 5 in the vertical eye scan procedure to construct the eye upper outline (see the blue curve in Figure 151) Use the data recorded in step 11 in the same procedure to construct the eye lower outline (see the orange curve in Figure 151). In half rate mode, each SPO count is 1/64 of the lane rate unit interval (UI). To convert the SPO counts, multiply the SPO counts by 1/64th of the UI. To convert the comparator counts to volts, multiply the counts by +4 mV or −4mV depending on the comparator voltage sign used.

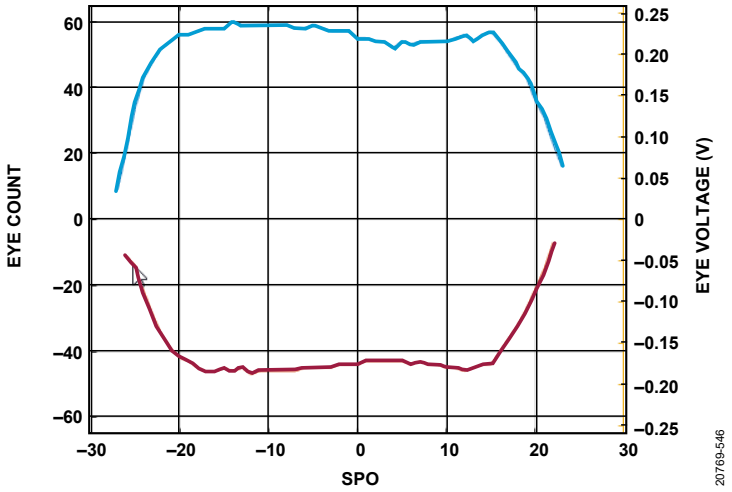

Figure 151. Example Eye Diagram Created from Half Rate Eye Scan Data

2D Eye Scan for Lane Rates > 16 Gbps (Quarter Rate)

Eye scans in quarter rate mode can only be run after performing a calibration on the PHY. Refer to the JESD204C Receiver DFE Operation Above 16 Gbps section for details on the JESD204B/C receiver PHY calibration.

In quarter rate mode, the eye scan is performed using internal firmware functions. These internal functions need to be called manually. The inputs and outputs of these functions are passed through registers. The registers needed to perform the eye scan in quarter rate mode are listed in Table 183 and Table 184. The process for implementing the 2D eye scan is shown in Figure 152. This flow is implemented in the int32_t_adi_adxxxx_jesd_rx_quarter_rate_eye_scan() and int32_t adi_adxxxx_jesd_rx_vertical_eye_scan() API functions. To execute these API functions, the JESD204B/C link should already be established and sending data. The API function is configured to store the data in a csv file with the SPO value and the four quadrants values.

Here is an example of how to call this API. 0 is the lane on which the scan occurs.

err = adi_ad9081_qr_eye_scan(&ad9081_dev, 0);

The process for the 2D eye scan is enumerated in the following steps.

1. Read the following CBUS bit field and store its value EN_FLASH_MASK_DES_RC
2. Enable flash output counting by writing 0x0A to EN_FLASH_MASK_DES_RC bit field.
3. Move SPO code one step to the left by writing to SPO_SETTING bit field. Make sure that SPO_LATCH bit is 0b'0 when setting SPO code.
4. Set SPO_LATCH bit to 0b'1 to latch in the new SPO code and then set it back to 0b'0.
5. Set the vertical sweep in the positive direction by setting RX_VERT_SCAN_DIR to 0b'1.
6. Set the lane on which the eye scan is run using RX_ARG_LANE bit field.
7. Set the state machine to the vertical eye scan state by setting RX_SET_STATE to 0x14.
8. Move the state machine to the new state by setting RX_STATE_GO to 0b'1.
9. Wait 500 µs.
10. Confirm that the scan is done, and the state machine is idle by reading RX_STATE_GO and RX_AT_IDLE. If RX_STATE_GO = 0b'0 and RX_AT_IDLE = 0b'1, proceed to next step. Otherwise wait until the condition above is met.

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11. Read the positive eye scan results by reading RX_VERT_SCAN_R0 (stepUpPosEye) and RX_VERT_SCAN_R1 (stepDownPosEye) registers.
12. Set the vertical sweep in the negative direction by setting RX_VERT_SCAN_DIR to 0b'0.
13. Repeat Step 8 through Step 11.
14. Read the negative eye scan results by reading RX_VERT_SCAN_R0 (stepUpNegEye) and RX_VERT_SCAN_R1 (stepDownNegEye) registers
15. Keep sweeping the SPO to the left by repeating Step 4 through Step 15 until a SPO value of 16 on the left side is reached.
16. Move SPO back to the center, 0, one step at a time.
17. Move SPO code one step to the right by writing to SPO_SETTING bit field. Make sure that SPO_LATCH bit is 0b'0 when setting SPO code.
18. Set SPO_LATCH bit to 0b'1 to latch in the new SPO code and then set it back to 0b'0.
19. Repeat Step 6 through Step 15.
20. Keep sweeping the SPO to the right by repeating Step 18 through Step 20 until a SPO value of 16 on the right side is reached.
21. Move SPO back to the center, 0, one step at a time.
22. Restore the value stored in step 1 to its corresponding register.

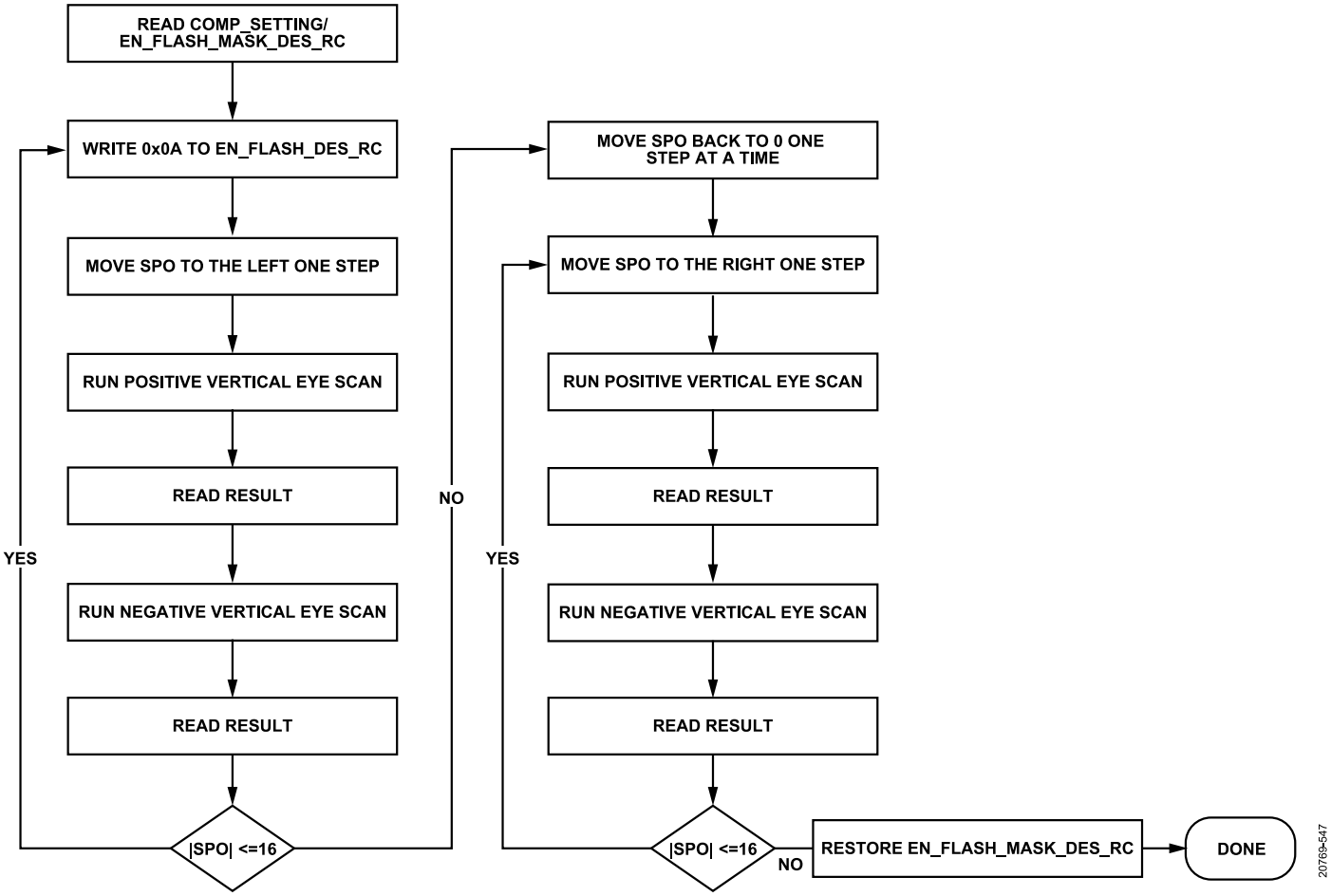

Figure 152. Quarter Rate 2D Eye Scan Flow Diagram

Creating the Quarter Rate Mode Eye Diagram

Once the eye-scan procedure outlined in Figure 152 completes, the data collected in Step 2, Step 12, and Step 15 can be used to construct the eye diagram. To construct the upper part of the eye diagram, use the following equations:

Quadrant1 = stepUpPosEye

Quadrant2 = stepUpNegEye

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Quadrant3 = stepDownNegEye

Quadrant4 = - stepDownPosEye

Plot the four quadrants of the eye calculated from the equations above against their corresponding SPO value. The formed shape enclosed between the four curves forms the eye diagram.

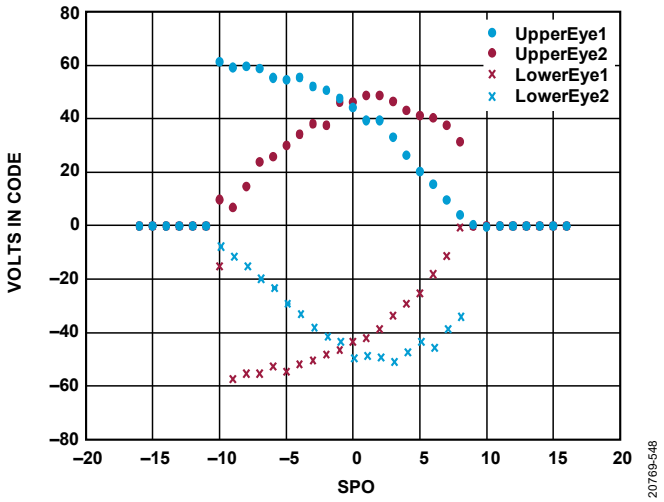

Figure 153. Example Eye Diagram Created from Quarter Rate Eye Scan Data

Table 182. JRX CBUS Registers Needed for Horizonal Eye Scan

Address	Bits	Name	Description	Reset	Access
0x000D	7	SPO_LATCH	Latches in new SPO value	0	R/W
	[6:0]	SPO_SETTING	SPO value in twos complement	0x00	R/W
0x00CA	[5:0]	COMP_SETTING	Sets comparator voltage in steps of 4 mV	0x0	R/W
0x00D2	0	COMP_POLARITY	Set the Comparator voltage sign. 0 for positive voltage and 1 for negative voltages.	0	R/W

Table 183. Registers Needed for QR Eye Diagram

Address	Bits	Bit Name	Description	Reset	Access
0x21C0	[5:0]	RX_SET_STATE	State of Calibration state machine	0x00	R/W
0x21C1	0	RX_STATE_GO	Setting this high moves cal state machine to the state set in RX_SET_STATE	0b'0	R/W
0x21D1	6	RX_VERT_SCAN_DIR	Vertical ISI argument c0not1	0b'1	R/W
	[3:0]	RX_ARG_LANE	Selects which lane internal function are run on	0x00	R/W
0x21D5	[7:0]	RX_VERT_SCAN_R0	Vertical eye scan results	0b'0	R
0x21D6	[7:0]	RX_VERT_SCAN_R1	Vertical eye scan results	0b'0	R
0x21DD	0	RX_AT_IDLE	This indicates that Rx is at idle	0b'0	R

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Table 184. CBUS Registers Needed for QR Eye Scan

Address	Bits	Bit Name	Description	Reset	Access
0x0008	[7:2]	Reserved	Reserved		
	[1:0]	SEL_LF_DLLSLEW_DES_RC	DLL Slew Rate Control	0b'10	R/W
0x00FA	[7:4]	EN_FLASH_MASK_DES_RC	In QR Mode. Flash DLL accumulator Enable	0xF	R/W
	[3:0]	EN_FLASH_SRS_DES_RC	(Not sure what this does)	0x0	R/W

JESD204B/C Receiver Datapath PRBS Testing

The device includes a PRBS pattern checker following the JESD204B/C receiver as shown in Figure 150, which can be used for PRBS checking of decoded and deframed samples. Because of this, the JESD204B/C receiver datapath PRBS checker can also be used to validate proper transport layer mapping.

The datapath PRBS pattern checker requires that the JESD204B/C link is established. The PRBS pattern checker can synchronize with a PRBS7, PRBS9, PRBS15, or PRBS31 data pattern. The error counts for failing lanes are reported through registers. Note that the datapath sample PRBS checker is valid only on modes where NP = 8, 12, and 16. NP = 24 is not currently supported.

The pattern checker checks the PRBS pattern per virtual converter, two virtual converters at a time (one channel). Therefore, the PRBS pattern at the JESD204B/C transmitter must be loaded per virtual converter. To perform datapath PRBS testing on the device, take the following steps:

1. Start sending a framed PRBS7, PRBS9, PRBS15, PRBS23, or PRBS31 pattern from the JESD204B/C transmitter with the JESD204B link set up correctly. Ensure that an appropriate 8-, 12-, or 16-bit PRBS pattern is being transmitted according the NP parameter.
   - If using the PRBS pattern checker to validate transport layer sample mapping, and the JESD204B/C receiver mode contains more than 2 virtual converters (M>2), send the pattern to M0 and M1 only, while sending 0s to the remaining virtual converters. Otherwise, send the pattern to all valid virtual converters.
2. Write to PRBS_CHNL_SEL (Register 0x2061, Bits[5:3]) to select the tested channel (set of virtual converters).
   - Note that the mapping of virtual converters to the channel is M0M1->ch0, M2M3->ch1, and so on. So, if M=2, then only Channel 0 is necessary to check.
3. Select and write the appropriate PRBS pattern to PRBS_MODE (Register 0x2062, Bits[2:0]), as shown in Table 192.
4. Write a 1 to SAMPLE_PRBS_ENABLE (Register 0x2061, Bit 6) to enable the datapath PRBS test.
5. Toggle CLR_ERRORS (Register 0x2061, Bit 2) from 0 to 1 and then back to 0 to clear the error counter and error flags.
6. Write a 1 to UPDATE_ERROR_COUNT (Register 0x2061, Bit 0) to enable the error counter update.
7. Wait 500 ms.
8. Read PRBS_ERROR_FLAG (0x2063[3:2]) and PRBS_INVALID_DATA_FLAG (0x2063[1:0]).
9. If PRBS_ERROR_FLAG indicates an error:
   - Write a 0 to UPDATE_ERROR_COUNT (Register 0x2061, Bit 0) to disable the error counter update.
   - Read the number of PRBS errors with PRBS_COUNT_I (Register 0x2064) and PRBS_COUNT_Q (Register 0x2065). The maximum error count is 255.
10. Repeat Step 2 to Step 9 for each channel needed to test every virtual converter up to M = 16.
    - If using the PRBS pattern checker to validate transport layer sample mapping, and the JESD204B/C receiver mode contains more than 2 virtual converters (M > 2), repeat Step 1 as well, sending the appropriate pattern to each set of virtual converts to match the expectation at the receiver. For example, on the second time through, send the PRBS pattern to M2/M3 and send 0s to the remaining virtual converters.
11. To stop the test, write a 0 to SAMPLE_PRBS_ENABLE (Register 0x2061, Bit 6).

Users may find it useful to invert the polarity or reverse the endianness on the PRBS pattern, depending on the logic device's implementation of the PRBS pattern generation. These pattern checking functions are controlled by the PRBS_INV_IMAG (Register 0x2062, Bit 4), PRBS_INV_REAL (Register 0x2062, Bit 3), and SWAP_ENDIANNESS (Register 0x2061, Bit 1) bit fields that are described in Table 188.

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JRx Datapath PRBS Test Examples

To illustrate how the sample PRBS checker expects to receive data from the PRBS pattern generator in the logic device, three examples are provided. The first two examples are for two different modes where NP= 16. Figure 154 shows how the first sixteen 16-bit PRBS7 samples are assigned converter sample numbers. These sample numbers and PRBS sample data is the same for each converter (M[n..0]) for a given JESD204B/C configuration.

Datapath PRBS Test Example 1

The first example is for JESD204C receiver mode 16 (L.M.F.S.NP = 8.16.4.1.16). Table 185 shows how converter samples from the 16 virtual converters are mapped into lanes and frames, starting with M0 and M1 on lane 0 all the way to M14M15 on lane 7. Because the PRBS checker expects a PRBS pattern per converter, the PRBS samples for each converter is expected to be the same. Table 185 shows how the M0 and M1 samples are the same and how they get mapped onto lane 0. The sample mapping for the rest of the lanes is the same except for M2M3, M4M5, and so on.

If using the PRBS pattern checker to validate transport layer mapping, send the PRBS pattern to one channel (set of w converters) at a time while sending 0s to the other channels. To ensure there is no intra-channel sample swapping, the PRBS can be sent to just one converter at a time while sending 0s to the other converter within the channel.

Datapath PRBS Test Example 2

The second example is for JESD204C receiver mode 6 (L.M.F.S.NP = 2.2.2.1.16). Because this mode has only two virtual converters and two lanes, the sample and lane mapping are much simpler, as shown in Table 186 and requires only one iteration through the test process described above. As with the first example and validating sample mapping, the user can send the PRBS pattern to only one of the converters while sending 0s to the other converter to ensure no sample swapping has taken place.

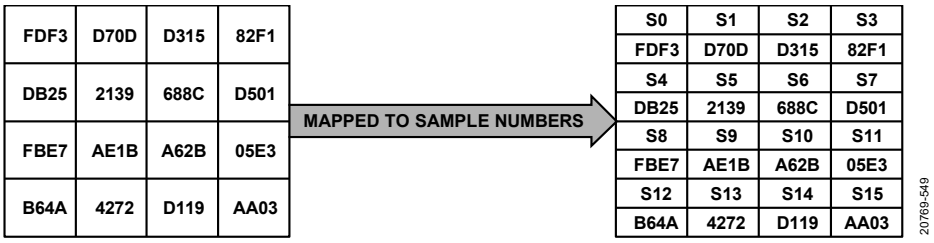

Figure 154. First 16 16-bit PRBS7 Samples Mapped to Converter Sample Number

Table 185. PRBS Sample Mapping Example 1: MxFE JRx Mode 16 (L = 8, M = 16, F = 4, S = 1, NP = 16)

			0									
		Lanes	MxSy	Sample	Value	1	2	3	4	5	6	7
Block 0	Frame 0	Octet 0	M0S0[15:8]	S0	FD	M2S0[15:8]	M4S0[15:8]	M6S0[15:8]	M8S0[15:8]	M10S0[15:8]	M12S0[15:8]	M14S0[15:8]
		Octet 1	M0S0[7:0]	S0	F3	M2S0[7:0]	M4S0[7:0]	M6S0[7:0]	M8S0[7:0]	M10S0[7:0]	M12S0[7:0]	M14S0[7:0]
		Octet 2	M1S0[15:8]	S0	FD	M3S0[15:8]	M5S0[15:8]	M7S0[15:8]	M9S0[15:8]	M11S0[15:8]	M13S0[15:8]	M15S0[15:8]
		Octet 3	M1S0[7:0]	S0	F3	M3S0[7:0]	M5S0[7:0]	M7S0[7:0]	M9S0[7:0]	M11S0[7:0]	M13S0[7:0]	M15S0[7:0]
	Frame 1	Octet 4	M0S1[15:8]	S1	D7	M2S1[15:8]	M4S1[15:8]	M6S1[15:8]	M8S1[15:8]	M10S1[15:8]	M12S1[15:8]	M14S1[15:8]
		Octet 5	M0S1[7:0]	S1	D0	M2S1[7:0]	M4S1[7:0]	M6S1[7:0]	M8S1[7:0]	M10S1[7:0]	M12S1[7:0]	M14S1[7:0]
		Octet 6	M1S1[15:8]	S1	D7	M3S1[15:8]	M5S1[15:8]	M7S1[15:8]	M9S1[15:8]	M11S1[15:8]	M13S1[15:8]	M15S1[15:8]
		Octet 7	M1S1[7:0]	S1	D0	M3S1[7:0]	M5S1[7:0]	M7S1[7:0]	M9S1[7:0]	M11S1[7:0]	M13S1[7:0]	M15S1[7:0]
Block 1	Frame 2	Octet 0	M0S2[15:8]	S2	D3	•	•	•	•	•	•	•
		Octet 1	M0S2[7:0]	S2	15	•	•	•	•	•	•	•
		Octet 2	M1S2[15:8]	S2	D3	•	•	•	•	•	•	•
		Octet 3	M1S2[7:0]	S2	15	•	•	•	•	•	•	•

DEVICE TEST MODES

Table 185. PRBS Sample Mapping Example 1: MxFE JRx Mode 16 (L = 8, M = 16, F = 4, S = 1, NP = 16) (Continued)

			0										
		Lanes	MxSy	Sample	Value	1	2	3	4	5	6	7
	Frame 3	Octet 4	M0S3[15:8]	S3	82	•	•	•	•	•	•	•
		Octet 5	M0S3[7:0]	S3	F1	•	•	•	•	•	•	•
		Octet 6	M1S3[15:8]	S3	82	•	•	•	•	•	•	•
		Octet 7	M1S3[7:0]	S3	F1	•	•	•	•	•	•	•
			At the Tx, send PRBS pattern to channel 0 (M0, M1) first time through the procedure (send 0s to the remaining channels if using this test to validate sample mapping)			Second time through the procedure send PRBS pattern to channel 1 (M2,M3) and 0s to the remaining channels (if validating sample mapping)…and so on, until all 8 channels have been tested.						

Table 186. PRBS Sample Mapping Example 2: MxFE JRx Mode 36 (L = 2, M = 2, F = 2, S = 1, NP = 16)

		Lanes	0			1		
			MxSy	Sample	Value	MxSy	Sample	Value
Block 0	Frame 0	Octet 0	M0S0[15:8]	S0	FD	M1S0[15:8]	S0	FD
		Octet 1	M0S0[7:0]		F3	M1S0[7:0]		F3
	Frame 1	Octet 0	M0S1[15:8]	S1	D7	M1S1[15:8]	S1	D7
		Octet 1	M0S1[7:0]		D0	M1S1[7:0]		D0
	Frame 2	Octet 0	M0S2[15:8]	S2	D3	M1S2[15:8]	S2	D3
		Octet 1	M0S2[7:0]		15	M1S2[7:0]		15
	Frame 3	Octet 0	M0S3[15:8]	S3	82	M1S3[15:8]	S3	82
		Octet 1	M0S3[7:0]		F1	M1S3[7:0]		F1
Block 1	Frame 4	Octet 0	M0S4[15:8]	S4	DB	M1S4[15:8]	S4	DB
		Octet 1	M0S4[7:0]		25	M1S4[7:0]		25
	Frame 5	Octet 0	M0S5[15:8]	S5	21	M1S5[15:8]	S5	21
		Octet 1	M0S5[7:0]		39	M1S5[7:0]		39
	Frame 6	Octet 0	M0S6[15:8]	S6	68	M1S6[15:8]	S6	68
		Octet 1	M0S6[7:0]		8C	M1S6[7:0]		8C
	Frame 7	Octet 0	M0S7[15:8]	S7	D5	M1S7[15:8]	S7	D5
		Octet 1	M0S7[7:0]		01	M1S7[7:0]		01
			For this mode, there is only one channel (M0, M1). So, at the Tx, just send the pattern once to channel 0. This covers all the samples across all virtual converters.					

Datapath PRBS Test Example 3

The third example is for a mode where NP= 12. Figure 155 shows how the first 16 12-bit PRBS7 samples are assigned converter sample numbers. As with the 16-bit samples, these sample numbers and PRBS sample data is the same for each converter (M[n..0]) for a given JESD204B/C configuration.

This example is for JESD204C receiver mode 16 (L.M.F.S.NP = 8.2.3.8.12). Table 187 shows how converter samples from the two virtual converters are mapped into lanes and frames, starting with M0 samples mapped to lanes 0-3 and M1 samples being mapped to lanes 4-7. Because the PRBS checker expects a PRBS pattern per converter, the PRBS samples for each converter is expected to be the same. Table 187 shows how the M0 and M1 samples are the same and how they get mapped across the appropriate lanes.

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Figure 155. First 16 12-Bit PRBS7 Samples Mapped to Converter Sample Number

Table 187. PRBS Sample Mapping Example 3: MxFE JRx Mode 6 (L = 8, M = 2, F = 3, S = 8, NP = 12)

		Lanes	0	1	2	3	4	5	6	7
Block 0	Frame 0	Octet 0	M0S0[11:4]	M0S2[11:4]	M0S4[11:4	M0S6[11:4]	M1S0[11:4]	M1S2[11:4]	M1S4[11:4	M1S6[11:4]
		PRBS Data	fd	D3	DB	68	fd	D3	DB	68
		Octet 1(M)	M0S0[3:0]	M0S2[3:0]	M0S4[3:0]	M0S6[3:0]	M1S0[3:0]	M1S2[3:0]	M1S4[3:0]	M1S6[3:0]
		PRBS Data	F	1	2	8	F	1	2	8
		Octet 1(L)	M0S1[11:8]	M0S3[11:8]	M0S5[11:8]	M0S7[11:8]	M1S1[11:8]	M1S3[11:8]	M1S5[11:8]	M1S7[11:8]
		PRBS Data	D	8	2	D	D	8	2	D
		Octet 2	M0S1[7:0]	M0S3[7:0]	M0S5[7:0]	M0S7[7:0]	M1S1[7:0]	M1S3[7:0]	M1S5[7:0]	M1S7[7:0]
		PRBS Data	70	2F	13	50	70	2F	13	50
	Frame 1	Octet 0	M0S8[11:4]	M0S10[11:4]	M0S12[11:4]	M0S14[11:4]	M1S8[11:4]	M1S10[11:4]	M1S12[11:4	M1S14[11:4]
		PRBS Data	FB	A6	B6	D1	FB	A6	B6	D1
		Octet 1(M)	M0S8[3:0]	M0S10[3:0]	M0S12[3:0]	M0S14[3:0]	M1S8[3:0]	M1S10[3:0]	M1S12[3:0]	M1S14[3:0]
		PRBS Data	E	2	4	1	E	2	4	1
		Octet 1(L)	M0S9[11:8]	M0S11[11:8]	M0S13[11:8]	M0S15[11:8]	M1S9[11:8]	M1S11[11:8]	M1S13[11:8]	M1S15[11:8]
		PRBS Data	A	0	4	A	A	0	4	A
		Octet 2	M0S9[7:0]	M0S11[7:0]	M0S13[7:0]	M0S15[7:0]	M1S9[7:0]	M1S11[7:0]	M1S13[7:0]	M1S15[7:0]
		PRBS Data	E1	5E	27	A0	E1	5E	27	A0
	Frame 2	Octet 0	M0S16[11:4]	M0S18[11:4]	M0S20[11:4]	M0S22[11:4]	M1S16[11:4]	M1S18[11:4]	M1S20[11:4]	M1S22[11:4]
		Octet 1	M0S16[3:0]	M0S18[3:0]	M0S20[3:0]	M0S22[3:0]	M1S16[3:0]	M1S18[3:0]	M1S20[3:0]	M1S22[3:0]
			M0S17[11:8]	M0S19[11:8]	M0S21[11:8]	M0S23[11:8]	M1S17[11:8]	M1S19[11:8]	M1S21[11:8]	M1S23[11:8]
		Octet 2	M0S17[7:0]	M0S19[7:0]	M0S21[7:0]	M0S23[7:0]	M1S17[7:0]	M1S19[7:0]	M1S21[7:0]	M1S23[7:0]
Block 1 (1st 7 Octets)	Frame 3	Octet 0	M0S24[11:4]	M0S26[11:4]	M0S28[11:4]	M0S30[11:4]	M1S24[11:4]	M1S26[11:4]	M1S28[11:4]	M1S30[11:4]
		Octet 1	M0S24[3:0]	M0S26[3:0]	M0S28[3:0]	M0S30[3:0]	M1S24[3:0]	M1S26[3:0]	M1S28[3:0]	M1S30[3:0]
			M0S25[11:8]	M0S27[11:8]	M0S29[11:8]	M0S31[11:8]	M1S25[11:8]	M1S27[11:8]	M1S29[11:8]	M1S31[11:8]
		Octet 2	M0S25[7:0]	M0S27[7:0]	M0S29[7:0]	M0S31[7:0]	M1S25[7:0]	M1S27[7:0]	M1S29[7:0]	M1S31[7:0]
	Frame 4	Octet 0	M0S32[11:4]	M0S34[11:4]	M0S36[11:4]	M0S38[11:4]	M1S32[11:4]	M1S34[11:4]	M1S36[11:4]	M1S38[11:4]
		Octet 1	M0S32[3:0]	M0S34[3:0]	M0S36[3:0]	M0S38[3:0]	M1S32[3:0]	M1S34[3:0]	M1S36[3:0]	M1S38[3:0]
			M0S33[11:8]	M0S35[11:8]	M0S37[11:8]	M0S39[11:8]	M1S33[11:8]	M1S35[11:8]	M1S37[11:8]	M1S39[11:8]
		Octet 2	M0S33[7:0]	M0S35[7:0]	M0S37[7:0]	M0S39[7:0]	M1S33[7:0]	M1S35[7:0]	M1S37[7:0]	M1S39[7:0]

JESD204B/C Receiver Datapath PRBS API

The device API supports the Datapath PRBS pattern checking in the adi_adxxxx_jesd.c that comes as part of the device API package. The API function call is adi_adxxxx_jesd_rx_ sample_PRBS_test().

For more information, refer to the AD9081/AD9082/AD9986/AD9988 API specification, integration, and porting guide, Revision 1.1.0 or later. This document is part of the API release package.

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Table 188. Datapath PRBS Test Registers

Address	Bits	Bit Name	Description	Reset	Access
0x2061	6	SAMPLE_PRBS_ENABLE	Sample PRBS Test Enable. 0 = sample PRBS test is inactive. 1 = start sample PRBS test.		R/W
	[5:3]	PRBS_CHNL_SEL	Channelizer Channel Select for Sample PRBS Test. 0 = select Channelizer 0 for testing. 1 = select Channelizer 1 for testing. 2 = select Channelizer 2 for testing. 3 = select Channelizer 3 for testing. 4 = select Channelizer 4 for testing. 5 = select Channelizer 5 for testing. 6 = select Channelizer 6 for testing. 7 = select Channelizer 7 for testing.		R/W
	2	CLR_ERRORS	Clear PRBS Errors. Toggle this bit from 0 to 1 and then back to 0 to clear the PRBS error flags in Register 0x2063.		R/W
	1	SWAP_ENDIANNESS	Swap Endianness (Bit Reversal). 0 = do not swap endianness. 1 = reverse the bit order of the PRBS sample checker.		R/W
	0	UPDATE_ERROR_COUNT	Update Error Counter. Toggle this bit from 0 to 1 and the back to 0 to update the PRBS error counter in Register 0x2064 to Register 0x2069.		R/W
0x2062	4	PRBS_INV_IMAG	1= invert the data of the imaginary path to the sample PRBS checker	0x0	R/W
	3	PRBS_INV_REAL	1= invert the data of the real path to the sample PRBS checker	0x0	R/W
	[2:0]	PRBS_MODE	Sample PRBS Test Mode. 0 = pattern checker is off. 1 = PRBS7. 2 = PRBS9. 3 = PRBS15. 4 = PRBS23. 5 = PRBS31. All other settings = not valid.		R/W
0x2063	3	PRBS_ERROR_FLAG_Q	Q-Data Sample PRBS Error Flag. 0 = no errors detected in the Q- datapath of the selected channel. 1 = error(s) detected in the Q- datapath of the selected channel.		R
	2	PRBS_ERROR_FLAG_I	I-Data Sample PRBS Error Flag. 0 = no invalid data detected in the I- datapath of the selected channel. 1 = invalid data detected in the I- datapath of the selected channel.		R
	1	PRBS_INVALID_DATA_FLAG_Q	Q-Data Sample PRBS Invalid Data Flag. 0 = no invalid data detected in the Q-datapath of the selected channel. 1 = error(s), invalid data detected in the Q-datapath of the selected channel.		R
	0	PRBS_INVALID_DATA_FLAG_I	I-Data Sample PRBS Invalid Data Flag. 0 = no errors detected in the I-datapath of the selected channel. 1 = invalid data detected in the I-datapath of the selected channel.		R
0x2064	[7:0]	ERROR_COUNT_I[7:0]	I-Data Sample PRBS Error Counter Readback. These registers display the number of PRBS errors detected on the selected channel (PRBS_CHNL_SEL) when updated using UPDATE_ERROR_COUNT (Register 0x2061, Bit 0).		R
0x2065	[7:0]	ERROR_COUNT_I[15:8]			R
0x2066	[7:0]	ERROR_COUNT_I[23:16]			R
0x2067	[7:0]	ERROR_COUNT_Q[7:0]	Q-data Sample PRBS Error Counter Readback. These registers display the number of PRBS errors detected on the selected channel (PRBS_CHNL_SEL) when updated using UPDATE_ERROR_COUNT (Register 0x2061, Bit 0).		R
0x2068	[7:0]	ERROR_COUNT_Q[15:8]			R
0x2069	[7:0]	ERROR_COUNT_Q[23:16]			R

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Short Transport Layer (STPL) Test

To test the frame mapping of the JESD204B/C Transmitter, it is recommended to use the sample pattern checker described in the JESD204B/C Receiver Datapath PRBS Testing section. The method for performing this test will be included in a subsequent revision of this document. It is currently recommended to use the JESD204B/C Receiver Datapath PRBS Testing method for validating transport layer mapping.

JESD204B DEBUG GUIDE

The following debugging guide addresses common issues that can be encountered during device operation, including possible causes and basic troubleshooting techniques as a checklist to perform on the system. The majority of device issues can be resolved by following this guide. This guide also lists the actions to take and register values to record as well as the issue descriptions when reporting them to Analog Devices. Including the required information at the time of request helps speed up problem resolution and enables the Analog Devices support team to provide a fast turnaround.

Table 189. JESD204B Symptom Checklist

Cause	Action
PHY PRBS Failure	Wrong PRBS test setting. PLL not locked. Lane FIFO full or empty. Any bit of LANE_FIFO_FULLANDLANE_FIFO_EMPTY is 1. Lane P/N is inverted. Power supply is out of range. Input signal to part is deteriorated on the signal path. Signal output from transmit is incorrect.
Lane Crossbar Mapping	Lane crossbar mapping is incorrect.
Reg0x04ee~0x4f5 Bits[1:3] and Bit 5, Not for Corresponding Enabled Lane	General debug method. JESD mode is not correct. SyncB never goes low. ILAS sequence is not compliant to JESD specification. Register 0x04ee, Bit 2 to Register 0x04f5, Bit 2 is not 1 for enabled lanes. Invalid setup and hold time of periodic or gapped periodic SYSREF.
Invalid Mode Bit Read Back 1	Invalid JESD mode or interpolation mode. JESD/interpolation mode mismatch.
Need Assistance from Analog Devices	Issue description. Read back registers.

PHY PRBS FAILURE

Table 190 lists the possible causes and actions to take if a PHY PRBS test fails. SPI registers related to debugging this failure include the following:

- Register 0x0722, Bit 3: PLL is locked when this bit is high.
- Register 0x05AD: lane FIFO full flag.
- Register 0x05AE: lane FIFO empty flag.
- Register 0x058D, Bit 6 to Register 0x0594, Bit 6: inverse the JESD deserialized data.

Table 190. Possible PHY PRBS Failure Causes and Actions

Cause	Action
Wrong PRBS Test Setting	Use correct setting. Refer JESD204B/C receiver PHY PRBS testing.
PLL Not Locked (Register 0x0722, Bit 3 = 0)	Check the chip initialization sequence. Check the chip clock inputs
Lane FIFO Full or Empty. (Any LANE_FIFO_FULL and LANE_FIFO_EMPTY Bit = 1)	The clock between JESD204B transmit and receive is not synchronized well. The lane rate is not set correctly. Refer datasheet to set the correct lane rate.
Lane P/N Inverted	Set 0x058d~0x0594 corresponding bit to 1 to invert P/N.
Power Supply Out of Range	Check each power supply to make sure each one is in the specified range in the datasheet.
Input Signal to Device is Deteriorated on the Signal Path	Refer datasheet -> spo sweep to check the signal integrity. Use scope to check the signal just before the part if the signal eye diagram looks odd.
Signal Output from Transmit is Incorrect	Check the transmit PRBS generator design. If possible, do PRBS loopback test on transmit itself.

LANE CROSSBAR MAPPING

The SPI registers related to debugging this failure include the following:

- Register 0x061b, Bits[4:0] to Register 0x0622, Bits[4:0]: JESD204B transmitter lane crossbar. Set these bits to select which logical lane feeds the physical lane.
- Register 0x058d, Bits[4:0] to Register 0x0594, Bits[4:0]: JESD204B/C receiver lane crossbar. Use these bits to select the physical lane to use for a particular logical lane.

JESD204B DEBUG GUIDE

If the lane crossbar mapping is incorrect, record the one shot value from the related registers and ensure that the connection between generator logic lane to the generator PHY lane to the receiver PHY lane to the receiver logic lane is correct.

8-BIT/10-BIT DATA LINK ERRORS

Table 191 lists the causes and actions required in debugging errors that result from Bit 5 and Bits[3:1] in Register 0X04EE to Register 0X04F5 not being equal to 1 for the corresponding enabled lane. SPI registers related to debugging this failure include the following:

- Register 0x058d, Bits[4:0] to Register 0x0594, Bits[4:0]: lane assignment
- Register 0x04ee, Bit 1 to Register 0x04f5, Bit 1: whether the correct CGS is received
- Register 0x04eeBit 2 to Register 0x04f5, Bit2: whether the computed CKS matches received from the ILAS. These registers do not affect the link setup.
- Register 0x04ee, Bit 3 to Register 0x04f5, Bit 3: whether there is a transition from CGS to ILAS.
- Register 0x04ee, Bit 5 to Register 0x04f5, Bit 5: whether the ILAS sequence is correct.
- Register 0x04fe to Register 0x0505, Register 0x050e to Register 0x0515, and Register 0x051e to Register 0x0525: error count.

Table 191. Possible Causes and Actions

Cause	Action
General Debug Method	Check PRBS on each lane first. If PRBS fails, refer PHY PRBS failure. Check 058d[4:0]~0x0594[4:0] if there is lane assignment mismatch.
JESD Mode is not Correct	Check Register 0x04a0, Bit 0, and Register 0x0636[, Bit 0, if JESD mode is valid at the receive and transmit side respectively.
SyncB Never Goes Low	Follow Analog Devices recommended initialization procedure. Check that SYNC~ source and board circuitry (both SYNC+ and SYNC−, if differential) are properly configured to produce logic levels compliant for the SYNC~ receive device. If logic level is not compliant, then review circuitry for source and receiver configurations to find the problem. Otherwise, consult device manufacturer.
ILAS Sequence is not Compliant to JESD Specification	Check if the ILAS sequence is a kind of ramp pattern. This check function can be disabled by setting Register 0x04be, Bit 3 = 0. Check if receive K setting matches to transmit. Check if the setting of Register 0x0558 matches to transmit. Check if there are required /R/, /Q/, and /A/ key words in the ILAS stream and if they are in the correct position.
Register 0x04ee, Bit 3, to Register 0x04f5, Bit 2, is not 1 for enabled lanes.	Toggle Register 0x04be, Bit 4, to try different CKS calculation mode.
Invalid setup and hold time of periodic or gapped periodic SYSREF.	Check if the period of SYSREF is N times of LMFC period. Use Subclass 0 for troubleshooting.

INVALID MODE BIT READBACK

Table 193 lists the cause and action required in debugging errors associated with an improper configuration setting for either the JESD204B/C transmitter or JESD204B/C receiver link. The SPI registers related to debugging this failure are described in Table 192.

Table 192. Datapath PRBS Test Registers

Address	Bits	Name	Description
0x04A0	0	JRX_TPL_CFG_INVALID[1]	1 = Input config not supported according to VALID_x in F_NP_L and S_NS_F parameters
0x0636	0	JTX_TPL_INVALID_CFG	1 = Input cfg not supported. Input cfg not supported according to JTX_VALID_S_NS_F_NP

[1] JTX_TPL_INVALID_ CFG not valid for AD9081 and AD9082.

Table 193. Possible Causes and Actions

Cause	Action
Invalid JESD mode or interpolation mode	For the transmitter, check Register 0x01FE, Bits[5:0] (JESD_Mode), Register 0x01FF, Bits[7:4] (COARSE_INTERP_SEL), Register 0x01FF, Bits[3:0] (FINE_INTERP_SEL), Register 0x04c0, Bit 5 (JRX_dl_204b_enable) and Register 0x055e, Bit 7 (JRX_dl_204c_enable). For the receiver, check JESD transmitter configuration parameter registers (Register 0x063D to Register 0x0644)], Register 0x0282[3:0] (COARSE_DEC_SEL), Register 0x0283, Bits[2:0] (FINE_DEC_SEL), Register 0x0284,

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Table 193. Possible Causes and Actions (Continued)

Cause	Action
	Bits[7:0] (DDC_OVERALL_DECIM), Register 0x0289, Bits[7:0] (CHIP_DECIMATION_RATIO) and Register 0x0611 (JTX_link_204c_sel: 00 – JESD204B; 01 – JESD204C).
JESD204 or interpolation mode mismatch	Check if the combination of JESD mode and interpolation mode is in the supported table.

JESD204C DEBUG GUIDE

The debugging guide lists some common issues that can be encountered with device JESD204C operation. It includes possible causes and basic troubleshooting techniques as a quick check list to perform on your system. The majority of device problems can be resolved by following this guide. This guide also lists the actions to follow and register values to record along with the issue descriptions when reporting them to Analog Devices. Including the required information at the time of request helps speed up problem resolution and enables the Analog Devices support team to provide a fast turn-around.

For the transmit path, there are a number of status bits to evaluate the health of the JESD204C link. These are accessible through the app_show_link_status() API function. These bits and the API function are described in the 64-Bit/66-Bit Error Monitoring and Resynchronization section.

For the receive path, there are a couple of status bits on the JESD204B/C transmitter side that are helpful when debugging link errors. These are the JTX_PLL_LOCKED (0x0701[7]) and JTX_PHASE_ESTABLISHED (0x0713[0]) bits, as described in Table 53. Both these bits can be accessed using the adi_ad9081_jesd_tx_link_status_get() function of the API.

Table 194. JESD204C Symptom Quick Checklist

Cause	Action
PHY PRBS Failure	Wrong PRBS test setting
	PLL not locked
	Lane FIFO full or empty. Any bit of LANE_FIFO_FULLANDLANE_FIFO_EMPTY is 1
	Lane P/N is inverted
	Power supply is out of range
	Input signal to part is deteriorated on the signal path
	Signal output from transmit is wrong
Lane Crossbar Mapping	Lane crossbar mapping is incorrect
Register 0x055e, Bits[6:4] is not 6	Cannot find consistent correct synchronization header
	Cannot find 00001 pattern at the correct position header stream or cannot find it at all
Invalid mode bit read back 1	Invalid JESD mode or interpolation mode
	JESD/interpolation mode mismatch
Need assistance from Analog Devices	Issue description
	Read back registers

PHY PRBS FAILURE

Table 195 lists the possible causes and actions to take if a PHY PRBS test fails. SPI registers related to debugging this failure include the following:

- Register 0x0722, Bit 3: PLL is locked when this bit is high.
- Register 0x05AD: lane FIFO full flag.
- Register 0x05AE: lane FIFO empty flag.
- Register 0x058D, Bit 6 to Register 0x0594, Bit 6: inverse the JESD deserialized data.

Table 195. Possible PHY PRBS Failure Causes and Actions

Cause	Action
Wrong PRBS Test Setting	Use correct setting. Refer JESD204B/C receiver PHY PRBS testing.
PLL Not Locked (Register 0x0722, Bit 3 = 0)	Check the chip initialization sequence. Check the chip clock inputs
Lane FIFO Full or Empty. (Any LANE_FIFO_FULL and LANE_FIFO_EMPTY Bit = 1)	The clock between JESD204B transmit and receive is not synchronized well. The lane rate is not set correctly. Refer datasheet to set the correct lane rate.
Lane P/N Inverted	Set 0x058d~0x0594 corresponding bit to 1 to invert P/N.
Power Supply Out of Range	Check each power supply to make sure each one is in the specified range in the datasheet.
Input Signal to Device is Deteriorated on the Signal Path	Refer datasheet -> spo sweep to check the signal integrity. Use scope to check the signal just before the part if the signal eye diagram looks odd.
Signal Output from Transmit is Incorrect	Check the transmit PRBS generator design. If possible, do PRBS loopback test on transmit itself.

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LANE CROSSBAR MAPPING

Table 196 lists the cause and action required in debugging errors resulting from improper mapping of physical and logical lanes on the JESD204B/C transmitter or JESD204B/C receiver link. The SPI registers related to debugging this failure are as follows:

- Register 0x061b, Bits[4:0] to Register 0x0622, Bits[4:0]: JESD204B/C transmitter lane crossbar, setting here selects which logical lane must feed the physical lane.
- Register 0x058d, Bits[4:0] to Register 0x0594, Bits[4:0]: JESD204B/C receiver lane crossbar, physical lane selection to use for particular logical lane.

Table 196. Possible Causes and Actions

Cause	Action
Lane crossbar mapping is incorrect	Record the lane mapping value from related registers. Make sure the connection between generator's logic lane -> generator's PHY lane -> receiver's PHY lane -> receiver's logic lane is correct.

REGISTER 0X055E, BITS[6:4], IS NOT 6

Table 197 lists the cause and action required in debugging errors resulting when the JESD204B/C link is not locked as indicated when 0x06 is readback from Bits[6:4] in Register 0x055E. Figure 156 shows flow chart of read back bit values for this register during the locking process. The SPI registers related to debugging this failure are as follows:

The related registers include the following:

- Register 0x056b, Bits[3:0]to Register 0x0572, Bits[3:0]: Count of multiblock alignment errors.
- Register 0x0574, Bits[5:0] to Register 0x057b, Bits[5:0]: Count of block alignment errors.

Table 197. Possible Causes and Actions

Cause	Action
Cannot find consistently correct synchronization header.	Check Register 0x0574, Bits[5:0] to Register 0x057b, Bits[5:0] if there are block alignment errors.
Cannot find 00001 pattern at the correct position of synchronization header stream or cannot find at all.	Check Register 0x056b, Bits[3:0] to Register 0x0572, Bits[3:0] if there are multiblock alignment errors.

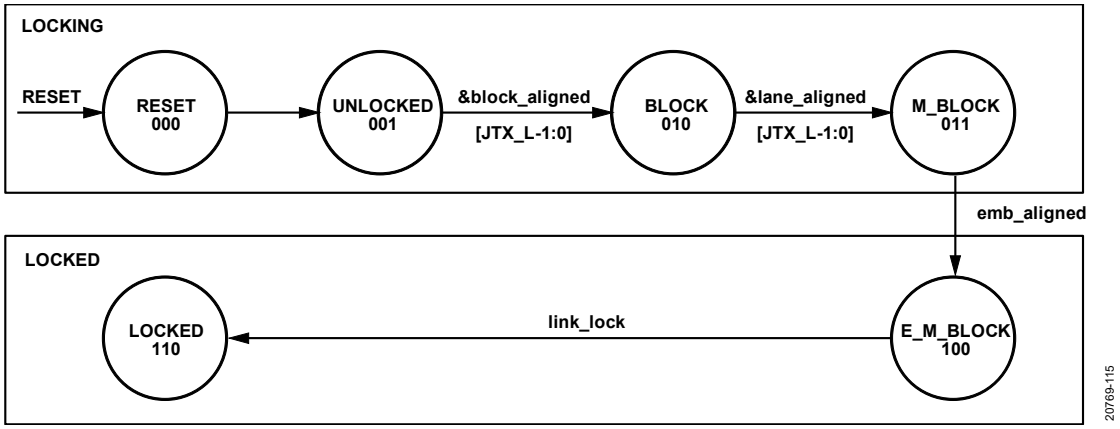

Figure 156. Flow Chart Showing Readback Values of Bits[6:4] of Register 0x55E

INVALID MODE BIT READBACK IS 1

Table 199 lists the possible causes and action required in debugging errors associated with an improper configuration setting for either the JESD204C transmitter or JESD204C receiver link. The SPI registers related to debugging this failure are described in Table 198.

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Table 198. Invalid Mode Test Registers

Address	Bits	Bit Name	Description
0x04A0	0	JRX_TPL_CFG_INVALID	1 = Input config not supported according to VALID_* in F_NP_L and S_NS_F parameters
0x0636	0	JTX_TPL_INVALID_CFG[1]	1 = Input cfg not supported. Input cfg not supported according to JTX_VALID_S_NS_F_NP

[1] JTX_TPL_INVALID_ CFG not valid for AD9081 and AD9082.

Table 199. Possible Causes and Actions

Cause	Action
Invalid JESD mode or interpolation mode	For transmit, check Register 0x01FE, Bits[5:0] (JESD_Mode), Register 0x01FF, Bits[7:4] (COARSE_INTERP_SEL), Register 0x01FF, Bits[3:0] (FINE_INTERP_SEL), Register 0x04c0, Bit 5 (JRX_dl_204b_enable) and Register 0x055e, Bit 7 (JRX_dl_204c_enable). For the receiver, check the JESD transmitter configuration parameter registers (Register 0x063D to Register 0x0644)],, Register 0x0282, Bits[3:0] (COARSE_DEC_SEL), Register 0x0283, Bits[2:0] (FINE_DEC_SEL), Register 0x0284, Bits[7:0] (DDC_OVERALL_DECIM), Register 0x0289, Bits[7:0] (CHIP_DECIMATION_RATIO) and Register 0x0611 (JTX_link_204c_sel: 00 = JESD204B; 01 = JESD204C).
JESD/interpolation mode mismatch	Check if the combination of JESD mode and interpolation mode is in the supported table.

NEED ANALOG DEVICES DEBUG ASSISTANCE

If the user requires additional assistance to debug a JESD204B/C link issue, please answer the following questions to assist in the debug effort.

- Does PRBS pass on required lanes?
- Does Register 0x55E, Bits[6:4] readback a 0x6?
- What is the receive/transmit JESD configuration parameter?
- Dual or single link operation?
- Read back the following registers:
  - Register 0x0722, Register 0x05AD, Register 0x05AE , Register 0x058d, Bit 6 to Register 0x0594, Bit 6, Register 0x058d, Bits[4:0] to Register 0x0594, Bits[4:0], Register 0x04a0, Bit 0, Register 0x0636, Bit 0, Register 0x01fa, Bits[5:0], Register 0x01fb, Bits[7:4], Register 0x01fb, Bits[3:0], Register 0x04c0, Bit 5, Register 0x055e, Bit 7, Register 0x0702, Bits[4:0], Register 0x0702, Bit 5, Register 0x0702, Bit 6, Register 0x0282, Bits[3:0], Register 0x0283, Bits[2:0], Register 0x0284, Bits[7:0], Register 0x0289, Bits[7:0], Register 0x0611, Register 0x055e, Bits[6:4], Register 0x056b, Bits[3:0] to Register 0x0572, Bits[3:0], Reg 0x0574, Bits[5:0] to Register 0x057b, Bits[5:0], Register 0x727, Register 0x729, Register 0x72a, Register 0x72d.
- Follow this procedure to read back Register 0x742:
  - Write: Register 0x740, value: 0xbc
  - Write: Register 0x72f, Bit 0, value: 0
  - Write: Register 0x72f, Bit 0, value: 1
  - Write: Register 0x72e, Bit 0, value: 1
  - Read: Register 0x742
  - Write: Register 0x72f, Bit 0, value: 0

REGISTER DETAILS

AD9081, AD9082, AD9986, and AD9988 Device Register Map

Table 200.

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0000	SPI_INTFCONFA	7	SOFTRESET_M		Soft Reset (Mirror).	0x0	R
		6	LSBFIRST_M		LSB First (Mirror).	0x0	R
		5	ADDRINC_M		Addr Inc (Mirror).	0x0	R
		4	SDOACTIVE_M		SDO Active (Mirror).	0x0	R
		3	SDOACTIVE		SDO Active.	0x0	R/W
		2	ADDRINC		Addr Inc.	0x0	R/W
				1	Streaming Addresses are Incremented.		
				0	Streaming Addresses are Decremented.		
		1	LSBFIRST		LSB First.	0x0	R/W
				1	Shift LSB in first.		
				0	Shift MSB in First.		
		0	SOFTRESET		Soft Reset. This bit automatically clears to 0 after performing a reset operation.	0x0	R/W
				1	Pulse the SoftReset line.		
				0	Reset the SoftReset line.		
0x0001	SPI_INTFCONFB	7	SINGLEINS		Single Instruction.	0x0	R/W
				1	1: Perform Single Transfers.		
				0	0: Perform Multi-Transfers.		
		[6:0]	RESERVED		Reserved.	0x0	R/W
0x0003	CHIP_TYPE	[7:0]	CHIP_TYPE		Chip Type:.	0x0	R
				0x0F	0x0F: MxFE.		
				0x03	0x03: High Speed ADC.		
				0x04	0x04: High Speed DAC.		
0x0004	PROD_ID_LSB	[7:0]	PROD_ID_LSB		Product ID LSB.	0xXX	R
				0x82	AD9082.		
				0x86	AD9986.		
				0x81	AD9081.		
				0x88	AD9988.		
				0x07	AD9207.		
				0x09	AD9209.		
				0x77	AD9177.		
0x0005	PROD_ID_MSB	[7:0]	PROD_ID_MSB		Product ID MSB.	0xXX	R
				0x90	AD9081 / AD9082.		
				0x99	AD9988 / AD9986.		
				0x92	AD9207 / AD9209.		
				0x91	AD9177.		
0x0006	CHIP_GRADE	[7:4]	PROD_GRADE		Product grade information.	0xX	R
				0x23	AD9082 / AD9986 / AD9207.		
				0x13	AD9082.		
				0xA3	AD9081 / AD9988 / AD9209 / AD9177.		
				0xB3	AD9081.		
		[3:0]	DEV_REVISION		Device revision information.	0x3	R
0x000B	SPI_REVISION	[7:0]	SPI_REVISION		SPI Revision Register (undocumented to customer).	0x1	R
				0	0x00: Draft 0.9e or earlier.		
				1	0x01: Revision 1.0.		
				Else	0x02-0xFF: Undefined.		
0x000C	VENDOR_ID_LSB	[7:0]	CHIP_VENDOR_ID[7:0]		Vendor ID.	0x56	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x000D	VENDOR_ID_MSB	[7:0]	CHIP_VENDOR_ID[15:8]		Vendor ID.	0x4	R
0x0010	CHIP_ID_L	[7:0]	CHIP_ID_L		Chip ID L.	0x0	R
0x0011	CHIP_ID_M1	[7:0]	CHIP_ID_M1		Chip ID M1.	0x0	R
0x0012	CHIP_ID_M2	[7:0]	CHIP_ID_M2		Chip ID M2.	0x0	R
0x0013	CHIP_ID_H	[7:0]	CHIP_ID_H		Chip ID H.	0x0	R
0x0018	ADC_COARSE_PAGE	7	COARSE_DDC3_PAGE		Paging bit for Coarse DDC3.	0x1	R/W
		6	COARSE_DDC2_PAGE		Paging bit for Coarse DDC2.	0x1	R/W
		5	COARSE_DDC1_PAGE		Paging bit for Coarse DDC1.	0x1	R/W
		4	COARSE_DDC0_PAGE		Paging bit for Coarse DDC0.	0x1	R/W
		3	ADC3_PAGE		Paging bit for ADC3 for AD9081/AD9988/AD9209.	0x1	R/W
		2	ADC2_PAGE		Paging bit for ADC2 for AD9081/AD9988/AD9209.	0x1	R/W
					Paging bit for ADC1 for AD9082/AD9986/AD9207.	0x1	R/W
		1	ADC1_PAGE		Paging bit for ADC1 for AD9081/AD9988/AD9209.	0x1	R/W
		0	ADC0_PAGE		Paging bit for ADC0 for AD9081/AD9988/AD9082/ AD9986/AD9209/AD9207.	0x1	R/W
0x0019	FINE_DDC_PAGE	7	FINE_DDC7_PAGE		Paging bit for Fine DDC7.	0x1	R/W
		6	FINE_DDC6_PAGE		Paging bit for Fine DDC6.	0x1	R/W
		5	FINE_DDC5_PAGE		Paging bit for Fine DDC5.	0x1	R/W
		4	FINE_DDC4_PAGE		Paging bit for Fine DDC4.	0x1	R/W
		3	FINE_DDC3_PAGE		Paging bit for Fine DDC3.	0x1	R/W
		2	FINE_DDC2_PAGE		Paging bit for Fine DDC2.	0x1	R/W
		1	FINE_DDC1_PAGE		Paging bit for Fine DDC1.	0x1	R/W
		0	FINE_DDC0_PAGE		Paging bit for Fine DDC0.	0x1	R/W
0x001A	JTX_PAGE	[7:2]	RESERVED		Reserved.	0x0	R
		1	JTX_LINK1_PAGE		SPI write to link 1 enable. Only applies when in dual link mode. Paging bit for JTX Link1	0x1	R/W
				1	1 = Framer 1 is being written to.		
		0	JTX_LINK0_PAGE		SPI write to link 0 enable. Paging bit for JTX Link0	0x1	R/W
				1	1 = Framer 0 is being written to.		
0x001B	PAGEINDX_DAC_MAINDP_ DAC	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	DACPAGE_MSK		Sets DAC and main Tx Datapath paging. Each high bit in this field pages a DAC/Datapath as follows (starting at the LSB): DAC 0, DAC 1, DAC 2, DAC 3.	0xF	R/W
0x001C	PAGEINDX_DAC_CHAN	[7:0]	DACCHAN_MSK		Sets Tx channel paging. Each high bit in this field pages a complex channel as follows (starting at the LSB): ch0, ch1, ch2, ch3, ch4, ch5, ch6, ch7.	0xFF	R/W
0x001D	PAGEINDX_DAC_JRX	[7:4]	RESERVED		Reserved.	0x0	R
		[3:2]	MODS_MSK		DAC mod_switch page select, to page Mode Multiplexer 0 or Mode Multiplexer 1.	0x3	R/W
				x1	x 1 = Page Mode Multiplexer 0.		
				1x	1 x = Page Mode Multiplexer 1.		
		[1:0]	JRX_LINK_MSK		DAC JRX link page mask. Selects which Deframer is being written to (only needed when in dual link mode). All registers in this table are paged so that each link 's registers are addressed independently.	0x3	R/W
				01	2b'01 = selects link 0.		
				10	2b'10 = selects link 1 (only needed when in dual link mode).		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				11	2b'11 = selects both links.		
0x001E	PFILT_CTL_PAGE	[7:2]	RESERVED		Reserved.	0x0	R
		1	PFILT_ADC_PAIR1_PAGE		Paging bit for PFILT ADC Pair 1.	0x1	R/W
		0	PFILT_ADC_PAIR0_PAGE		Paging bit for PFILT ADC Pair 0.	0x1	R/W
0x001F	PFILT_COEFF_PAGE	[7:4]	RESERVED		Reserved.	0x0	R
		3	PFILT_COEFF_PAGE3		Paging bit for PFILT Coeff bank3.	0x1	R/W
		2	PFILT_COEFF_PAGE2		Paging bit for PFILT Coeff bank2.	0x1	R/W
		1	PFILT_COEFF_PAGE1		Paging bit for PFILT Coeff bank1.	0x1	R/W
		0	PFILT_COEFF_PAGE0		Paging bit for PFILT Coeff bank0.	0x1	R/W
0x0020	IRQ_ENABLE_0	7	RESERVED		Reserved.	0x0	R
		6	EN_DATA_READY		Enable JESD204 receiver ready (JRX_DATA_READY) low interrupt.	0x0	R/W
		5	EN_LANE_FIFO	0 1	Enable lane FIFO overflow/underflow interrupt and sets the function of the IRQ_ LANE_FIFO bit. 0 = IRQ_LANE_FIFO shows current status of the lane FIFO error monitor (detects FIFO full or empty conditions). 1 = IRQ_LANE_FIFO latches a FIFO error condition (becomes a sticky bit) if it ever occurs and enables the IRQ pin.	0x0	R/W
		[4:3]	RESERVED		Reserved.	0x0	R/W
		2	EN_SYSREF_IRQ	0 1	Enables the IRQ pin and sets the function of the IRQ_SYSREF_JITTER bit. 0 = IRQ_SYSREF_JITTER shows current status of the SYSREF jitter monitor whose threshold is set by the SYSREF_ERR_WINDOW register (0x00B7). 1 = IRQ_SYSREF_JITTER latches a SYSREF jitter monitor error condition (becomes a sticky bit) if it ever occurs and enables the IRQ pin.	0x0	R/W
		[1:0]	RESERVED		Reserved.	0x0	R/W
0x0021	IRQ_ENABLE_1	7	EN_PAERR_1		Enable PA protection error interrupt for DAC1.	0x0	R/W
		6	EN_HWIPERR_1		See IRQ_HWIPERR1.	0x0	R/W
		5	EN_DAC1_CAL_DONE_IRQ		Enable DAC1 calibration complete interrupt.	0x0	R/W
		4	EN_DAC1_MAIN_DP_BIST_DONE_IRQ		enable DAC1_MAIN_DP_BIST_done IRQ.	0x0	R/W
		3	EN_PAERR_0		Enable PA protection error interrupt for DAC0.	0x0	R/W
		2	EN_HWIPERR_0		See IRQ_HWIPERR0.	0x0	R/W
		1	EN_DAC0_CAL_DONE_IRQ		Enable DAC0 calibration complete interrupt.	0x0	R/W
		0	EN_DAC0_MAIN_DP_BIST_DONE_IRQ		enable DAC0_MAIN_DP_BIST_done IRQ.	0x0	R/W
0x0022	IRQ_ENABLE_2	7	EN_PAERR_3		Enable PA protection error interrupt for DAC3.	0x0	R/W
		6	EN_HWIPERR_3		See IRQ_HWIPERR3.	0x0	R/W
		5	EN_DAC3_CAL_DONE_IRQ		Enable DAC3 calibration complete interrupt.	0x0	R/W
		4	EN_DAC3_MAIN_DP_BIST_DONE_IRQ		enable _DAC3_MAIN_DP_BIST_done IRQ.	0x0	R/W
		3	EN_PAERR_2		Enable PA protection error interrupt for DAC2.	0x0	R/W
		2	EN_HWIPERR_2		See IRQ_HWIPERR2.	0x0	R/W
		1	EN_DAC2_CAL_DONE_IRQ		Enable DAC2 calibration complete interrupt.	0x0	R/W
		0	EN_DAC2_MAIN_DP_BIST_DONE_IRQ		enable DAC2_MAIN_DP_BIST_done IRQ.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0023	IRQ_ENABLE_3	7	EN_DLL_LOST23		See IRQ_DLL_LOST.	0x0	R/W
		6	EN_DLL_LOCK23		See IRQ_DLL_LOCK.	0x0	R/W
		5	EN_DLL_LOST01		See IRQ_DLL_LOST.	0x0	R/W
		4	EN_DLL_LOCK01		See IRQ_DLL_LOCK.	0x0	R/W
		3	EN_PLL_LOST_SLOW		See IRQ_PLL_LOST_SLOW.	0x0	R/W
		2	EN_PLL_LOST_FAST		See IRQ_PLL_LOST_FAST.	0x0	R/W
		1	EN_PLL_LOCK_SLOW		See IRQ_PLL_LOCK_SLOW.	0x0	R/W
		0	EN_PLL_LOCK_FAST		See IRQ_PLL_LOCK_FAST.	0x0	R/W
0x0024	IRQ_ENABLE_4	7	EN_DP3_DLL_VTH_PASS		dp3 dll vth in range enable.	0x0	R/W
		6	EN_DP2_DLL_VTH_PASS		dp2 dll vth in range enable.	0x0	R/W
		5	EN_DP1_DLL_VTH_PASS		dp1 dll vth in range enable.	0x0	R/W
		4	EN_DP0_DLL_VTH_PASS		dp0 dll vth in range enable.	0x0	R/W
		3	EN_DP3_DLL_VTH_FAIL		dp3 dll vth out of range enable.	0x0	R/W
		2	EN_DP2_DLL_VTH_FAIL		dp2 dll vth out of range enable.	0x0	R/W
		1	EN_DP1_DLL_VTH_FAIL		dp1 dll vth out of range enable.	0x0	R/W
		0	EN_DP0_DLL_VTH_FAIL		dp0 dll vth out of range enable.	0x0	R/W
0x0026	IRQ_STATUS0	7	RESERVED		Reserved.	0x0	R
		6	IRQ_DATA_READY		JESD receiver's data_ready is low. If EN_DATA_READY is low, IRQ_DATA_READY shows current status. If EN_DATA_READY is high, IRQ_DATA_READY latches and pulls the IRQB_x pin low (x = MUX_DATA_READY setting). Writing a 1 to IRQ_DATA_READY when latched clears it.	0x0	R/W
		5	IRQ_LANE_FIFO		If EN_LANE_FIFO_IRQ = 0: Shows the real time status of the FIFO error monitor: 0 = Lane FIFO is not currently in an overflow/ underflow condition. 1 = Lane FIFO is in an overflow/underflow condition.	0x0	R/W
					If EN_LANE_FIFO_IRQ = 1: Indicates if a lane FIFO overflow/underflow condition has ever occurred (sticky bit) since power-on reset or last clearing of the bit. 0 = Lane FIFO has not experienced an overflow/ underflow condition since last clearing of the bit 1 = Lane FIFO has experienced an overflow/ underflow condition since last clearing of the bit and triggered an interrupt by pulling the IRQB_x pin low (x = MUX_LANE_FIFO setting). Write any value to the IRQ_LANE_FIFO when latched to clear the register.		
		[4:3]	RESERVED		Reserved.	0x0	R/W
		2	IRQ_SYSREF_JITTER	0 1	If EN_SYSREF_IRQ = 0: Shows the real time status of SSYREF jitter monitor:. 0 = SYSREF is currently within the SYSREF jitter limits as set by the SYSREF_ERR_WINDOW register (0x00B7). 1 = SYSREF is currently outside the SYSREF jitter limits as set by the SYSREF_ERR_WINDOW register (0x00B7).	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				--	If EN_SYSREF_IRQ = 1: Indicates if a SYSREF jitter monitor error condition (has ever occurred (sticky bit) since power-on reset or last clearing of the bit.		
				0	0 = SYSREF has been within the SYSREF jitter limits as set by the SYSREF_ERR_WINDOW register (0x00B7) since last clearing of the bit.		
				1	1 = SYSREF has gone outside the SYSREF jitter limit as set by the SYSREF_ERR_WINDOW register (0x00B7) and triggered an interrupt by pulling the IRQB_x pin low (x = MUX_SYSREF_JITTER setting).		
				--	Write any value to the IRQ_SYSREF_JITTER when latched to clear the register.		
		[1:0]	RESERVED		Reserved.	0x0	R/W
0x0027	IRQ_STATUS1	7	IRQ_PAERR1		DAC1 PA error. If EN_PAERR1 is low, IRQ_PAERR1 shows current status. If EN_PAERR1 is high, IRQ_PAERR1 latches and pulls the IRQB_x pin low (x = MUX_PAERR1 setting). Writing a 1 to IRQ_PAERR1 when latched clears it.	0x0	R/W
		[6:4]	RESERVED		Reserved.	0x0	R/W
		3	IRQ_PAERR0		DAC0 PA error. If EN_PAERR0 is low, IRQ_PAERR0 shows current status. If EN_PAERR0 is high, IRQ_PAERR0 latches and pulls the IRQB_x pin low (x = MUX_PAERR0 setting). Writing a 1 to IRQ_PAERR0 when latched clears it.	0x0	R/W
		[2:0]	RESERVED		Reserved.	0x0	R/W
0x0028	IRQ_STATUS2	7	IRQ_PAERR3		DAC3 PA error. If EN_PAERR3 is low, IRQ_PAERR3 shows current status. If EN_PAERR3 is high, IRQ_PAERR3 latches and pulls the IRQB_x pin low (x = MUX_PAERR3 setting). Writing a 1 to IRQ_PAERR3 when latched clears it.	0x0	R/W
		[6:4]	RESERVED		Reserved.	0x0	R/W
		3	IRQ_PAERR2		DAC2 PA error. If EN_PAERR2 is low, IRQ_PAERR2 shows current status. If EN_PAERR2 is high, IRQ_PAERR2 latches and pulls the IRQB_x pin low (x = MUX_PAERR2 setting). Writing a 1 to IRQ_PAERR2 when latched clears it.	0x0	R/W
		[2:0]	RESERVED		Reserved.	0x0	R/W
0x0029	IRQ_STATUS3	7	RESERVED		Reserved.	0x0	R/W
		6	IRQ_DLL_LOCK23		DLL locked. If EN_DLL_LOCK is low, IRQ_DLL_LOCK shows current status. If EN_DLL_LOCK is high, IRQ_DLL_LOCK latches and pulls the IRQB_x pin low (x = MUX_DLL_LOCK setting). Writing a 1 to IRQ_DLL_LOCK when latched clears it.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R/W
		4	IRQ_DLL_LOCK01		DLL locked. If EN_DLL_LOCK is low, IRQ_DLL_LOCK shows current status. If EN_DLL_LOCK is high, IRQ_DLL_LOCK latches and pulls the IRQB_x pin low (x = MUX_DLL_LOCK setting). Writing a 1 to IRQ_DLL_LOCK when latched clears it.	0x0	R/W
		3	IRQ_PLL_LOST_SLOW		If slow lock enabled: DAC PLL lost. If EN_PLL_LOST_SLOW is low,	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					IRQ_PLL_LOST_SLOW shows current status. If EN_PLL_LOST_SLOW is high, IRQ_PLL_LOST_SLOW latches and pulls the IRQB_x pin low (x = MUX_PLL_LOST_SLOW setting). Writing a 1 to IRQ_PLL_LOST_SLOW when latched clears it.		
		2	IRQ_PLL_LOST_FAST		If fast lock enabled: DAC PLL lost. If EN_PLL_LOST_FAST is low, IRQ_PLL_LOST_FAST shows current status. If EN_PLL_LOST_FAST is high, IRQ_PLL_LOST_FAST latches and pulls the IRQB_x pin low (x = MUX_PLL_LOST_FAST setting). Writing a 1 to IRQ_PLL_LOST_FAST when latched clears it.	0x0	R/W
		1	IRQ_PLL_LOCK_SLOW		If slow lock enabled: DAC PLL locked. If EN_PLL_LOCK_SLOW is low, IRQ_PLL_LOCK_SLOW shows current status. If EN_PLL_LOCK_SLOW is high, IRQ_PLL_LOCK_SLOW latches and pulls the IRQB_x pin low (x = MUX_PLL_LOCK_SLOW setting). Writing a 1 to IRQ_PLL_LOCK_SLOW when latched clears it.	0x0	R/W
		0	IRQ_PLL_LOCK_FAST		If fast lock enabled: DAC PLL locked. If EN_PLL_LOCK_FAST is low, IRQ_PLL_LOCK_FAST shows current status. If EN_PLL_LOCK_FAST is high, IRQ_PLL_LOCK_FAST latches and pulls the IRQB_x pin low (x = MUX_PLL_LOCK_FAST setting). Writing a 1 to IRQ_PLL_LOCK_FAST when latched clears it.	0x0	R/W
0x002C	IRQ_OUTPUT_MUX_0	7	MUX_JESD_IRQ		Select which IRQ pin is connected to the JESD IRQ sources.	0x0	R/W
				0	Route IRQ signal to the IRQB0 pin.		
				1	Route IRQ signal to the IRQB1 pin.		
		6	MUX_DATA_READY		Select which IRQ pin is connected to the DATA READY IRQ sources. 0: Route IRQ signal to the IRQB0 pin. 1: Route IRQ signal to the IRQB1 pin.	0x0	R/W
				0	disable interrupt.		
				1	enable interrupt.		
		5	MUX_LANE_FIFO		Select which IRQ pin is connected to the LANE FIFO error sources.	0x0	R/W
				0	disable interrupt.		
				1	enable interrupt.		
		[4:3]	RESERVED		Reserved.	0x0	R/W
		2	MUX_SYSREF_JITTER		Select which IRQ pin is connected to the SYSREF JITTER source. 0: Route IRQ signal to the IRQB0 pin. 1: Route IRQ signal to the IRQB1 pin.	0x0	R/W
				0	0: Route IRQ signal to the IRQB0 pin.		
				1	1: Route IRQ signal to the IRQB1 pin.		
		[1:0]	RESERVED		Reserved.	0x0	R/W
0x002D	IRQ_OUTPUT_MUX_1	7	MUX_PAERR1		Select which IRQ pin is connected to the PAERR1 source.	0x0	R/W
				0	0: Route IRQ signal to the IRQB0 pin.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				1	1: Route IRQ signal to the IRQB1 pin.		
		[6:4]	RESERVED		Reserved.	0x0	R/W
		3	MUX_PAERR0		Select which IRQ pin is connected to the PAERR0 source.	0x0	R/W
				0	0: Route IRQ signal to the IRQB0 pin.		
				1	1: Route IRQ signal to the IRQB1 pin.		
		[2:0]	RESERVED		Reserved.	0x0	R/W
0x002E	IRQ_OUTPUT_MUX_2	7	MUX_PAERR3		Select which IRQ pin is connected to the PAERR3 source.	0x0	R/W
				0	0: Route IRQ signal to the IRQB0 pin.		
				1	1: Route IRQ signal to the IRQB1 pin.		
		[6:4]	RESERVED		Reserved.	0x0	R/W
		3	MUX_PAERR2		Select which IRQ pin is connected to the PAERR2 source.	0x0	R/W
				0	0: Route IRQ signal to the IRQB0 pin.		
				1	1: Route IRQ signal to the IRQB1 pin.		
		[2:0]	RESERVED		Reserved.	0x0	R/W
0x002F	IRQ_OUTPUT_MUX_3	7	RESERVED		Reserved.	0x1	R/W
		6	MUX_DLL_LOCK23		Select which IRQ pin is connected to the DLL LOCK 23 source.	0x1	R/W
				0	0: Route IRQ signal to the IRQB0 pin.		
				1	1: Route IRQ signal to the IRQB1 pin.		
		5	RESERVED		Reserved.	0x0	R/W
		4	MUX_DLL_LOCK01		Select which IRQ pin is connected to the DLL LOCK01 source.	0x0	R/W
				0	0: Route IRQ signal to the IRQB0 pin.		
				1	1: Route IRQ signal to the IRQB1 pin.		
		3	MUX_PLL_LOST_SLOW		Select which IRQ pin is connected to the PLL LOST SLOW source.	0x0	R/W
				0	0: Route IRQ signal to the IRQB0 pin.		
				1	1: Route IRQ signal to the IRQB1 pin.		
		2	MUX_PLL_LOST_FAST		Select which IRQ pin is connected to the PLL LOST FAST source.	0x0	R/W
				0	0: Route IRQ signal to the IRQB0 pin.		
				1	1: Route IRQ signal to the IRQB1 pin.		
		1	MUX_PLL_LOCK_SLOW		Select which IRQ pin is connected to the PLL LOCK SLOW source.	0x0	R/W
				0	0: Route IRQ signal to the IRQB0 pin.		
				1	1: Route IRQ signal to the IRQB1 pin.		
		0	MUX_PLL_LOCK_FAST		Select which IRQ pin is connected to the PLL LOCK FAST source.	0x0	R/W
				0	0: Route IRQ signal to the IRQB0 pin.		
				1	1: Route IRQ signal to the IRQB1 pin.		
0x0032	IRQ_STATUS_ALL	[7:1]	RESERVED		Reserved.	0x0	R
		0	IRQ_STATUS_ALL		OR THE BITS IN 0X26-0X2B. WRITING A ONE TO THIS BIT WILL CLEAR ANY LATCHED IRQB SIGNALS IN 0X26-0X2B.	0x0	R/W
0x0033	GPIO_STATUS0	7	GPIO_TXEN1_IN		Reads the TXEN1 value on GPIO4 if set as an input.	0x0	R
		6	GPIO_DAC_NCO_FFH5_IN		Reads the dac_nco_ffh5 value on GPIO3 if set as an input.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		5	GPIO_DAC_NCO_FFH4_IN		Reads the dac_nco_ffh4 value on GPIO2 if set as an input.	0x0	R
		4	RESERVED		Reserved.	0x0	R
		3	GPIO_DAC_NCO_FFH3_IN		Reads the dac_nco_ffh3 value on GPIO1 if set as an input.	0x0	R
		2	RESERVED		Reserved.	0x0	R
		1	GPIO_DAC_NCO_FFH2_IN		Reads the dac_nco_ffh2 value on GPIO0 if set as an input.	0x0	R
		0	RESERVED		Reserved.	0x0	R
0x0034	GPIO_STATUS1	[7:5]	RESERVED		Reserved.	0x0	R
		4	GPIO_DAC_NCO_FFH1_IN		Reads the dac_nco_ffh1 value on SYNCB- if set as an input.	0x0	R
		3	GPIO_DAC_NCO_FFH0_IN		Reads the dac_nco_ffh0 value on SYNCB+ if set as an input.	0x0	R
		2	GPIO_DAC_NCO_STROBE_IN		Reads the dac_nco_strobe value on GPIO5 if set as an input.	0x0	R
		1	GPIO_TXEN3_IN		Reads the txen3 value on GPIO5 if set as an input.	0x0	R
		0	GPIO_DAC_NCO_FFH6		Reads the dac_nco_ffh6 value on GPIO4 if set as an input.	0x0	R
0x0035	GPIO_CFG0	[7:4]	GPIO1_CFG		GIPO1 configuration.	0x0	R/W
				0x0	High-Z (disabled).		
				0x1	Output: PA1_EN.		
				0x2	Do not use.		
				0x3	Input: NCO FFH3.		
				0xA	Output: NCO main-subordinate sync: main out.		
				0xB	Input: NCO main-subordinate sync: subordinate in.		
		[3:0]	GPIO0_CFG		GIPO0 configuration.	0x0	R/W
				0x0	High-Z (disabled).		
				0x1	Output: PA0_EN.		
				0x2	Do not use.		
				0x3	Input: NCO FFH2.		
				0xA	Output: NCO main-subordinate sync: main out.		
				0xB	Input: NCO main-subordinate sync: subordinate in.		
0x0036	GPIO_CFG1	[7:4]	GPIO3_CFG		GIPO3 configuration.	0x0	R/W
				0x0	High-Z (disabled).		
				0x1	Do not use.		
				0x2	Output: PA3_EN.		
				0x3	Input: NCO FFH5.		
				0xA	Output: NCO main-subordinate sync: main out.		
				0xB	Input: NCO main-subordinate sync: subordinate in.		
		[3:0]	GPIO2_CFG		GIPO2 configuration.	0x0	R/W
				0x0	High-Z (disabled).		
				0x1	Output: PA2_EN.		
				0x2	Do not use.		
				0x3	Input: NCO FFH4.		
				0xA	Output: NCO main-subordinate sync: main out.		
				0xB	Input: NCO main-subordinate sync: subordinate in.		
0x0037	GPIO_CFG2	[7:4]	GPIO5_CFG		GIPO5 configuration.	0x0	R/W
				0x0	High-Z (disabled).		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0x1	Input: TXEN3.		
				0x2	Input: NCO FFH Strobe (latch all FFH[n] inputs).		
				0x3	Do not use.		
				0xA	Output: NCO main-subordinate sync: main out.		
				0xB	Input: NCO main-subordinate sync: subordinate in.		
		[3:0]	GPIO4_CFG		GIPO4 configuration.	0x0	R/W
				0x0	High-Z (disabled).		
				0x1	Input: TXEN1.		
				0x2	Input: NCO FFH6.		
				0x3	Do not use.		
				0xA	Output: NCO main-subordinate sync: main out.		
				0xB	Input: NCO main-subordinate sync: subordinate in.		
0x0038	GPIO_CFG3	[7:4]	SYNC1_OUTBN_CFG		SYNCOUTB1- pin configuration. Program bit SEL_SYNCB_MODE_RC (reg 0x042a[0]) to configure the SYNCOUTB1 port as either two single-ended pins or one differential pin.	0x0	R/W
				0x0	High-Z (disabled) or differential output if SEL_SYNCB_MODE_RC = 1.		
				0x1	Single end input: NCO FFH1.		
		[3:0]	SYNC1_OUTBP_CFG		SYNCOUTB1+ pin configuration. Program bit SEL_SYNCB_MODE_RC (reg 0x042a[0]) to configure the SYNCOUTB1 port as either two single-ended pins or one differential pin.	0x0	R/W
				0x0	High-Z (disabled).		
				0x1	single end output: JESD204B SYNCOUTB1 signal.		
				0x2	Do not use.		
				0x3	single end input: NCO FFH0.		
				0x9	differential output: JESD204B SYNCOUTB1 signal if SEL_SYNCB_MODE_RC = 1.		
0x0061	DLL_CTRL0	[7:1]	RESERVED		Reserved.	0x34	R/W
		0	DLL_ENABLE		DLL controller enable.	0x0	R/W
				0	Disable DLL controller - Use static SPI settings.		
				1	Enable DLL controller - Use controller with feedback loop.		
0x0063	DLL_STATUS	[7:2]	RESERVED		Reserved.	0x0	R
		1	DLL_LOST		DLL lost indicator. This is a sticky bit indicating there was a falling edge of dll_locked. To clear this bit, perform a SPI write to this register.	0x0	R/W
		0	DLL_LOCKED		DLL lock indicator. This control reads back 1 if the DLL successfully locks.	0x0	R
0x0090	DAC_POWERDOWN	[7:4]	RESERVED		Reserved.	0xF	R
		3	DAC_PD3		Powers down DAC 3.	0x1	R/W
		2	DAC_PD2		Powers down DAC 2.	0x1	R/W
		1	DAC_PD1		Powers down DAC 1.	0x1	R/W
		0	DAC_PD0		Powers down DAC 0.	0x1	R/W
0x0091	ACLK_CTRL	[7:4]	RESERVED		Reserved.	0x0	R
		3	PD_TXDIGCLK		Control bit needed as part of the oneshot sync sequence along with SPI_SWAP_ADC_SYN (0x0180[7]). See the SYSREF Setup/Sync Procedure section.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[2:1]	RESERVED		Reserved.	0x0	R
		0	ACLK_POWERDOWN		Analog clock receiver power down.	0x1	R/W
0x0092	ACLK_CTRL2	[7:6]	RESERVED		Reserved.	0x0	R
		5	ANACENTER_ACLK_DCC_GT50		Flag to indicate ACLK duty cycle is bigger than 50%.	0x0	R
		4	ANACENTER_ACLK_DCC_EQ50		Flag to indicate ACLK duty cycle is 50%.	0x0	R
		[3:0]	ANACENTER_ACLK_DCC_ADJ		ACLK duty cycle adjustment bits (need step size).	0x0	R/W
0x0093	PLL_CLK_DIV	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	PLL_DIVIDEFACTOR		PLL output clock divider factor “D”	0x0	R/W
				00	0: div1.		
				01	1: div2.		
				10	2: div3.		
				11	3: div4.		
0x0094	PLL_BYPASS	[7:5]	RESERVED		Reserved.	0x0	R
		4	EN_PDPLL_WHENBYPASS		Enable to auto power down entire PLL when pll_bypass is set 1. Set this bit low if you want to debug PLL while at PLL bypass mode.	0x1	R
		[3:1]	RESERVED		Reserved.	0x0	R
		0	PLL_BYPASS		Enable direct clocking (bypassing the PLL clock).	0x0	R/W
				0	Use the PLL clock.		
				1	Bypass the PLL, and use direct clock.		
0x00B0	SYNC_LMFC_DELAY_FRAME	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	SYNC_LMFC_DELAY_SET_FRM		SYSREF to LMFC/LEMC coarse delay (in frame units).	0x0	R/W
0x00B1	SYNC_LMFC_DELAY	[7:0]	SYNC_LMFC_DELAY_SET		SYSREF to LMFC/LEMC fine delay (in DAC clock units).	0x0	R/W
0x00B2	SYNC_LMFC_STAT0	[7:0]	SYNC_LMFC_DELAY_STAT[7:0]		SYSREF to LMFC/LEMC delay status (in DAC clock units).	0x0	R/W
0x00B3	SYNC_LMFC_STAT1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	SYNC_LMFC_DELAY_STAT[11:8]		SYSREF to LMFC/LEMC delay status (in DAC clock units).	0x0	R
0x00B4	SYSREF_COUNT	[7:0]	SYSREF_COUNT		Number of SYSREF edges to be ignored before sync (pulse counting mode). Set to non-0 enables pulse counting mode. See detailed description in multi-chip sync section.	0x0	R/W
0x00B5	SYSREF_PHASE0	[7:0]	SYSREF_PHASE[7:0]		Phase offset between monitored SYSREF and internal LMFC/LEMC in DAC clock units. Write any value to these registers to initiate a phase value update.	0x0	R/W
0x00B6	SYSREF_PHASE1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	SYSREF_PHASE[11:8]		Phase offset between monitored SYSREF and internal LMFC/LEMC in DAC clock units. Write any value to these registers to initiate a phase value update.	0x0	R/W
0x00B7	SYSREF_ERR_WINDOW	7	SYSREF_WITHIN_LMFC_ERRWINDOW		When this register = 1, the latest SYSREF is within the error window centered by LMFC.	0x0	R
		[6:0]	SYSREF_ERR_WINDOW		Amount of jitter/drift allowed on the SYSREF input. SYSREF jitter variations or drift larger than this value triggers an interrupt (DAC clock units).	0x0	R/W
0x00B8	SYSREF_MODE	[7:6]	RESERVED		Reserved.	0x0	R
		5	INIT_SYNC_DONE		Initial sync done flag (after initial power-up).	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		4	ONESHOT_SYNC_DONE		one-shot sync done flag (after enabling SYSREF and following the SYSREF Setup/Sync Procedure).	0x0	R
		[3:2]	RESERVED		Reserved.	0x0	R/W
		1	SYSREF_MODE_ONESHOT		Enable one shot synchronization rotation mode.	0x0	R/W
		0	SYSREF_MODE_CONTINUOUS		Enable continuous synchronization rotation mode.	0x0	R/W
0x00B9	ROTATION_MODE	[7:5]	RESERVED		Reserved.	0x1	R
		4	NCORST_AFTER_ROT_EN		When set to 1, all NCOs will be reset after either digital reset or one-shot sync.	0x1	R/W
		[3:2]	RESERVED		Reserved.	0x0	R
		[1:0]	ROTATION_MODE		Rotation mode options.	0x0	R/W
				00	00 = In subclass 0, clock rotation occurs immediately. If in subclass 1, Rotate clocks as soon as SYSREF_MODE_ONESHOT (0x00B8[1]) is enabled and pulses arrive at the SYSREF± input.		
				01	01 = Device powers down the JESD link prior to clock rotation and brings the link back up afterwards.		
				10	10 = Device powers down the datapath (using soft on/off function) prior to clock rotation and brings the datapath back up afterwards.		
				11	11 = Device powers down the JESD link and the datapath (using soft on/off function) prior to clock rotation and brings the datapath and link back up afterwards.		
				--	If EN_SYSREF_IRQ = 0: Shows the real time status of SSYREF jitter monitor:.		
0x00BA	SYSREF_AVERAGE	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	SYSREF_AVERAGE		Sets how many SYSREF pulses are averaged is in sampled mode and no averaging is done. This bit field must be set prior to enabling one shot mode.	0x0	R/W
0x00BC	NCO_SYNC_MS_TRIG	[7:1]	RESERVED		Reserved.	0x0	R
		0	NCO_SYNC_MS_TRIG		Set to 1 to trigger main-subordinate NCO synchronization, self-clearing.	0x0	R/W
0x00BD	RX_TX_LMFC_LCM	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	RX_TX_LMFC_LCM		If the JTx LMFC/LEMC period is an integer multiple of the JRx LMFC/LEMC set to 0. Otherwise, set it to the value of LCM to 1. For example, if Rx/Tx = 3/2, set to 5. If Rx/Tx = 2, set to 1. If Tx/Rx = 5/3, set to 14. Otherwise, set it to the value of LCM to 1. For example, If Rx/Tx = 3/2, set to 5. If Rx/Tx = 2, set to 1. If Tx/Rx = 5/3, set to 14.	0x0	R/W
0x00C0	CLOCKING_CTRL	[7:6]	RESERVED		Reserved.	0x0	R
		[5:4]	DIRECT_LOOPBACK_MODE		Direct loop back mode control. [0]: Enable: Set 1 to route ADC data directly to DAC output. [1]: Mode control: ADC converts 12 bits but with some extended dynamic range. Setting this bit to 1 clips ADC to 12 bit range and removes extended dynamic range. ADC value is MSB justified into DAC output. Setting this bit to 0 allows extended range to pass to the DAC but only half the amplitude is available to allow the extended range.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[3:2]	RESERVED		Reserved.	0x0	R
		1	TXCLK_EN		Enable transmit dig source clock. TX datapath clock enable bit,.	0x1	R/W
				0	0 = HSADC (AD9207/AD9209) device configurations.		
				1	1 = DAC only or MxFE (AD9081/AD9988/AD9082/AD9986/AD9177) device configurations.		
		0	RXCLK_EN		enable rx dig source clock.	0x1	R/W
0x00C2	LOOPBACK_CB_CTRL	[7:0]	LOOPBACK_CB_CTRL		Loop back crossbar control. Controls which ADC[n] maps to each DAC[n]: [7:6]: two-bit value sets the ADC number that maps to DAC3 [5:4]: two-bit value sets the ADC number that maps to DAC2 [3:2]: two-bit value sets the ADC number that maps to DAC1	0x0	R/W
					[1:0]: two-bit value sets the ADC number that maps to DAC0		
				00	ADC0.		
				01	ADC1.		
				10	ADC2.		
				11	ADC3.		
0x00C3	RETIMER_DEBUG0	[7:4]	DAC_DATA_XOR_EN		enable DAC data scrambling in sync and retimer block.	0x0	R/W
				00	[0] for DAC0.		
				01	[1] for DAC1.		
				10	[2] for DAC2.		
				11	[3] for DAC3.		
		[3:0]	DAC_DATA_INVERSION_EN		enable DAC data 2's compliment inversion in sync and retime block.	0x0	R/W
				00	[0] for DAC0.		
				01	[1] for DAC1.		
				10	[2] for DAC2.		
				11	[3] for DAC3.		
0x00C5	SYNC_DEBUG0	[7:6]	RESERVED		Reserved.	0x0	R
		5	AVRG_FLOW_EN		Set to 1 when using SYSREF averaging mode.	0x0	R/W
		[4:0]	RESERVED		Reserved.	0x7	R/W
0x00C7	MANUAL_LMFC_PERIOD0	[7:0]	LMFC_PERIOD_SPI[7:0]		LMFC period from SPI setting in fdac/4 units.	0x80	R/W
0x00C8	MANUAL_LMFC_PERIOD1	[7:5]	RESERVED		Reserved.	0x0	R
		4	LMFC_PERIOD_SPI_EN		Enable LMFC period from SPI. LMFC period form SPI setting instead of JESD mode setting.	0x0	R/W
		3	RESERVED		Reserved.	0x0	R
		[2:0]	LMFC_PERIOD_SPI[10:8]		LMFC period from SPI setting in fdac/4 units.	0x1	R/W
0x00CB	NCOSYNC_SYSREF_MODE	[7:4]	RESERVED		Reserved.	0x1	R
		[3:2]	NCO_SYNC_SYSREF_MODE_RX		Control how RX NCO is synced by SYSREF.	0x1	R/W
				00	0: immediately by SYSREF;.		
				01	1: by next LMFC rising edge after SYSREF;.		
				10	2: by next LMFC falling edge after SYSREF;.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				11	3: reserved.		
		[1:0]	NCO_SYNC_SYSREF_MODE		Control how TX NCO is synced by SYSREF.	0x1	R/W
				00	0: immediately by SYSREF.		
				01	1: by next LMFC rising edge after SYSREF.		
				10	2: by next LMFC falling edge after SYSREF.		
				11	3: reserved.		
0x00CC	NCOSYNC_MS_MODE	[7:4]	NCO_SYNC_MS_EXTRA_LMFC_NUM		In NCO main-subordinate sync mode, set how many extra LMFC cycles to delay before an NCO reset is issued. This control is only valid when NCO_SYNC_MS_MODE=1 and NCO_SYNC_MS_TRIG_SOURCE != 0.	0x0	R/W
		[3:2]	NCO_SYNC_MS_TRIG_SOURCE		Select which source to trigger Leader-Follower mode for the main device.	0x1	R/W
				00	0: SYSREF;.		
				01	1: LMFC rise;.		
				10	2: LMFC fall.		
		[1:0]	NCO_SYNC_MS_MODE		Control main-subordinate mode for NCO sync.	0x0	R/W
				00	0: disable;.		
				01	1: set as leader;.		
				10	2: set as follower;.		
				11	3: disable.		
0x00D0	SPI_ENABLE_DAC	[7:5]	RESERVED		Reserved.	0x0	R
		4	SPI_EN_DAC_ANA		Enable access to DAC registers in range 0x105-0x134. Each DAC has its own register block. All DACs may be written concurrently. DAC registers should be read back one DAC at a time. DAC register selection is done through the register 0x1B[3:0] with one bit for each DAC. It is recommended that during normal operation that this bit be set to zero to limit SPI clock corruption of the sample clock.	0x1	R/W
		3	SPI_EN_ANACENTER		Enable access to control registers in ranges 0x90-0xA6, 0xE0-0x100, 0xE90-oxEAE. This enable is also automatically enabled by SPI_EN_DAC_ANA = 1. It is recommended that during normal operation that this bit be set to zero to limit SPI clock corruption of the sample clock.	0x1	R/W
		2	SPI_EN_D2ACENTER		Enable access to control register is ranges 0x195-0x19F, and 0xF60-oxFBA. It is recommended that during normal operation that this bit be set to zero to limit SPI clock corruption of the sample clock.	0x1	R/W
		1	SPI_EN_D2A1		Enable access to control registers is ranges 0x180-0x194, 0x60-0x7E, and 0x140-0x178. This will only access these registers for DAC2, DAC3, ADC1, and ADC3. SPI_EN_D2A0 is used for the same ranges on the DAC0, DAC1, ADC0, ADC2 side of the device. Both register sets can be written concurrently by setting both SPI_EN_D2Ax to 1. Only one side should be read from at a time.	0x1	R/W
		0	SPI_EN_D2A0		Enable access to control registers is ranges 0x180-0x194, 0x60-0x7E, and 0x140-0x178. This will only access these registers for DAC0, DAC1, ADC0, and ADC2. SPI_EN_D2A1 is used for the	0x1	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					same ranges on the DAC2, DAC3, ADC1, ADC3 side of the device. Both register sets can be written concurrently by setting both SPI_EN_D2Ax to 1. Only one side should be read from at a time.		
0x00D1	SPI_ENABLE_ADC	[7:6]	RESERVED		Reserved.	0x0	R
		5	SPI_EN_REG32_ADC1		Global enable, ADC1 analog register spi access through the 32bit SPI register.	0x0	R
		4	SPI_EN_REG32_ADC0		Global enable, ADC0 analog register spi access through the 32bit SPI register.	0x0	R
		[3:2]	RESERVED		Reserved.	0x0	R
		1	SPI_EN_REG8_ADC1		Global enable for spi access through the 8bit SPI register. Always set to 1.	0x0	R/W
		0	SPI_EN_REG8_ADC0		Global enable for spi access through the 8bit SPI register. Always set to 1.	0x0	R/W
0x00E0	POWERDOWN_REG_0	7	D_PD_REG		Powerdown regulator (allows external override).	0x0	R/W
		[6:4]	D_PD_CURR		Powerdown bias block: fixed currents, poly currents and 1p5 ref.	0x0	R/W
		3	D_PD_VCO_BUF		Powerdown vco buffer.	0x0	R/W
		2	D_PD_VCO_DRIVER		powerdown vco driver (inside vco).	0x0	R/W
		1	D_PD_VCO_DIV		powerdown vco output divider.	0x0	R/W
		0	D_PD_DIV8		powerdown divide by 8.	0x0	R/W
0x00E1	POWERDOWN_REG_1	[7:5]	RESERVED		Reserved.	0x0	R
		4	D_PD_CP		powerdown charge pump.	0x0	R/W
		3	D_PD_COARSE_BUFF		Powerdown coarse buffer.	0x0	R/W
		2	D_PD_VCM_F		Powerdown vcm fine block.	0x0	R/W
		1	D_PD_VCM_C		Powerdown vcm coarse block.	0x0	R/W
		0	D_PD_REFCLK_DIV		Powerdown pre-divider.	0x0	R/W
0x00E2	RESET_REG	[7:2]	RESERVED		Reserved.	0x0	R
		1	D_CAL_RESET		resets vco calibration.	0x0	R/W
		0	RESERVED		Reserved.	0x0	R/W
0x00E3	INPUT_MISC_REG	[7:2]	RESERVED		Reserved.	0x4	R
		[1:0]	D_REFIN_DIV		PLL input reference clock division factor “R”. Divides reference clock to provide Phase frequency Detector input frequency.	0x0	R/W
				00	00 = /1.		
				01	01 = /2.		
				10	10 = /3.		
				11	11 = /4.		
0x00E4	CHARGEPUMP_REG_0	7	RESERVED		Reserved.	0x0	R/W
		6	D_CP_CAL_EN		Enable PLL charge pump calibration to reduce reference spur.	0x0	R/W
		[5:0]	D_CP_CURRENT		Charge Pump Current.	0x10	R/W
				000000	000000: 100uA;.		
				000001	000001:200uA;.		
				0000--	- - -.		
				111110	111110: 6.3mA;.		
				111111	111111:6.4mA.		
0x00E6	VCM_CONTROL_REG	[7:4]	D_VCM_F_CONTROL		offsets from Vcm.	0xD	R/W
		[3:0]	D_VCM_C_CONTROL		offsets output from Vf.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x00E7	BIAS_REG_0	[7:6]	D_REG_SLICE_SEL		reg slice selection.	0x2	R/W
				00	00: 5mA;.		
				01	01: 10 mA;.		
				10	10: 20 mA;.		
				11	11: 30 mA.		
		[5:0]	D_BIAS_FIXED_TRIM		bias fixed trim values.	0x0	R/W
				000000	000000: 0% current change;.		
				011111	011111: -25% Current change;.		
				100000	100000: 25% current change.		
0x00E8	BIAS_REG_1	7	RESERVED		Reserved.	0x0	R
		6	D_REG_BYPASS_FIT		bypass regulator filter.	0x0	R/W
		[5:0]	D_BIAS_POLY_TRIM		bias poly trim values.	0x0	R/W
				000000	000000: 0% current change;.		
				011111	011111: -8% voltage (1.375);.		
				100000	100000: 25% current change(1.625).		
0x00E9	DIVIDER_REG	[7:6]	RESERVED		Reserved.	0x0	R
		[5:0]	D_DIVIDE_CONTROL		PLL Feedback divider “N” value. Valid values are 0x02 – 0x32 (50 decimal). Total feedback value of PLL = N * value set by D_CONTROL_HS_FB_DIV.	0x8	R/W
0x00EA	VCO_CAL_CONTROL_REG_0	[7:0]	D_IMPALA_CAL_CONTROL[7:0]		Calibration control reg. <1:0>: Pll lock decision count. 2'b11 = 8 count; 2'b10 = 4 count; 2'b01 = 2 count; 2'b00 = 1 count;. <2>: cal_override controls d_control_vco_cal. <3> Spur Buster: dont_pass_m. <4> Spur Buster: override. <7:5> Spur Buster gain. <10:8> Spur Buster fb,. <11> enable fast lock,. <12> enable dual vco mode. <13> enable infinite vco counts after switch in dual vco mode,. <14> force value for the VCO select (0 fast, 1 slow). <15> enable frequency lock feature.	0x60	R/W
0x00EB	VCO_CAL_CONTROL_REG_1	[7:0]	D_IMPALA_CAL_CONTROL[15:8]		Calibration control reg. <1:0>: Pll lock decision count. 2'b11 = 8 count; 2'b10 = 4 count; 2'b01 = 2 count; 2'b00 = 1 count;. <2>: cal_override controls d_control_vco_cal. <3> Spur Buster: dont_pass_m. <4> Spur Buster: override. <7:5> Spur Buster gain. <10:8> Spur Buster fb,. <11> enable fast lock,. <12> enable dual vco mode. <13> enable infinite vco counts after switch in dual vco mode,. <14> force value for the VCO select (0 fast, 1 slow).	0x1D	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					<15> enable frequency lock feature.		
0x00EC	VCO_CAL_LOCK_REG	[7:6]	RESERVED		Reserved.	0x0	R
		[5:4]	D_CONTROL_HS_FB_DIV		VCO output divider “M” in feedback path*,* prior to “N” divider.	0x2	R/W
				00	00 = /5		
				01	01 = /7		
				10	b10 = /8		
				11	b11 = /11		
		3	RESERVED		Reserved.	0x0	R
		[2:1]	D_PLL_LOCK_CONTROL		Lock detector mode. Lock detector counts large or small number of input pfd clocks and compares to feedback pfd clock count. 00: Lock detector disabled 01: Short count “fast” lock detector enabled 10: Long count “slow” lock detector enabled 11: both “fast” and “slow” lock detectors enabled. Locks can be read out at: IRQ_PLL_LOCK_FAST and IRQ_PLL_LOCK_SLOW.	0x3	R/W
		0	RESERVED		Reserved.	0x0	R/W
0x00ED	VCO_CAL_MOMCAP_REG_0	[7:0]	D_VCO_MOMCAP[10:3]		displays the momcap selection from vco_cal.	0x0	R
0x00EE	VCO_CAL_MOMCAP_REG_1	[7:6]	D_VCO_FINE_CAP_PRE		vco cap options.	0x2	R/W
				00	00: 32 fF.		
				01	01: 64 fF.		
				10	10: 96 fF.		
				11	11: 128 fF.		
		5	D_VCO_CAL_TYPE		sets vco calibration type.	0x0	R/W
		[4:3]	D_IMPALA_TEMP		temperature information for the clock multiplier PLL.	0x2	R/W
				00	00: turn off;.		
				01	01: cold;.		
				10	10: nom;.		
				11	11:hot.		
		[2:0]	D_VCO_MOMCAP[2:0]		displays the momcap selection from vco_cal.	0x0	R
0x00F7	CHARGEPUMP_REG_2	[7:6]	RESERVED		Reserved.	0x0	R
		[5:0]	D_CP_BLEED		Changes charge pump current bleed values. Not included in this version.	0x0	R/W
0x00FA	FASTV_COMP_HIGHL_REG_0	[7:0]	D_FASTV_COMP_HIGHL[7:0]		Upper momcap limit for FAST VCO.	0xFF	R/W
0x00FB	FASTV_COMP_HIGHL_REG_1	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	D_FASTV_COMP_HIGHL[10:8]		Upper momcap limit for FAST VCO.	0x2	R/W
0x00FE	SLOWV_COMP_HIGHL_REG_0	[7:0]	D_SLOWV_COMP_HIGHL[7:0]		Upper momcap limit for SLOW VCO.	0x7F	R/W
0x00FF	SLOWV_COMP_HIGHL_REG_1	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	D_SLOWV_COMP_HIGHL[10:8]		Upper momcap limit for SLOW VCO.	0x5	R/W
0x0117	FSC0	[7:4]	FSC_MIN_CTRL		Sets minimum FSC. (Paged by DDSM_MSK). fsc_min = code*(25/16) mA.	0x4	R/W
				0-15	fsc_min = code*(25/16) mA.		
		[3:2]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[1:0]	FSC_CTRL[1:0]	0-1023	Sets full-scale current(fsc), Paged by DDSM_MSK fsc = fsc_min + code*(25/1024) mA. fsc = fsc_min + code*(25/1024) mA.	0x0	R/W
0x0118	FSC1	[7:0]	FSC_CTRL[9:2]	0-1023	Sets full-scale current(fsc), Paged by DDSM_MSK fsc = fsc_min + code*(25/1024) mA. fsc = fsc_min + code*(25/1024) mA.	0x88	R/W
0x0140	DECODE_MODE	[7:5]	RESERVED		Reserved.	0x0	R
		4	MSB_MODE	0 1	MSB shuffle: enable shuffling (randomly selecting) active MSB segments for each new DAC sampling cycle. shuffle disabled. shuffle enabled.	0x0	R/W
		[3:1]	RESERVED		Reserved.	0x0	R
		0	ISB_MODE	0 1	ISB shuffle: enable shuffling (randomly selecting) active ISB segments for each new DAC sampling cycle. shuffle disabled. shuffle enabled.	0x0	R/W
0x0143	MSB_ROTATION	[7:6]	RESERVED		Reserved.	0x0	R
		5	MSB_ROTATION_EN		Enable MSB slow rotation: Whenever MSB_MODE = 1'b0 (no shuffling), enable MSB rotation by setting MSB_ROTATION_EN = 1 to reduce aging effects over device life. This bit will slowly rotate the pattern of MSBs to ensure equal aging and consistent performance over time. MSB_ROTATION_EN may remain set whether shuffle is enabled or disabled.	0x0	R/W
		[4:0]	MSB_ROTATION_SPD		speed control for MSB rotation. 0: fastest (DACCLK/64), 1: DACCLK/128, … , n: DACCLK/(64*2^n).	0x3	R/W
0x0180	ADC_DIVIDER_CTRL	7	SPI_SWAP_ADC_SYNC		Control bit needed as part of the one shot sync sequence along with PD_TXDIGCLK (0x0091[2]). See the SYSREF Setup/Sync Procedure section.	0x0	R/W
		[6:5]	RESERVED		Reserved.	0x0	R/W
		4	ADCDIVN_PD		Control power down of the ADC clock divider.	0x1	R/W
		[3:2]	RESERVED		Reserved.	0x0	R
		[1:0]	ADCDIVN_DIVRATIO_SPI	00 01 10 11	Control the divider ratio “L” for ADC clock. 0: div1. 1: div2. 2: div3. 3: div4.	0x0	R/W
0x0181	MUSHI_CTRL	[7:6]	RESERVED		Reserved.	0x0	R
		5	MUSHI_PD1_DUM		power down just the mushi dummy path generator for DAC 1.	0x0	R/W
		4	MUSHI_PD1		power down the whole mushi path for DAC 1.	0x0	R/W
		[3:2]	RESERVED		Reserved.	0x0	R
		1	MUSHI_PD0_DUM		power down just the mushi dummy path generator for dac 0.	0x0	R/W
		0	MUSHI_PD0		power down the whole mushi path for DAC 0.	0x0	R/W
0x0183	ENABLE_TIMING_CTRL_DAC0	[7:6]	RESERVED		Reserved.	0x0	R
		[5:4]	MUSHICLKEN_CTRL_DAC0		mushi and decoder clock enable control for DAC0:.	0x2	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				01	1: force clock off,.		
				10	2: force clock on.		
				else	0 or 3, let TXen SM control the clock enable,.		
		[3:2]	DECODERFORCEHIGH_CTRL_DAC0		Decoder force high control for DAC0:.	0x2	R/W
				01	1: force decoder output high,.		
				10	2: not force decoder high.		
				else	0 or 3, let TXen SM control decoder force high,.		
		[1:0]	SWDCLKEN_CTRL_DAC0		SWD clock enable control for DAC0:.	0x2	R/W
				01	1: force clock off.		
				10	2: force clock on.		
				else	0 or 3, let TXen SM control the clock enable.		
0x0184	ENABLE_TIMING_CTRL_DAC1	[7:6]	RESERVED		Reserved.	0x0	R
		[5:4]	MUSHICLKEN_CTRL_DAC1		mushi and decoder clock enable control for DAC1:.	0x2	R/W
				01	1: force clock off,.		
				10	2: force clock on.		
				else	0 or 3, let TXen SM control the clock enable,.		
		[3:2]	DECODERFORCEHIGH_CTRL_DAC1		Decoder force high control for DAC1:.	0x2	R/W
				01	1: force decoder output high,.		
				10	2: not force decoder high.		
				else	0 or 3, let TXen SM control decoder force high,.		
		[1:0]	SWDCLKEN_CTRL_DAC1		SWD clock enable control for DAC1:.	0x2	R/W
				01	1: force clock off,.		
				10	2: force clock on.		
				else	0 or 3, let TXen SM control the clock enable,.		
0x0185	ENABLE_TIMING_CTRL_GENERAL	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DLLCLK_ENCTRL		DLL clock enable control:.	0x2	R/W
				01	1: force clock off.		
				10	2: force clock on.		
				else	0 or 3, let TXen SM control the clock enable,.		
0x0187	HANDOFF_DEBUG	7	SELECTION_LSB7_DAC1		select data source for LSB7 for dac1. 0: real data; 1: pilot or parity bit.	0x0	R/W
		6	DATA_DEXOR_EN_DAC1		enable DAC data de-scramble in decoder for dac1.	0x0	R/W
		5	PARITY_CLEAR_DAC1		to clear parity results for dac1.	0x0	R/W
		4	PARITY_EN_DAC1		enable parity check for dac1.	0x0	R/W
		3	SELECTION_LSB7_DAC0		select data source for LSB7 for dac0. 0: real data; 1: pilot or parity bit.	0x0	R/W
		2	DATA_DEXOR_EN_DAC0		enable DAC data de-scramble in decoder for dac0.	0x0	R/W
		1	PARITY_CLEAR_DAC0		to clear parity results for dac0.	0x0	R/W
		0	PARITY_EN_DAC0		enable parity check for dac0.	0x0	R/W
0x0192	D2A_DCC_CODE_OVRD	7	D2ADCC_CODE_SEL		set to 1 to select manual dcc code.	0x0	R/W
		6	RESERVED		Reserved.	0x0	R/W
		[5:0]	D2ADCC_MANUAL_CODE		dcc manual code source.	0x0	R/W
0x0196	ADC_CLK_CTRL0	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	ADC_DRIVER_DATA_CTRL		The swing level of ADC clock driver can be adjusted, while the output impedance doesn't change.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0-20	0-20: Swing = 993mV - code*99mV. Note that swing can be negative (inverts clock).		
0x0198	CLK_CTRL1	[7:2]	RESERVED		Reserved.	0x0	R
		1	SEL_ADC_CLK_DRIVER		Reused bit. SYSREF input network control in single-ended mode, configure neg leg level. 0: SYSREFn must be pulled to 1V by user. 1: Pulls an internal reference to 1V. User need not drive SYSREFn.	0x0	R/W
				0	Direct DAC clock.		
				1	PLL clock.		
		0	PD_ADC_DRIVER		The ADC clock driver is powered down by setting this bit high.	0x1	R/W
0x019A	SYSREF_CTRL	7	RESERVED		Reserved.	0x0	R/W
		6	SYSREF_INPUTMODE		0: DC couple, 1: AC couple.	0x0	R/W
		[5:1]	RESERVED		Reserved.	0x0	R
		0	SYSREF_PD		Power down the SYSREF receiver and sync circuitry.	0x0	R/W
0x019E	SYSREF_CTRL2	[7:1]	RESERVED		Reserved.	0x0	R
		0	SYSREF_SAMPLE_TYPE		Clock, which samples SYSREF First.	0x0	R/W
				0	0 – SYSREF is sampled by Reference Clock and then by high speed clock.		
				1	1 – SYSREF is sampled directly by high speed clock.		
0x01A0	DDSC_DATAPATH_CFG	7	RESERVED		Reserved.	0x0	R
		6	DDSC_NCO_EN		DDSC NCO enable.	0x0	R/W
				0	Disable channel NCO.		
				1	Enable channel NCO.		
		[5:3]	RESERVED		Reserved.	0x0	R
		2	DDSC_MODULUS_EN		DDSC MODULUS enable.	0x0	R/W
				0	Disable modulus DDS.		
				1	Enable modulus DDS.		
		1	DDSC_SEL_SIDEBAND		Selects upper or lower sideband from modulation result.	0x0	R/W
				0	Use upper sideband.		
				1	Use lower sideband = spectral flip.		
		0	TEST_TONE_EN		Enable test tone generation by sending DC to input of channel DDS. Set the amplitude in the DC_OFFSET bitfield.	0x0	R/W
				0	Disable test tone generation.		
				1	Enable test tone generation.		
0x01A1	DDSC_FTW_UPDATE	[7:1]	RESERVED		Reserved.	0x0	R
		0	DDSC_FTW_LOAD_REQ		Frequency tuning word update request from SPI.	0x0	R/W
				1	0 to 1 transition loads the FTW and then autoclear this bit.		
0x01A2	DDSC_FTW0	[7:0]	DDSC_FTW[7:0]		Sets DDSC_FTW. ; If DDSC_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSC_FTW/2^48). If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x01A3	DDSC_FTW1	[7:0]	DDSC_FTW[15:8]		Sets DDSC_FTW. ; If DDSC_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSC_FTW/2^48). . If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48	0x0	R/W
0x01A4	DDSC_FTW2	[7:0]	DDSC_FTW[23:16]		Sets DDSC_FTW. ; If DDSC_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSC_FTW/2^48). If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01A5	DDSC_FTW3	[7:0]	DDSC_FTW[31:24]		Sets DDSC_FTW. ; If DDSC_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSC_FTW/2^48). If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01A6	DDSC_FTW4	[7:0]	DDSC_FTW[39:32]		Sets DDSC_FTW. ; If DDSC_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSC_FTW/2^48). If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01A7	DDSC_FTW5	[7:0]	DDSC_FTW[47:40]		Sets DDSC_FTW. ; If DDSC_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSC_FTW/2^48). If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01A8	DDSC_PHASE_OFFSET0	[7:0]	DDSC_NCO_PHASE_OFFSET[7:0]		Set channel NCO phase offset. Code is in 16-bit 2's complement. Degrees offset = 180*(code/2^15).	0x0	R/W
0x01A9	DDSC_PHASE_OFFSET1	[7:0]	DDSC_NCO_PHASE_OFFSET[15:8]		Set channel NCO phase offset. Code is in 16-bit 2's complement. Degrees offset = 180*(code/2^15).	0x0	R/W
0x01AA	DDSC_ACC_MODULUS0	[7:0]	DDSC_ACC_MODULUS[7:0]		Sets DDSC_ACC_MODULUS. If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01AB	DDSC_ACC_MODULUS1	[7:0]	DDSC_ACC_MODULUS[15:8]		Sets DDSC_ACC_MODULUS. If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01AC	DDSC_ACC_MODULUS2	[7:0]	DDSC_ACC_MODULUS[23:16]		Sets DDSC_ACC_MODULUS.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.		
0x01AD	DDSC_ACC_MODULUS3	[7:0]	DDSC_ACC_MODULUS[31:24]		Sets DDSC_ACC_MODULUS. If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01AE	DDSC_ACC_MODULUS4	[7:0]	DDSC_ACC_MODULUS[39:32]		Sets DDSC_ACC_MODULUS. If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01AF	DDSC_ACC_MODULUS5	[7:0]	DDSC_ACC_MODULUS[47:40]		Sets DDSC_ACC_MODULUS. If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01B0	DDSC_ACC_DELTA0	[7:0]	DDSC_ACC_DELTA[7:0]		Sets DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01B1	DDSC_ACC_DELTA1	[7:0]	DDSC_ACC_DELTA[15:8]		Sets DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01B2	DDSC_ACC_DELTA2	[7:0]	DDSC_ACC_DELTA[23:16]		Sets DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01B3	DDSC_ACC_DELTA3	[7:0]	DDSC_ACC_DELTA[31:24]		Sets DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01B4	DDSC_ACC_DELTA4	[7:0]	DDSC_ACC_DELTA[39:32]		Sets DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01B5	DDSC_ACC_DELTA5	[7:0]	DDSC_ACC_DELTA[47:40]		Sets DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSC_FTW + DDSC_ACC_DELTA/DDSC_ACC_MODULUS) / 2^48.	0x0	R/W
0x01B6	DC_OFFSET0	[7:0]	DC_OFFSET[7:0]		DC test tone amplitude. This amplitude goes to both I and Q paths - set to 0x7fff for a full-scale tone (ensure TEST_TONE_EN==1).	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x01B7	DC_OFFSET1	[7:0]	DC_OFFSET[15:8]		DC test tone amplitude. This amplitude goes to both I and Q paths - set to 0x7fff for a full-scale tone (ensure TEST_TONE_EN==1).	0x0	R/W
0x01B8	CHNL_GAIN0	[7:0]	CHNL_GAIN[7:0]		CHNL_GAIN 12bit for each chan. 0-4095: Channel gain = code/2^11.	0x8	R/W
				0-4095	Channel gain = code/2^11.		
0x01B9	CHNL_GAIN1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CHNL_GAIN[11:8]		CHNL_GAIN 12bit for each chan. 0-4095: Channel gain = code/2^11.	0x0	R/W
				0-4095	Channel gain = code/2^11.		
0x01C6	CHNL_SKEW_ADJUST	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CHNL_SKEW_ADJ		channels skew adjustment, which is used to give a relative skew between different channels. User can get a delay of -4 to +4 modulator clock, which is fs/(post_interp*4) with respect to each other channel. Bit 3 is used to indicate a negative delay. To achieve -3 delay user programs 11 ('b1011). For 8xNx mode, only positive delay is supported.	0x0	R/W
				1	1=invert.		
0x01C7	CHNL_NCO_SYNC	[7:0]	NCO_SYNC_CHNL_SEL		select NCO sync channel.	0x0	R/W
0x01C8	MAINDP_DAC_1XXX_ENABLES	7	MAINDP_DAC_1XXX_EN_SPI		enable the SPI configured maindp_dac crossbar enables, or else the design uses the hard coded one.	0x0	R/W
		[6:4]	RESERVED		Reserved.	0x0	R
		[3:0]	MAINDP_DAC_1XXX_ENABLES		crossbar enables for 1x1x or 1x-non1x modes when maindp_dac_1xx_en_spi is set to 1. This is a two-dimension array, and the first dimension is decided by DAC page. Example like …	0x0	R/W
				00	maindp_dac_1xxx_enables[0][3:0] decides which maindp goes to DAC0,.		
				01	maindp_dac_1xxx_enables[1][3:0] decides which maindp goes to DAC1,.		
				10	maindp_dac_1xxx_enables[2][3:0] decides which maindp goes to DAC2,.		
				11	maindp_dac_1xxx_enables[3][3:0] decides which maindp goes to DAC3.		
				--	If maindp_dac_1xxx_enables[1][3:0]=4'b1000, it means maindp3 goes to DAC1.		
0x01C9	DDSM_DATAPATH_CFG	7	RESERVED		Reserved.	0x0	R
		6	EN_CMPLX_MODULATION		Enable complex modulation from main/final DDS. Real output only when set to 0.	0x0	R/W
				0	Channel NCOs reset or update their FTW based on channel NCO update requests.		
				1	Channel NCOs reset or update their FTW based on main datapath NCO update requests.		
		[5:4]	DDSM_MODE		Mod switch mode. Paged using MODS_MSK.	0x0	R/W
				00	I output from each datapath NCO goes to its respective DAC.		
				01	Sum of I inputs to each datapath NCO is divided by 2 then sent to DAC 0. Sum of Q inputs to each datapath NCO is divided by 2 then sent to DAC 1. The datapath NCOs themselves are bypassed.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				11	Sum of I outputs from each datapath NCO is divided by 2 then sent to DAC 0. DAC 1 is not used and its output is tied to midscale.		
		3	DDSM_NCO_EN		DDSM NCO enable.	0x0	R/W
				0	0: Disable main datapath NCO.		
				1	1: Enable main datapath NCO.		
		2	DDSM_MODULUS_EN		DDSM modulus enable.	0x0	R/W
				0	0: Disable modulus DDS.		
				1	1: Enable modulus DDS.		
		1	DDSM_SEL_SIDEBAND		Selects upper or lower sideband from modulation result.	0x0	R/W
				0	0: Use upper sideband.		
				1	1: Use lower sideband = spectral flip.		
		0	RESERVED		Reserved.	0x0	R
0x01CA	DDSM_FTW_UPDATE	[7:1]	RESERVED		Reserved.	0x0	R
		0	DDSM_FTW_LOAD_REQ		Frequency tuning word update request from SPI.	0x0	R/W
				1	1: 0 to 1 transition loads the FTW and then autoclear this bit.		
0x01CB	DDSM_FTW0	[7:0]	DDSM_FTW[7:0]		Sets DDSM_FTW. If DDSM_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSM_FTW/2^48). If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01CC	DDSM_FTW1	[7:0]	DDSM_FTW[15:8]		Sets DDSM_FTW. If DDSM_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSM_FTW/2^48). If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01CD	DDSM_FTW2	[7:0]	DDSM_FTW[23:16]		Sets DDSM_FTW. If DDSM_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSM_FTW/2^48). If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01CE	DDSM_FTW3	[7:0]	DDSM_FTW[31:24]		Sets DDSM_FTW. If DDSM_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSM_FTW/2^48). If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01CF	DDSM_FTW4	[7:0]	DDSM_FTW[39:32]		Sets DDSM_FTW. If DDSM_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSM_FTW/2^48). If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					+ DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.		
0x01D0	DDSM_FTW5	[7:0]	DDSM_FTW[47:40]		Sets DDSM_FTW. If DDSM_MODULUS_EN is low, main datapath NCO frequency = FDAC * (DDSM_FTW/2^48). If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01D1	DDSM_PHASE_OFFSET0	[7:0]	DDSM_NCO_PHASE_OFFSET[7:0]		Set main datapath NCO phase offset. Code is in 16-bit 2's complement. Degrees offset = 180*(code/2^15).	0x0	R/W
0x01D2	DDSM_PHASE_OFFSET1	[7:0]	DDSM_NCO_PHASE_OFFSET[15:8]		Set main datapath NCO phase offset. Code is in 16-bit 2's complement. Degrees offset = 180*(code/2^15).	0x0	R/W
0x01D3	DDSM_ACC_MODULUS0	[7:0]	DDSM_ACC_MODULUS[7:0]		Sets DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01D4	DDSM_ACC_MODULUS1	[7:0]	DDSM_ACC_MODULUS[15:8]		Sets DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01D5	DDSM_ACC_MODULUS2	[7:0]	DDSM_ACC_MODULUS[23:16]		Sets DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01D6	DDSM_ACC_MODULUS3	[7:0]	DDSM_ACC_MODULUS[31:24]		Sets DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01D7	DDSM_ACC_MODULUS4	[7:0]	DDSM_ACC_MODULUS[39:32]		Sets DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01D8	DDSM_ACC_MODULUS5	[7:0]	DDSM_ACC_MODULUS[47:40]		Sets DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01D9	DDSM_ACC_DELTA0	[7:0]	DDSM_ACC_DELTA[7:0]		Sets DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01DA	DDSM_ACC_DELTA1	[7:0]	DDSM_ACC_DELTA[15:8]		Sets DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					+ DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.		
0x01DB	DDSM_ACC_DELTA2	[7:0]	DDSM_ACC_DELTA[23:16]		Sets DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01DC	DDSM_ACC_DELTA3	[7:0]	DDSM_ACC_DELTA[31:24]		Sets DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01DD	DDSM_ACC_DELTA4	[7:0]	DDSM_ACC_DELTA[39:32]		Sets DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01DE	DDSM_ACC_DELTA5	[7:0]	DDSM_ACC_DELTA[47:40]		Sets DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, main datapath NCO frequency = FDAC * (DDSM_FTW + DDSM_ACC_DELTA/DDSM_ACC_MODULUS) / 2^48.	0x0	R/W
0x01E0	MAIN_DC_OFFSET0	[7:0]	DC_OFST[7:0]		used for main dp DC ofset.	0x0	R/W
0x01E1	MAIN_DC_OFFSET1	[7:0]	DC_OFST[15:8]		used for main dp DC ofset.	0x0	R/W
0x01E5	DDSM_CAL_FTW0	[7:0]	DDSM_CAL_FTW[7:0]		FTW of the calibration accumulator.	0x0	R/W
0x01E6	DDSM_CAL_FTW1	[7:0]	DDSM_CAL_FTW[15:8]		FTW of the calibration accumulator.	0x0	R/W
0x01E7	DDSM_CAL_FTW2	[7:0]	DDSM_CAL_FTW[23:16]		FTW of the calibration accumulator.	0x0	R/W
0x01E8	DDSM_CAL_FTW3	[7:0]	DDSM_CAL_FTW[31:24]		FTW of the calibration accumulator.	0x0	R/W
0x01E9	DDSM_CAL_MODE_DEF	[7:3]	RESERVED		Reserved.	0x0	R
		2	DDSM_EN_CAL_ACC	0 1	Enable clock cal accumulator. 0: Disable that is, do not clock the cal frequency accumulator. 1: Enable that is, turn on the clock to the cal frequency accumulator.	0x0	R/W
		1	DDSM_EN_CAL_DC_INPUT	0 1	Enable DC input to cal DDS. 0: Mux in datapath signal to the input of the final DDS. 1: Mux in DC to the input of the final DDS.	0x0	R/W
		0	DDSM_EN_CAL_FREQ_TUNE	0 1	Enable tuning of the signal to cal frequency. 0: Disable cal frequency tuning. 1: Enable cal frequency tuning.	0x0	R/W
0x01F0	MAINDP_ENABLE	[7:4]	DAC_MAINDP_EN		enable bits of maindp/dac when SPI maindp enable is set to 1.	0xF	R/W
		3	RESERVED		Reserved.	0x0	R
		[2:1]	HB3_90bandwidth_EN		enable the 90% BW HB3 filter.	0x0	R
		0	RESERVED		Reserved.	0x0	R
0x01F1	TXEN_ROUTE_CTRL	[7:0]	TXEN_ROUTE_CTRL		txen route control when en_txen_flexible_route bit is 1. When 4 txen pins (two dedicate txen pin and two GPIOs) are used, these bits are used to map these 4 physical pins to logical txen pins.	0xE4	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					When Bits[7:6] are 2'b11: logical txen 3 will from txen GPIO1;. When Bits[1:0] are 2'b10: logical txen 0 will from txen pin 1;. When Bits[5:4] are 2'b10: logical txen 2 will from txen pin 1;. When Bits[5:4] are 2'b01: logical txen 2 will from txen GPIO0;. When Bits[5:4] are 2'b11: logical txen 2 will from txen GPIO1;. When Bits[7:6] are 2'b01: logical txen 3 will from txen GPIO0;. When Bit [7:6] are 2'b10: logical txen 3 will from txen pin 1;. When Bits[7:6] are 2'b00: logical txen 3 will from txen pin 0;. When Bits[5:4] are 2'b00: logical txen 2 will from txen pin 0;. When Bits[1:0] are 2'b01: logical txen 0 is from txen GPIO0;. When Bits[1:0] are 2'b00: logical txen 0 will from txen pin 0;. When Bits[3:2] are 2'b11: logical txen 1 will from txen GPIO1;. When Bits[1:0] are 2'b11: logical txen 0 will from txen GPIO1;. When Bits[3:2] are 2'b01: logical txen 1 will from txen GPIO0;. When Bit [3:2] are 2'b10: logical txen 1 will from txen pin 1;. When Bits[3:2] are 2'b00: logical txen 1 will from txen pin 0;.		
0x01F2	TX_ENABLE0	[7:5]	RESERVED		Reserved.	0x0	R
		4	EN_TXEN_FLEXIBLE_ROUTE		enable flexible txen route	0x0	R/W
		3	TXEN_DAC_FSC3		Selects what full-scale current bitfields to use when TX_EN1 is low.	0x0	R/W
		2	TXEN_DAC_FSC2		Selects what full-scale current bitfields to use when TX_EN1 is low.	0x0	R/W
		1	TXEN_DAC_FSC1		Selects what full-scale current bitfields to use when TX_EN1 is low.	0x0	R/W
				0	Use FSC (registers 0x59 and 0x5A).		
				1	Use TXENB_FSC (registers 0x72 and 0x73).		
		0	TXEN_DAC_FSC0		Selects what full-scale current bitfields to use when TX_EN0 is low.	0x0	R/W
				0	Use FSC (registers 0x59 and 0x5A).		
				1	Use TXENB_FSC (registers 0x72 and 0x73).		
0x01F3	TX_ENABLE1	7	ANA_FSC_ENABLE_SELECT		Newly added in TXFE, default(0) is sel txdac_on, else sel txen	0x0	R/W
		[6:0]	RESERVED		Reserved.	0x0	R
0x01FB	DATAPATH_NCO_SYNC_CFG	[7:4]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		3	EN_SYNC_ALL_CHNL_NCO_RESETS	0 1	Selects whether the channel NCOs are reset in response to a reset request or FTW update request to the main datapath NCO. Note that when this bit is enabled, registers 0x0203 and 0x0204 control which NCOs are reset in response to an alignment edge; when this bit is disabled only the main NCOs is reset. This bit is paged by DACPAGE_MSK. Channel NCOs reset or update their FTW based on channel NCO update requests. Channel NCOs reset or update their FTW based on main datapath NCO update requests.	0x1	R
		2	RESERVED		Reserved.	0x0	R
		1	ALL_NCO_SYNC_ACK		Used to signal ack that all the active nco's have been loaded.	0x0	R
		0	START_NCO_SYNC		Generates an internal trigger signal to sync the NCOs on the rising edge, if the NCOs are reset using SPI (not SYSREF or LMFC). This bit must be toggled from 0 to 1, and is paged by DACPAGE_MSK.	0x0	R/W
0x01FE	JESD_MODE	7	MODE_NOT_IN_TABLE		Programmed JESD_MODE and INTERP_MODE combination is not correct.	0x0	R
		6	COM_SYNC		Combine SYNCBs in dual link case.	0x0	R/W
		[5:0]	JESD_MODE		Quick configuration setting for JESD204B/C receiver parameters according to the JESD204B or C Mode column in the “DAC Path Supported JESD204B Modes” or “ DAC Path Supported JESD204C Modes” tables.	0x0	R/W
0x01FF	INTRP_MODE	[7:4]	COARSE_INTERP_SEL[3:0]	0001 0010 0100	Sets main datapath (coarse) interpolation rate. See mode table for usage and compatible JESD modes/ channel interpolation rates. Valid settings are 1, 2, 4, 6, 8, 12. 1 = no interpolation. 2 = 2x interpolation. 4 = 4x interpolation, etc.	0x8	R/W
		[3:0]	FINE_INTERP_SEL[3:0]	0001 0010 0100	Sets channel (fine) interpolation rate. See mode table for usage and compatible JESD modes/main datapath interpolation rates. Valid settings are 1, 2, 3, 4, 6, 8. 1 = no interpolation. 2 = 2x interpolation. 4 = 4x interpolation, etc.	0x4	R/W
0x0201	DIG_RESET	[7:1]	RESERVED		Reserved.	0x0	R
		0	DIG_RESET	0 1	Async Reset for all the digital logic. Includes JESD digital, digital clock generation, digital datapath. Normal operating mode. Reset the digital logic.	0x1	R/W
0x0203	MAIN_NCO_RST_EN	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	SPI_MAIN_NCO_RST_EN	0 1	Enable Reset Mode for Main Datapath NCOs. DATAPATH_NCO_SYNC_CFG[3] must be high as well to enable resetting. 0: Disable NCO resetting. 1: Enable NCO resetting on nco reset events.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0204	CHNL_NCO_RST_EN	[7:0]	SPI_CHNL_NCO_RST_EN		Enable Reset Mode for Channel NCOs. DATAPATH_NCO_SYNC_CFG[3] must be high as well to enable resetting.	0x0	R/W
				0	0: Disable NCO resetting.		
				1	1: Enable NCO resetting on nco reset events.		
0x0205	ALIGN_STS	[7:3]	RESERVED		Reserved.	0x0	R
		2	ALIGN_ARM		Transition low to high triggers an internal NCO reset signal, on the next received SYSREF pulse.	0x0	R/W
		[1:0]	RESERVED		Reserved.	0x0	R/W
0x0210	DAC_SUPPLY_MONITOR	[7:6]	RESERVED		Reserved.	0x0	R
		5	DAVDD_DAC01_MON1		DAC0/DAC1 1V mushi supply monitor.	0x0	R
		4	DAVDD_DAC23_MON1		DAC2/DAC3 1V mushi supply monitor.	0x0	R
		3	DVDD_DAC01_MON1		DAC0/DAC1 1V supply monitor.	0x0	R
		2	DVDD_DAC23_MON1		DAC2/DAC3 1V supply monitor.	0x0	R
		1	AVDD_DAC01_MON2		DAC0/DAC1/BG 2V supply monitor.	0x0	R
		0	AVDD_DAC23_MON2		DAC2/DAC3 2V supply monitor.	0x0	R
0x0211	CLOCK_SUPPLY_MONITOR	[7:4]	RESERVED		Reserved.	0x0	R
		3	REF_UP_CLOCK_MON1		SERDES Reference/uP clock supply monitor.	0x0	R
		2	HS_CLOCK_MON1		Clock high speed supply monitor.	0x0	R
		1	LS_CLOCK_MON1		Clock low speed supply monitor.	0x0	R
		0	DACPLLVDD_MON2		DAC PLL 2V supply monitor.	0x0	R
0x0212	ADC0_SUPPLY_MONITOR	[7:5]	RESERVED		Reserved.	0x0	R
		4	ADC0_REF_MON2		ADC0 reference 2V supply monitor.	0x0	R
		3	ADC0_REFADC_MON1		ADC0 refadc 1V supply monitor.	0x0	R
		2	ADC0_BUF_MON1		ADC0 1V/2V buffer supply monitor.	0x0	R
		1	ADC0_CORE_MON1		ADC0 1V pipe supply monitor.	0x0	R
		0	ADC0_CLK_MON1		ADC0 1V clock supply monitor.	0x0	R
0x0213	ADC1_SUPPLY_MONITOR	[7:5]	RESERVED		Reserved.	0x0	R
		4	ADC1_REF_MON2		ADC1 reference 2V supply monitor.	0x0	R
		3	ADC1_REFADC_MON1		ADC1 refadc 1V supply monitor.	0x0	R
		2	ADC1_BUF_MON1		ADC1 1V/2V buffer supply monitor.	0x0	R
		1	ADC1_CORE_MON1		ADC1 1V pipe supply monitor.	0x0	R
		0	ADC1_CLK_MON1		ADC1 1V clock supply monitor.	0x0	R
0x0280	ADC_COARSE_CB	[7:4]	C_MXR_IQ_SFL		Bits to Configure IQ Input Shuffling at the Coarse DDC Inputs. There are four bits, one for each of the CDDCs Bit0 controls CDDC0 Bit1 controls CDDC1 Bit2 controls CDDC2 Bit3 controls CDDC3 For each CDDC, the functionality is:	0x0	R/W
				0	0 -> no IQ shuffle.		
				1	1 -> shuffle I-Q at the input of CDDCx.		
		[3:0]	ADC_COARSE_CB		Bits to Configure ADC to Coarse DDC Crossbar. Settings 00 and 01 are applicable to devices with 4 ADCs. Settings 10 and 11 are applicable to devices with 2 ADCs. Apart from these settings, the required COARSE_DDCs should be enabled	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					in COARSE_DDC_EN register. Bits 2 and 3 are reserved. 00 - Quad ADC Real Mode - The four ADC connects to four Coarse DDCs. (With PFILT Cross bar, there any ADC can connect to any DDC). 01 - Quad ADC Complex Mode - There are two IQ pairs. One pair connects to Coarse DDC 0 and 1. Another pair connects to Coarse DDC 2 and 3. 10 - Dual ADC Real Mode - One ADC connects to Coarse DDC0 and 2. Another ADC connects to Coarse DDC1 and 3. 11 - Dual ADC Complex Mode - There is one IQ pair. That single pair connects to all four Coarse DDCs. Apart from these settings, the required COARSE_DDCs should be enabled in COARSE_DDC_EN register. Bits 2 and 3 are reserved.		
0x0281	COARSE_FINE_CB	[7:0]	COARSE_FINE_CB		Bits to Configure Coarse to Fine DDC Crossbar. Apart from below settings, the required Fine DDCs should be enabled in FINE_DDC_EN register. Bit[0] - 0 connects Coarse DDC1 to Fine DDC1 and 1 connects Coarse DDC2 to Fine DDC1. Bit[1] - 0 connects Coarse DDC1 to Fine DDC2 and 1 connects Coarse DDC2 to Fine DDC2. Bit[2] - 0 connects Coarse DDC1 to Fine DDC3 and 1 connects Coarse DDC2 to Fine DDC3. Bit[3] - 0 connects Coarse DDC1 to Fine DDC4 and 1 connects Coarse DDC2 to Fine DDC4. Bit[4] - 0 connects Coarse DDC3 to Fine DDC5 and 1 connects Coarse DDC4 to Fine DDC5. Bit[5] - 0 connects Coarse DDC3 to Fine DDC6 and 1 connects Coarse DDC4 to Fine DDC6. Bit[6] - 0 connects Coarse DDC3 to Fine DDC7 and 1 connects Coarse DDC4 to Fine DDC7. Bit[7] - 0 connects Coarse DDC3 to Fine DDC8 and 1 connects Coarse DDC4 to Fine DDC8.	0x0	R/W
0x0282	COARSE_DEC_CTRL	[7:6]	COARSE_MXR_IF		Coarse Mixer Modes. DDC Intermediate Frequency (IF) Mode. 00:Variable IF Mode: Mixers and NCO enabled. ddc_phase_inc can be used to digitally tune the IF frequency. 01: 0 Hz IF Mode: Mixers bypassed and NCO disabled. Since input is real ddc_c2r_en is restricted to be zero in this case. 10: Fs/4 Hz IF Mode: Mixers and NCO enabled in special down-mixing by Fs/4 mode. 11: Test Mode: Input samples are forced to +0.999… (+FS). NCO is enabled. This test mode allows the NCO's to directly drive the decimation filters and is useful when evaluating the performance of the NCOs and decimation filters.	0x0	R/W
		5	COARSE_GAIN		Enables/Disables 6dB Gain in Final HB1 Stage. 0 - 6dB gain not enabled in Coarse stage HB1.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				1	1- 6dB gain enabled in Coarse stage HB1.		
		4	COARSE_C2R_EN		Enables/Disables Complex to Real Conversion. 0 - Complex to Real not enabled 1- Complex to Real enabled Note that C2R should not be enabled if decimation value selected are 1,3,6 For other modes C2R should be enabled only if coarse stage output is directly going out of the DDC bypassing fine stage	0x0	R/W
		[3:0]	COARSE_DEC_SEL		Bits to Configure Coarse DDC Decimation. 0000 - Decimate by 2 0001 - Decimate by 4 0101 - Decimate by 6 1000 - Decimate by 3 1100 - Decimate by 1 These represent complex decimation. When C2R is enabled, decimation becomes half. For example: 0001 would become decimate by 2.	0x0	R/W
0x0283	FINE_DEC_CTRL	[7:6]	FINE_MXR_IF		Fine Mixer Modes. DDC Intermediate Frequency (IF) Mode. 00:Variable IF Mode: Mixers and NCO enabled. ddc_phase_inc can be used to digitally tune the IF frequency. 01: 0 Hz IF Mode: Mixers bypassed and NCO disabled. Since input is real ddc_c2r_en is restricted to be zero in this case. 10: Fs/4 Hz IF Mode: Mixers and NCO enabled in special down-mixing by Fs/4 mode. 11: Test Mode: Input samples are forced to +0.999… (+FS). NCO is enabled. This test mode allows the NCO's to directly drive the decimation filters and is useful when evaluating the performance of the NCOs and decimation filters.	0x0	R/W
				00			
				01			
				10			
				11			
		5	FINE_GAIN		Enables/Disables 6dB Gain in Final HB1 Stage.	0x0	R/W
				0	0: - 6dB gain not enabled in Fine stage HB1.		
				1	1: - 6dB gain enabled in Fine stage HB1.		
		4	FINE_C2R_EN		Enables/Disables Complex to Real Conversion. 0 - Complex to Real not enabled 1 - Complex to Real enabled C2R should not be enabled for decimation of 3,6,12 and 24	0x0	R/W
		3	RESERVED		Reserved.	0x0	R
		[2:0]	FINE_DEC_SEL		Bits to Configure Fine DDC Decimation. These represents complex decimation. When C2R is enabled, decimation becomes half. for example: 0001 would become decimate by 2.	0x0	R/W
				000	000 - Decimate by 2.		
				001	001 - Decimate by 4.		
				010	010 - Decimate by 8.		
				011	011 - Decimate by 16.		
				100	100 - Decimate by 3.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				101 110 111	101 - Decimate by 6. 110 - Decimate by 12. 111 - Decimate by 24.		
0x0284	DDC_OVERALL_DECIM	[7:0]	DDC_OVERALL_DECIM		End to End "overall" Decimation. Indicates the overall decimation value for every Fine DDC ==> Coarse DDC Decimation * Fine DDC Decimation. . Example if Coarse decimation is 6 and Fine decimation is 8, 48 is programmed in this register. If C2R is enabled, then overall decimation is, (Coarse Decimation * Fine Decimation) / 2 Example if Coarse decimation is 6 and Fine decimation is 8 and C2R enabled, 24 is programmed in this register.	0x0	R/W
0x0285	COARSE_DDC_EN	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	COARSE_DDC_EN		Enables/Disables Coarse DDCs. Bit[3] - "1" Enables Coarse DDC4 and "0" Disables Coarse DDC4. Bit[2] - "1" Enables Coarse DDC3 and "0" Disables Coarse DDC3. Bit[1] - "1" Enables Coarse DDC2 and "0" Disables Coarse DDC2. Bit[0] - "1" Enables Coarse DDC1 and "0" Disables Coarse DDC1.	0x0	R/W
0x0286	FINE_DDC_EN	[7:0]	FINE_DDC_EN		Enables/Disables Fine DDCs. Bit[6] - "1" Enables Fine DDC7 and "0" Disables Fine DDC7. Bit[5] - "1" Enables Fine DDC6 and "0" Disables Fine DDC6. Bit[7] - "1" Enables Fine DDC8 and "0" Disables Fine DDC8. Bit[4] - "1" Enables Fine DDC5 and "0" Disables Fine DDC5. Bit[3] - "1" Enables Fine DDC4 and "0" Disables Fine DDC4. Bit[0] - "1" Enables Fine DDC1 and "0" Disables Fine DDC1. Bit[2] - "1" Enables Fine DDC3 and "0" Disables Fine DDC3. Bit[1] - "1" Enables Fine DDC2 and "0" Disables Fine DDC2.	0x0	R/W
0x0287	FINE_BYPASS	[7:0]	FINE_BYPASS		Bypasses Fine Stage DDC. Bit[0] - "1" Bypasses the entire fine DDC1, and final output is from preceding coarse stage DDC and "0" Fine DDC1 is not bypassed (Provided it is enabled in Fine_DDC_EN register). Bit[1] - "1" Bypasses the entire fine DDC2, and final output is from preceding coarse stage DDC and "0" Fine DDC2 is not bypassed (Provided it is enabled in Fine_DDC_EN register). Bit[2] - "1" Bypasses the entire fine DDC3, and final output is from preceding coarse stage DDC and "0" Fine DDC3 is not bypassed (Provided it is enabled in Fine_DDC_EN register).	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					Bit[3] - "1" Bypasses the entire fine DDC4, and final output is from preceding coarse stage DDC and "0" Fine DDC4 is not bypassed (Provided it is enabled in Fine_DDC_EN register). Bit[4] - "1" Bypasses the entire fine DDC5, and final output is from preceding coarse stage DDC and "0" Fine DDC5 is not bypassed (Provided it is enabled in Fine_DDC_EN register). Bit[5] - "1" Bypasses the entire fine DDC6, and final output is from preceding coarse stage DDC and "0" Fine DDC6 is not bypassed (Provided it is enabled in Fine_DDC_EN register). Bit[6] - "1" Bypasses the entire fine DDC7, and final output is from preceding coarse stage DDC and "0" Fine DDC7 is not bypassed (Provided it is enabled in Fine_DDC_EN register). Bit[7] - "1" Bypasses the entire fine DDC8, and final output is from preceding coarse stage DDC and "0" Fine DDC8 is not bypassed (Provided it is enabled in Fine_DDC_EN register).		
0x0289	CHIP_DECIMATION_RATIO	[7:0]	CHIP_DECIMATION_RATIO		Chip Decimation Ratio. Chip Decimation Ratio. There are two chip_decimation_ratio registers (Two pages corresponding to two links) Within a link, all the DDCs should have same data rate. When DDCs are programmed to have different decimation (within same link), then rates are different. Finally before entering the JTX, DDC rates must match. chip_decimation_ratio register is defined for this purpose which holds the least decimation value across the DDCs (in a given link). All the DDCs are "up-sampled" as per chip_decimation_ratio register so that final data rates of DDCs are matching and the rate correspond to chip_decimation_ratio. (If any DDC is already matching ratio chip_decimation_ratio then up-sampling is not done for that DDC). Programming guideline: For example in a test, if Coarse0 and Fine0 are connected and their respective decimation are 4 and 8, the total decimation is 32. This 32 has to be written to ddc_overall_decimation register of Fine0. In the same test if Coarse1 and Fine1 are connected and their respective decimation are 4 and 4, the total decimation is 16. This 16 has to be written to ddc_overall_decimation register of Fine1. Assume these are the only DDCs programmed and both belong to link0.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					Now in Chip Decimation Ratio register of link0 we have to write 16. (As 16 is the least overall decimation among DDCs present in link0). There is no encoding in chip decimation ratio register and ddc_overall_decimation registers of Fine DDC. Decimation value has to be directly programmed in those registers. In case if C2R is enabled, then total_decimation/2 has to be programmed in those registers. (Again least value to be programmed in chip decimation ratio register).		
0x028A	COMMON_HOP_EN	[7:1]	RESERVED		Reserved.	0x0	R
		0	COMMON_HOP_EN		Common Hop Enable. When this bit is enabled and gpio based hopping is selected, frequency hopping is done at the same time for all the Coarse DDC NCOs bypassing the profile_pins[5:4]. When this bit is disabled and gpio based hopping is selected, frequency hopping is done for the Coarse DDC NCO selected by profile_pins[5:4].	0x0	R/W
0x02A1	CTRL_0_1_SEL	[7:4]	DFORMAT_CTRL_BIT_1_SEL		Control Bit 1 Mux Selection. Converter Control Bit 1 Selection.	0x0	R/W
				0000	0x0: Overrange Bit.		
				0001	0x1: Tie low (1'b0).		
				0010	0x2: Signal Monitor (SMON) Bit.		
				0011	0x3: Fast Detect (FD) Bit.		
				0100	0x4: Reserved.		
				0101	0x5: SYSREF.		
				0110	0x6: Reserved.		
				0111	0x7: Reserved.		
				1000	0x8: NCO Channel Selection Bit 0.		
				1001	0x9: NCO Channel Selection Bit 1.		
				1010	0xA: NCO Channel Selection Bit 2.		
				1011	0xB: NCO Channel Selection Bit 3.		
		[3:0]	DFORMAT_CTRL_BIT_0_SEL		Control Bit 0 Mux Selection. Converter Control Bit 0 Selection.	0x0	R/W
				0000	0x0: Overrange Bit.		
				0001	0x1: Tie low (1'b0).		
				0010	0x2: Signal Monitor (SMON) Bit.		
				0011	0x3: Fast Detect (FD) Bit.		
				0100	0x4: Reserved.		
				0101	0x5: SYSREF.		
				0110	0x6: Reserved.		
				0111	0x7: Reserved.		
				1000	0x8: NCO Channel Selection Bit 0.		
				1001	0x9: NCO Channel Selection Bit 1.		
				1010	0xA: NCO Channel Selection Bit 2.		
				1011	0xB: NCO Channel Selection Bit 3.		
0x02A2	CTRL_2_SEL	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	DFORMAT_CTRL_BIT_2_SEL		Control Bit 2 Mux Selection. Converter Control Bit 2 Selection.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0000	0x0: Overrange Bit.		
				0001	0x1: Tie low (1'b0).		
				0010	0x2: Signal Monitor (SMON) Bit.		
				0011	0x3: Fast Detect (FD) Bit.		
				0100	0x4: Reserved.		
				0101	0x5: SYSREF.		
				0110	0x6: Reserved.		
				0111	0x7: Reserved.		
				1000	0x8: NCO Channel Selection Bit 0.		
				1001	0x9: NCO Channel Selection Bit 1.		
				1010	0xA: NCO Channel Selection Bit 2.		
				1011	0xB: NCO Channel Selection Bit 3.		
0x02A3	OUT_FORMAT_SEL	[7:3]	RESERVED		Reserved.	0x0	R
		2	DFORMAT_INV		Output Data Inversion Enable. Digital ADC Sample Invert.	0x0	R/W
				0	0: ADC sample data is NOT inverted.		
				1	1: ADC sample data is inverted.		
		[1:0]	DFORMAT_SEL		Output Data Format Selection. Digital ADC Data Format Select (DFS).	0x0	R/W
				00	00: 2's complement (default).		
				01	01: Offset Binary.		
				10	10: Gray Code.		
				11	11: Reserved.		
0x02A4	OVR_CLR_0	[7:0]	DFORMAT_OVR_CLR[7:0]		Overrange Status Clear. Converter Over-range Clear bit(active high) Once an Over-range sticky bit has been set, it remains set until explicitly cleared by writing a "1" to the corresponding dformat_ovr_clear[15:0] bit . The dformat_ovr_clear[15:0] bit must be cleared for further overrange to be reported . [0] = Over-range Sticky bit clear for converter 0 [1] = Over-range Sticky bit clear for converter 1 [2] = Over-range Sticky bit clear for converter 2 etc.	0x0	R/W
0x02A5	OVR_CLR_1	[7:0]	DFORMAT_OVR_CLR[15:8]		Overrange Status Clear. Converter Over-range Clear bit(active high) Once an Over-range sticky bit has been set, it remains set until explicitly cleared by writing a "1" to the corresponding dformat_ovr_clear[15:0] bit . The dformat_ovr_clear[15:0] bit must be cleared for further overrange to be reported . [0] = Over-range Sticky bit clear for converter 0 [1] = Over-range Sticky bit clear for converter 1 [2] = Over-range Sticky bit clear for converter 2 etc.	0x0	R/W
0x02A6	OVR_STATUS_0	[7:0]	DFORMAT_OVR_STATUS[7:0]		Output Overrange Status Indicator. Converter Over-range Indication Sticky Bits (active high) . One bit for each virtual converter 0: No Over-Range has occurred 1: Over-Range has occurred This bit is set to "1" if converter is driven beyond the specified input range. It is "sticky," i.e., it remains set until explicitly cleared by writing a "1" to the corresponding dformat_ovr_clear[15:0] bit . The corresponding dformat_ovr_clear[15:0] bit would need to be cleared for further overflows to be	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					reported [0] = Over-range Sticky bit for converter 0 [1] = Over-range Sticky bit for converter 1 [2] = Over-range Sticky bit for converter 2 etc.		
0x02A7	OVR_STATUS_1	[7:0]	DFORMAT_OVR_STATUS[15:8]		Output Overrange Status Indicator. Converter Over-range Indication Sticky Bits (active high) . One bit for each virtual converter 0: No Over-Range has occurred 1: Over-Range has occurred This bit is set to "1" if converter is driven beyond the specified input range. It is "sticky," i.e., it remains set until explicitly cleared by writing a "1" to the corresponding dformat_ovr_clear[15:0] bit . The corresponding dformat_ovr_clear[15:0] bit would need to be cleared for further overflows to be reported [0] = Over-range Sticky bit for converter 0 [1] = Over-range Sticky bit for converter 1 [2] = Over-range Sticky bit for converter 2 etc.	0x0	R
0x02A8	OUT_RES	[7:6]	RESERVED		Reserved.	0x0	R
		5	DFORMAT_DDC_DITHER_EN		Dformat DDC Dither En. Dformat dither enable for DDC mode.	0x0	R/W
				0	0: dformat dither disable.		
				1	1: dformat dither enable.		
		4	DFORMAT_FBW_DITHER_EN		Dformat FBW Dither En. Dformat dither enable for FBW mode.	0x0	R/W
				0	0: dformat dither disable.		
				1	1: dformat dither enable.		
		[3:0]	DFORMAT_RES		Data Output Resolution. Chip Output Resolution. Must match ADC converter resolution set by JTX_N_CFG	0x0	R/W
				0x0	16-bit resolution.		
				0x1	15-bit resolution.		
				0x2	14-bit resolution.		
				0x3	13-bit resolution.		
				0x4	12-bit resolution.		
				0x5	11-bit resolution.		
				0x6	10-bit resolution.		
				0x7	9-bit resolution.		
				0x8	8-bit resolution.		
					All other values are invalid.		
0x02A9	FD_SEL_0	[7:0]	DFORMAT_FD_SEL[7:0]		FD Data Select. FD output at the Converter.	0x0	R/W
				0x0000	None of the Converter has FD data.		
				0x0001	FD data at Converter 0.		
				0x0002	FD data at Converter 1.		
				-			
				-			
				-			
				0x0007	FD data at Converters 0,1,2.		
				-			
				0xFFFF	FD data at all 16 Converters.		
0x02AA	FD_SEL_1	[7:0]	DFORMAT_FD_SEL[15:8]		FD Data Select. FD output at the Converter.	0x0	R/W
				0x0000	None of the Converter has FD data.		
				0x0001	FD data at Converter 0.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0x0002 - - -	FD data at Converter 1.		
				0x0007 - 0xFFFF	FD data at Converters 0,1,2. FD data at all 16 Converters.		
0x02AB	FBW_SEL_0	[7:0]	DFORMAT_FBW_SEL[7:0]		FBW Data Select. FBW output at the Converter.	0x0	R/W
				0x0000	None of the Converter has FBW data.		
				0x0001	FBW data at Converter 0.		
				0x0002	FBW data at Converter 1.		
				-	- -.		
				-	- -.		
				0x0007	FBW data at Converters 0,1,2.		
				-	- -.		
				-	- -.		
				0xFFFF	FBW data at all 16 Converters.		
0x02AC	FBW_SEL_1	[7:0]	DFORMAT_FBW_SEL[15:8]		FBW Data Select. FBW output at the Converter.	0x0	R/W
				0x0000	None of the Converter has FBW data.		
				0x0001	FBW data at Converter 0.		
				0x0002	FBW data at Converter 1.		
				-	- -.		
				-	- -.		
				0x0007	FBW data at Converters 0,1,2.		
				-	- -.		
				-	- -.		
				0xFFFF	FBW data at all 16 Converters.		
0x02AD	TMODE_SEL_0	[7:0]	DFORMAT_TMODE_SEL[7:0]		D-formatter test mode Data Select (16-bits). “TMODE” output at the Converter 00b8.	0x0	R/W
				0x0000	None of the Converters have Tmode data.		
				0x0001	Tmode data at Converter 0.		
				0x0002	Tmode data at Converter 1.		
				-	- -.		
				-	- -.		
				0x0007	Tmode data at Converters 0,1,2.		
				-	- -.		
				0xFFFF	Tmode data at all 16 Converters.		
0x02AE	TMODE_SEL_1	[7:0]	DFORMAT_TMODE_SEL[15:8]		D-formatter test mode Data Select (16-bits). “TMODE” output at the Converter 00b8.	0x0	R/W
				0x0000	None of the Converters have Tmode data.		
				0x0001	Tmode data at Converter 0.		
				0x0002	Tmode data at Converter 1.		
				-	- -.		
				-	- -.		
				0x0007	Tmode data at Converters 0,1,2.		
				-	- -.		
				0xFFFF	Tmode data at all 16 Converters.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x02B0	TMODE_I_CTRL1	[7:4]	TMODE_I_TYPE_SEL		Test Mode Generation Selection. I-data pattern routed to even-numbered DFout outputs as enabled by DFORMAT_TMODE_SEL[15:0].	0x0	R/W
				0000	Off - Normal Operation.		
				0001	Midscale short.		
				0010	Positive Full-Scale.		
				0011	Negative Full-Scale.		
				0100	Alternating Checkerboard.		
				0101	PN23 Sequence.		
				0110	PN9 Sequence.		
				0111	1/0 Word Toggle.		
				1000	User Pattern Test Mode (not currently valid).		
				1001	PN7.		
				1010	PN15.		
				1011	PN31.		
				1100	Unused.		
				1101	Unused.		
				1110	Unused.		
				1111	Ramp Output.		
		[3:0]	TMODE_I_PN_SEL		Reserved.	0x0	R/W
0x02B1	TMODE_I_CTRL2	7	TMODE_I_FLUSH		Tmode I Flush Signal. This is synchronized and risedge detected to issue a LFSR/ramp/user pattern restart, that is, a synchronous reset of the lfsr/ramp/user pattern.	0x0	R/W
		6	TMODE_I_PN_FORCE_RST		Tmode I Pn Force Rst. Force Reset of the PN generation Logic.	0x0	R/W
		[5:0]	RESERVED		Reserved.	0x0	R/W
0x02B2	TMODE_I_USR_PAT0_LSB	[7:0]	TMODE_I_USR_PAT0[7:0]		Tmode I Usr Pat0.	0x0	R/W
0x02B3	TMODE_I_USR_PAT0_MSB	[7:0]	TMODE_I_USR_PAT0[15:8]		Tmode I Usr Pat0.	0x0	R/W
0x02B4	TMODE_I_USR_PAT1_LSB	[7:0]	TMODE_I_USR_PAT1[7:0]		Tmode I Usr Pat1.	0x0	R/W
0x02B5	TMODE_I_USR_PAT1_MSB	[7:0]	TMODE_I_USR_PAT1[15:8]		Tmode I Usr Pat1.	0x0	R/W
0x02B6	TMODE_I_USR_PAT2_LSB	[7:0]	TMODE_I_USR_PAT2[7:0]		Tmode I Usr Pat2.	0x0	R/W
0x02B7	TMODE_I_USR_PAT2_MSB	[7:0]	TMODE_I_USR_PAT2[15:8]		Tmode I Usr Pat2.	0x0	R/W
0x02B8	TMODE_I_USR_PAT3_LSB	[7:0]	TMODE_I_USR_PAT3[7:0]		Tmode I Usr Pat3.	0x0	R/W
0x02B9	TMODE_I_USR_PAT3_MSB	[7:0]	TMODE_I_USR_PAT3[15:8]		Tmode I Usr Pat3.	0x0	R/W
0x02C6	RXEN0_SEL0	[7:0]	RXEN0_FDDC_SEL		RXEN0 Based Power Saving for Fine DDCs. Bits [7:0] correspond to Fine DDCs 7 down to Fine DDC 0	0x0	R/W
				0	0 - No clock gating based on RXEN for Fine DDC.		
				1	1 - Clock gating of Fine DDC if RXEN is low.		
0x02C7	RXEN0_SEL1	[7:6]	RXEN0_ADC_SEL		RXEN0 Based Power Saving for ADC Cores.	0x0	R/W
				00	No clock gating/powerdown based on RXEN0 for the ADC cores.		
				01	Clock gating/Powerdown of ADC0 and ADC2 for AD9081/AD9209/AD9988, ADC0 for AD9082/AD9207/AD9986, if RXEN0 is low.		
				10	Clock gating/Powerdown of ADC1 and ADC3 for AD9081/AD9209/AD9988, ADC1 for AD9082/AD9207/AD9986, if RXEN0 is low.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				11	Clock gating/Powerdown of all ADC cores, if RXEN0 is low.		
		[5:4]	RXEN0_JTXL_SEL		RXEN0 Based Power Saving for JTX Link Digital. Bits [1:0] correspond to JTX link 1 down to JTX Link 0	0x0	R/W
				0	0 - No clock gating based on RXEN for JTX digital.		
				1	1 - Clock gating of JTX digital if RXEN is low.		
		[3:0]	RXEN0_CDDC_SEL		RXEN0 Based Power Saving for Coarse DDCs. Bits[3:0] correspond to Coarse DDCs 3 down to Coarse DDC 0	0x0	R/W
				0	0 - No clock gating based on RXEN for Coarse DDC.		
				1	1 - Clock gating of Coarse DDC if RXEN is low.		
0x02C8	RXEN0_SEL2	[7:0]	RXEN0_JTXPHY_SEL		RXEN0 Based Power Saving for JTX SERDES Lanes. Bits[7:0] correspond to JTX SERDES lane 7 down to lane 0	0x0	R/W
				0	0 - No clock gating/powerdown based on RXEN for SERDES lanes.		
				1	1 - Clock gating/Powerdown of SERDES lanes if RXEN is low.		
0x02C9	RXEN1_SEL0	[7:0]	RXEN1_FDDC_SEL		RXEN1 Based Power Saving for Fine DDCs. Bits [7:0] correspond to Fine DDCs 7 down to Fine DDC 0	0x0	R/W
				0	0 - No clock gating based on RXEN for Fine DDC.		
				1	1 - Clock gating of Fine DDC if RXEN is low.		
0x02CA	RXEN1_SEL1	[7:6]	RXEN1_ADC_SEL		RXEN1 Based Power Saving for ADC Cores.	0x0	R/W
				00	No clock gating/powerdown based on RXEN1 for the ADC cores.		
				01	Clock gating/Powerdown of ADC0 and ADC2 for AD9081/AD9209/AD9988, ADC0 for AD9082/ AD9207/AD9986, if RXEN1 is low.		
				10	Clock gating/Powerdown of ADC1 and ADC3 for AD9081/AD9209/AD9988, ADC1 for AD9082/ AD9207/AD9986, if RXEN1 is low.		
				11	Clock gating/Powerdown of all ADC cores, if RXEN1 is low.		
		[5:4]	RXEN1_JTXL_SEL		RXEN1 Based Power Saving for JTX Link Digital. Bits[1:0] correspond to JTX link 1 down to JTX Link 0	0x0	R/W
				0	0 - No clock gating based on RXEN for JTX digital.		
				1	1 - Clock gating of JTX digital if RXEN is low.		
		[3:0]	RXEN1_CDDC_SEL		RXEN1 Based Power Saving for Coarse DDCs. Bits[3:0] correspond to Coarse DDCs 3 down to Coarse DDC 0	0x0	R/W
				0	0 - No clock gating based on RXEN for Coarse DDC.		
				1	1 - Clock gating of Coarse DDC if RXEN is low.		
0x02CB	RXEN1_SEL2	[7:0]	RXEN1_JTXPHY_SEL		RXEN1 Based Power Saving for JTX SERDES Lanes. Bits[7:0] correspond to JTX SERDES lane 7 down to lane 0	0x0	R/W
				0	0 - No clock gating/powerdown based on RXEN for SERDES lanes.		
				1	1 - Clock gating/Powerdown of SERDES lanes if RXEN is low.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x02CC	FINE_DDC_STATUS_SEL	[7:4]	RESERVED		Reserved.	0x0	R
		[3:2]	FINE_DDC_Q_STATUS_SEL		Fine DDC Q Status Select. Fine DDC Q samples status select. It is used to select FD and SMON status bits for DDC Q samples.	0x0	R/W
				00	0: ADC 0 selected.		
				01	1: ADC 1 selected.		
				10	2: ADC 2 selected.		
				11	3: ADC 3 selected.		
		[1:0]	FINE_DDC_I_STATUS_SEL		Fine DDC I Status Select. Fine DDC I samples status select. It is used to select FD and SMON status bits for DDC I samples.	0x0	R/W
				00	0: ADC 0 selected.		
				01	1: ADC 1 selected.		
				10	2: ADC 2 selected.		
				11	3: ADC 3 selected.		
0x02CD	FD_EQ_STATUS_SEL	[7:4]	RESERVED		Reserved.	0x0	R
		[3:2]	FD_EQ_Q_STATUS_SEL		FDELAY EQ Q Status Select. Fdelay Eq Q samples status select. It is used to select FD and SMON status bits for Q samples.	0x0	R/W
				00	0: ADC 0 selected.		
				01	1: ADC 1 selected.		
				10	2: ADC 2 selected.		
				11	3: ADC 3 selected.		
		[1:0]	FD_EQ_I_STATUS_SEL		FDELAY EQ I Status Select. Fdelay Eq I samples status select. It is used to select FD and SMON status bits for I samples.	0x0	R/W
				00	0: ADC 0 selected.		
				01	1: ADC 1 selected.		
				10	2: ADC 2 selected.		
				11	3: ADC 3 selected.		
0x02CE	RXENGP0_SEL0	[7:0]	RXENGP0_FDDC_SEL		GPIO RXEN0 Based Power Saving for Fine DDCs. Bits [7:0] correspond to Fine DDCs 7 down to Fine DDC 0.	0x0	R/W
				0	0 - No clock gating based on RXEN for Fine DDC.		
				1	1- Clock gating of Fine DDC if RXEN is low.		
0x02CF	RXENGP0_SEL1	[7:6]	RXENGP0_ADC_SEL		GPIO RXEN0 Based Power Saving for ADC Cores.	0x0	R/W
				00	No clock gating/powerdown based on GPIO RXEN0 for the ADC cores.		
				01	Clock gating/Powerdown of ADC0 and ADC2 for AD9081/AD9209/AD9988, ADC0 for AD9082/ AD9207/AD9986, if GPIO RXEN0 is low.		
				10	Clock gating/Powerdown of ADC1 and ADC3 for AD9081/AD9209/AD9988, ADC1 for AD9082/ AD9207/AD9986, if GPIO RXEN0 is low.		
				11	Clock gating/Powerdown of all ADC cores, if GPIO RXEN0 is low.		
		[5:4]	RXENGP0_JTXL_SEL		GPIO RXEN0 Based Power Saving for JTX Link Digital. Bits [1:0] correspond to JTX link 1 down to JTX Link 0.	0x0	R/W
				0	0 - No clock gating based on RXEN for JTX digital.		
				1	1- Clock gating of JTX digital if RXEN is low.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[3:0]	RXENGP0_CDDC_SEL		GPIO RXEN0 Based Power Saving for Coarse DDCs. Bits [3:0] correspond to Coarse DDCs 3 down to Coarse DDC 0.	0x0	R/W
				0	0 - No clock gating based on RXEN for Coarse DDC.		
				1	1 - Clock gating of Coarse DDC if RXEN is low.		
0x02D0	RXENGP0_SEL2	[7:0]	RXENGP0_JTXPHY_SEL		GPIO RXEN0 Based Power Saving for JTX SERDES Lanes. Bits [7:0] correspond to JTX SERDES lane 7 down to lane 0.	0x0	R/W
				0	0 - No clock gating/powerdown based on RXEN for SERDES lanes.		
				1	1 - Clock gating/Powerdown of SERDES lanes if RXEN is low.		
0x02D1	RXENGP1_SEL0	[7:0]	RXENGP1_FDDC_SEL		GPIO RXEN1 Based Power Saving for Fine DDCs. Bits [7:0] correspond to Fine DDCs 7 down to Fine DDC 0.	0x0	R/W
				0	0 - No clock gating based on RXEN for Fine DDC.		
				1	1 - Clock gating of Fine DDC if RXEN is low.		
0x02D2	RXENGP1_SEL1	[7:6]	RXENGP1_ADC_SEL		GPIO RXEN1 Based Power Saving for ADC Cores.	0x0	R/W
				00	No clock gating/powerdown based on GPIO RXEN1 for the ADC cores.		
				01	Clock gating/Powerdown of ADC0 and ADC2 for AD9081/AD9209/AD9988, ADC0 for AD9082/AD9207/AD9986, if GPIO RXEN1 is low.		
				10	Clock gating/Powerdown of ADC1 and ADC3 for AD9081/AD9209/AD9988, ADC1 for AD9082/AD9207/AD9986, if GPIO RXEN1 is low.		
				11	Clock gating/Powerdown of all ADC cores, if GPIO RXEN1 is low.		
		[5:4]	RXENGP1_JTXL_SEL		GPIO RXEN1 Based Power Saving for JTX Link Digital. Bits [1:0] correspond to JTX link 1 down to JTX Link 0.	0x0	R/W
				0	0 - No clock gating based on RXEN for JTX digital.		
				1	1 - Clock gating of JTX digital if RXEN is low.		
		[3:0]	RXENGP1_CDDC_SEL		GPIO RXEN1 Based Power Saving for Coarse DDCs. Bits [3:0] correspond to Coarse DDCs 3 down to Coarse DDC 0.	0x0	R/W
				0	0 - No clock gating based on RXEN for Coarse DDC.		
				1	1 - Clock gating of Coarse DDC if RXEN is low.		
0x02D3	RXENGP1_SEL2	[7:0]	RXENGP1_JTXPHY_SEL		GPIO RXEN1 Based Power Saving for JTX SERDES Lanes. Bits [7:0] correspond to JTX SERDES lane 7 down to lane 0.	0x0	R/W
				0	0 - No clock gating/powerdown based on RXEN for SERDES lane.		
				1	1 - Clock gating/Powerdown of SERDES lanes if RXEN is low.		
0x02D4	TMODE_Q_CTRL1	[7:4]	TMODE_Q_TYPE_SEL		Test Mode Generation Selection. Q-data pattern routed to odd-numbered DFout outputs as enabled by DFORMAT_TMODE_SEL[15:0].	0x0	R/W
				0000	Off - Normal Operation.		
				0001	Midscale short.		
				0010	Positive Full-Scale.		
				0011	Negative Full-Scale.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0100	Alternating Checkerboard.		
				0101	PN23 Sequence.		
				0110	PN9 Sequence.		
				0111	1/0 Word Toggle.		
				1000	User Pattern Test Mode (not currently valid).		
				1001	PN7.		
				1010	PN15.		
				1011	PN31.		
				1100	Unused.		
				1101	Unused.		
				1110	Unused.		
				1111	Ramp Output.		
		[3:0]	TMODE_Q_PN_SEL		Reserved.	0x0	R/W
0x02D5	TMODE_Q_CTRL2	7	TMODE_Q_FLUSH		Tmode Q Flush Signal. This is synchronized and risedge detected to issue a LFSR/ramp/user pattern restart, that is, a synchronous reset of the lfsr/ramp/ user pattern.	0x0	R/W
		6	TMODE_Q_PN_FORCE_RST		Tmode Q Pn Force Rst. Force Reset of the PN generation Logic.	0x0	R/W
		[5:0]	RESERVED		Reserved.	0x0	R/W
0x02D6	TMODE_Q_USR_PAT0_LSB	[7:0]	TMODE_Q_USR_PAT0[7:0]		Tmode Q Usr Pat0.	0x0	R/W
0x02D7	TMODE_Q_USR_PAT0_MSB	[7:0]	TMODE_Q_USR_PAT0[15:8]		Tmode Q Usr Pat0.	0x0	R/W
0x02D8	TMODE_Q_USR_PAT1_LSB	[7:0]	TMODE_Q_USR_PAT1[7:0]		Tmode Q Usr Pat1.	0x0	R/W
0x02D9	TMODE_Q_USR_PAT1_MSB	[7:0]	TMODE_Q_USR_PAT1[15:8]		Tmode Q Usr Pat1.	0x0	R/W
0x02DA	TMODE_Q_USR_PAT2_LSB	[7:0]	TMODE_Q_USR_PAT2[7:0]		Tmode Q Usr Pat2.	0x0	R/W
0x02DB	TMODE_Q_USR_PAT2_MSB	[7:0]	TMODE_Q_USR_PAT2[15:8]		Tmode Q Usr Pat2.	0x0	R/W
0x02DC	TMODE_Q_USR_PAT3_LSB	[7:0]	TMODE_Q_USR_PAT3[7:0]		Tmode Q Usr Pat3.	0x0	R/W
0x02DD	TMODE_Q_USR_PAT3_MSB	[7:0]	TMODE_Q_USR_PAT3[15:8]		Tmode Q Usr Pat3.	0x0	R/W
0x02E9	COARSE_FSRC_EN	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	COARSE_FSRC_EN		Enables/Disables Coarse DDCs.	0x0	R/W
				--	Bit[0] - "1" Enables Coarse DDC1 and "0" Disables Coarse DDC1.		
				--	Bit[1] - "1" Enables Coarse DDC2 and "0" Disables Coarse DDC2.		
				--	Bit[2] - "1" Enables Coarse DDC3 and "0" Disables Coarse DDC3.		
				--	Bit[3] - "1" Enables Coarse DDC4 and "0" Disables Coarse DDC4.		
0x02EA	TMODE_I_USR_PAT4_LSB	[7:0]	TMODE_I_USR_PAT4[7:0]		Tmode I Usr Pat4.	0x0	R/W
0x02EB	TMODE_I_USR_PAT4_MSB	[7:0]	TMODE_I_USR_PAT4[15:8]		Tmode I Usr Pat4.	0x0	R/W
0x02EC	TMODE_I_USR_PAT5_LSB	[7:0]	TMODE_I_USR_PAT5[7:0]		Tmode I Usr Pat5.	0x0	R/W
0x02ED	TMODE_I_USR_PAT5_MSB	[7:0]	TMODE_I_USR_PAT5[15:8]		Tmode I Usr Pat5.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x02EE	TMODE_I_USR_PAT6_LSB	[7:0]	TMODE_I_USR_PAT6[7:0]		Tmode I Usr Pat6.	0x0	R/W
0x02EF	TMODE_I_USR_PAT6_MSB	[7:0]	TMODE_I_USR_PAT6[15:8]		Tmode I Usr Pat6.	0x0	R/W
0x02F0	TMODE_I_USR_PAT7_LSB	[7:0]	TMODE_I_USR_PAT7[7:0]		Tmode I Usr Pat7.	0x0	R/W
0x02F1	TMODE_I_USR_PAT7_MSB	[7:0]	TMODE_I_USR_PAT7[15:8]		Tmode I Usr Pat7.	0x0	R/W
0x02F2	TMODE_Q_USR_PAT4_LSB	[7:0]	TMODE_Q_USR_PAT4[7:0]		Tmode Q Usr Pat4.	0x0	R/W
0x02F3	TMODE_Q_USR_PAT4_MSB	[7:0]	TMODE_Q_USR_PAT4[15:8]		Tmode Q Usr Pat4.	0x0	R/W
0x02F4	TMODE_Q_USR_PAT5_LSB	[7:0]	TMODE_Q_USR_PAT5[7:0]		Tmode Q Usr Pat5.	0x0	R/W
0x02F5	TMODE_Q_USR_PAT5_MSB	[7:0]	TMODE_Q_USR_PAT5[15:8]		Tmode Q Usr Pat5.	0x0	R/W
0x02F6	TMODE_Q_USR_PAT6_LSB	[7:0]	TMODE_Q_USR_PAT6[7:0]		Tmode Q Usr Pat6.	0x0	R/W
0x02F7	TMODE_Q_USR_PAT6_MSB	[7:0]	TMODE_Q_USR_PAT6[15:8]		Tmode Q Usr Pat6.	0x0	R/W
0x02F8	TMODE_Q_USR_PAT7_LSB	[7:0]	TMODE_Q_USR_PAT7[7:0]		Tmode Q Usr Pat7.	0x0	R/W
0x02F9	TMODE_Q_USR_PAT7_MSB	[7:0]	TMODE_Q_USR_PAT7[15:8]		Tmode Q Usr Pat7.	0x0	R/W
0x02FA	RXEN_CTRL	[7:6]	RESERVED		Reserved.	0x0	R
		5	RXENGP1_POL		Polarity Control for GPIO RXEN1.	0x0	R/W
				0	0=> Active high.		
				1	1=> Active Low.		
		4	RXENGP0_POL		Polarity Control for GPIO RXEN0.	0x0	R/W
				0	0=> Active high.		
				1	1=> Active Low.		
		3	RXEN1_POL		Polarity Control for RXEN1.	0x0	R/W
				0	0=> Active high.		
				1	1=> Active Low.		
		2	RXEN0_POL		Polarity Control for RXEN0.	0x0	R/W
				0	0=> Active high.		
				1	1=> Active Low.		
		1	RXEN1_USETXEN		TXEN USAGE Instead of RXEN.	0x0	R/W
				0	0=> RXEN1 itself is used by design.		
				1	1=> TXEN1 pin is sued instead of RXEN1.		
		0	RXEN0_USETXEN		TXEN USAGE Instead of RXEN.	0x0	R/W
				0	0=> RXEN0 itself is used by design.		
				1	1=> TXEN0 pin is sued instead of RXEN0.		
0x02FB	RXEN_SPI_CTRL	7	RXENGP1_SPI		SPI Control for GPIO RXEN1.	0x0	R/W
				0	0=> Active high.		
				1	1=> Active Low.		
		6	RXENGP0_SPI		SPI Control for GPIO RXEN0.	0x0	R/W
				0	0=> Active high.		
				1	1=> Active Low.		
		5	RXEN1_SPI		SPI Control for RXEN1.	0x0	R/W
				0	0=> Active high.		
				1	1=> Active Low.		
		4	RXEN0_SPI		SPI Control for RXEN0.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0	0=> Active high.		
				1	1=> Active Low.		
		3	RXENGP1_SPIEN		SPI Control Enable for GPIO RXEN1.	0x0	R/W
				0	0=> Active high.		
				1	1=> Active Low.		
		2	RXENGP0_SPIEN		SPI Control Enable for GPIO RXEN0.	0x0	R/W
				0	0=> Active high.		
				1	1=> Active Low.		
		1	RXEN1_SPIEN		SPI Control Enable for RXEN1.	0x0	R/W
				0	0=> Active high.		
				1	1=> Active Low.		
		0	RXEN0_SPIEN		SPI Control Enable for RXEN0.	0x0	R/W
				0	0=> Active high.		
				1	1=> Active Low.		
0x02FC	RXEN_NOVALP_CTRL1	7	RXENGP1_1F_CTRL		RXENGP1 Control Enable for 1f.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		6	RXEN1_1F_CTRL		RXEN1 Control Enable for 1f.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		5	RXENGP0_0F_CTRL		RXENGP0 Control Enable for 0f.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		4	RXEN0_0F_CTRL		RXEN0 Control Enable for 0f.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		3	RXENGP1_1S_CTRL		RXENGP1 Control Enable for 1s.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		2	RXEN1_1S_CTRL		RXEN1 Control Enable for 1s.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		1	RXENGP0_0S_CTRL		RXENGP0 Control Enable for 0s.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		0	RXEN0_0S_CTRL		RXEN0 Control Enable for 0s.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
0x02FD	RXEN_NOVALP_CTRL2	7	RXENGP1_3F_CTRL		RXENGP1 Control Enable for 3f.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		6	RXEN1_3F_CTRL		RXEN1 Control Enable for 3f.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		5	RXENGP0_2F_CTRL		RXENGP0 Control Enable for 2f.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		4	RXEN0_2F_CTRL		RXEN0 Control Enable for 2f.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		3	RXENGP1_3S_CTRL		RXENGP1 Control Enable for 3s.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		2	RXEN1_3S_CTRL		RXEN1 Control Enable for 3s.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		1	RXENGP0_2S_CTRL		RXENGP0 Control Enable for 2s.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
		0	RXEN0_2S_CTRL		RXEN0 Control Enable for 2s.	0x0	R/W
				0	0=> Disable Control.		
				1	1=> Enable Control.		
0x0300	BE_SOFT_OFF_GAIN_CTRL	7	BE_SOFT_OFF_GAIN_EN		gain, which	0x0	R/W
		[6:0]	RESERVED		Reserved.	0x0	R
0x0301	BE_SOFT_OFF_ENABLE0	7	ENA_SHORT_PAERR_SOFTOFF		Enable short PA error soft off. Short here means the average window is small, only 1,2,4,8 average clock cycle is available. So it is fast to get an average power data.	0x1	R/W
		6	ENA_LONG_PAERR_SOFTOFF		Enable long PA error soft off. Long here means the average window is long compared with the short average. 2^9 ~2^19 cycles are used.	0x1	R/W
		[5:4]	RESERVED		Reserved.	0x0	R
		3	ENA_JESD_ERR_SOFTOFF		Enable JESD side error soft off. There are JESD204B errors like bad disparity, NIT, UEK, … This enable bit is to enable the soft off for all these JESD source errors.	0x0	R/W
		2	ROTATE_SOFT_OFF_EN		sync Logic rotation is also a soft off source. This bit is to enable the sync Logic rotate to trigger the DAC output soft off. Note that 0x3b[0] must also be high.	0x1	R/W
		1	TXEN_SOFT_OFF_EN		Txen is a soft off source. This bit is to enable TXENx falling edge to trigger the DAC output soft off.	0x1	R/W
		0	SPI_SOFT_OFF_EN		Trigger a soft off process by SPI. This bit setting to 1 triggers a soft off. Data must be non-zero for the soft-off to take effect.	0x0	R/W
0x0302	BE_SOFT_OFF_ENABLE1	[7:2]	RESERVED		Reserved.	0x0	R
		1	ENA_204C_CRCERR_SOFTOFF		Enable 204C CRC error soft off. If 204C CRC error happen, enabling this bit triggers a soft off event.	0x0	R/W
		0	ENA_DLL_UNLOCK_SOFTOFF		happen	0x0	R/W
0x0303	BE_SOFT_ON_ENABLE	7	SPI_SOFT_ON_EN		Trigger a soft on process by SPI. This bit setting to 1 triggers a soft on. Data must be non-zero for the soft-off to take effect.	0x0	R/W
		6	LONG_LEVEL_SOFTON_EN		Setting this bit to 1, soft on will happen as long as txen and data_ready is high. Thus, in a scenario when a soft off process happen, but txen and data_ready is 1, then a soft on will automatically trigger after the soft off process.	0x0	R/W
		[5:0]	RESERVED		Reserved.	0x0	R
0x0304	PA_COMMON_CTRL	[7:3]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		2	SOFT_OFF_GAIN_ALL_ENABLE		enable the soft off gain block at the same time for all DAC/link.	0x0	R/W
		1	LONG_PA_ALL_ENABLE		enable the long PA protect block at the same time for all DAC/link.	0x0	R/W
		0	SHORT_PA_ALL_ENABLE		enable the short PA protect at the same time for all DAC/link.	0x0	R/W
0x0305	LONG_PA_THRES_LSB	[7:0]	LONG_PA_THRESHOLD[7:0]		Long average power threshold for comparison.	0x0	R/W
0x0306	LONG_PA_THRES_MSB	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LONG_PA_THRESHOLD[12:8]		Long average power threshold for comparison.	0x0	R/W
0x0307	LONG_PA_CONTROL	7	LONG_PA_ENABLE	0 1	Long PA enable options. 0 = The long average power detection and correction are turned off. 1 = Enable average power calculation and error detection.	0x0	R/W
		[6:4]	RESERVED		Reserved.	0x0	R
		[3:0]	LONG_PA_AVG_TIME	0-15	Sets length of long_pa averaging. If coarse_interp_sel!=1: PA_clock_period = 4*coarse_interp_sel*DAC_clock_period Else: If fine_interp_sel!=1: PA_clock_period = 8*coarse_interp_sel*DAC_clock_period Else: PA_clock_period = 32*DAC_clock_period 0: Average for 2^(9+code) PA clock periods. 1: Average for 2^(10+code) PA clock periods. 2: Average for 2^(11+code) PA clock periods. 3: Average for 2^(12+code) PA clock periods. 4: Average for 2^(13+code) PA clock periods. 5: Average for 2^(14+code) PA clock periods. 6: Average for 2^(15+code) PA clock periods. 7: Average for 2^(16+code) PA clock periods. 8: Average for 2^(17+code) PA clock periods. 9: Average for 2^(18+code) PA clock periods. 10: Average for 2^(19+code) PA clock periods. 0-15: Average for 2^(9+code) PA clock periods. Average for 2^(9+code) PA clock periods.	0x0	R/W
0x0308	LONG_PA_POWER_LSB	[7:0]	LONG_PA_POWER[7:0]		Read the calculated long average power. The average power = I^2+Q^2. Note: only 6MSB of I/Q are used for this calculation.	0x0	R
0x0309	LONG_PA_POWER_MSB	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LONG_PA_POWER[12:8]		Read the calculated long average power. The average power = I^2+Q^2. Note: only 6 MSB of I/Q are used for this calculation.	0x0	R
0x030A	SHORT_PA_THRES_LSB	[7:0]	SHORT_PA_THRESHOLD[7:0]		Short average power threshold for comparison.	0x0	R/W
0x030B	SHORT_PA_THRES_MSB	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	SHORT_PA_THRESHOLD[12:8]		Short average power threshold for comparison.	0x0	R/W
0x030C	SHORT_PA_CONTROL	7	SHORT_PA_ENABLE	0 1	Short PA enable options. 0 = The short average power detection and correction are turned off. 1 = Enable average power calculation and error detection.	0x0	R/W
		[6:2]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[1:0]	SHORT_PA_AVG_TIME		Sets length of short_pa averaging.	0x0	R/W
					If coarse_interp_sel!=1: PA_clock_period = 4*coarse_interp_sel*DAC_clock_period Else: If fine_interp_sel!=1: PA_clock_period = 8*coarse_interp_sel*DAC_clock_period Else: PA_clock_period = 32*DAC_clock_period 0: Average for 2^0 PA clock periods. 1: Average for 2^1 PA clock periods. 2: Average for 2^2 PA clock periods. 3: Average for 2^3 PA clock periods.		
				0-3	Average for 2^code PA clock periods.		
0x030D	SHORT_PA_POWER_LSB	[7:0]	SHORT_PA_POWER[7:0]		Short average power bus = I^2+Q^2 (I/Q use 6MSB of databus).	0x0	R
0x030E	SHORT_PA_POWER_MSB	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	SHORT_PA_POWER[12:8]		Short average power bus = I^2+Q^2 (I/Q use 6MSB of databus).	0x0	R
0x030F	TXEN_SM_0	[7:1]	RESERVED		Reserved.	0x0	R
		0	ENA_TXENSM		Enable TXEN state machine.	0x0	R/W
0x031F	PA_PROT_PIN_CTRL0	7	RESERVED		Reserved.	0x0	R/W
		6	ENA_SHORT_PAPROT_PIN_AVGPOW		1: Short average power detected errors are routed to GPIO pin.	0x0	R/W
		5	ENA_LONG_PAPROT_PIN_AVGPOW		1: Long average power detected errors are routed to GPIO pin.	0x0	R/W
		4	ENA_PAPROT_PIN_JRX_204C_CRC_ERR		1: 204C crc detected errors are routed to GPIO pin.	0x0	R/W
		3	ENA_PAPROT_PIN_JESD_ERRORS		1: 204B detected errors are routed to GPIO pin.	0x0	R/W
		2	ENA_PAPROT_PIN_BLSM		Enable PA protect pin from blanking state machine (this signal occurs during sync rotations and in response to TXENx falling low).	0x0	R/W
		1	ENA_PAPROT_PIN_TXENSM		Enable PA protect pin from Tx enable state machine.	0x0	R/W
		0	SPI_PA_CTRL		If ENA_PAPROT_PIN_SPI is high and this is high, PAPROT==1.	0x0	R/W
0x0320	PA_PROT_PIN_CTRL1	[7:3]	RESERVED		Reserved.	0x0	R
		2	ENA_PAPROT_PIN_SRERR		1: Slew rate detected errors are routed to GPIO pin. NOTE: This is not working properly in R1R.	0x0	R/W
		[1:0]	RESERVED		Reserved.	0x0	R/W
0x0321	BLANKING_CTRL	[7:4]	RESERVED		Reserved.	0x0	R
		3	SPI_TXEN		Txen control from SPI enable bit. Only used if ENA_SPI_TXEN==1.	0x0	R/W
		2	ENA_SPI_TXEN		Enable SPI Tx enable.	0x0	R/W
		[1:0]	RESERVED		Reserved.	0x0	R
0x0322	TXEN_FLUSH_CTRL0	[7:1]	RESERVED		Reserved.	0x0	R
		0	SPI_FLUSH_EN		enables	0x1	R/W
0x0342	SMON_STATUS_FCNT	[7:0]	SMON_STATUS_FCNT		Signal Monitor Frame Counter. Increments whenever period counter expires.	0x0	R
0x0343	SMON_PERIOD_0	[7:0]	SMON_PERIOD[7:0]		Signal Monitor Period. 32-bit value sets no. of clock cycles over which signal monitor performs operation.	0x0	R/W
0x0344	SMON_PERIOD_1	[7:0]	SMON_PERIOD[15:8]		Signal Monitor Period. 32-bit value sets no. of clock cycles over which signal monitor performs operation.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0345	SMON_PERIOD_2	[7:0]	SMON_PERIOD[23:16]		Signal Monitor Period. 32-bit value sets no. of clock cycles over which signal monitor performs operation.	0x0	R/W
0x0346	SMON_PERIOD_3	[7:0]	SMON_PERIOD[31:24]		Signal Monitor Period. 32-bit value sets no. of clock cycles over which signal monitor performs operation.	0x0	R/W
0x0347	SMON_STATUS_CTRL	[7:4]	RESERVED		Reserved.	0x0	R
		[3:1]	SMON_STATUS_RDSEL		Signal Monitor Status Readback Selection. 0x1 for Peak detector.	0x0	R/W
		0	SMON_STATUS_UPDATE		Status Update. A high transition on this signal causes the status value to change in the regmap.	0x0	R/W
0x0348	SMON_SFRAMER	[7:2]	SMON_SFRAMER_INSEL		Signal Monitor Serial Framer Input Selection.	0x0	R/W
		1	SMON_SFRAMER_MODE		Signal Monitor Serial Framer Mode Selection.	0x0	R/W
		0	SMON_SFRAMER_EN		Signal Monitor Serial Framer Enable.	0x0	R/W
0x0349	SMON_SYNC_CTRL	[7:2]	RESERVED		Reserved.	0x0	R
		1	SMON_SYNC_NEXT		SMON Next Synchronization Mode.	0x0	R/W
				0	0: Continuous mode.		
				1	1: Next Synchronization Mode.		
		0	SMON_SYNC_EN		SMON Synchronization Enable.	0x0	R/W
0x034A to 0x034C by 1	SMON_STATUSn	[7:0]	SMON_STATUS		Signal Monitor Serial Data Output. 20 bits Signal Monitor Serial Data Output bits.	0x0	R
0x034D	SMON_THRESH_LOW0	[7:0]	SMON_THRESH_LOW[7:0]		Signal Monitor GPIO Lower Threshold. 11-bit lower threshold for the absolute value of peak detected.	0x0	R/W
0x034E	SMON_THRESH_LOW1	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	SMON_THRESH_LOW[10:8]		Signal Monitor GPIO Lower Threshold. 11-bit lower threshold for the absolute value of peak detected.	0x0	R/W
0x034F	SMON_THRESH_HIGH0	[7:0]	SMON_THRESH_HIGH[7:0]		Signal Monitor GPIO Upper Threshold. 11-bit upper threshold for the absolute value of peak detected	0x0	R/W
0x0350	SMON_THRESH_HIGH1	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	SMON_THRESH_HIGH[10:8]		Signal Monitor GPIO Upper Threshold. 11-bit upper threshold for the absolute value of peak detected	0x0	R/W
0x0400	Leader_PD	[7:1]	RESERVED		Reserved.	0x0	R
		0	PD_Leader_RC		Leader power down for JESD deserializers. Must be set to 0 to un-mask individual PHY_PD bits.	0x1	R/W
0x0401	PHY_PD	[7:0]	PD_DES_RC_CH		PHY power down. Bit per lane – For example 0xF0 powers down physical lanes 7:4.	0xEE	R/W
0x0402	GENERIC_PD	[7:2]	RESERVED		Reserved.	0x0	R
		1	PD_SYNCA_RC			0x0	R/W
				0	0 = SYNC0OUTB± is on.		
				1	1 = SYNC0OUTB± is powered down.		
		0	PD_SYNCB_RC			0x1	R/W
				0	0 = SYNC1OUTB± is on.		
				1	1 = SYNC1OUTB± is powered down.		
0x0405	CDR_RESET	[7:1]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		0	RSTB_DES_RC		Leader resetb (active low reset) for JESD deserializers.	0x0	R/W
0x0406	CBUS_ADDR	[7:0]	CBUS_ADDR_DES_RC		Deserializer Control bus address select. Sets the address within the deserializer CBUS to access.	0x0	R/W
0x0407	CBUS_WRSTROBE_PHY	[7:0]	CBUS_WSTROBE_DES_RC_CH		Strobe signal sent to selected deserializers to load data in cbus_wdata_des_rc <7:0>. Bits are "decoded" as described below.	0x0	R/W
				0x00	no strobe sent to deserializers to write data.		
				0x01	Write strobe sent to Lane 0 deserializer to write data.		
				0x02	Write strobe sent to Lane 1 deserializer to write data.		
				0x03	Write strobe sent to Lanes 0 and 1 deserializer to write data.		
				0x04	Write strobe sent to Lane 2 deserializer to write data.		
				0x05	Write strobe sent to Lanes 0 and 2 to write data.		
				0x06	Write strobe sent to Lanes 1 and 2 deserializers to write data.		
				0x07	Write strobe sent to Lanes 0 to 2 deserializers to write data.		
				-	- -.		
				-	- -.		
				0x0F	Write strobe sent to Lanes 0 to 3 deserializers to write data.		
				-	- -.		
				0x1F	Write strobe sent to Lanes 0 to 4 deserializers to write data.		
				-	- -.		
				0xFF	Write strobe sent to Lanes 0 to 7 deserializers to write data.		
0x0408	CBUS_WDATA	[7:0]	CBUS_WDATA_DES_RC		Control Bus data, channel selected with CBUS_WSTROBE_DES_RC_CH register.	0x0	R/W
0x0429	SYNCA	[7:1]	RESERVED		Reserved.	0x0	R
		0	SEL_SYNCA_MODE_RC		Set to 0 to select CMOS operation, to 1 to select LVDS operation.	0x0	R/W
0x042A	SYNCB	[7:1]	RESERVED		Reserved.	0x0	R
		0	SEL_SYNCB_MODE_RC		Set to 0 to select CMOS operation, to 1 to select LVDS operation.	0x0	R/W
0x0457	LF_PARDATAMODE_DES_RC0	[7:6]	SEL_LF_PARDATAMODE_DES_RC_CH3		00 = 66 bits (204C), 10 = 40 bit (204B).	0x0	R/W
		[5:4]	SEL_LF_PARDATAMODE_DES_RC_CH2		00 = 66 bits (204C), 10 = 40 bit (204B).	0x0	R/W
		[3:2]	SEL_LF_PARDATAMODE_DES_RC_CH1		00 = 66 bits (204C), 10 = 40 bit (204B).	0x0	R/W
		[1:0]	SEL_LF_PARDATAMODE_DES_RC_CH0		00 = 66 bits (204C), 10 = 40 bit (204B).	0x0	R/W
0x0458	LF_PARDATAMODE_DES_RC1	[7:6]	SEL_LF_PARDATAMODE_DES_RC_CH7		00 = 66 bits (204C), 10 = 40 bit (204B).	0x0	R/W
		[5:4]	SEL_LF_PARDATAMODE_DES_RC_CH6		00 = 66 bits (204C), 10 = 40 bit (204B).	0x0	R/W
		[3:2]	SEL_LF_PARDATAMODE_DES_RC_CH5		00 = 66 bits (204C), 10 = 40 bit (204B).	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[1:0]	SEL_LF_PARDATAMODE_DES_RC_CH4		00 = 66 bits (204C), 10 = 40 bit (204B).	0x0	R/W
0x0459	LF_QUARTERRATE_DES_RC	[7:0]	SEL_LF_QUARTERRATE_DES_RC		select LF_quarterrate_des_rc.	0x0	R/W
0x04A0	JRX_TPL_0	[7:4]	JRX_TPL_SYSREF_N_SHOT_COUNT		Mask all incoming SYSREF pulses except the Nth pulse where N is the value programmed + 1. Only used when n_shot_enable is high.	0x0	R/W
		3	JRX_TPL_SYSREF_N_SHOT_ENABLE		Mask all incoming SYSREF pulses except the Nth pulse specified by the n_shot_count. Disabling this causes all SYSREF pulses to be sampled (continuous mode) and reset the n_shot counter.	0x0	R/W
		2	JRX_TPL_SYSREF_RCVD		signal indicating that SYSREF phase has been established	0x0	R
		1	JRX_TPL_USR_DATA_RDY		valid signal that indicate output conv_sample	0x0	R
		0	JRX_TPL_CFG_INVALID		Input config not supported according to VALID_* in F_NP_L and S_NS_F parameters	0x0	R
0x04A1	JRX_TPL_1	7	RESERVED		Reserved.	0x0	R
		6	JRX_TPL_BITFIELD		This bit must be set to '0'.	0x1	R/W
		[5:3]	RESERVED		Reserved.	0x0	R
		2	JRX_TPL_SYSREF_IGNORE_WHEN_LINKED		Mask incoming SYSREF when SYNC~ is de-asserted. Applies to 204B operation only.	0x0	R/W
		[1:0]	RESERVED		Reserved.	0x0	R
0x04A3	JRX_TPL_3	[7:0]	JRX_TPL_PHASE_ADJUST[7:0]		16-bit register used to delay the transport layer LMFC/LEMC relative to the device "local" LMFC/LEMC in JRx_sample_clock cycles.	0x0	R/W
0x04A4	JRX_TPL_4	[7:0]	JRX_TPL_PHASE_ADJUST[15:8]		16-bit register used to delay the transport layer LMFC/LEMC relative to the device "local" LMFC/LEMC in JRx_sample_clock cycles.	0x0	R/W
0x04A5	JRX_TPL_5	[7:0]	JRX_TPL_PHASE_DIFF		Difference between the local LMFC/LEMC boundary and the arriving data's LMFC/LEMC boundary in JRX_SAMPLE_CLOCK cycles	0x0	R
0x04A8	JRX_L0_2	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	JRX_LID_CFG		Lane identification number (within link).	0x0	R/W
0x04A9	JRX_L0_3	7	JRX_DSCR_CFG	 0 1	JRx descrambler control. Descrambling disabled. Descrambling enabled (mandatory if using 64b/66b Link Layer.	0x0	R/W
		[6:0]	RESERVED		Reserved.	0x0	R
0x04AA	JRX_L0_4	[7:0]	JRX_F_CFG		Number of octets per frame per lane. F = N / 16 * M * N' / L.	0x0	R/W
0x04AB	JRX_L0_5	[7:0]	JRX_K_CFG		Number of frames in a multi-frame/block.	0x0	R/W
0x04AC	JRX_L0_6	[7:0]	JRX_M_CFG		Number of converters per device.	0x0	R/W
0x04AD	JRX_L0_7	[7:6]	JRX_CS_CFG		Number of control bits per sample.	0x0	R/W
		[5:0]	RESERVED		Reserved.	0x0	R
0x04AE	JRX_L0_8	[7:5]	JRX_SUBCLASSV_CFG	 000 001 010to3 ' b111	Sets the subclass operation for the JRx. subclass 0. subclass 1. 010 -111 are invalid.	0x0	R/W
		[4:0]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x04AF	JRX_L0_9	[7:4]	JRX_JESDV_CFG		JESD204 version.	0x0	R/W
				000	000 – JESD204A.		
				001	001 – JESD204B.		
		[3:0]	JRX_S_CFG		Samples per converter per frame.	0x0	R/W
0x04B0	JRX_L0_10	[7:1]	RESERVED		Reserved.	0x0	R/W
		0	JRX_HD_CFG		High Density format enabled.	0x0	R/W
0x04BF	JRX_DL_204B_1	[7:0]	JRX_DL_204B_ETH		NIT, and	0x0	R/W
0x04C0	JRX_DL_204B_2	[7:6]	RESERVED		Reserved.	0x0	R
		5	JRX_DL_204B_ENABLE		JESD204B (8b/10b) Link Enable:.	0x0	R/W
				0	Disable 8b/10b Link Layer (204B).		
				1	Enable 8b/10b Link Layer (204B).		
		[4:0]	RESERVED		Reserved.	0x0	R
0x04CF to 0x04D6 by 1	JRX_DL_204B_17_LANEn	7	RESERVED		Reserved.	0x0	R
		[6:4]	JRX_DL_204B_ECNT_RST		Reset error counters for lanes (L-1) to 0. Each lane's counters are addressed as follows:.	0x0	R/W
				--	[0] Bad Disparity Error (BD).		
				--	[1] Not-In-Table Error (NIT).		
				--	[2] Unexpected K-char. Error (UEK).		
		3	RESERVED		Reserved.	0x0	R
		[2:0]	JRX_DL_204B_ECNT_ENA		Error counter enables for lanes (L-1) to 0. Each lane's counters are addressed as follows:.	0x0	R/W
				--	[0] Bad Disparity Error (BD).		
				--	[1] Not-In-Table Error (NIT).		
				--	[2] Unexpected K-char. Error (UEK).		
0x04DE to 0x04E5 by 1	JRX_DL_204B_18_LANEn	7	RESERVED		Reserved.	0x0	R
		[6:4]	JRX_DL_204B_ECNT_TCR		Error Counters' Terminal Count-Reached indicator for lanes (L-1) to 0. Set to 1 when the corresponding counter Terminal Count value of 0xFF has been reached. If Ecnt_TCH[][i] is set, the Terminal Count value for the corresponding counter is held until the counter is reset by the user, otherwise, the counter rolls over and continues counting. Each lane's counters are addressed as follows:	0x0	R
				--	[0] Bad Disparity Error (BD).		
				--	[1] Not-In-Table Error (NIT).		
				--	[2] Unexpected K-char. Error (UEK).		
		3	RESERVED		Reserved.	0x0	R
		[2:0]	JRX_DL_204B_ECNT_TCH		Error Counters' Terminal Count hold enable for lanes (L-1) to 0. When set, the designated counter is to hold the Terminal Count value of 0xFF when it is reached until the counter is reset by the user. Otherwise the designated counter rolls over. .Each lane's counters are addressed as follows:	0x0	R/W
				--	[0] Bad Disparity Error (BD).		
				--	[1] Not-In-Table Error (NIT).		
				--	[2] Unexpected K-char. Error (UEK).		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x04EE to 0x04F5 by 1	JRX_DL_204B_20_LANEn	7	JRX_DL_204B_UEK		Unexpected K-character errors status for lanes [L-1:0]. 1=UEK has occurred. Per lane register addressing for each of these bits (0x04EE applies to Lane0, 0x04EF applies to Lane1, etc.).	0x0	R
		6	JRX_DL_204B_NIT		Not-In-Table errors status for all instantiated lanes (according to the "L" parameter) 1=NIT has occurred.	0x0	R
		5	JRX_DL_204B_ILS		Initial Lane Synchronization status for lanes [L-1:0], 1=ILAS passes.	0x0	R
		4	JRX_DL_204B_ILD		Inter-Lane De-skew status for lanes [L-1:0] 1= lanes are deskewed.	0x0	R
		3	JRX_DL_204B_FS		Frame Synchronization status for lanes [L-1:0] 1=Frame Synchronization is achieved.	0x0	R
		2	JRX_DL_204B_CKS		Computed CheckSum status for lanes [L-1:0] 1=checksum is correct.	0x0	R
		1	JRX_DL_204B_CGS		Code Group Synchronization status for lanes [L-1:0] 1=CGS is achieved.	0x0	R
		0	JRX_DL_204B_BDE		Bad Disparity errors status for lanes [L-1:0]. 1=BD has occurred.	0x0	R
0x04FE to 0x0505 by 1	JRX_DL_204B_19_LANEn	[7:0]	JRX_DL_204B_BD_CNT		Bad Disparity error counter. Per lane register addressing (0x04FE->Lane0, 0x04FF->Lane1, etc.).	0x0	R
0x050E to 0x0515 by 1	JRX_DL_204B_21_LANEn	[7:0]	JRX_DL_204B_UEK_CNT		Unexpected K-character error counter. Per lane register addressing (0x050E->Lane0, 0x050F->Lane1, etc.).	0x0	R
0x051E to 0x0525 by 1	JRX_DL_204B_22_LANEn	[7:0]	JRX_204B_NIT_CNT		Not-in-table error counter. Per lane register addressing (0x051E->Lane0, 0x051F->Lane1, etc.	0x0	R
0x055E	JRX_DL_204C_0	7	JRX_DL_204C_ENABLE		Enable/Disable 64b/66b Link Layer (204C).	0x0	R/W
				0	0 = Disable 64b/66b Link Layer (204C).		
				1	1 = Enable 64b/66b Link Layer (204C).		
		[6:4]	JRX_DL_204C_STATE		JRX state machine status.	0x0	R
				000	Reset.		
				010	Synchronization header alignment done.		
				011	Extended multiblock synchronization complete.		
				100	Extended multiblock alignment complete.		
				110	Link is up and running.		
		3	JRX_DL_204C_CLR_ERR_CNT		Clear all error counters.	0x0	R/W
		[2:0]	RESERVED		Reserved.	0x0	R
0x0562	JRX_DL_204C_4_LANEn	[7:0]	JRX_DL_204C_LANE_SKEW[7:0]		Relative lane skew in UI. Compare lanes for accurate skew.	0x0	R
0x056B	JRX_DL_204C_5_LANEn	7	JRX_DL_204C_LANE_SKEW[8]		Relative lane skew in UI. Compare lanes for accurate skew.	0x0	R
		[6:4]	RESERVED		Reserved.	0x0	R
		[3:0]	JRX_DL_204C_MB_ERR_CNT		Count of multiblock alignment errors	0x0	R
0x0574	JRX_DL_204C_6_LANEn	[7:6]	RESERVED		Reserved.	0x0	R
		[5:0]	JRX_DL_204C_SH_ERR_CNT		Count of block alignment errors	0x0	R
0x057C	JRX_DL_204C_7	[7:4]	JRX_DL_204C_EMB_ERR_CNT		Count of EMB alignment errors	0x0	R
0x057E	JRX_DL_204C_9	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	JRX_E_CFG		Number of MB in EMB(minus 1), (256*E)%F=0, E=LCM(F,256)/256	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0584-0x058B	JRX_DL_204C_10_LANEn	[7:0]	JRX_DL_204C_CRC_ERR_CNT		Per lane count of CRC parity errors0x0584 is lane0 CRC error count0x0585 is lane1 CRC error countetc	0x0	R
0x058C	JRX_CORE_1	7	JRX_SYSREF_FOR_RELINK	1	Lane data is masked after SYNC~ is asserted until another SYSREF pulse is received. Applies to 204B operation only. 1 = Device waits for the first SYSREF edge to arrive before bringing the link up instead of immediately locking to the incoming data stream.	0x0	R/W
		6	JRX_SYSREF_FOR_STARTUP		Lane data is masked until an incoming SYSREF phase has been established after reset. This prevents link operation without deterministic latency.	0x0	R/W
		[5:2]	RESERVED		Reserved.	0x0	R
		1	JRX_CHKSUM_LSB_ALG	0 1	JESD204B Receiver Checksum Algorithm (applies to 204B operation only). 0 = calculate checksum from 8 bit registers defined by JESD specification (0s included for unused bits). 1 = calculate checksum from individual fields.	0x0	R/W
		0	RESERVED		Reserved.	0x0	R
0x058D	JRX_CORE_2_LANE0	7	RESERVED		Reserved.	0x0	R
		6	JRX_LINK_LANE0_INVERSE		Per-lane control for inversing data on each physical lane.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		[4:0]	JRX_SRC_LANE0	000 001 010 011 100 101 110 111	Logical Lane 0 assignment. Logical Lane 0 assignment. 0 = from PHY lane 0, etc. Logical Lane 0 assignment. 1 = from PHY lane 1, etc. Logical Lane 0 assignment. 2 = from PHY lane 2, etc. Logical Lane 0 assignment. 3 = from PHY lane 3, etc. Logical Lane 0 assignment. 4 = from PHY lane 4, etc. Logical Lane 0 assignment. 5 = from PHY lane 5, etc. Logical Lane 0 assignment. 6 = from PHY lane 6, etc. Logical Lane 0 assignment. 7 = from PHY lane 7, etc.	0x0	R/W
0x058E	JRX_CORE_2_LANE1	7	RESERVED		Reserved.	0x0	R
		6	JRX_LINK_LANE1_INVERSE		Per-lane control for inversing data on each physical lane.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		[4:0]	JRX_SRC_LANE1	000 001 010 011	Logical Lane 1 assignment. Logical Lane 1 assignment. 0 = from PHY lane 0, etc. Logical Lane 1 assignment. 1 = from PHY lane 1, etc. Logical Lane 1 assignment. 2 = from PHY lane 2, etc. Logical Lane 1 assignment. 3 = from PHY lane 3, etc.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				100	Logical Lane 1 assignment. 4 = from PHY lane 4, etc.		
				101	Logical Lane 1 assignment. 5 = from PHY lane 5, etc.		
				110	Logical Lane 1 assignment. 6 = from PHY lane 6, etc.		
				111	Logical Lane 1 assignment. 7 = from PHY lane 7, etc.		
0x058F	JRX_CORE_2_LANE2	7	RESERVED		Reserved.	0x0	R
		6	JRX_LINK_LANE2_INVERSE		Per-lane control for inversing data on each physical lane.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		[4:0]	JRX_SRC_LANE2		Logical Lane 2 assignment.	0x0	R/W
				000	Logical Lane 2 assignment. 0 = from PHY lane 0, etc.		
				001	Logical Lane 2 assignment. 1 = from PHY lane 1, etc.		
				010	Logical Lane 2 assignment. 2 = from PHY lane 2, etc.		
				011	Logical Lane 2 assignment. 3 = from PHY lane 3, etc.		
				100	Logical Lane 2 assignment. 4 = from PHY lane 4, etc.		
				101	Logical Lane 2 assignment. 5 = from PHY lane 5, etc.		
				110	Logical Lane 2 assignment. 6 = from PHY lane 6, etc.		
				111	Logical Lane 2 assignment. 7 = from PHY lane 7, etc.		
0x0590	JRX_CORE_2_LANE3	7	RESERVED		Reserved.	0x0	R
		6	JRX_LINK_LANE3_INVERSE		Per-lane control for inversing data on each physical lane.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		[4:0]	JRX_SRC_LANE3		Logical Lane 3 assignment.	0x0	R/W
				000	Logical Lane 3 assignment. 0 = from PHY lane 0, etc.		
				001	Logical Lane 3 assignment. 1 = from PHY lane 1, etc.		
				010	Logical Lane 3 assignment. 2 = from PHY lane 2, etc.		
				011	Logical Lane 3 assignment. 3 = from PHY lane 3, etc.		
				100	Logical Lane 3 assignment. 4 = from PHY lane 4, etc.		
				101	Logical Lane 3 assignment. 5 = from PHY lane 5, etc.		
				110	Logical Lane 3 assignment. 6 = from PHY lane 6, etc.		
				111	Logical Lane 3 assignment. 7 = from PHY lane 7, etc.		
0x0591	JRX_CORE_2_LANE4	7	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		6	JRX_LINK_LANE4_INVERSE		Per-lane control for inversing data on each physical lane.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		[4:0]	JRX_SRC_LANE4		Logical Lane 4 assignment.	0x0	R/W
				000	Logical Lane 4 assignment. 0 = from PHY lane 0, etc.		
				001	Logical Lane 4 assignment. 1 = from PHY lane 1, etc.		
				010	Logical Lane 4 assignment. 2 = from PHY lane 2, etc.		
				011	Logical Lane 4 assignment. 3 = from PHY lane 3, etc.		
				100	Logical Lane 4 assignment. 4 = from PHY lane 4, etc.		
				101	Logical Lane 4 assignment. 5 = from PHY lane 5, etc.		
				110	Logical Lane 4 assignment. 6 = from PHY lane 6, etc.		
				111	Logical Lane 4 assignment. 7 = from PHY lane 7, etc.		
0x0592	JRX_CORE_2_LANE5	7	RESERVED		Reserved.	0x0	R
		6	JRX_LINK_LANE5_INVERSE		Per-lane control for inversing data on each physical lane.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		[4:0]	JRX_SRC_LANE5		Logical Lane 5 assignment.	0x0	R/W
				000	Logical Lane 5 assignment. 0 = from PHY lane 0, etc.		
				001	Logical Lane 5 assignment. 1 = from PHY lane 1, etc.		
				010	Logical Lane 5 assignment. 2 = from PHY lane 2, etc.		
				011	Logical Lane 5 assignment. 3 = from PHY lane 3, etc.		
				100	Logical Lane 5 assignment. 4 = from PHY lane 4, etc.		
				101	Logical Lane 5 assignment. 5 = from PHY lane 5, etc.		
				110	Logical Lane 5 assignment. 6 = from PHY lane 6, etc.		
				111	Logical Lane 5 assignment. 7 = from PHY lane 7, etc.		
0x0593	JRX_CORE_2_LANE6	7	RESERVED		Reserved.	0x0	R
		6	JRX_LINK_LANE6_INVERSE		Per-lane control for inversing data on each physical lane.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		[4:0]	JRX_SRC_LANE6		Logical Lane 6 assignment.	0x0	R/W
				000	Logical Lane 6 assignment. 0 = from PHY lane 0, etc.		
				001	Logical Lane 6 assignment. 1 = from PHY lane 1, etc.		
				010	Logical Lane 6 assignment. 2 = from PHY lane 2, etc.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				011	Logical Lane 6 assignment. 3 = from PHY lane 3, etc.		
				100	Logical Lane 6 assignment. 4 = from PHY lane 4, etc.		
				101	Logical Lane 6 assignment. 5 = from PHY lane 5, etc.		
				110	Logical Lane 6 assignment. 6 = from PHY lane 6, etc.		
				111	Logical Lane 6 assignment. 7 = from PHY lane 7, etc.		
0x0594	JRX_CORE_2_LANE7	7	RESERVED		Reserved.	0x0	R
		6	JRX_LINK_LANE7_INVERSE		Per-lane control for inversing data on each physical lane.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		[4:0]	JRX_SRC_LANE7		Logical Lane 7 assignment.	0x0	R/W
				000	Logical Lane 7 assignment. 0 = from PHY lane 0, etc.		
				001	Logical Lane 7 assignment. 1 = from PHY lane 1, etc.		
				010	Logical Lane 7 assignment. 2 = from PHY lane 2, etc.		
				011	Logical Lane 7 assignment. 3 = from PHY lane 3, etc.		
				100	Logical Lane 7 assignment. 4 = from PHY lane 4, etc.		
				101	Logical Lane 7 assignment. 5 = from PHY lane 5, etc.		
				110	Logical Lane 7 assignment. 6 = from PHY lane 6, etc.		
				111	Logical Lane 7 assignment. 7 = from PHY lane 7, etc.		
0x0596	GENERAL_JRX_CTRL	7	RESERVED		Reserved.	0x0	R/W
		6	LINK1_SYNCB_COMB_EN		link1 syncb output selection.	0x0	R/W
				0	0 = Normal operation.		
				1	1 = Combine link0 and link1 syncb signals as link1 syncb output.		
		5	LINK0_SYNCB_COMB_EN		link0 syncb output selection.	0x0	R/W
				0	0 = Normal operation.		
				1	1 = Combine link0 and link1 syncb signals as link1 syncb output.		
		4	RESERVED		Reserved.	0x0	R
		3	JRX_LINK_MODE		Single/Dual link selection.	0x0	R/W
				0	0 = Single link.		
				1	1 = Dual link.		
		2	JRX_LINK_SEPARATE_EN		Link0 and Link1 control.	0x0	R/W
				0	0 = Both links controlled by bit 0 of JRX_LINK_EN (0x0596[0]).		
				1	1 = Link0 and Link1 controlled independently by JRX_LINK_EN (0x0596[1:0]) bits 0 and 1 respectively.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[1:0]	JRX_LINK_EN		Bit 0 = link0, 0 = Disable link0, 1 = Enable link0 Bit 1 = link1, 0 = Disable link1, 1 = Enable link1 Bit 1 only enabled if JRX_LINK_SEPARATE_EN (0x0596[2]) = 1.	0x0	R/W
				0	Bit 0 = link0, 0 = Disable link0, 1 = Enable link0.		
				1	Bit 1 = link1, 0 = Disable link1, 1 = Enable link1; Bit 1 only enabled if JRX_LINK_SEPARATE_EN (0x0596[2]) = 1.		
0x0598	SYNCB_GEN_1	[7:4]	SYNCB_ERR_DUR		Duration of SYNCxOUTB± low for purpose of sync error report. Duration = (.5 + code) PCLK cycles. To most closely match spec, set this as close as possible to F/2 PCLK cycles. This is shared between SYNCOUTB0 and SYNCOUTB1. 0 = SYNCxOUTB± low for 0.5 PCLK cycles 1 = SYNCxOUTB± low for 1.5 PCLK cycles Etc.	0x0	R/W
		[3:0]	RESERVED		Reserved.	0x0	R
0x05AD	FIFO_STATUS_REG_0	[7:0]	LANE_FIFO_FULL		Bit x corresponds to FIFO full flag for data from SERDINx.	0x0	R
0x05AE	FIFO_STATUS_REG_1	[7:0]	LANE_FIFO_EMPTY		Bit x corresponds to FIFO empty flag for data from SERDINx.	0x0	R
0x05BB	JRX_204C_IRQ	[7:6]	RESERVED		Reserved.	0x0	R
		5	JRX_204C_SH_IRQ		JRX 204C SH IRQ status. After the number of block alignment errors is greater than the threshold, IRQ is created.	0x0	R/W
		4	JRX_204C_MB_IRQ		JRX 204C MB IRQ status. After the number of multiblock alignment errors is greater than the threshold, IRQ is created.	0x0	R/W
		3	JRX_204C_CRC_IRQ		JRX 204C CRC IRQ status. After the CRC error is detected, IRQ is created. 1 = CRC-12 mismatch between JTX and JRX.	0x0	R/W
		2	JRX_204C_SH_IRQ_ENABLE		JRX 204C SH IRQ enable.	0x0	R/W
				0	0: disable JRX_204C_SH_IRQ.		
				1	1: enable JRX_204C_SH_IRQ output.		
		1	JRX_204C_MB_IRQ_ENABLE		JRX 204C MB IRQ enable.	0x0	R/W
				0	0: disable JRX_204C_MB_IRQ.		
				1	1: enable JRX_204C_MB_IRQ output.		
		0	JRX_204C_CRC_IRQ_ENABLE			0x0	R/W
				0	0: disable CRC-12 mismatch interrupt;.		
				1	1 = Enable CRC-12 mismatch interrupt;.		
0x0600	JTX_CORE_0_CONV0	7	JTX_CONV_MASK_0		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_0		Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals.	0xF	R/W
				0000	0 = map virtual converter0 to DFOUT0.		
				0001	1 = map virtual converter0 to DFOUT1.		
				00--	- -.		
				00--	- -.		
				1111	15 = map virtual converter0 to DFOUT15.		
0x0601	JTX_CORE_0_CONV1	7	JTX_CONV_MASK_1		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[6:0]	JTX_CONV_SEL_1	0000 0001 00-- 00-- 1111	Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals. 0 = map virtual converter1 to DFOUT0. 1 = map virtual converter1 to DFOUT1. - -. - -. 15 = map virtual converter1 to DFOUT15.	0xF	R/W
0x0602	JTX_CORE_0_CONV2	7	JTX_CONV_MASK_2		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_2	0000 0001 00-- 00-- 1111	Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals. 0 = map virtual converter2 to DFOUT0. 1 = map virtual converter2 to DFOUT1. - -. - -. 15 = map virtual converter2 to DFOUT15.	0xF	R/W
0x0603	JTX_CORE_0_CONV3	7	JTX_CONV_MASK_3		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_3	0000 0001 00-- 00-- 1111	Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals. 0 = map virtual converter3 to DFOUT0. 1 = map virtual converter3 to DFOUT1. - -. - -. 15 = map virtual converter3 to DFOUT15.	0xF	R/W
0x0604	JTX_CORE_0_CONV4	7	JTX_CONV_MASK_4		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_4	0000 0001 00-- 00-- 1111	Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals. 0 = map virtual converter4 to DFOUT0. 1 = map virtual converter4 to DFOUT1. - -. - -. 15 = map virtual converter4 to DFOUT15.	0xF	R/W
0x0605	JTX_CORE_0_CONV5	7	JTX_CONV_MASK_5		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_5	0000 0001 00-- 00-- 1111	Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals. 0 = map virtual converter5 to DFOUT0. 1 = map virtual converter5 to DFOUT1. - -. - -. 15 = map virtual converter5 to DFOUT15.	0xF	R/W
0x0606	JTX_CORE_0_CONV6	7	JTX_CONV_MASK_6		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[6:0]	JTX_CONV_SEL_6		Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals.	0xF	R/W
				0000	0 = map virtual converter6 to DFOUT0.		
				0001	1 = map virtual converter6 to DFOUT1.		
				00--	- -.		
				00--	- -.		
				1111	15 = map virtual converter6 to DFOUT15.		
0x0607	JTX_CORE_0_CONV7	7	JTX_CONV_MASK_7		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_7		Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals.	0xF	R/W
				0000	0 = map virtual converter7 to DFOUT0.		
				0001	1 = map virtual converter7 to DFOUT1.		
				00--	- -.		
				00--	- -.		
				1111	15 = map virtual converter7 to DFOUT15.		
0x0608	JTX_CORE_0_CONV8	7	JTX_CONV_MASK_8		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_8		Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals.	0xF	R/W
				0000	0 = map virtual converter8 to DFOUT0.		
				0001	1 = map virtual converter8 to DFOUT1.		
				00--	- -.		
				00--	- -.		
				1111	15 = map virtual converter8 to DFOUT15.		
0x0609	JTX_CORE_0_CONV9	7	JTX_CONV_MASK_9		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_9		Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals.	0xF	R/W
				0000	0 = map virtual converter9 to DFOUT0.		
				0001	1 = map virtual converter9 to DFOUT1.		
				00--	- -.		
				00--	- -.		
				1111	15 = map virtual converter9 to DFOUT15.		
0x060A	JTX_CORE_0_CONV10	7	JTX_CONV_MASK_10		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_10		Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals.	0xF	R/W
				0000	0 = map virtual converter10 to DFOUT0.		
				0001	1 = map virtual converter10 to DFOUT1.		
				00--	- -.		
				00--	- -.		
				1111	15 = map virtual converter10 to DFOUT15.		
0x060B	JTX_CORE_0_CONV11	7	JTX_CONV_MASK_11		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[6:0]	JTX_CONV_SEL_11		Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals.	0xF	R/W
				0000	0 = map virtual converter11 to DFOUT0.		
				0001	1 = map virtual converter11 to DFOUT1.		
				00--	- -.		
				00--	- -.		
				1111	15 = map virtual converter11 to DFOUT15.		
0x060C	JTX_CORE_0_CONV12	7	JTX_CONV_MASK_12		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_12		Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals.	0xF	R/W
				0000	0 = map virtual converter12 to DFOUT0.		
				0001	1 = map virtual converter12 to DFOUT1.		
				00--	- -.		
				00--	- -.		
				1111	15 = map virtual converter12 to DFOUT15.		
0x060D	JTX_CORE_0_CONV13	7	JTX_CONV_MASK_13		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_13		Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals.	0xF	R/W
				0000	0 = map virtual converter13 to DFOUT0.		
				0001	1 = map virtual converter13 to DFOUT1.		
				00--	- -.		
				00--	- -.		
				1111	15 = map virtual converter13 to DFOUT15.		
0x060E	JTX_CORE_0_CONV14	7	JTX_CONV_MASK_14		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_14		Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals.	0xF	R/W
				0000	0 = map virtual converter14 to DFOUT0.		
				0001	1 = map virtual converter14 to DFOUT1.		
				00--	- -.		
				00--	- -.		
				1111	15 = map virtual converter14 to DFOUT15.		
0x060F	JTX_CORE_0_CONV15	7	JTX_CONV_MASK_15		Control for masking unused channels, 0: unmask, 1: mask.	0x1	R/W
		[6:0]	JTX_CONV_SEL_15		Converter sample crossbar selection. See Mux4 (JTX JESD Data Router) section. Per virtual-converter control for mapping to DFOUTx signals.	0xF	R/W
				0000	0 = map virtual converter15 to DFOUT0.		
				0001	1 = map virtual converter15 to DFOUT1.		
				00--	- -.		
				00--	- -.		
				1111	15 = map virtual converter15 to DFOUT15.		
0x0611	JTX_CORE_1	[7:6]	RESERVED		Reserved.	0x0	R/W
		[5:4]	JTX_LINK_204C_SEL		Link layer Select.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				00 01 else	0 = use 8b/10b Link Layer (204B). 1 = use 64b/66b Link Layer (204C). All other values are invalid.		
		[3:0]	RESERVED		Reserved.	0x0	R
0x061B	JTX_CORE_2_LANE0	7	JTX_LANE0_PD_STATUS	 0 1 --	JESD204B/C Transmitter Lane Power-Down Status. JTX_LANE0_PD_STATUS reflects the power status of the lane based on the JTX_LAN0E_ASSIGN setting. Physical lane in use based on link and crossbar configuration 0 = Lane in use. 1 = Lane is powered down. Per-lane control for each physical lane (for example, Register 0x061B for PHY Lane0, Register 0x61C for PHY Lane1, and so on.	0x0	R
		6	JTX_FORCE_LANE0_PD	 0 1	JESD204B/C Transmitter Force Power-Down. 0 = Lane power set by JTX_LANE_ASSIGN setting. 1 = Lane is off, Transmit 0s.	0x0	R/W
		5	JTX_LANE0_INV	 0 1	Invert JTx logical lane0 data. 0 = don't invert. 1 = invert logical polarity.	0x0	R/W
		[4:0]	JTX_LANE0_ASSIGN		0x061B-0x0622 bits 4:0 are per-lane control for setting the logical lane source (0-7) for each physical lane. (little endian – 0x061B assigns logical lane for PHY lane 0, etc.). PHY Lane 0 assignment. 0 = from Logical lane 0, etc.	0x7	R/W
0x061C	JTX_CORE_2_LANE1	7	JTX_LANE1_PD_STATUS		JESD204B/C Transmitter Lane Power-Down Status. JTX_LANE1_PD_STATUS reflects the power status of the lane based on the JTX_LANE1_ASSIGN setting. Physical lane in use based on link and crossbar configuration	0x0	R
		6	JTX_FORCE_LANE1_PD	 0 1	Sets the JTx logical lane source (0-7) for each JTx physical lane. (little endian – 0x061B assigns logical lane for PHY lane 0). 0 = Lane power set by JTX_LANE_ASSIGN setting. 1 = Lane is off, Transmit 0s.	0x0	R/W
		5	JTX_LANE1_INV	 0 1	Invert JTx logical lane1 data. 0 = don't invert. 1 = invert logical polarity.	0x0	R/W
		[4:0]	JTX_LANE1_ASSIGN		PHY Lane 1 assignment. 1 = from Logical lane 1, etc. Lane crossbar selection. Setting here selects which logical lane should feed the physical lane.	0x7	R/W
0x061D	JTX_CORE_2_LANE2	7	JTX_LANE2_PD_STATUS		JESD204B/C Transmitter Lane Power-Down Status. JTX_LANE2_PD_STATUS reflects the power status of the lane based on the JTX_LANE2_ASSIGN setting. Physical lane in use based on link and crossbar configuration	0x0	R
		6	JTX_FORCE_LANE2_PD	 0 1	Sets the JTx logical lane source (0-7) for each JTx physical lane. (little endian – 0x061B assigns logical lane for PHY lane 0). 0 = Lane power set by JTX_LANE_ASSIGN setting. 1 = Lane is off, Transmit 0s.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		5	JTX_LANE2_INV	0 1	Invert JTx logical lane2 data. 0 = don't invert. 1 = invert logical polarity.	0x0	R/W
		[4:0]	JTX_LANE2_ASSIGN		PHY Lane 2 assignment. 2 = from Logical lane 2, etc. Lane crossbar selection. Setting here selects which logical lane should feed the physical lane.	0x7	R/W
0x061E	JTX_CORE_2_LANE3	7	JTX_LANE3_PD_STATUS		JESD204B/C Transmitter Lane Power-Down Status. JTX_LANE3_PD_STATUS reflects the power status of the lane based on the JTX_LANE3_ASSIGN setting. Physical lane in use based on link and crossbar configuration	0x0	R
		6	JTX_FORCE_LANE3_PD	0 1	Sets the JTx logical lane source (0-7) for each JTx physical lane. (little endian – 0x061B assigns logical lane for PHY lane 0). 0 = Lane power set by JTX_LANE_ASSIGN setting. 1 = Lane is off, Transmit 0s.	0x0	R/W
		5	JTX_LANE3_INV	0 1	Invert JTx logical lane3 data. 0 = don't invert. 1 = invert logical polarity.	0x0	R/W
		[4:0]	JTX_LANE3_ASSIGN		PHY Lane 3 assignment. 3 = from Logical lane 3, etc. Lane crossbar selection. Setting here selects which logical lane should feed the physical lane.	0x7	R/W
0x061F	JTX_CORE_2_LANE4	7	JTX_LANE4_PD_STATUS		JESD204B/C Transmitter Lane Power-Down Status. JTX_LANE4_PD_STATUS reflects the power status of the lane based on the JTX_LANE4_ASSIGN setting. Physical lane in use based on link and crossbar configuration	0x0	R
		6	JTX_FORCE_LANE4_PD	0 1	Sets the JTx logical lane source (0-7) for each JTx physical lane. (little endian – 0x061B assigns logical lane for PHY lane 0). 0 = Lane power set by JTX_LANE_ASSIGN setting. 1 = Lane is off, Transmit 0s.	0x0	R/W
		5	JTX_LANE4_INV	0 1	Invert JTx logical lane4 data. 0 = don't invert. 1 = invert logical polarity.	0x0	R/W
		[4:0]	JTX_LANE4_ASSIGN		PHY Lane 4 assignment. 4 = from Logical lane 4, etc. Lane crossbar selection. Setting here selects which logical lane should feed the physical lane.	0x7	R/W
0x0620	JTX_CORE_2_LANE5	7	JTX_LANE5_PD_STATUS		JESD204B/C Transmitter Lane Power-Down Status. JTX_LANE5_PD_STATUS reflects the power status of the lane based on the JTX_LANE5_ASSIGN setting. Physical lane in use based on link and crossbar configuration	0x0	R
		6	JTX_FORCE_LANE5_PD	0 1	Sets the JTx logical lane source (0-7) for each JTx physical lane. (little endian – 0x061B assigns logical lane for PHY lane 0). 0 = Lane power set by JTX_LANE_ASSIGN setting. 1 = Lane is off, Transmit 0s.	0x0	R/W
		5	JTX_LANE5_INV	0 1	Invert JTx logical lane5 data. 0 = don't invert. 1 = invert logical polarity.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[4:0]	JTX_LANE5_ASSIGN		PHY Lane 5 assignment. 5 = from Logical lane 5, etc. Lane crossbar selection. Setting here selects which logical lane should feed the physical lane.	0x7	R/W
0x0621	JTX_CORE_2_LANE6	7	JTX_LANE6_PD_STATUS		JESD204B/C Transmitter Lane Power-Down Status. JTX_LANE6_PD_STATUS reflects the power status of the lane based on the JTX_LANE6_ASSIGN setting. Physical lane in use based on link and crossbar configuration	0x0	R
		6	JTX_FORCE_LANE6_PD		Sets the JTx logical lane source (0-7) for each JTx physical lane. (little endian – 0x061B assigns logical lane for PHY lane 0).	0x0	R/W
				0	0 = Lane power set by JTX_LANE_ASSIGN setting.		
				1	1 = Lane is off, Transmit 0s.		
		5	JTX_LANE6_INV		Invert JTx logical lane6 data.	0x0	R/W
				0	0 = don't invert.		
				1	1 = invert logical polarity.		
		[4:0]	JTX_LANE6_ASSIGN		PHY Lane 6 assignment. 6 = from Logical lane 6, etc. Lane crossbar selection. Setting here selects which logical lane should feed the physical lane.	0x7	R/W
0x0622	JTX_CORE_2_LANE7	7	JTX_LANE7_PD_STATUS		JESD204B/C Transmitter Lane Power-Down Status. JTX_LANE7_PD_STATUS reflects the power status of the lane based on the JTX_LANE7_ASSIGN setting. Physical lane in use based on link and crossbar configuration	0x0	R
		6	JTX_FORCE_LANE7_PD		Sets the JTx logical lane source (0-7) for each JTx physical lane. (little endian – 0x061B assigns logical lane for PHY lane 0).	0x0	R/W
				0	0 = Lane power set by JTX_LANE_ASSIGN setting.		
				1	1 = Lane is off, Transmit 0s.		
		5	JTX_LANE7_INV		Invert JTx logical lane7 data.	0x0	R/W
				0	0 = don't invert.		
				1	1 = invert logical polarity.		
		[4:0]	JTX_LANE7_ASSIGN		PHY Lane 7 assignment. 7 = from Logical lane 7, etc. Lane crossbar selection. Setting here selects which logical lane should feed the physical lane.	0x7	R/W
0x0624	JTX_CORE_3	[7:6]	RESERVED		Reserved.	0x0	R/W
		[5:4]	JTX_TEST_GEN_SEL		Enables and selects the test pattern insertion point.	0x3	R/W
				00	0 = insert pattern before transport layer.		
				01	1 = insert pattern before PHY layer.		
				10	2 = insert pattern before link layer.		
				11	3 = JTx test pattern generation is not enabled.		
		[3:0]	JTX_TEST_GEN_MODE		Selects the data pattern to be generated.	0x0	R/W
				0001	1 = CHECKER_BOARD.		
				0010	2 = WORD_TOGGLE.		
				0011	3 = PN31.		
				0101	5 = PN15.		
				0111	7 = PN7.		
				1000	8 = RAMP.		
				1110	14 = Repeat user data pattern as programmed via jtx_test_user_data[65:0].		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				1111 else	15 = Transmit single occurrence of user data pattern as programmed via jtx_test_user_data[65:0] Else = Not valid. Else = Not valid.		
0x0625	JTX_CORE_4	[7:0]	JTX_TEST_USER_DATA[7:0]		User-programmable data pattern (up to 66 bits).	0x0	R/W
0x0626	JTX_CORE_5	[7:0]	JTX_TEST_USER_DATA[15:8]		User-programmable data pattern (up to 66 bits).	0x0	R/W
0x0627	JTX_CORE_6	[7:0]	JTX_TEST_USER_DATA[23:16]		User-programmable data pattern (up to 66 bits).	0x0	R/W
0x0628	JTX_CORE_7	[7:0]	JTX_TEST_USER_DATA[31:24]		User-programmable data pattern (up to 66 bits).	0x0	R/W
0x0629	JTX_CORE_8	[7:0]	JTX_TEST_USER_DATA[39:32]		User-programmable data pattern (up to 66 bits).	0x0	R/W
0x062A	JTX_CORE_9	[7:0]	JTX_TEST_USER_DATA[47:40]		User-programmable data pattern (up to 66 bits).	0x0	R/W
0x062B	JTX_CORE_10	[7:0]	JTX_TEST_USER_DATA[55:48]		User-programmable data pattern (up to 66 bits).	0x0	R/W
0x062C	JTX_CORE_11	[7:0]	JTX_TEST_USER_DATA[63:56]		User-programmable data pattern (up to 66 bits).	0x0	R/W
0x062D	JTX_CORE_12	[7:5]	JTX_SYNC_N_SEL	0 1	SYNC~ crossbar selection, Selects which SYNCxINB± pin to source the SYNC_IN signal. Ignored when JTX_NUM_LINKS == 1;. 0 = SYNC0INB±. 1 = SYNC1INB±.	0x0	R/W
		[4:2]	RESERVED		Reserved.	0x0	R
		[1:0]	JTX_TEST_USER_DATA[65:64]		User-programmable data pattern (up to 66 bits).	0x0	R/W
0x062E	JTX_CORE_13	[7:1]	RESERVED		Reserved.	0x0	R
		0	JTX_LINK_EN	0 1	link enable. This bit field enables the clock generation for DDC, JTX. 0: link is disabled. 1: link is enabled.	0x0	R/W
0x0630	JTX_TPL_0	[7:3]	RESERVED		Reserved.	0x7	R/W
		2	JTX_CONV_ASYNCHRONOUS		JESD204B/C Transport Layer mode is asynchronous. This bit identifies asynchronous modes and should be set according the JTx Mode tables in the JESD204B/C Transmitter Mode Tables section.	0x0	R/W
		1	JTX_TPL_TEST_EN	0 1	Long transport layer (LTPL) data pattern enable. 0 = LTPL disabled. 1 = LTPL enabled.	0x0	R/W
		0	RESERVED		Reserved.	0x0	R/W
0x0632	JTX_TPL_2	[7:0]	JTX_TPL_PHASE_ADJUST[7:0]		JTx tranport layer LMFC phase adjust. Used to delay the transport layer LMFC/LEMC relative to the device “local” LMFC/LEMC in JTx_sample_clock cycles. Output LMFC phase adjustment in conv_clk cycles. Maximum value is k*s/ns-1	0x0	R/W
0x0633	JTX_TPL_3	[7:0]	JTX_TPL_PHASE_ADJUST[15:8]		JTx tranport layer LMFC phase adjust. Used to delay the transport layer LMFC/LEMC relative to the device “local” LMFC/LEMC in JTx_sample_clock cycles. Output LMFC phase adjustment in conv_clk cycles. Maximum value is k*s/ns-1	0x0	R/W
0x0634	JTX_TPL_4	[7:0]	JTX_TPL_TEST_NUM_FRAMES[7:0]		Number of frames (minus 1) in the long transport layer test pattern.	0x0	R/W
0x0635	JTX_TPL_5	[7:0]	JTX_TPL_TEST_NUM_FRAMES[15:8]		Number of frames (minus 1) in the long transport layer test pattern.	0x0	R/W
0x0636	JTX_TPL_6	7	JTX_TPL_SYSREF_IGNORE_WHEN_LINKED		See field documentation. Mask incoming SYSREF when SYNC~ is de-asserted. Applies to 204B operation only.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		6	JTX_TPL_SYSREF_CLR_PHASE_ERR		Clear jtx_tpl_sysref_phase_err.	0x0	R/W
		5	JTX_TPL_SYSREF_MASK		Mask the SYSREF input for subclass 0 operation.	0x0	R/W
				0	0 = SYSREF is not masked (subclass 1 mode).		
				1	1 = SYSREF is masked (subclass 0 mode).		
		[4:3]	RESERVED		Reserved.	0x0	R
		2	JTX_TPL_SYSREF_PHASE_ERR		Incoming SYSREF has been registered at an unexpected time. Incoming SYSREF has been registered at an unexpected time from the previously established SYSREF phase	0x0	R
		1	JTX_TPL_SYSREF_RCVD		SYSREF phase has been established.	0x0	R
		0	JTX_TPL_INVALID_CFG		Input cfg not supported. Input cfg not supported according to JTX_VALID_S_NS_F_NP	0x0	R
0x0638	JTX_TPL_8	[7:0]	JTX_TPL_LATENCY_ADDED		See field documentation. Latency through the buffer has been added by this amount from the starting value of jtx_tpl_latency_adjust. This may increment on LEMC boundaries until buffer under-run is resolved. jtx_conv_asynchronous causes this value to be static.	0x0	R
0x0639	JTX_TPL_9	[7:0]	JTX_TPL_BUF_FRAMES		Frame delay through transport layer buffer.	0x0	R
0x063B	JTX_L0_1	[7:4]	JTX_ADJCNT_CFG		Number of adjustment resolution steps. Number of adjustment resolution steps to adjust DAC LMFC. Applies to Subclass 2 operation only	0x0	R/W
		[3:0]	JTX_BID_CFG		Bank ID Extension to DID.	0x0	R/W
0x063D	JTX_L0_3	7	JTX_SCR_CFG		JTx Scrambler enable.	0x0	R/W
				0	0 = Scrambling disabled.		
				1	1 = Scrambling enabled (mandatory if using 64b/66b Link Layer).		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	JTX_L_CFG		JTx number of lanes per link + 1.	0x0	R/W
				0	0 = 1 lane.		
				1	1 = 2 lanes, etc.		
				Else	Values of 4, 6 and ≥ 8 are not valid.		
0x063E	JTX_L0_4	[7:0]	JTX_F_CFG		JTx number of octets per frame (F = JTX F configuration + 1). Number of octets per frame per lane.	0x0	R/W
				0x00	0 = 1 octet.		
				0x01	1 = 2 octets.		
				0x02	2 = 3 octets.		
				0x03	3 = 4 octets.		
				0x05	5 = 6 octets.		
				0x07	7 = 8 octets.		
				0x0B	11 = 12 octets.		
				0x0F	15 = 16 octets.		
				0x17	23 = 24 octets.		
				else	All other values are invalid.		
0x063F	JTX_L0_5	[7:0]	JTX_K_CFG		JTx number of frames per multiframe (K = JTX K configuration + 1). Only values where F × K is divisible by 4 can be used.	0x0	R/W
0x0640	JTX_L0_6	[7:0]	JTX_M_CFG		JTx number of virtual converters per link (M=JTX M configuration + 1).	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0000	0 = 1 virtual converter.		
				0001	1 = 2 virtual converters.		
				0010	2 = 3 virtual converters.		
				0011	3 = 4 virtual converters.		
				0100	5 = 6 virtual converters.		
				0101	7 = 8 virtual converters.		
				0110	11 = 12 virtual converters.		
				0111	15 = 16 virtual converters.		
				else	All other values are invalid.		
0x0641	JTX_L0_7	[7:6]	JTX_CS_CFG		Number of control bits (CS) per sample.	0x0	R/W
				00	0 = No control bits (CS = 0).		
				01	1 = 1 control bit (CS = 1), Control bit 2 only.		
				10	2 = 2 control bits (CS = 2), Control bits 2 and 1 only.		
				11	3 = 3 control bits (CS = 3), all control bits (Control Bits 2, 1, and 0).		
		5	RESERVED		Reserved.	0x0	R
		[4:0]	JTX_N_CFG		ADC converter resolution (N = JTX N configuration + 1).	0x0	R/W
				00111	7 = 8-bit resolution		
				01000	8 = 9-bit resolution		
				01001	9 = 10-bit resolution		
				01010	10 = 11-bit resolution		
				01011	11 = 12-bit resolution.		
				01100	12 = 13-bit resolution		
				01101	13 = 14-bit resolution		
				01110	14 = 15-bit resolution		
				01111	15 = 16-bit resolution.		
					All other values are invalid.		
0x0642	JTX_L0_8	[7:5]	JTX_SUBCLASSV_CFG		Sets the subclass operation for the JTx. Device Subclass Version	0x0	R/W
					2: align transmission and LMFC boundaries to SYNC~		
					1: align transmission and LMFC boundaries to sysref		
					0: transmission and LMFC boundaries are arbitrary		
				000	000 = subclass 0.		
				001	001 = subclass 1.		
				Else	010 -111 are invalid.		
		[4:0]	JTX_NP_CFG		ADC number of bits per sample(N').	0x0	R/W
				01011	11 = 12-bits.		
				01111	15 = 16-bits.		
				10111	23 = 24-bits.		
					All other values are invalid.		
0x0643	JTX_L0_9	[7:5]	JTX_JESDV_CFG		Reflects the JESD204x version. This is only used to populate the “JESDV” field in the Link configuration parameters that are sent across the link during the second multiframe of ILAS when the 8b/10b link layer is used (therefore, does not apply to JESD204C).	0x0	R/W
				000	000 = JESD204A.		
				001	001 = JESD204B.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				Else	All other values are invalid.		
		[4:0]	JTX_S_CFG		Samples per converter frame cycle (S = JTX S configuration + 1).	0x0	R/W
				000	0 = 1 samples per converter.		
				001	1 = 2 samples per converter.		
				011	3 = 4 samples per converter.		
				111	7 = 8 samples per converter.		
				Else	All other values are invalid.		
0x0644	JTX_L0_10	7	JTX_HD_CFG		Reflects the status of the JESD204 high density (HD) mode (indicates when converter samples are split across multiple lanes. This is only used to populate the “HD” field in the Link configuration parameters that are sent across the link during the second multiframe of ILAS when the 8b/10b link layer is used.	0x0	R/W
				0	0 = Samples are not split across lanes.		
				1	1 = Samples are split across 2 lanes.		
				Else	All other values are invalid.		
		[6:0]	RESERVED		Reserved.	0x0	R
0x0650 to 0x0657 by 1	JTX_L0_14_LANEn	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	JTX_LID_CFG		Lane identification number (within link).	0x0	R/W
0x0659	JTX_DL_204B_0	[7:1]	RESERVED		Reserved.	0x0	R/W
		0	JTX_DL_204B_BYP_ACG_CFG		Alignment character generation bypass. 1 = bypass alignment character generation (204B).	0x0	R/W
0x065C	JTX_DL_204B_3	7	JTX_DL_204B_CLEAR_SYNC_NE_ COUNT		Clear counter of SYNC~ falling edges.	0x0	R/W
		6	JTX_DL_204B_TESTMODE_IGNORE_ SYNCN_CFG		ignore sync_n input during D21.5 and RPAT modes.	0x0	R/W
		5	JTX_DL_204B_SYNC_N		JESD204 Frame Sync. Active low. Synchronous upon rising edge pclk. 0=transmit code group sync (K characters).	0x0	R
				--	Subclass 0: Internal LMFC held in reset by sync_n=0.		
				--	Subclass 1: Internal LMFC reset for 1-pclk by falling edge sync_n.		
		4	JTX_DL_204B_TPL_TEST_EN_CFG		Turn on JESD Pattern Sequence test mode.	0x0	R/W
		3	RESERVED		Reserved.	0x0	R
		[2:1]	JTX_DL_204B_RJSPAT_SEL_CFG		High Frequency Patterns Test Mode configuration.	0x0	R/W
				00	00 = RPAT Sequence.		
				01	01 = JSPAT Sequence.		
				10	10 = JTSPAT Sequence.		
				11	11 = Unused.		
		0	JTX_DL_204B_RJSPAT_EN_CFG		Enable RPAT/JSPAT/JTSPAT Generator. Enable RPAT/JSPAT/JTSPAT Generator.	0x0	R/W
				0	0 = off.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				1	1 = on (Note: Must also set JTX_DL_204B_PHY_DATA_SEL_CFG, 0x065F[2] = 1).		
0x065D	JTX_DL_204B_4	7	JTX_DL_204B_SYNC_N_FORCE_EN		1 = Force SYNCxINB signal to value specified in 0x065D[6].	0x0	R/W
		6	JTX_DL_204B_SYNC_N_FORCE_VAL		SYNCxINB logic if force enabled (0x065D[7] = 1). '0' or '1'.	0x0	R/W
		[5:4]	RESERVED		Reserved.	0x0	R
		[3:0]	JTX_DL_204B_STATE		QBF State status. Description from tx_sm rtl CGS, //0 ILA_M0R, //1 ILA_M0, //2 ILA_M1R, //3 ILA_M1C1, //4 ILA_M1C2, //5 ILA_M1C3, //6 ILA_M1, //7 ILA_M2R, //8 ILA_M2, //9 ILA_M3R, //A ILA_M3, //B ILA_BP, //C UDATA //D	0x0	R
0x0667	JTX_DL_204C_0	[7:1]	RESERVED		Reserved.	0x0	R
		0	JTX_CRC_REVERSE_CFG		1 = Reverse bit ordering of CRC in metaword (204C).	0x0	R/W
0x0668	JTX_DL_204C_1	[7:0]	JTX_E_CFG		Number of multiblocks in extended multiblock (minus 1). 204C mode only. Number of multiblocks in extended multiblock (minus 1). (256 * EMB) % F = 0, EMB = LCM(F, 256) / 256 00 0 = 1 multiblock in the extended multiblock. 10 2 = 3 multiblocks in the extended multiblock. Else All other values are invalid.	0x0	R/W
0x0670 to 0x0677 by 1	JTX_PHY_IFX_0_LANEn	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	JTX_BR_LOG2_RATIO		For receiver only operation and AD9207 and AD9209: 0000 0 = no bit repeat, for lane rates > 8 Gbps 0001 1 = 2×bit repeat, for lane rates > 4 Gbps and ≤ 8 Gbps 0010 2 = 4×bit repeat, for lane rates > 2 Gbps and ≤ 4 Gbps 0011 3 = 8×bit repeat, for lane rates ≥ 1 Gbps and ≤ 2 Gbps Else = not validFor transmit and receive operation, JTX_BR_LOG2_RATIO is set such that the bit rate is > 8Gbps OR equal to the JRx bit rate, whichever yields the greater ratio value.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0000 0001 0010 0011	0 = no bit repeat, JESD204B/C receive to JESD204B/C transmit lane rate ratio is 1:1 and JTx lane rate > 8Gbps 1 = 2×bit repeat, JESD204B/C receive to JESD204B/C transmit lane rate ratio is 2:1 or JTx lane rate is > 4 Gbps and ≤ 8 Gbps 2 = 4×bit repeat, JESD204B/C receive to JESD204B/C transmit lane rate ratio is 4:1 or JTx lane rate is > 2 Gbps and ≤ 4 3 = 8×bit repeat, JESD204B/C receive to JESD204B/C transmit lane rate ratio is 8:1 or JTx lane rate is ≥ 1 Gbps and ≤ 2 Gbps		
0x0701	PLL_STATUS	7	JTX_PLL_LOCKED		PLL Locked Status Bit.	0x0	R
		[7:0]	RESERVED	0010	Reserved.	0x0	R
0x0702	JTX_QUICK_CFG	[7:6]	JTX_MODE_S_SEL	0011	Select the 'S' value for the JESD mode enable by JTX_QUICK_CFG. See JTX JESD204B/C mode tables. Not valid for AD9081, AD9082, AD9207, and AD9209.	0x0	R/W
		[5:0]	JTX_MODE		Quick configuration setting for JESD204B/C transmitter parameters according to "JESD204B_Mode" and "JESD204C_Mode" numbers in the mode tables in the "JESD204B/C Transmitter Mode Tables" section. Not valid for AD9081, AD9082, AD9207, and AD9209.	0x1	R/W
0x0703	JTX_LINK_CTRL1	[7:1]	RESERVED		Reserved.	0x0	R
		0	JTX_LANE_PD_STATUS	0 1	JTX lane power-down status. Reflects power status of lane based on the JTX_LANE_ASSIGN setting Per-lane control for each physical lane. (little endian – 0x061B controls PHY lane 0, etc.). 0 = lane in use. 1 = lane is powered down.	0x0	R/W
0x0706	JTX_SER_CLK_INVERT	7	RESERVED		Reserved.	0x0	R
		6	LOOPBACK_JTX_CONV_CLK_INVERT		Loopback 3 conv_clk clock invert.	0x0	R/W
		5	LOOPBACK_JTX_LANE_CLK_INVERT		Loopback 1 ifx_clk clock invert.	0x0	R/W
		4	LOOPBACK_JTX_LINK_CLK_INVERT		Loopback 2 link_pclk clock invert.	0x0	R/W
		[3:1]	RESERVED		Reserved.	0x0	R
		0	JTX_SER_CLK_INVERT	0 1	JTX serial clock invert in dout;. Don't invert the serial clock at the data output. Invert the serial clock at the data output.	0x0	R/W
0x070A	RESET_CTRL_REG	[7:1]	RESERVED		Reserved.	0x0	R
		0	JTX_SER_BITFIELD		This bit must be set to 1 if in the device is in an asynchronous (ASYNC) mode. See JESD204B/C mode tables in the "JESD204B/C Transmitter Mode Tables" and "JESD204B/C Receiver Mode Tables" sections.	0x0	R/W
0x0710	FORCE_LINK_RESET_REG	[7:5]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		4	FORCE_LINK_DIGITAL_RESET	0 1	Resets the JTx link. This bit field is used to reset each link independently. 0 = disable reset. 1 = force reset.	0x0	R/W
		[3:1]	RESERVED		Reserved.	0x0	R
		0	FORCE_LINK_RESET	0 1	Resets the JTx link0 and link1 independently (must use JTX_LINK_PAGE bit). 0 = disable reset. 1 = force reset.	0x1	R/W
0x0711	QC_MODE_STATUS	[7:1]	RESERVED		Reserved.	0x0	R
		0	JTX_INVALID_MODE		Invalid mode bit.	0x0	R
0x0712	K_EMB_QC_OVERRIDE	[7:1]	RESERVED		Reserved.	0x0	R
		0	JTX_K_EMB_QC_OVERRIDE		k_emb qc values override in qc mode.	0x0	R/W
0x0713	PHASE_ESTABLISH_STATUS	[7:1]	RESERVED		Reserved.	0x0	R
		0	JTX_PHASE_ESTABLISHED		phase established readback.	0x0	R
0x0717	PLL_REF_CLK_DIV1_REG	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DIVM_LCPLL_RC_RX	00 01 Else	Lane rate selections based on 204B and 204C. Selects output division rate; 0->no divider, 1->divide by 2Replica of divm_lcpll_rc in SERDES lcpll regmap If in 204B mode: 0 = Lane rate > 8Gbps, 1= Lane rate ≤ 8Gbps. If in 204C mode: 0 = Lane rate ≤ 16Gbps, 1= Lane rate > 16Gbps. All other values are invalid.	0x2	R/W
0x0720	LCPLL_RST	[7:1]	RESERVED		Reserved.	0x0	R
		0	RSTB_LCPLL_RC		Force link reset from Regmap.	0x0	R/W
0x0721	PLL_ENABLE_CTRL	[7:6]	RESERVED		Reserved.	0x0	R
		5	LCPLL_JTX_PLL_BYPASS_LOCK		Bypass PLL lock input.	0x0	R/W
		[4:1]	RESERVED		Reserved.	0x0	R
		0	PWRUP_LCPLL		Power up PLL. Power up PLL, starts LDO, Starts Calibration, sends out PLL locked when done. Set to 1 to force power up - will not read back correctly if PLL is powered up internally.	0x0	R/W
0x0722	PLL_STATUS	[7:5]	RESERVED		Reserved.	0x0	R
		4	LOSSLOCK_LCPLL_RS	0 1	SERDES PLL Loss of Lock. 0 = SERDES PLL did not lose lock. 1 = SERDES PLL lost lock.	0x0	R
		3	RFPLLLOCK_LCPLL_RS	0 1	SERDES PLL Lock. 0 = SERDES PLL is not locked. 1 = SERDES PLL is locked.	0x0	R
		[2:1]	RESERVED		Reserved.	0x0	R
		3	RFPLLLOCK_LCPLL_RS		PLL is locked when this bit is HIGH.	0x0	R
0x0726	PLL_ENCAL	[7:1]	RESERVED		Reserved.	0x0	R
		0	FIXED SERDES PLL BIT FIELD		This bit must be kept at its default state of 1b'0.	0x0	R/W
0x0727	LCPLL_REF_CLK_DIV1_REG	7	RESERVED		Reserved.	0x0	R/W
		6	SERDES PLL BIT FIELD_1		This bitfield value is set based on Lane rate.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0	Set to 0 for lane rates ≤ 8Gbps.		
				1	Set to 1 for lane rates above 8Gbps.		
		[5:4]	SERDES PLL BIT FIELD_10			0x2	R/W
				--	If in 204B mode: set to 1 for lane rates ≤ 8Gbps and set to 0 for lane rates > 8Gbps.		
				--	If in 204C mode: set to 1 for lane rates ≤ 16Gbps and set to 0 for lane rates > 16Gbps.		
		3	RESERVED		Reserved.	0x0	R
		[2:0]	SERDES PLL BIT FIELD_0			0x2	R/W
				--	If in 204B mode: set to 0 for lane rates ≤ 8Gbps and set to 1 for lane rates > 8Gbps.		
				--	If in 204C mode: set to 0 for lane rates ≤ 16Gbps and set to 1 for lane rates > 16Gbps.		
0x0728	PLL_DIV2	[7:0]	SERDES PLL BIT FIELD_9		For Tx-only operating 204B modes:. For Tx-only or full-chip operating 204B modes: 40 = 1Gpbs ≤ Lane rate < 2Gbps 20 = 2Gpbs ≤ Lane rate < 4Gbps 10 = 4Gpbs ≤ Lane rate < 8Gbps If ""F"" is a power of 2 30 = 4Gpbs ≤ Lane rate < 8Gbps If ""F"" is not a power of 2 5 = 8Gpbs ≤ Lane rate < 16Gbps if ""F"" is a power of 2 15 = 8Gpbs ≤ Lane rate < 16Gbps if ""F"" is a power of 2 For Tx-only operating 204C modes: 22 = 6Gpbs ≤ Lane rate < 8Gbps 11 = Lane rate > 8Gbps If ""F"" is a power of 2 33 = Lane rate > 8Gbps If ""F"" is not a power of 2 For simultaneous Rx only operation or when using AD9207 or AD9209, refer to the JTX mode tables in the "JESD204B/C Transmitter Mode Tables" section of the user guide for the appropriate setting.	0x5	R/W
0x072A	PLL_DIVOVD	[7:4]	RESERVED		Reserved.	0x0	R
		3	SERDES PLL BIT FIELD_6		Must be set to 1.	0x1	R/W
		2	SERDES PLL BIT FIELD_5		Must be set to 1.	0x1	R/W
		1	SERDES PLL BIT FIELD_4		Must be set to 1.	0x1	R/W
		0	SERDES PLL BIT FIELD_3		Must be set to 1.	0x1	R/W
0x072B	PLL_RXDIVRATE	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	SERDES PLL BIT FIELD_7		This register value to be set based on Lane rate.	0x8	R/W
				0x0	Set to 0 for lane rates between 4 and 8 Gbps.		
				0x1	Set to 1 for lane rates ≤ 4 Gbps.		
				0x8	Set to 8 for lane rates above 8Gbps.		
0x072D	PLL_REFCLK_CPL	[7:2]	RESERVED		Reserved.	0x0	R
		1	SERDES PLL BIT FIELD_8		Must be set to 0. Enables additional /3 on input reference clock to PLL.	0x0	R/W
		0	RESERVED		Reserved.	0x1	R/W
0x0740	CBUS_ADDR	[7:0]	CBUS_ADDR_LCPLL_RC		Control bus address select.	0x0	R/W
0x0741	CBUS_WDATA	[7:0]	CBUS_WDATA_LCPLL_RC		Control Bus data,. Control Bus data, channel selected with cbus_wstrobe_ser signal	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0750	PWR_DN	[7:0]	PD_SER[7:0]		Power down serializer channel, Bit per channel (<0>=ch0, <1>=ch1 ..etc.) 1= channel off,.	0xFF	R/W
0x0751	PWR_DN2	[7:0]	PD_SER[15:8]		Power down serializer channel, Bit per channel (<0>=ch0, <1>=ch1 ..etc.) 1= channel off,.	0xFF	R/W
0x0752	JTX_SWING	7	RESERVED		Reserved.	0x0	R
		[6:4]	JTX_LANE1_SWING		Sets the output swing level relative to the SVDD1 supply.	0x1	R/W
				000	000 = 1.0 x SVDD1.		
				001	001 = 0.85 x SVDD1.		
				010	010 = 0.75 x SVDD1.		
				011	011 = 0.50 x SVDD1.		
				1xx	1xx = invalid.		
		3	RESERVED		Reserved.	0x0	R
		[2:0]	JTX_LANE0_SWING		Sets the output swing level relative to the SVDD1 supply. Output swing level for JESD, 0=1.0*VTT, 1=0.850*VTT, 2=0.750*VTT, 3=0.500*VTT	0x1	R/W
				000	000 = 1.0 x SVDD1.		
				001	001 = 0.85 x SVDD1.		
				010	010 = 0.75 x SVDD1.		
				011	011 = 0.50 x SVDD1.		
				1xx	1xx = invalid.		
0x0753	JTX_SWING2	7	RESERVED		Reserved.	0x0	R
		[6:4]	JTX_LANE3_SWING		Sets the output swing level relative to the SVDD1 supply.	0x1	R/W
				000	000 = 1.0 x SVDD1.		
				001	001 = 0.85 x SVDD1.		
				010	010 = 0.75 x SVDD1.		
				011	011 = 0.50 x SVDD1.		
				1xx	1xx = invalid.		
		3	RESERVED		Reserved.	0x0	R
		[2:0]	JTX_LANE2_SWING		Sets the output swing level relative to the SVDD1 supply.	0x1	R/W
				000	000 = 1.0 x SVDD1.		
				001	001 = 0.85 x SVDD1.		
				010	010 = 0.75 x SVDD1.		
				011	011 = 0.50 x SVDD1.		
				1xx	1xx = invalid.		
0x0754	JTX_SWING3	7	RESERVED		Reserved.	0x0	R
		[6:4]	JTX_LANE5_SWING		Sets the output swing level relative to the SVDD1 supply.	0x1	R/W
				000	000 = 1.0 x SVDD1.		
				001	001 = 0.85 x SVDD1.		
				010	010 = 0.75 x SVDD1.		
				011	011 = 0.50 x SVDD1.		
				1xx	1xx = invalid.		
		3	RESERVED		Reserved.	0x0	R
		[2:0]	JTX_LANE4_SWING		Sets the output swing level relative to the SVDD1 supply.	0x1	R/W
				000	000 = 1.0 x SVDD1.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				001	001 = 0.85 x SVDD1.		
				010	010 = 0.75 x SVDD1.		
				011	011 = 0.50 x SVDD1.		
				1xx	1xx = invalid.		
0x0755	JTX_SWING4	7	RESERVED		Reserved.	0x0	R
		[6:4]	JTX_LANE7_SWING		Sets the output swing level relative to the SVDD1 supply.	0x1	R/W
				000	000 = 1.0 x SVDD1.		
				001	001 = 0.85 x SVDD1.		
				010	010 = 0.75 x SVDD1.		
				011	011 = 0.50 x SVDD1.		
				1xx	1xx = invalid.		
		3	RESERVED		Reserved.	0x0	R
		[2:0]	JTX_LANE6_SWING		Sets the output swing level relative to the SVDD1 supply.	0x1	R/W
				000	000 = 1.0 x SVDD1.		
				001	001 = 0.85 x SVDD1.		
				010	010 = 0.75 x SVDD1.		
				011	011 = 0.50 x SVDD1.		
				1xx	1xx = invalid.		
0x075A	POST_TAP_LEVEL1	7	RESERVED		Reserved.	0x0	R
		[6:4]	JTX_LANE1_POST_TAP_LEVEL[0:7]		Sets the post-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				011	011 = 9dB.		
				100	100 = 12dB.		
				else	101-111 are invalid.		
		3	RESERVED		Reserved.	0x0	R
		[2:0]	JTX_LANE0_POST_TAP_LEVEL[0:7]		Sets the post-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				011	011 = 9dB.		
				100	100 = 12dB.		
				else	101-111 are invalid.		
0x075B	POST_TAP_LEVEL2	7	RESERVED		Reserved.	0x0	R
		[6:4]	JTX_LANE3_POST_TAP_LEVEL[0:7]		Sets the post-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				011	011 = 9dB.		
				100	100 = 12dB.		
				else	101-111 are invalid.		
		3	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[2:0]	JTX_LANE2_POST_TAP_LEVEL[0:7]'		Sets the post-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				011	011 = 9dB.		
				100	100 = 12dB.		
				else	101-111 are invalid.		
0x075C	POST_TAP_LEVEL3	7	RESERVED		Reserved.	0x0	R
		[6:4]	JTX_LANE5_POST_TAP_LEVEL[0:7]		Sets the post-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				011	011 = 9dB.		
				100	100 = 12dB.		
				else	101-111 are invalid.		
		3	RESERVED		Reserved.	0x0	R
		[2:0]	JTX_LANE4_POST_TAP_LEVEL[0:7]		Sets the post-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				011	011 = 9dB.		
				100	100 = 12dB.		
				else	101-111 are invalid.		
0x075D	POST_TAP_LEVEL4	7	RESERVED		Reserved.	0x0	R
		[6:4]	JTX_LANE7_POST_TAP_LEVEL[0:7]		Sets the post-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				011	011 = 9dB.		
				100	100 = 12dB.		
				else	101-111 are invalid.		
		3	RESERVED		Reserved.	0x0	R
		[2:0]	JTX_LANE6_POST_TAP_LEVEL[0:7]		Sets the post-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				011	011 = 9dB.		
				100	100 = 12dB.		
				else	101-111 are invalid.		
0x0762	PARDATAMODE_SER	[7:3]	RESERVED		Reserved.	0x0	R
		2	C2C_EN_SER_RC		Enable chip-to-chip mode. strobe signal sent to individual channel to load cbus_wdata<7:0> , active high, <0> = ch0, <1>=ch1,..	0x0	R/W
		[1:0]	PARDATAMODE_SER_RC		Selects JESD204B/C parallel data processing width.	0x1	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0	0 = 66 bits (204C).		
				1	1 = 40 bits (204B).		
0x0763	PRE_TAP_LEVEL_CH0	[7:0]	JTX_LANE0_PRE_TAP_LEVEL		Sets the pre-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				else	011-111 are invalid.		
0x0764	PRE_TAP_LEVEL_CH1	[7:0]	JTX_LANE1_PRE_TAP_LEVEL		Sets the pre-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				else	011-111 are invalid.		
0x0765	PRE_TAP_LEVEL_CH2	[7:0]	JTX_LANE2_PRE_TAP_LEVEL		Sets the pre-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				else	011-111 are invalid.		
0x0766	PRE_TAP_LEVEL_CH3	[7:0]	JTX_LANE3_PRE_TAP_LEVEL		Sets the pre-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				else	011-111 are invalid.		
0x0767	PRE_TAP_LEVEL_CH4	[7:0]	JTX_LANE4_PRE_TAP_LEVEL		Sets the pre-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				else	011-111 are invalid.		
0x0768	PRE_TAP_LEVEL_CH5	[7:0]	JTX_LANE5_PRE_TAP_LEVEL		Sets the pre-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				else	011-111 are invalid.		
0x0769	PRE_TAP_LEVEL_CH6	[7:0]	JTX_LANE6_PRE_TAP_LEVEL		Sets the pre-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				else	011-111 are invalid.		
0x076A	PRE_TAP_LEVEL_CH7	[7:0]	JTX_LANE7_PRE_TAP_LEVEL		Sets the pre-tap de-emphasis level in 3dB steps.	0x0	R/W
				000	000 = 0dB.		
				001	001 = 3dB.		
				010	010 = 6dB.		
				else	011-111 are invalid.		
0x0773	RSTB	[7:0]	RSTB_SER[7:0]		Resetb signal for Digital Logic,. Resetb signal for Digital Logic, 0=reset, 1=normal, <0>=ch0, <1>=ch1 ..	0x0	R/W
0x0774	RSTB2	[7:0]	RSTB_SER[15:8]		Resetb signal for Digital Logic,. Resetb signal for Digital Logic, 0=reset, 1=normal, <0>=ch0, <1>=ch1 ..	0x0	R/W
0x0782	EN_DRVSLICEOFFSET	[7:4]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		3	EN_DRVSLICEOFFSET_CH67_SER_RC		Poly Code Offset value for channels 12/13.	0x0	R/W
		2	EN_DRVSLICEOFFSET_CH45_SER_RC		Poly Code Offset value for channels 10/11.	0x0	R/W
		1	EN_DRVSLICEOFFSET_CH23_SER_RC		Poly Code Offset value for channels 8/9.	0x0	R/W
		0	EN_DRVSLICEOFFSET_CH01_SER_RC		Poly Code Offset value for channels 0/1.	0x0	R/W
0x0789	MAIN_DATA_INV	7	OUTPUTDATAINVERT_CH7_SER_RC		JTx, invert ch7 data,.	0x0	R/W
				0	0=normal.		
				1	1=invert.		
		6	OUTPUTDATAINVERT_CH6_SER_RC		JTx, invert ch6 data,.	0x0	R/W
				0	0=normal.		
				1	1=invert.		
		5	OUTPUTDATAINVERT_CH5_SER_RC		JTx, invert ch5 data,.	0x0	R/W
				0	0=normal.		
				1	1=invert.		
		4	OUTPUTDATAINVERT_CH4_SER_RC		JTx, invert ch14data,.	0x0	R/W
				0	0=normal.		
				1	1=invert.		
		3	OUTPUTDATAINVERT_CH3_SER_RC		JTx, invert ch3 data,.	0x0	R/W
				0	0=normal.		
				1	1=invert.		
		2	OUTPUTDATAINVERT_CH2_SER_RC		JTx, invert ch2 data,.	0x0	R/W
				0	0=normal.		
				1	1=invert.		
		1	OUTPUTDATAINVERT_CH1_SER_RC		JTx, invert ch1 data,.	0x0	R/W
				0	0=normal.		
				1	1=invert.		
		0	OUTPUTDATAINVERT_CH0_SER_RC		JTx, invert ch0 data,.	0x0	R/W
				0	0=normal.		
				1	1=invert.		
0x0797	SYNCA_CTRL	[7:4]	RESERVED		Reserved.	0x0	R
		3	PD_SYNCA_RX_RC		SYNC0INB Receiver Power Down.	0x1	R/W
					1 = power down		
		2	SYNCA_RX_PN_INV_RC		SYNC0INB Invert Signal Polarity.	0x0	R/W
					1 = invert ± polarity		
		1	SYNCA_RX_ONCHIP_TERM_RC		SYNC0INB On-Chip 100 Ω Termination Enable.	0x0	R/W
					1 = termination enabled		
		0	SYNCA_RX_MODE_RC		SYNC0INB Input Mode Select.	0x0	R/W
				0	0 = CMOS mode.		
				1	1 = differential mode.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0798	SYNCB_CTRL	[7:4]	RESERVED		Reserved.	0x0	R
		3	PD_SYNCB_RX_RC		SYNC1INB Receiver Power down. 1 = power down	0x1	R/W
		2	SYNCB_RX_PN_INV_RC		SYNC1INB Invert Signal Polarity. 1 = invert ± polarity	0x0	R/W
		1	SYNCB_RX_ONCHIP_TERM_RC		SYNC1INB On-Chip 100 Ω Termination Enable. 1 = termination enabled	0x0	R/W
		0	SYNCB_RX_MODE_RC		SYNC1INB Input Mode Select. 0 = CMOS mode. 1 = differential mode.	0x0	R/W
0x0800	DDSM_HOPF_CTRL0	[7:6]	DDSM_HOPF_MODE	00 01 10	Hopping frequency working mode,. 0: phase continuous switch;. 1: phase in-continuous switch;. 2: phase coherent switch between 32 NCOs.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		[4:0]	DDSM_HOPF_SEL		Selects the desired FTW to use (from FTW 0 to FTW31).	0x0	R/W
0x0806	DDSM_HOPF_FTW1_0	[7:0]	DDSM_HOPF_FTW1[7:0]		Hopping frequency FTW1.	0x0	R/W
0x0807	DDSM_HOPF_FTW1_1	[7:0]	DDSM_HOPF_FTW1[15:8]		Hopping frequency FTW1.	0x0	R/W
0x0808	DDSM_HOPF_FTW1_2	[7:0]	DDSM_HOPF_FTW1[23:16]		Hopping frequency FTW1.	0x0	R/W
0x0809	DDSM_HOPF_FTW1_3	[7:0]	DDSM_HOPF_FTW1[31:24]		Hopping frequency FTW1.	0x0	R/W
0x080A	DDSM_HOPF_FTW2_0	[7:0]	DDSM_HOPF_FTW2[7:0]		Hopping frequency FTW2.	0x0	R/W
0x080B	DDSM_HOPF_FTW2_1	[7:0]	DDSM_HOPF_FTW2[15:8]		Hopping frequency FTW2.	0x0	R/W
0x080C	DDSM_HOPF_FTW2_2	[7:0]	DDSM_HOPF_FTW2[23:16]		Hopping frequency FTW2.	0x0	R/W
0x080D	DDSM_HOPF_FTW2_3	[7:0]	DDSM_HOPF_FTW2[31:24]		Hopping frequency FTW2.	0x0	R/W
0x080E	DDSM_HOPF_FTW3_0	[7:0]	DDSM_HOPF_FTW3[7:0]		Hopping frequency FTW3.	0x0	R/W
0x080F	DDSM_HOPF_FTW3_1	[7:0]	DDSM_HOPF_FTW3[15:8]		Hopping frequency FTW3.	0x0	R/W
0x0810	DDSM_HOPF_FTW3_2	[7:0]	DDSM_HOPF_FTW3[23:16]		Hopping frequency FTW3.	0x0	R/W
0x0811	DDSM_HOPF_FTW3_3	[7:0]	DDSM_HOPF_FTW3[31:24]		Hopping frequency FTW3.	0x0	R/W
0x0812	DDSM_HOPF_FTW4_0	[7:0]	DDSM_HOPF_FTW4[7:0]		Hopping frequency FTW4.	0x0	R/W
0x0813	DDSM_HOPF_FTW4_1	[7:0]	DDSM_HOPF_FTW4[15:8]		Hopping frequency FTW4.	0x0	R/W
0x0814	DDSM_HOPF_FTW4_2	[7:0]	DDSM_HOPF_FTW4[23:16]		Hopping frequency FTW4.	0x0	R/W
0x0815	DDSM_HOPF_FTW4_3	[7:0]	DDSM_HOPF_FTW4[31:24]		Hopping frequency FTW4.	0x0	R/W
0x0816	DDSM_HOPF_FTW5_0	[7:0]	DDSM_HOPF_FTW5[7:0]		Hopping frequency FTW5.	0x0	R/W
0x0817	DDSM_HOPF_FTW5_1	[7:0]	DDSM_HOPF_FTW5[15:8]		Hopping frequency FTW5.	0x0	R/W
0x0818	DDSM_HOPF_FTW5_2	[7:0]	DDSM_HOPF_FTW5[23:16]		Hopping frequency FTW5.	0x0	R/W
0x0819	DDSM_HOPF_FTW5_3	[7:0]	DDSM_HOPF_FTW5[31:24]		Hopping frequency FTW5.	0x0	R/W
0x081A	DDSM_HOPF_FTW6_0	[7:0]	DDSM_HOPF_FTW6[7:0]		Hopping frequency FTW6.	0x0	R/W
0x081B	DDSM_HOPF_FTW6_1	[7:0]	DDSM_HOPF_FTW6[15:8]		Hopping frequency FTW6.	0x0	R/W
0x081C	DDSM_HOPF_FTW6_2	[7:0]	DDSM_HOPF_FTW6[23:16]		Hopping frequency FTW6.	0x0	R/W
0x081D	DDSM_HOPF_FTW6_3	[7:0]	DDSM_HOPF_FTW6[31:24]		Hopping frequency FTW6.	0x0	R/W
0x081E	DDSM_HOPF_FTW7_0	[7:0]	DDSM_HOPF_FTW7[7:0]		Hopping frequency FTW7.	0x0	R/W
0x081F	DDSM_HOPF_FTW7_1	[7:0]	DDSM_HOPF_FTW7[15:8]		Hopping frequency FTW7.	0x0	R/W
0x0820	DDSM_HOPF_FTW7_2	[7:0]	DDSM_HOPF_FTW7[23:16]		Hopping frequency FTW7.	0x0	R/W
0x0821	DDSM_HOPF_FTW7_3	[7:0]	DDSM_HOPF_FTW7[31:24]		Hopping frequency FTW7.	0x0	R/W
0x0822	DDSM_HOPF_FTW8_0	[7:0]	DDSM_HOPF_FTW8[7:0]		Hopping frequency FTW8.	0x0	R/W
0x0823	DDSM_HOPF_FTW8_1	[7:0]	DDSM_HOPF_FTW8[15:8]		Hopping frequency FTW8.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0824	DDSM_HOPF_FTW8_2	[7:0]	DDSM_HOPF_FTW8[23:16]		Hopping frequency FTW8.	0x0	R/W
0x0825	DDSM_HOPF_FTW8_3	[7:0]	DDSM_HOPF_FTW8[31:24]		Hopping frequency FTW8.	0x0	R/W
0x0826	DDSM_HOPF_FTW9_0	[7:0]	DDSM_HOPF_FTW9[7:0]		Hopping frequency FTW9.	0x0	R/W
0x0827	DDSM_HOPF_FTW9_1	[7:0]	DDSM_HOPF_FTW9[15:8]		Hopping frequency FTW9.	0x0	R/W
0x0828	DDSM_HOPF_FTW9_2	[7:0]	DDSM_HOPF_FTW9[23:16]		Hopping frequency FTW9.	0x0	R/W
0x0829	DDSM_HOPF_FTW9_3	[7:0]	DDSM_HOPF_FTW9[31:24]		Hopping frequency FTW9.	0x0	R/W
0x082A	DDSM_HOPF_FTW10_0	[7:0]	DDSM_HOPF_FTW10[7:0]		Hopping frequency FTW10.	0x0	R/W
0x082B	DDSM_HOPF_FTW10_1	[7:0]	DDSM_HOPF_FTW10[15:8]		Hopping frequency FTW10.	0x0	R/W
0x082C	DDSM_HOPF_FTW10_2	[7:0]	DDSM_HOPF_FTW10[23:16]		Hopping frequency FTW10.	0x0	R/W
0x082D	DDSM_HOPF_FTW10_3	[7:0]	DDSM_HOPF_FTW10[31:24]		Hopping frequency FTW10.	0x0	R/W
0x082E	DDSM_HOPF_FTW11_0	[7:0]	DDSM_HOPF_FTW11[7:0]		Hopping frequency FTW11.	0x0	R/W
0x082F	DDSM_HOPF_FTW11_1	[7:0]	DDSM_HOPF_FTW11[15:8]		Hopping frequency FTW11.	0x0	R/W
0x0830	DDSM_HOPF_FTW11_2	[7:0]	DDSM_HOPF_FTW11[23:16]		Hopping frequency FTW11.	0x0	R/W
0x0831	DDSM_HOPF_FTW11_3	[7:0]	DDSM_HOPF_FTW11[31:24]		Hopping frequency FTW11.	0x0	R/W
0x0832	DDSM_HOPF_FTW12_0	[7:0]	DDSM_HOPF_FTW12[7:0]		Hopping frequency FTW12.	0x0	R/W
0x0833	DDSM_HOPF_FTW12_1	[7:0]	DDSM_HOPF_FTW12[15:8]		Hopping frequency FTW12.	0x0	R/W
0x0834	DDSM_HOPF_FTW12_2	[7:0]	DDSM_HOPF_FTW12[23:16]		Hopping frequency FTW12.	0x0	R/W
0x0835	DDSM_HOPF_FTW12_3	[7:0]	DDSM_HOPF_FTW12[31:24]		Hopping frequency FTW12.	0x0	R/W
0x0836	DDSM_HOPF_FTW13_0	[7:0]	DDSM_HOPF_FTW13[7:0]		Hopping frequency FTW13.	0x0	R/W
0x0837	DDSM_HOPF_FTW13_1	[7:0]	DDSM_HOPF_FTW13[15:8]		Hopping frequency FTW13.	0x0	R/W
0x0838	DDSM_HOPF_FTW13_2	[7:0]	DDSM_HOPF_FTW13[23:16]		Hopping frequency FTW13.	0x0	R/W
0x0839	DDSM_HOPF_FTW13_3	[7:0]	DDSM_HOPF_FTW13[31:24]		Hopping frequency FTW13.	0x0	R/W
0x083A	DDSM_HOPF_FTW14_0	[7:0]	DDSM_HOPF_FTW14[7:0]		Hopping frequency FTW14.	0x0	R/W
0x083B	DDSM_HOPF_FTW14_1	[7:0]	DDSM_HOPF_FTW14[15:8]		Hopping frequency FTW14.	0x0	R/W
0x083C	DDSM_HOPF_FTW14_2	[7:0]	DDSM_HOPF_FTW14[23:16]		Hopping frequency FTW14.	0x0	R/W
0x083D	DDSM_HOPF_FTW14_3	[7:0]	DDSM_HOPF_FTW14[31:24]		Hopping frequency FTW14.	0x0	R/W
0x083E	DDSM_HOPF_FTW15_0	[7:0]	DDSM_HOPF_FTW15[7:0]		Hopping frequency FTW15.	0x0	R/W
0x083F	DDSM_HOPF_FTW15_1	[7:0]	DDSM_HOPF_FTW15[15:8]		Hopping frequency FTW15.	0x0	R/W
0x0840	DDSM_HOPF_FTW15_2	[7:0]	DDSM_HOPF_FTW15[23:16]		Hopping frequency FTW15.	0x0	R/W
0x0841	DDSM_HOPF_FTW15_3	[7:0]	DDSM_HOPF_FTW15[31:24]		Hopping frequency FTW15.	0x0	R/W
0x0842	DDSM_HOPF_FTW16_0	[7:0]	DDSM_HOPF_FTW16[7:0]		Hopping frequency FTW16.	0x0	R/W
0x0843	DDSM_HOPF_FTW16_1	[7:0]	DDSM_HOPF_FTW16[15:8]		Hopping frequency FTW16.	0x0	R/W
0x0844	DDSM_HOPF_FTW16_2	[7:0]	DDSM_HOPF_FTW16[23:16]		Hopping frequency FTW16.	0x0	R/W
0x0845	DDSM_HOPF_FTW16_3	[7:0]	DDSM_HOPF_FTW16[31:24]		Hopping frequency FTW16.	0x0	R/W
0x0846	DDSM_HOPF_FTW17_0	[7:0]	DDSM_HOPF_FTW17[7:0]		Hopping frequency FTW17.	0x0	R/W
0x0847	DDSM_HOPF_FTW17_1	[7:0]	DDSM_HOPF_FTW17[15:8]		Hopping frequency FTW17.	0x0	R/W
0x0848	DDSM_HOPF_FTW17_2	[7:0]	DDSM_HOPF_FTW17[23:16]		Hopping frequency FTW17.	0x0	R/W
0x0849	DDSM_HOPF_FTW17_3	[7:0]	DDSM_HOPF_FTW17[31:24]		Hopping frequency FTW17.	0x0	R/W
0x084A	DDSM_HOPF_FTW18_0	[7:0]	DDSM_HOPF_FTW18[7:0]		Hopping frequency FTW18.	0x0	R/W
0x084B	DDSM_HOPF_FTW18_1	[7:0]	DDSM_HOPF_FTW18[15:8]		Hopping frequency FTW18.	0x0	R/W
0x084C	DDSM_HOPF_FTW18_2	[7:0]	DDSM_HOPF_FTW18[23:16]		Hopping frequency FTW18.	0x0	R/W
0x084D	DDSM_HOPF_FTW18_3	[7:0]	DDSM_HOPF_FTW18[31:24]		Hopping frequency FTW18.	0x0	R/W
0x084E	DDSM_HOPF_FTW19_0	[7:0]	DDSM_HOPF_FTW19[7:0]		Hopping frequency FTW19.	0x0	R/W
0x084F	DDSM_HOPF_FTW19_1	[7:0]	DDSM_HOPF_FTW19[15:8]		Hopping frequency FTW19.	0x0	R/W
0x0850	DDSM_HOPF_FTW19_2	[7:0]	DDSM_HOPF_FTW19[23:16]		Hopping frequency FTW19.	0x0	R/W
0x0851	DDSM_HOPF_FTW19_3	[7:0]	DDSM_HOPF_FTW19[31:24]		Hopping frequency FTW19.	0x0	R/W
0x0852	DDSM_HOPF_FTW20_0	[7:0]	DDSM_HOPF_FTW20[7:0]		Hopping frequency FTW20.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0853	DDSM_HOPF_FTW20_1	[7:0]	DDSM_HOPF_FTW20[15:8]		Hopping frequency FTW20.	0x0	R/W
0x0854	DDSM_HOPF_FTW20_2	[7:0]	DDSM_HOPF_FTW20[23:16]		Hopping frequency FTW20.	0x0	R/W
0x0855	DDSM_HOPF_FTW20_3	[7:0]	DDSM_HOPF_FTW20[31:24]		Hopping frequency FTW20.	0x0	R/W
0x0856	DDSM_HOPF_FTW21_0	[7:0]	DDSM_HOPF_FTW21[7:0]		Hopping frequency FTW21.	0x0	R/W
0x0857	DDSM_HOPF_FTW21_1	[7:0]	DDSM_HOPF_FTW21[15:8]		Hopping frequency FTW21.	0x0	R/W
0x0858	DDSM_HOPF_FTW21_2	[7:0]	DDSM_HOPF_FTW21[23:16]		Hopping frequency FTW21.	0x0	R/W
0x0859	DDSM_HOPF_FTW21_3	[7:0]	DDSM_HOPF_FTW21[31:24]		Hopping frequency FTW21.	0x0	R/W
0x085A	DDSM_HOPF_FTW22_0	[7:0]	DDSM_HOPF_FTW22[7:0]		Hopping frequency FTW22.	0x0	R/W
0x085B	DDSM_HOPF_FTW22_1	[7:0]	DDSM_HOPF_FTW22[15:8]		Hopping frequency FTW22.	0x0	R/W
0x085C	DDSM_HOPF_FTW22_2	[7:0]	DDSM_HOPF_FTW22[23:16]		Hopping frequency FTW22.	0x0	R/W
0x085D	DDSM_HOPF_FTW22_3	[7:0]	DDSM_HOPF_FTW22[31:24]		Hopping frequency FTW22.	0x0	R/W
0x085E	DDSM_HOPF_FTW23_0	[7:0]	DDSM_HOPF_FTW23[7:0]		Hopping frequency FTW23.	0x0	R/W
0x085F	DDSM_HOPF_FTW23_1	[7:0]	DDSM_HOPF_FTW23[15:8]		Hopping frequency FTW23.	0x0	R/W
0x0860	DDSM_HOPF_FTW23_2	[7:0]	DDSM_HOPF_FTW23[23:16]		Hopping frequency FTW23.	0x0	R/W
0x0861	DDSM_HOPF_FTW23_3	[7:0]	DDSM_HOPF_FTW23[31:24]		Hopping frequency FTW23.	0x0	R/W
0x0862	DDSM_HOPF_FTW24_0	[7:0]	DDSM_HOPF_FTW24[7:0]		Hopping frequency FTW24.	0x0	R/W
0x0863	DDSM_HOPF_FTW24_1	[7:0]	DDSM_HOPF_FTW24[15:8]		Hopping frequency FTW24.	0x0	R/W
0x0864	DDSM_HOPF_FTW24_2	[7:0]	DDSM_HOPF_FTW24[23:16]		Hopping frequency FTW24.	0x0	R/W
0x0865	DDSM_HOPF_FTW24_3	[7:0]	DDSM_HOPF_FTW24[31:24]		Hopping frequency FTW24.	0x0	R/W
0x0866	DDSM_HOPF_FTW25_0	[7:0]	DDSM_HOPF_FTW25[7:0]		Hopping frequency FTW25.	0x0	R/W
0x0867	DDSM_HOPF_FTW25_1	[7:0]	DDSM_HOPF_FTW25[15:8]		Hopping frequency FTW25.	0x0	R/W
0x0868	DDSM_HOPF_FTW25_2	[7:0]	DDSM_HOPF_FTW25[23:16]		Hopping frequency FTW25.	0x0	R/W
0x0869	DDSM_HOPF_FTW25_3	[7:0]	DDSM_HOPF_FTW25[31:24]		Hopping frequency FTW25.	0x0	R/W
0x086A	DDSM_HOPF_FTW26_0	[7:0]	DDSM_HOPF_FTW26[7:0]		Hopping frequency FTW26.	0x0	R/W
0x086B	DDSM_HOPF_FTW26_1	[7:0]	DDSM_HOPF_FTW26[15:8]		Hopping frequency FTW26.	0x0	R/W
0x086C	DDSM_HOPF_FTW26_2	[7:0]	DDSM_HOPF_FTW26[23:16]		Hopping frequency FTW26.	0x0	R/W
0x086D	DDSM_HOPF_FTW26_3	[7:0]	DDSM_HOPF_FTW26[31:24]		Hopping frequency FTW26.	0x0	R/W
0x086E	DDSM_HOPF_FTW27_0	[7:0]	DDSM_HOPF_FTW27[7:0]		Hopping frequency FTW27.	0x0	R/W
0x086F	DDSM_HOPF_FTW27_1	[7:0]	DDSM_HOPF_FTW27[15:8]		Hopping frequency FTW27.	0x0	R/W
0x0870	DDSM_HOPF_FTW27_2	[7:0]	DDSM_HOPF_FTW27[23:16]		Hopping frequency FTW27.	0x0	R/W
0x0871	DDSM_HOPF_FTW27_3	[7:0]	DDSM_HOPF_FTW27[31:24]		Hopping frequency FTW27.	0x0	R/W
0x0872	DDSM_HOPF_FTW28_0	[7:0]	DDSM_HOPF_FTW28[7:0]		Hopping frequency FTW28.	0x0	R/W
0x0873	DDSM_HOPF_FTW28_1	[7:0]	DDSM_HOPF_FTW28[15:8]		Hopping frequency FTW28.	0x0	R/W
0x0874	DDSM_HOPF_FTW28_2	[7:0]	DDSM_HOPF_FTW28[23:16]		Hopping frequency FTW28.	0x0	R/W
0x0875	DDSM_HOPF_FTW28_3	[7:0]	DDSM_HOPF_FTW28[31:24]		Hopping frequency FTW28.	0x0	R/W
0x0876	DDSM_HOPF_FTW29_0	[7:0]	DDSM_HOPF_FTW29[7:0]		Hopping frequency FTW29.	0x0	R/W
0x0877	DDSM_HOPF_FTW29_1	[7:0]	DDSM_HOPF_FTW29[15:8]		Hopping frequency FTW29.	0x0	R/W
0x0878	DDSM_HOPF_FTW29_2	[7:0]	DDSM_HOPF_FTW29[23:16]		Hopping frequency FTW29.	0x0	R/W
0x0879	DDSM_HOPF_FTW29_3	[7:0]	DDSM_HOPF_FTW29[31:24]		Hopping frequency FTW29.	0x0	R/W
0x087A	DDSM_HOPF_FTW30_0	[7:0]	DDSM_HOPF_FTW30[7:0]		Hopping frequency FTW30.	0x0	R/W
0x087B	DDSM_HOPF_FTW30_1	[7:0]	DDSM_HOPF_FTW30[15:8]		Hopping frequency FTW30.	0x0	R/W
0x087C	DDSM_HOPF_FTW30_2	[7:0]	DDSM_HOPF_FTW30[23:16]		Hopping frequency FTW30.	0x0	R/W
0x087D	DDSM_HOPF_FTW30_3	[7:0]	DDSM_HOPF_FTW30[31:24]		Hopping frequency FTW30.	0x0	R/W
0x087E	DDSM_HOPF_FTW31_0	[7:0]	DDSM_HOPF_FTW31[7:0]		Hopping frequency FTW31.	0x0	R/W
0x087F	DDSM_HOPF_FTW31_1	[7:0]	DDSM_HOPF_FTW31[15:8]		Hopping frequency FTW31.	0x0	R/W
0x0880	DDSM_HOPF_FTW31_2	[7:0]	DDSM_HOPF_FTW31[23:16]		Hopping frequency FTW31.	0x0	R/W
0x0881	DDSM_HOPF_FTW31_3	[7:0]	DDSM_HOPF_FTW31[31:24]		Hopping frequency FTW31.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0941	TXFE_LOOPBACK MODE	[7:1]	RESERVED		Reserved.	0x0	R
		0	TXFE_LOOPBACK_MODES		Enable indirect loopback mode from JTX FIFO to JRX FIFO.	0x0	R/W
0x0950	JRX_TEST_0	[7:2]	RESERVED		Reserved.	0x0	R
		1	JRX_PRBS_LANE_UPDATE_ERROR_COUNT		Update error counters. Toggle this bit from 0 to 1 in order to update the error counters on all lanes.	0x0	R/W
		0	JRX_PRBS_LANE_CLEAR_ERRORS		Clear error counters. Toggle this bit from 0 to 1 in order to clear the error counters on all lanes.	0x0	R/W
0x0952	JRX_TEST_2	[7:3]	RESERVED		Reserved.	0x0	R/W
		[2:0]	JRX_PRBS_MODE		JRx PHY PRBS test mode.	0x0	R/W
				000	0 = Pattern checker is off.		
				001	1 = PRBS7.		
				010	2 = PRBS9.		
				011	3 = PRBS15.		
				100	4 = PRBS31.		
				101	5 = User data.		
				Else	Else = Not valid.		
0x0953 to 0x095A by 1	JRX_TEST_3_LANEn	7	JRX_PRBS_LANE_ERROR_FLAG		Error counter contains non-zero value. Clear error counter to clear error flag. Per lane register addressing (0x0953 applies to Lane0, 0x0954 applies to Lane1, etc.).	0x0	R
		6	JRX_PRBS_LANE_INVALID_DATA_FLAG		Invalid PRBS data.	0x0	R
				0	0 = Data received by PRBS checker is valid.		
				1	1 = Data received by PRBS checker is not valid (0's).		
		5	JRX_PRBS_LANE_INV		Inverted PRBS data.	0x0	R
				0	0 = Data received by PRBS checker is not inverted.		
				1	1 = Data received by PRBS checker is valid, but inverted.		
		[4:0]	RESERVED		Reserved.	0x0	R
0x095B to 0x0962 by 1	JRX_TEST_4_LANEn	[7:0]	JRX_PRBS_LANE_ERROR_COUNT[7:0]		JRx PRBS lane error counter. Contains the number of PRBS errors per lane. Per lane register addressing (0x095B applies to Lane0, 0x095C applies to Lane1, etc.).	0x0	R
0x0963 to 0x096A by 1	JRX_TEST_5_LANEn	[7:0]	JRX_PRBS_LANE_ERROR_COUNT[15:8]		JRx PRBS lane error counter. Contains the number of PRBS errors per lane. Per lane register addressing (0x095B applies to Lane0, 0x095C applies to Lane1, etc.).	0x0	R
0x096B to 0x0972 by 1	JRX_TEST_6_LANEn	[7:0]	JRX_PRBS_LANE_ERROR_COUNT[23:16]		JRx PRBS lane error counter. Contains the number of PRBS errors per lane. Per lane register addressing (0x095B applies to Lane0, 0x095C applies to Lane1, etc.).	0x0	R
0x0973	JRX_TEST_7	[7:0]	JRX_TEST_USER_DATA[7:0]		32-bit user data pattern. If JRX_PRBS_MODE = 4, program the user data pattern to match the data that is being sent by the logic device's JTx.	0x0	R/W
0x0974	JRX_TEST_8	[7:0]	JRX_TEST_USER_DATA[15:8]		32-bit user data pattern. If JRX_PRBS_MODE = 4, program the user data pattern to match the data that is being sent by the logic device's JTx.	0x0	R/W
0x0975	JRX_TEST_9	[7:0]	JRX_TEST_USER_DATA[23:16]		32-bit user data pattern. If JRX_PRBS_MODE = 4, program the user data pattern to match the data that is being sent by the logic device's JTx.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0976	JRX_TEST_10	[7:0]	JRX_TEST_USER_DATA[31:24]		32-bit user data pattern. If JRX_PRBS_MODE = 4, program the user data pattern to match the data that is being sent by the logic device's JTx.	0x0	R/W
0x0A00	COARSE_DDC_SYNC_CTRL	7	COARSE_DDC_TRIG_NCO_RESET_EN		DDC Trig NCO Reset Enable.	0x0	R/W
		[6:5]	RESERVED		Reserved.	0x0	R/W
		4	COARSE_DDC_SOFT_RESET		Digital downconverter Soft Reset. 0: Normal Operation 1: DDC Held in Reset. Note: this bit can be used to synchronize all the NCO's inside the DDC blocks.	0x0	R/W
		[3:2]	RESERVED		Reserved.	0x0	R
		1	COARSE_DDC_SYNC_NEXT		DDC Next Synchronization Mode. 0: Continuous mode is ignored Note: The SYSREF pin must an integer multiple of the NCO frequency in order for this function to operate correctly in continuous mode.	0x1	R/W
		0	COARSE_DDC_SYNC_EN		DDC Synchronization Enable. 0: Synchronization Disabled. is ignored Note: the SYSREF input pin must be enabled in order to synchronize the DDCs.	0x0	R/W
0x0A01	COARSE_DDC_SYNC_STATUS	[7:1]	RESERVED		Reserved.	0x0	R
		0	COARSE_DDC_SYNC_EN_CLEAR		DDC Sync Enable Clear Status. DDC Sync Enable Clear Status	0x0	R
0x0A03	COARSE_DDC_NCO_CTRL	[7:4]	COARSE_DDC0_NCO_CHAN_SEL_MODE		NCO Channel Selection Mode. Mode decoding is as follows: 0000: Register Map control (Use ddc_nco_regmap_chan_sel) 0001: profile_pins[0] Is used. Pin level control {3'b0, profile_pins[0]} 0010: profile_pins[1 :0] are used. Pin level control {2'b0, profile_pins[1:0]} 0011: profile_pins[2 :0] are used. Pin level control {1'b0, profile_pins[2:0]} 0100: profile_pins[3 :0] are used. Pin level control { profile_pins[3:0]} 0101-0111 : Reserved 1000: profile_pins[0] Pin edge control-increment internal counter when rising edge of profile_pins[0] Pin. 1001: profile_pins[1] Pin edge control-increment internal counter when rising edge of profile_pins[1] Pin. 1010: profile_pins[2] Pin edge control-increment internal counter when rising edge of profile_pins[2] Pin. 1011: profile_pins[3] Pin edge control-increment internal counter when rising edge of profile_pins[3] Pin.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					1100: FHT expire based control - increment internal counter when FHT is expired. 1101 to 1111: Reserved Note: For edge control/fht based control, the internal counter wraps once ddc_nco_regmap_chan_sel value is reached.		
		[3:0]	COARSE_DDC0_NCO_REGMAP_CHAN_SEL		NCO Channel Select Register map control. 0000: Select NCO Channel 0 0001: Select NCO Channel 1 0010: Select NCO Channel 2 0011: Select NCO Channel 3 0100 : Select NCO Channel 4 … 1111 : Select NCO Channel 15	0x0	R/W
0x0A04	COARSE_DDC_PROFILE_CTRL	7	COARSE_DDC0_PROFILE_UPDATE_MODE	0 1	DDC Profile Update Mode. DDC Phase Update Mode. 0: Instantaneous/Continuous Update. Phase increment and phase offset values are updated immediately. 1: Phase increment and phase offset values are updated synchronously either with the chip_transfer bit is set high or based on the GPIO pin low to high transition.The chip transfer bit is cleared once the transfer is complete.	0x0	R/W
		6	COARSE_DDC0_GPIO_CHIP_TRANSFER_MODE		DDC GPIO Chip Transfer Mode. Used when COARSE_DDC0_PROFILE_UPDATE_MODE is '1' 0: Phase increment and phase offset values are updated synchronously when the chip_transfer bit is set high. The chip transfer bit is cleared once the transfer is complete. 1: Phase increment and phase offset values are updated based on the GPIO pin low to high transition.	0x0	R/W
		[5:4]	RESERVED		Reserved.	0x0	R
		[3:0]	COARSE_DDC0_PROFILE_UPDATE_INDEX		Indexes the NCO channel whose phase and offset gets updated. The update method is based on the 'COARSE_DDC0_PROFILE_UPDATE_MODE', which could be continuous or require 'chip_transfer'. 0000: Update NCO Channel 0 0001: Update NCO Channel 1 0010: Update NCO Channel 2 0011: Update NCO Channel 3 0100 : Update NCO Channel 4 … 1111 : Update NCO Channel 15	0x0	R/W
0x0A05	COARSE_DDC_PHASE_INC0	[7:0]	COARSE_DDC0_PHASE_INC0		Bits [7:0] of PHASE INCREMENT. NCO Phase Increment Value.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.		
0x0A06	COARSE_DDC_PHASE_INC1	[7:0]	COARSE_DDC0_PHASE_INC1		Bits [15:8] of PHASE INCREMENT. NCO Phase Increment Value. Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x0A07	COARSE_DDC_PHASE_INC2	[7:0]	COARSE_DDC0_PHASE_INC2		Bits [23:16] of PHASE INCREMENT. NCO Phase Increment Value. Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x0A08	COARSE_DDC_PHASE_INC3	[7:0]	COARSE_DDC0_PHASE_INC3		Bits [31:24] of PHASE INCREMENT. NCO Phase Increment Value. Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x0A09	COARSE_DDC_PHASE_INC4	[7:0]	COARSE_DDC0_PHASE_INC4		Bits [39:32] of PHASE INCREMENT. NCO Phase Increment Value. Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x0A0A	COARSE_DDC_PHASE_INC5	[7:0]	COARSE_DDC0_PHASE_INC5		Bits [47:40] of PHASE INCRMENT. NCO Phase Increment Value. Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x0A0B	COARSE_DDC_PHASE_OFFSET0	[7:0]	COARSE_DDC0_PHASE_OFFSET0		Bits [7:0] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x0A0C	COARSE_DDC_PHASE_OFFSET1	[7:0]	COARSE_DDC0_PHASE_OFFSET1		Bits [15:8] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x0A0D	COARSE_DDC_PHASE_OFFSET2	[7:0]	COARSE_DDC0_PHASE_OFFSET2		Bits [23:16] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0A0E	COARSE_DDC_PHASE_OFFSET3	[7:0]	COARSE_DDC0_PHASE_OFFSET3		Bits [31:24] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x0A0F	COARSE_DDC_PHASE_OFFSET4	[7:0]	COARSE_DDC0_PHASE_OFFSET4		Bits [39:32] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x0A10	COARSE_DDC_PHASE_OFFSET5	[7:0]	COARSE_DDC0_PHASE_OFFSET5		Bits [47:40] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x0A11	COARSE_DDC_PHASE_INC_FRAC_A0	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_A0		Bits [7:0] of PHASE INCREMENT NUMERATOR. . Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W
0x0A12	COARSE_DDC_PHASE_INC_FRAC_A1	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_A1		Bits [15:8] of PHASE INCREMENT NUMERATOR. ; Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W
0x0A13	COARSE_DDC_PHASE_INC_FRAC_A2	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_A2		Bits [23:16] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W
0x0A14	COARSE_DDC_PHASE_INC_FRAC_A3	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_A3		Bits [31:24] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W
0x0A15	COARSE_DDC_PHASE_INC_FRAC_A4	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_A4		Bits [39:32] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W
0x0A16	COARSE_DDC_PHASE_INC_FRAC_A5	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_A5		Bits [47:40] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W
0x0A17	COARSE_DDC_PHASE_INC_FRAC_B0	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_B0		Bits [7:0] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x0A18	COARSE_DDC_PHASE_INC_FRAC_B1	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_B1		Bits [15:8] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x0A19	COARSE_DDC_PHASE_INC_FRAC_B2	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_B2		Bits [23:16] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x0A1A	COARSE_DDC_PHASE_INC_FRAC_B3	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_B3		Bits [31:24] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0A1B	COARSE_DDC_PHASE_INC_FRAC_B4	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_B4		Bits [39:32] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x0A1C	COARSE_DDC_PHASE_INC_FRAC_B5	[7:0]	COARSE_DDC0_PHASE_INC_FRAC_B5		Bits [47:40] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x0A1D	COARSE_DDC_TRANSFER_STATUS	[7:1]	RESERVED		Reserved.	0x0	R
		0	COARSE_DDC0_CHIP_TRANSFER_STATUS	0 1	DDC Chip Transfer Status. 0: Indicates the data transfer is not requested or not completed. 1: Transfer of data from main to subordinate registers is complete.	0x0	R
0x0A1E	COARSE_DDC_DITHER	[7:2]	RESERVED		Reserved.	0x0	R
		1	COARSE_DDC0_PHASE_DITHER_EN	0 1	Phase Dither Enable. 0: Enabled. 1: Disabled.	0x0	R/W
		0	RESERVED		Reserved.	0x0	R/W
0x0A1F	COARSE_DDC_TRANSFER_CTRL	[7:1]	RESERVED		Reserved.	0x0	R
		0	COARSE_DDC0_CHIP_TRANSFER		DDC Chip Transfer. 1: Used to synchronize the transfer of data from main to subordinate registers. 0: Do nothing. Note: This bit is used to update the DDC Phase Increment and Phase Offset registers when COARSE_DDC0_PROFILE_UPDATE_MODE = 1 and COARSE_DDC0_GPIO_CHIP_TRANSFER_MODE = 0.	0x0	R/W
0x0A20	COARSE_DDC_PSW_0	[7:0]	COARSE_DDC0_PSW0		Bits [7:0] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x0A21	COARSE_DDC_PSW_1	[7:0]	COARSE_DDC0_PSW1		Bits [15:8] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x0A22	COARSE_DDC_PSW_2	[7:0]	COARSE_DDC0_PSW2		Bits [23:16] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0A23	COARSE_DDC_PSW_3	[7:0]	COARSE_DDC0_PSW3		Bits [31:24] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x0A24	COARSE_DDC_PSW_4	[7:0]	COARSE_DDC0_PSW4		Bits [39:32] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x0A25	COARSE_DDC_PSW_5	[7:0]	COARSE_DDC0_PSW5		Bits [47:40] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x0A26	COARSE_DDC_ACTIVE_PHASE_INC0	[7:0]	COARSE_DDC0_ACTIVE_PHASE_INC0		Bits [7:0] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R
0x0A27	COARSE_DDC_ACTIVE_PHASE_INC1	[7:0]	COARSE_DDC0_ACTIVE_PHASE_INC1		Bits [15:8] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R
0x0A28	COARSE_DDC_ACTIVE_PHASE_INC2	[7:0]	COARSE_DDC0_ACTIVE_PHASE_INC2		Bits [23:16] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R
0x0A29	COARSE_DDC_ACTIVE_PHASE_INC3	[7:0]	COARSE_DDC0_ACTIVE_PHASE_INC3		Bits [31:24] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R
0x0A2A	COARSE_DDC_ACTIVE_PHASE_INC4	[7:0]	COARSE_DDC0_ACTIVE_PHASE_INC4		Bits [39:32] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R
0x0A2B	COARSE_DDC_ACTIVE_PHASE_INC5	[7:0]	COARSE_DDC0_ACTIVE_PHASE_INC5		Bits [47:40] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R
0x0A2C	COARSE_DDC_ACTIVE_PHASE_OFFSET0	[7:0]	COARSE_DDC0_ACTIVE_PHASE_OFFSET0		Bits [7:0] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0A2D	COARSE_DDC_ACTIVE_PHASE_OFFSET1	[7:0]	COARSE_DDC0_ACTIVE_PHASE_OFFSET1		Bits [15:8] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0A2E	COARSE_DDC_ACTIVE_PHASE_OFFSET2	[7:0]	COARSE_DDC0_ACTIVE_PHASE_OFFSET2		Bits [23:16] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0A2F	COARSE_DDC_ACTIVE_PHASE_OFFSET3	[7:0]	COARSE_DDC0_ACTIVE_PHASE_OFFSET3		Bits [31:24] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0A30	COARSE_DDC_ACTIVE_PHASE_OFFSET4	[7:0]	COARSE_DDC0_ACTIVE_PHASE_OFFSET4		Bits [39:32] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0A31	COARSE_DDC_ACTIVE_PHASE_OFFSET5	[7:0]	COARSE_DDC0_ACTIVE_PHASE_OFFSET5		Bits [47:40] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0A39	COARSE_COUNTER_LOAD_REG0	[7:0]	COARSE_COUNTER_LOAD_REG[7:0]		Counter Load Register.	0x0	R/W
0x0A3A	COARSE_COUNTER_LOAD_REG1	[7:0]	COARSE_COUNTER_LOAD_REG[15:8]		Counter Load Register.	0x0	R/W
0x0A3B	COARSE_COUNTER_LOAD_REG2	[7:0]	COARSE_COUNTER_LOAD_REG[23:16]		Counter Load Register.	0x0	R/W
0x0A3C	COARSE_COUNTER_LOAD_REG3	[7:0]	COARSE_COUNTER_LOAD_REG[31:24]		Counter Load Register.	0x0	R/W
0x0A3D	COARSE_COUNTER_LOAD_REG4	[7:0]	COARSE_COUNTER_LOAD_REG[39:32]		Counter Load Register.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0A3E	COARSE_COUNTER_LOAD_REG5	[7:0]	COARSE_COUNTER_LOAD_REG[47:40]		Counter Load Register.	0x0	R/W
0x0A80	FINE_DDC_SYNC_CTRL	7	FINE_DDC_TRIG_NCO_RESET_EN		DDC Trig NCO Reset Enable.	0x0	R/W
		[6:5]	RESERVED		Reserved.	0x0	R/W
		4	FINE_DDC_SOFT_RESET		Digital downconverter Soft Reset. Note: this bit can be used to synchronize all the NCO's inside the DDC blocks.	0x0	R/W
				0	0: Normal Operation.		
				1	1: DDC Held in Reset.		
		[3:2]	RESERVED		Reserved.	0x0	R
		1	FINE_DDC_SYNC_NEXT		DDC Next Synchronization Mode. Note: The SYSREF pin must an integer multiple of the NCO frequency in order for this function to operate correctly in continuous mode.	0x1	R/W
				0	0: Continuous mode.		
				1	is ignored		
		0	FINE_DDC_SYNC_EN		DDC Synchronization Enable. Note: the SYSREF input pin must be enabled in order to synchronize the DDCs.	0x0	R/W
				0	0: Synchronization Disabled.		
				1	is ignored		
0x0A81	FINE_DDC_SYNC_STATUS	[7:1]	RESERVED		Reserved.	0x0	R
		0	FINE_DDC_SYNC_EN_CLEAR		DDC Sync Enable Clear Status.	0x0	R
0x0A83	FINE_DDC_NCO_CTRL	[7:4]	FINE_DDC0_NCO_CHAN_SEL_MODE		NCO Channel Selection Mode. Mode decoding is as follows: 0000: Register Map control (Use ddc_nco_regmap_chan_sel) 0001: profile_pins[0] Is used. Pin level control {3'b0, profile_pins[0]} 0010: profile_pins[1 :0] are used. Pin level control {2'b0, profile_pins[1:0]} 0011: profile_pins[2 :0] are used. Pin level control {1'b0, profile_pins[2:0]} 0100: profile_pins[3 :0] are used. Pin level control { profile_pins[3:0]} 0101-0111 : Reserved 1000: profile_pins[0] Pin edge control-increment internal counter when rising edge of profile_pins[0] Pin. 1001: profile_pins[1] Pin edge control-increment internal counter when rising edge of profile_pins[1] Pin. 1010: profile_pins[2] Pin edge control-increment internal counter when rising edge of profile_pins[2] Pin. 1011: profile_pins[3] Pin edge control-increment internal counter when rising edge of profile_pins[3] Pin. 1100: FHT expire based control - increment internal counter when FHT is expired.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					1101 - 1111: Reserved Note: For edge control/fht based control, the internal counter wraps once ddc_nco_regmap_chan_sel value is reached.		
		[3:0]	FINE_DDC0_NCO_REGMAP_CHAN_SEL		NCO Channel Select Register map control. 0000: Select NCO Channel 0 0001: Select NCO Channel 1 0010: Select NCO Channel 2 0011: Select NCO Channel 3 0100 : Select NCO Channel 4 … … … 1111 : Select NCO Channel 15	0x0	R/W
0x0A84	FINE_DDC_PROFILE_CTRL	7	FINE_DDC0_PROFILE_UPDATE_MODE		DDC Profile Update Mode. DDC Phase Update Mode. 0: Instantaneous/Continuous Update. Phase increment and phase offset values are updated immediately. 1: Phase increment and phase offset values are updated synchronously either with the chip_transfer bit is set high or based on the GPIO pin low to high transition. The chip transfer bit is cleared once the transfer is complete.	0x0	R/W
		6	FINE_DDC0_GPIO_CHIP_TRANSFER_MODE		DDC GPIO Chip Transfer Mode. Used when FINE_DDC0_PROFILE_UPDATE_MODE is 1. 0: Phase increment and phase offset values are updated synchronously when the chip_transfer bit is set high. The chip transfer bit is cleared once the transfer is complete. 1: Phase increment and phase offset values are updated based on the GPIO pin low to high transition.	0x0	R/W
		[5:4]	RESERVED		Reserved.	0x0	R
		[3:0]	FINE_DDC0_PROFILE_UPDATE_INDEX		Profile Update Index. Indexes the NCO channel whose phase and offset gets updated. The update method is based on the 'FINE_DDC0_PROFILE_UPDATE_MODE', which could be continuous or require 'chip_transfer'. 0000: Update NCO Channel 0 0001: Update NCO Channel 1 0010: Update NCO Channel 2 0011: Update NCO Channel 3 0100 : Update NCO Channel 4 … … … 1111 : Update NCO Channel 15	0x0	R/W
0x0A85	FINE_DDC_PHASE_INC0	[7:0]	FINE_DDC0_PHASE_INC0		Bits [7:0] of PHASE INCREMENT. NCO Phase Increment Value.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					Twos Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.		
0x0A86	FINE_DDC_PHASE_INC1	[7:0]	FINE_DDC0_PHASE_INC1		Bits [15:8] of PHASE INCREMENT. NCO Phase Increment Value. Twos Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x0A87	FINE_DDC_PHASE_INC2	[7:0]	FINE_DDC0_PHASE_INC2		Bits [23:16] of PHASE INCREMENT. NCO Phase Increment Value. Twos Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x0A88	FINE_DDC_PHASE_INC3	[7:0]	FINE_DDC0_PHASE_INC3		Bits [31:24] of PHASE INCREMENT. NCO Phase Increment Value. Twos Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x0A89	FINE_DDC_PHASE_INC4	[7:0]	FINE_DDC0_PHASE_INC4		Bits [39:32] of PHASE INCREMENT. NCO Phase Increment Value. Twos Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x0A8A	FINE_DDC_PHASE_INC5	[7:0]	FINE_DDC0_PHASE_INC5		Bits [47:40] of PHASE INCREMENT. NCO Phase Increment Value. Twos Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x0A8B	FINE_DDC_PHASE_OFFSET0	[7:0]	FINE_DDC0_PHASE_OFFSET0		Bits [7:0] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x0A8C	FINE_DDC_PHASE_OFFSET1	[7:0]	FINE_DDC0_PHASE_OFFSET1		Bits [15:8] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x0A8D	FINE_DDC_PHASE_OFFSET2	[7:0]	FINE_DDC0_PHASE_OFFSET2		Bits [23:16] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x0A8E	FINE_DDC_PHASE_OFFSET3	[7:0]	FINE_DDC0_PHASE_OFFSET3		Bits [31:24] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x0A8F	FINE_DDC_PHASE_OFFSET4	[7:0]	FINE_DDC0_PHASE_OFFSET4		Bits [39:32] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x0A90	FINE_DDC_PHASE_OFFSET5	[7:0]	FINE_DDC0_PHASE_OFFSET5		Bits [47:40] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x0A91	FINE_DDC_PHASE_INC_FRAC_A0	[7:0]	FINE_DDC0_PHASE_INC_FRAC_A0		Bits [7:0] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W
0x0A92	FINE_DDC_PHASE_INC_FRAC_A1	[7:0]	FINE_DDC0_PHASE_INC_FRAC_A1		Bits [15:8] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0A93	FINE_DDC_PHASE_INC_FRAC_A2	[7:0]	FINE_DDC0_PHASE_INC_FRAC_A2		Bits [23:16] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W
0x0A94	FINE_DDC_PHASE_INC_FRAC_A3	[7:0]	FINE_DDC0_PHASE_INC_FRAC_A3		Bits [31:24] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W
0x0A95	FINE_DDC_PHASE_INC_FRAC_A4	[7:0]	FINE_DDC0_PHASE_INC_FRAC_A4		Bits [39:32] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W
0x0A96	FINE_DDC_PHASE_INC_FRAC_A5	[7:0]	FINE_DDC0_PHASE_INC_FRAC_A5		Bits [47:40] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator.	0x0	R/W
0x0A97	FINE_DDC_PHASE_INC_FRAC_B0	[7:0]	FINE_DDC0_PHASE_INC_FRAC_B0		Bits [7:0] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x0A98	FINE_DDC_PHASE_INC_FRAC_B1	[7:0]	FINE_DDC0_PHASE_INC_FRAC_B1		Bits [15:8] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x0A99	FINE_DDC_PHASE_INC_FRAC_B2	[7:0]	FINE_DDC0_PHASE_INC_FRAC_B2		Bits [23:16] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x0A9A	FINE_DDC_PHASE_INC_FRAC_B3	[7:0]	FINE_DDC0_PHASE_INC_FRAC_B3		Bits [31:24] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x0A9B	FINE_DDC_PHASE_INC_FRAC_B4	[7:0]	FINE_DDC0_PHASE_INC_FRAC_B4		Bits [39:32] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x0A9C	FINE_DDC_PHASE_INC_FRAC_B5	[7:0]	FINE_DDC0_PHASE_INC_FRAC_B5		Bits [47:40] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x0A9D	FINE_DDC_TRANSFER_STATUS	[7:1]	RESERVED		Reserved.	0x0	R
		0	FINE_DDC0_CHIP_TRANSFER_STATUS	0 1	DDC Chip Transfer Status. 1: Transfer of data from main to subordinate registers is complete. 0: Indicates the data transfer is not requested or not completed. DDC chip Transfer Status Bit 0: Indicates the data transfer is not requested or not completed. 1: Transfer of data from main to subordinate registers is complete.	0x0	R
0x0A9E	FINE_DDC_DITHER	[7:2]	RESERVED		Reserved.	0x0	R
		1	FINE_DDC0_PHASE_DITHER_EN	0 1	Phase Dither Enable. 0: Enabled. 1: Disabled.	0x0	R/W
		0	RESERVED		Reserved.	0x0	R/W
0x0A9F	FINE_DDC_TRANSFER_CTRL	[7:1]	RESERVED		Reserved.	0x0	R
		0	FINE_DDC0_CHIP_TRANSFER		DDC Chip Transfer.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					1: Used to synchronize the transfer of data from main to subordinate registers. 0: Do nothing. Note: This bit is used to update the DDC Phase Increment and Phase Offset registers when FINE_DDC0_PROFILE_UPDATE_MODE = 1 and FINE_DDC0_GPIO_CHIP_TRANSFER_MODE = 0.		
0x0AA0	FINE_DDC_PSW_0	[7:0]	FINE_DDC0_PSW0		Bits [7:0] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x0AA1	FINE_DDC_PSW_1	[7:0]	FINE_DDC0_PSW1		Bits [15:8] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x0AA2	FINE_DDC_PSW_2	[7:0]	FINE_DDC0_PSW2		Bits [23:16] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x0AA3	FINE_DDC_PSW_3	[7:0]	FINE_DDC0_PSW3		Bits [31:24] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x0AA4	FINE_DDC_PSW_4	[7:0]	FINE_DDC0_PSW4		Bits [39:32] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x0AA5	FINE_DDC_PSW_5	[7:0]	FINE_DDC0_PSW5		Bits [47:40] of DDC Profile Select Word (PSW). The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x0AA6	FINE_DDC_ACTIVE_PHASE_INC0	[7:0]	FINE_DDC0_ACTIVE_PHASE_INC0		Bits [7:0] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R
0x0AA7	FINE_DDC_ACTIVE_PHASE_INC1	[7:0]	FINE_DDC0_ACTIVE_PHASE_INC1		Bits [15:8] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R
0x0AA8	FINE_DDC_ACTIVE_PHASE_INC2	[7:0]	FINE_DDC0_ACTIVE_PHASE_INC2		Bits [23:16] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R
0x0AA9	FINE_DDC_ACTIVE_PHASE_INC3	[7:0]	FINE_DDC0_ACTIVE_PHASE_INC3		Bits [31:24] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R
0x0AAA	FINE_DDC_ACTIVE_PHASE_INC4	[7:0]	FINE_DDC0_ACTIVE_PHASE_INC4		Bits [39:32] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0AAB	FINE_DDC_ACTIVE_PHASE_INC5	[7:0]	FINE_DDC0_ACTIVE_PHASE_INC5		Bits [47:40] of ACTIVE PHASE INCREMENT. NCO Active Phase Increment Value.	0x0	R
0x0AAC	FINE_DDC_ACTIVE_PHASE_OFFSET0	[7:0]	FINE_DDC0_ACTIVE_PHASE_OFFSET0		Bits [7:0] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0AAD	FINE_DDC_ACTIVE_PHASE_OFFSET1	[7:0]	FINE_DDC0_ACTIVE_PHASE_OFFSET1		Bits [15:8] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0AAE	FINE_DDC_ACTIVE_PHASE_OFFSET2	[7:0]	FINE_DDC0_ACTIVE_PHASE_OFFSET2		Bits [23:16] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0AAF	FINE_DDC_ACTIVE_PHASE_OFFSET3	[7:0]	FINE_DDC0_ACTIVE_PHASE_OFFSET3		Bits [31:24] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0AB0	FINE_DDC_ACTIVE_PHASE_OFFSET4	[7:0]	FINE_DDC0_ACTIVE_PHASE_OFFSET4		Bits [39:32] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0AB1	FINE_DDC_ACTIVE_PHASE_OFFSET5	[7:0]	FINE_DDC0_ACTIVE_PHASE_OFFSET5		Bits [47:40] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x0AB9	FINE_COUNTER_LOAD_REG0	[7:0]	FINE_COUNTER_LOAD_REG[7:0]		Counter Load Register.	0x0	R/W
0x0ABA	FINE_COUNTER_LOAD_REG1	[7:0]	FINE_COUNTER_LOAD_REG[15:8]		Counter Load Register.	0x0	R/W
0x0ABB	FINE_COUNTER_LOAD_REG2	[7:0]	FINE_COUNTER_LOAD_REG[23:16]		Counter Load Register.	0x0	R/W
0x0ABC	FINE_COUNTER_LOAD_REG3	[7:0]	FINE_COUNTER_LOAD_REG[31:24]		Counter Load Register.	0x0	R/W
0x0ABD	FINE_COUNTER_LOAD_REG4	[7:0]	FINE_COUNTER_LOAD_REG[39:32]		Counter Load Register.	0x0	R/W
0x0ABE	FINE_COUNTER_LOAD_REG5	[7:0]	FINE_COUNTER_LOAD_REG[47:40]		Counter Load Register.	0x0	R/W
0x0B00	EQ_CTRL	[7:3]	RESERVED		Reserved.	0x0	R
		2	EQ_GPIO_EN		GPIO Enable for EQ. GPIO_EN: (default 0). 0 : The bitfield EQSEL selects among four set of coefficient values (COEF0_* , COEF1_*, COEF2_* or COEF3_*) 1: GPIO inputs to EQ select among four set of coefficient values (COEF0_* , COEF1_*, COEF2_* or COEF3_*)	0x0	R/W
		[1:0]	RESERVED		Reserved.	0x0	R
0x0B01	CSHIFT0	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CSHIFT0		Cyclic Shifts Required on Data. CSHIFT0[3:0] for FD: (default 8). 0 : -8 cycle shift 1 : -7 cycle shift 2 : -6 cycle shift 3 : -5 cycle shift 4 : -4 cycle shift 5 : -3 cycle shift 6 : -2 cycle shift 7 : -1 cycle shift 8 : 0 cycle shift 9 : +1 cycle shift A : +2 cycle shift B : +3 cycle shift C : +4 cycle shift D : +5 cycle shift	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					E : +6 cycle shift F : +7 cycle shift		
0x0B02	CSHIFT1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CSHIFT1		Cyclic Shifts Required on Data. CSHIFT1[3:0] for FD: (default 8). 0 : -8 cycle shift 1 : -7 cycle shift 2 : -6 cycle shift 3 : -5 cycle shift 4 : -4 cycle shift 5 : -3 cycle shift 6 : -2 cycle shift 7 : -1 cycle shift 8 : 0 cycle shift 9 : +1 cycle shift A : +2 cycle shift B : +3 cycle shift C : +4 cycle shift D : +5 cycle shift E : +6 cycle shift F : +7 cycle shift	0x0	R/W
0x0B03	CSHIFT2	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CSHIFT2		Cyclic Shifts Required on Data. CSHIFT2[3:0] for FD: (default 8). 0 : -8 cycle shift 1 : -7 cycle shift 2 : -6 cycle shift 3 : -5 cycle shift 4 : -4 cycle shift 5 : -3 cycle shift 6 : -2 cycle shift 7 : -1 cycle shift 8 : 0 cycle shift 9 : +1 cycle shift A : +2 cycle shift B : +3 cycle shift C : +4 cycle shift D : +5 cycle shift E : +6 cycle shift F : +7 cycle shift	0x0	R/W
0x0B04	CSHIFT3	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CSHIFT3		Cyclic Shifts Required on Data. CSHIFT3[3:0] for FD: (default 8). 0 : -8 cycle shift 1 : -7 cycle shift 2 : -6 cycle shift 3 : -5 cycle shift 4 : -4 cycle shift 5 : -3 cycle shift 6 : -2 cycle shift 7 : -1 cycle shift 8 : 0 cycle shift	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					9 : +1 cycle shift A : +2 cycle shift B : +3 cycle shift C : +4 cycle shift D : +5 cycle shift E : +6 cycle shift F : +7 cycle shift		
0x0B05	CD_CTRL	[7:3]	RESERVED		Reserved.	0x0	R
		2	CD_GPIO_EN		Enable GPIO for CD. CD_GPIO_EN: (default 0).	0x0	R/W
				0	0: The bit field CDSEL selects amongst four CSHIFT values.		
				1	1: GPIO input selects amongst four CSHIFT values.		
		[1:0]	CDSEL		Select Amongst Four Cyclic Delay Values. CDSEL[1:0] for CDELAY: (default 0).	0x0	R/W
				00	0: CSHIFT0 are delays applied.		
				01	1: CSHIFT1 are delays applied.		
				10	2: CSHIFT2 are delays applied.		
				11	3: CSHIFT3 are delays applied.		
0x0B06	FD_CTRL	[7:6]	RESERVED		Reserved.	0x0	R
		5	EQ_UPSAMP_CLK_SEL		EQ Upsampler Clock Select.	0x0	R/W
				0	0: dformat_link0_clk selected.		
				1	1: dformat_link1_clk_selected.		
		4	FDELAY_DOWNSAMPLE_EN		Fdelay Downsample Enable.	0x0	R/W
				0	0:Disable Down Sample.		
				1	1:Enable Down Sample.		
		3	FD_EN		Enables/Disables FD block.	0x0	R/W
				0	0: Disable FD.		
				1	1: Enable FD.		
		2	FD_GPIO_EN		Enable GPIO for FD. FD_GPIO_EN: (default 0).	0x0	R/W
				0	0: The bit field FDSEL selects amongst four FSHIFT values.		
				1	1: GPIO input selects amongst four FSHIFT values.		
		[1:0]	FDSEL		Select Amongst Four Fractional Delay Values. FDSEL[1:0] for FD: (default 0).	0x0	R/W
				00	0: FSHIFT0 are delays applied.		
				01	1: FSHIFT1 are delays applied.		
				10	2: FSHIFT2 are delays applied.		
				11	3: FSHIFT3 are delays applied.		
0x0B07	FSHIFT0	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	FSHIFT0		Fractional Delay Required on Data. FSHIFT0[3:0] for FD: (default 0). 0 : no cycle shift 1 : 1/16 cycle shift 2 : 2/16 cycle shift 3 : 3/16 cycle shift 4 : 4/16 cycle shift 5 : 5/16 cycle shift 6 : 6/16 cycle shift 7 : 7/16 cycle shift 8 : 8/16 cycle shift	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					9 : 9/16 cycle shift 10 : 10/16 cycle shift 11: 11/16 cycle shift 12 : 12/16 cycle shift 13: 13/16 cycle shift 14 : 14/16 cycle shift 15 : 15/16 cycle shift		
0x0B08	FSHIFT1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	FSHIFT1		Fractional Delay Required on Data. FSHIFT1[3:0] for FD: (default 0). 0 : no cycle shift 1 : 1/16 cycle shift 2 : 2/16 cycle shift 3 : 3/16 cycle shift 4 : 4/16 cycle shift 5 : 5/16 cycle shift 6 : 6/16 cycle shift 7 : 7/16 cycle shift 8 : 8/16 cycle shift 9 : 9/16 cycle shift 10 : 10/16 cycle shift 11: 11/16 cycle shift 12 : 12/16 cycle shift 13: 13/16 cycle shift 14 : 14/16 cycle shift 15 : 15/16 cycle shift	0x0	R/W
0x0B09	FSHIFT2	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	FSHIFT2		Fractional Delay Required on Data. FSHIFT2[3:0] for FD: (default 0). 0 : no cycle shift 1 : 1/16 cycle shift 2 : 2/16 cycle shift 3 : 3/16 cycle shift 4 : 4/16 cycle shift 5 : 5/16 cycle shift 6 : 6/16 cycle shift 7 : 7/16 cycle shift 8 : 8/16 cycle shift 9 : 9/16 cycle shift 10 : 10/16 cycle shift 11: 11/16 cycle shift 12 : 12/16 cycle shift 13: 13/16 cycle shift 14 : 14/16 cycle shift 15 : 15/16 cycle shift	0x0	R/W
0x0B0A	FSHIFT3	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	FSHIFT3		Fractional Delay Required on Data. FSHIFT3[3:0] for FD: (default 0). 0 : no cycle shift 1 : 1/16 cycle shift 2 : 2/16 cycle shift	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					3 : 3/16 cycle shift 4 : 4/16 cycle shift 5 : 5/16 cycle shift 6 : 6/16 cycle shift 7 : 7/16 cycle shift 8 : 8/16 cycle shift 9 : 9/16 cycle shift 10 : 10/16 cycle shift 11: 11/16 cycle shift 12 : 12/16 cycle shift 13: 13/16 cycle shift 14 : 14/16 cycle shift 15 : 15/16 cycle shift		
0x0B12	PFILT_DIN_SELECT	[7:4]	RESERVED		Reserved.	0x0	R
		[3:2]	PFILT_DIN_Q_SEL		Pfilt Q Path Din Select. PFILT_DIN_Q_SEL: Page 0 (PFILT_CTL_PAGE_MSK[0] == 1) PFILT Q-path Din Select 0: ADC1 data at pfilt Q-path input 1: ADC2 data at pfilt Q-path input 2: ADC3 data at pfilt Q-path input 3: ADC0 data at pfilt Q-path input Page 1 (PFILT_CTL_PAGE_MSK[1] == 1) PFILT Q-path Din Select 0: ADC3 data at pfilt I-path input 1: ADC0 data at pfilt I-path input 2: ADC1 data at pfilt I-path input 3: ADC2 data at pfilt I-path input	0x0	R/W
		[1:0]	PFILT_DIN_I_SEL		Pfilt I Path Din Select. PFILT_DIN_I_SEL: Page 0 (PFILT_CTL_PAGE_MSK[0] == 1) PFILT I-path Din Select 0: ADC0 data at pfilt I-path input 1: ADC1 data at pfilt I-path input 2: ADC2 data at pfilt I-path input 3: ADC3 data at pfilt I-path input Page 1 (PFILT_CTL_PAGE_MSK[1] == 1) PFILT I-path Din Select 0: ADC2 data at pfilt I-path input 1: ADC3 data at pfilt I-path input 2: ADC0 data at pfilt I-path input 3: ADC1 data at pfilt I-path input	0x0	R/W
0x0B13	PFILT_OUT_SELECT	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	PFILT_OUT_SELECT		Pfilt Output Mux Out Selection.	0x0	R/W
				00	0: ADC Data (default).		
				01	1: Pfilt I-path Data.		
				10	2: Pfilt Q-path Data.		
				11	3: reserved.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x0B14	CDELAY_ENABLE	[7:1]	RESERVED		Reserved.	0x0	R
		0	CD_EN		Cdelay Enable.	0x0	R/W
				0	0: Pfilt out mux data at Cdelay mux output.		
				1	1: Cdelay output data at Cdelay mux output.		
0x0B18	FDELAY_IO_MUX_SEL	[7:1]	RESERVED		Reserved.	0x0	R
		0	FDELAY_IO_MUX_SEL		Mapping of Fdelay with Coarse ddc mixer; Fdelay IO Mux Sel.	0x0	R/W
				0	0: Fdelay IO connected with Coarse_DDC0 mixer.		
				1	1: Fdelay IO connected with Coarse_DDC3 mixer.		
0x0B19	ORX_CTRL1	[7:4]	RESERVED		Reserved.	0x0	R
		3	ORX_FD_CTL		ORX Based FDel Control Enable. Enables/Disables ORX (GPIO/Regmap) based control of FracDelay. 0 =>disables control 1 => Enables control	0x0	R/W
		2	ORX_REG		Regmap ORX Enable. Enables/Disables ORX blocks (if ORX_REG_EN =1 and ORX_GPIO_EN=0).	0x1	R/W
				0	0: Disable ORX blocks.		
				1	1: Enable ORX blocks.		
		1	ORX_REG_EN		Regmap ORX Control Enable. Enables/Disables Regmap based control of ORx blocks. 0: Disable Regmap based control 1: Enable Regmap based control ORX_REG is the controlling regmap bit	0x0	R/W
		0	ORX_GPIO_EN		GPIO ORX Control Enable. Enables/Disables GPIO based control of ORx blocks.	0x0	R/W
				0	0: Disable GPIO based control.		
				1	1: Enable GPIO based control.		
0x0B1A	ORX_CTRL2	[7:4]	ORX_PFIR_CTL		ORX Based PFIR Control Enable. Each of bits [3:0] Enables/Disables ORX(GPIO/Regmap) based control of PFIR[3:0]. 0 =>disables control 1 => Enables control	0x0	R/W
		[3:0]	ORX_CD_CTL		ORX Based CycDel Control Enable. Each of bits [3:0] Enables/Disables ORX(GPIO/Regmap) based control of CycDelay[3:0] 0 =>disables control 1 => Enables control	0x0	R/W
0x0C0C	PFIR_MODE	[7:4]	PFIR_Q_MODE		Pfir Q Mode. Programmable Filter (PFIR) Mode. 000: Disabled (filters bypassed) 001: Real N-Tap Filter for each I/Q channel (X only) 010: Real 2 * N-Tap Filter for each I/Q channel (X and Y together) 100: Real set of two cascaded N-Tap Filters for each I/Q channel (X then Y cascaded) 101: Full Complex Filter using Four Real N-Tap Filters for the I/Q channels (pfir_i_mode must also be set to 101) 110-111: Reserved. Programmable Filter (PFIR) Mode	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					000: Disabled (filters bypassed) 001: Real N-Tap Filter for each I/Q channel (X only) 010: Real 2 * N-Tap Filter for each I/Q channel (X and Y together) 100: Real set of two cascaded N-Tap Filters for each I/Q channel (X then Y cascaded) 101: Full Complex Filter using Four Real N-Tap Filters for the I/Q channels (pfir_i_mode must also be set to 101) 110-111: Reserved		
		[3:0]	PFIR_I_MODE		Pfir I Mode. Programmable Filter (PFIR) Mode 000: Disabled (filters bypassed) 001: Real N-Tap Filter for each I/Q channel (X only) 010: Real 2 * N-Tap Filter for each I/Q channel (X and Y together) 100: Real set of two cascaded N-Tap Filters for each I/Q channel (X then Y cascaded) 101: Full Complex Filter using Four Real N-Tap Filters for the I/Q channels (pfir_q_mode must also be set to 101) 110-111: Reserved. Programmable Filter (PFIR) Mode 000: Disabled (filters bypassed) 001: Real N-Tap Filter for each I/Q channel (X only) 010: Real 2 * N-Tap Filter for each I/Q channel (X and Y together) 100: Real set of two cascaded N-Tap Filters for each I/Q channel (X then Y cascaded) 101: Full Complex Filter using Four Real N-Tap Filters for the I/Q channels (pfir_q_mode must also be set to 101) 110-111: Reserved	0x0	R/W
0x0C0D	PFIR_I_GAIN	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	PFIR_IY_GAIN		Pfir Iy Gain. Programmable Gain/Loss (twos complement). 100-101: Undefined 110: -12 dB Loss 111: -6 dB Loss 000: 0 dB Gain 001: +6 dB Gain 010: +12 dB Gain 011: Undefined. Programmable Gain/Loss (two's complement) 100-101: Undefined 110: -12 dB Loss 111: -6 dB Loss 000: 0 dB Gain 001: +6 dB Gain 010: +12 dB Gain 011: Undefined	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[2:0]	PFIR_IX_GAIN		Pfir Ix Gain. Programmable Gain/Loss (twos complement).	0x0	R/W
					100-101: Undefined 110: -12 dB Loss 111: -6 dB Loss 000: 0 dB Gain 001: +6 dB Gain 010: +12 dB Gain 011: Undefined. Programmable Gain/Loss (twos complement) 100-101: Undefined 110: -12 dB Loss 111: -6 dB Loss 000: 0 dB Gain 001: +6 dB Gain 010: +12 dB Gain 011: Undefined		
0x0C0F	PFIR_Q_GAIN	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	PFIR_QY_GAIN		Pfir Qy Gain. Programmable Gain/Loss (two's complement).	0x0	R/W
				110	110: -12 dB Loss.		
				111	111: -6 dB Loss.		
				000	000: 0 dB Gain.		
				001	001: +6 dB Gain.		
				010	010: +12 dB Gain.		
				011	011: Undefined.		
				else	100-101: Undefined.		
		[2:0]	PFIR_QX_GAIN		Pfir Qx Gain. Programmable Gain/Loss (two's complement).	0x0	R/W
				110	110: -12 dB Loss.		
				111	111: -6 dB Loss.		
				000	000: 0 dB Gain.		
				001	001: +6 dB Gain.		
				010	010: +12 dB Gain.		
				011	011: Undefined.		
				else	100-101: Undefined.		
0x0C11	DELAY_SETTING	[7:0]	DELAY_SETTING		Delay Setting for Half Complex mode.	0x0	R/W
0x0C17	PFIR_COEFF_TRANSFER	[7:1]	RESERVED		Reserved.	0x0	R
		0	PFIR_COEFF_TRANSFER		Pfir Coeff Transfer. Coefficient Transfer Signal. Transfers all coefficient data from main registers to subordinate registers.	0x0	R/W
0x0C1A	HC_PROG_DELAY	7	RESERVED		Reserved.	0x0	R
		[6:0]	HC_PROG_DELAY		I Programmable delay line setting for image cancellation filter.	0x0	R/W
0x0C1C	QUAD_MODE	[7:1]	RESERVED		Reserved.	0x0	R
		0	QUAD_MODE		Quad mode select.	0x0	R/W
0x0C1D	COEFF_LOAD_SEL	7	GPIO_CONFIG1			0x0	R/W
		6	RESERVED		Reserved.	0x0	R/W
		5	COEFF_CLEAR		Clears the currently selected main coefficient bank.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		4	COMPLEX_LOAD			0x0	R/W
		3	REAL_CROSS_Q_LOAD			0x0	R/W
		2	REAL_CROSS_I_LOAD			0x0	R/W
		1	REAL_Q_LOAD			0x0	R/W
		0	REAL_I_LOAD			0x0	R/W
0x0C1E	RD_COEFF_PAGE_SEL	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	RD_COEFF_PAGE_SEL		Selects the coefficient page for PFILT.	0x0	R/W
0x0FB0	SYSREF_CONTROL	[7:4]	RESERVED		Reserved.	0x0	R
		3	SPI_SYSREF_EN		Enables sysref capture.	0x0	R/W
		[2:0]	RESERVED		Reserved.	0x0	R
0x0FB1	SPI_EN_FDLY_SYS	[7:2]	RESERVED		Reserved.	0x0	R
		1	SPI_EN_SFDLY_SYS		Bit to enable super fine delay on the SYSREF input. Register 0x0FB3 sets the super fine delay amount 1 = enable super fine delay. Note that there is a small phase step from SYSREF delay “off” to SYSREF delay “on”.	0x0	R/W
		0	SPI_EN_FDLY_SYS		Bit to enable fine delay on the SYSREF input. Register 0x0FB2 sets the fine delay amount. 1 = enable fine delay. Note that there is a small phase step from SYSREF delay “off” to SYSREF delay “on”.	0x0	R/W
0x0FB2	SPI_TRM_FINE_DLY_SYS	[7:0]	SPI_TRM_FINE_DLY_SYS		Fine delay adjustment of the SYSREF input in 1.1 ps steps with a max adjustment range of 56 ps. Applicable when 0x0FB1[0] = 1. Note the maximum effective setting is 0x2F where the 56 ps of adjustment range is realized. Values above this have no effect on the delay.	0x0	R/W
0x0FB3	SPI_TRM_SUPER_FINE_DLY_SYS	[7:0]	SPI_TRM_SUPER_FINE_DLY_SYS		Super-fine delay adjustment of the SYSREF input in ~16 fs steps. Applicable when 0x0FB1[1] = 1. Maximum superfine delay is approximately 4 ps (255×16 fs).	0x0	R/W
0x0FB6	SYSREF_CTRL	[7:2]	RESERVED		Reserved.	0x0	R
		1	SYSREF_TRANSITION_SEL		SYSREF Transition Selection.	0x0	R/W
				0	0: SYSREF is valid on LOW to HIGH transitions using selected CLK edge.		
				1	1: SYSREF is valid on HIGH to LOW transitions using selected CLK edge.		
		0	SYSREF_EDGE_SEL		SYSREF Capture Edge Selection.	0x0	R/W
				0	0: SYSREF Captured on Rising Edge of CLK input.		
				1	1: SYSREF Captured on Falling Edge of CLK input.		
0x0FB7	SYSREF_HOLD	[7:0]	SYSREF_HOLD		Read only register used with SYSREF_SETUP to determine if a potential setup or hold time violation exists. See the SYSREF Setup and Hold Time Monitor section.	0x0	R
0x0FB8	SYSREF_SETUP	[7:0]	SYSREF_SETUP		Read only register used with SYSREF_SETUP to determine if a potential setup or hold time violation exists. See the SYSREF Setup and Hold Time Monitor section.	0x0	R
0x0FB9	SYSREF_DC_SE_MODE_SEL	[7:5]	RESERVED		Reserved.	0x0	R
		4	SYSREF_SINGLE_END_MODE_SEL		0: not single ended, 1: 1.8V single ended input mode.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[3:1]	RESERVED		Reserved.	0x1	R
		0	SYSREF_DC_MODE_SEL		0 = ac couple,1 = dc couple.	0x1	R/W
0x1721	MBIAS_SPARE1	[7:6]	CMBUF_PD		Power down common-mode buffer.	0x0	R/W
				10	10: always use for AD9082, AD9986, AD9207.		
				11	11: always use for AD9081, AD9988, AD9209.		
				else	Other values are undefined.		
		[5:0]	RESERVED		Reserved.	0x0	R
0x1729	SPI_NVG	[7:1]	RESERVED		Reserved.	0x1F	R
		0	SPI_EN_NVG_1P0		SPI Enable bit for NVG.	0x0	R/W
0x1732	SPI_CMIN_INPUT	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	SPI_CMIN_INPUT_SEL		select inputs to CMFB circuit of input buffer.	0x0	R/W
				0000	0000: always use for AD9082, AD9986, AD9207.		
				1110	1110: always use for AD9081, AD9988, AD9209.		
				else	Other values are undefined.		
0x1733	SPI_CMIN_OUT	7	RESERVED		Reserved.	0x0	R
		[6:3]	SPI_CMIN_OUT_SEL		select outputs to CMFB circuit of input buffer.	0x0	R/W
				0000	0000: AC coupled mode for AD9082, AD9986, AD9207.		
				0100	0100: DC coupled mode for AD9082, AD9986, AD9207, AD9081, AD9988, AD9209.		
				1110	1110: AC coupled mode for AD9081, AD9988, AD9209.		
				else	Other values are undefined.		
		[2:0]	SPI_CMIN_OUT_PULDWN		Pulls VCMx pin low when common-mode buffer disabled.	0x0	R/W
				011	011: AC coupled mode for AD9082, AD9986, AD9207.		
				100	100: AC coupled mode for AD9081, AD9988, AD9209.		
				111	111: DC coupled mode for AD9082, AD9986, AD9207, AD9081, AD9988, AD9209.		
				else	Other values are undefined.		
0x1900 to 0x1A7E by 2	COEFF_LSBn	[7:0]	COEFF[7:0]		Coefficient. PFILT COEF0. PFILT COEF0	0x0	R/W
0x1901 to 0x1A7F by 2	COEFF_MSBn	[7:0]	COEFF[15:8]		Coefficient. PFILT COEF0. PFILT COEF0	0x0	R/W
0x2008	CLK_PLL_STATUS	[7:2]	RESERVED		Reserved.	0x0	R
		1	PLL_LOCK_FAST		Fast lock detect readback for clocking PLL. This readback is enabled by setting D_PLL_LOCK_CONTROL (0xEC[2:1]) to either 1 or 3.	0x0	R
		0	PLL_LOCK_SLOW		Slow lock detect readback for clocking PLL. This readback is enabled by setting D_PLL_LOCK_CONTROL (0xEC[2:1]) to either 2 or 3.	0x0	R
0x2061	SAMPLE_PRBS_CTRL0	7	RESERVED		Reserved.	0x0	R
		6	SAMPLE_PRBS_ENABLE		Sample PRBS test enable.	0x0	R/W
				0	0 = Sample PRBS test is inactive.		
				1	1 = Start sample PRBS test.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		[5:3]	PRBS_CHNL_SEL		Channelizer channel select for sample PRBS test.	0x0	R/W
				000	0 = select Channelizer 0 for testing.		
				001	1 = select Channelizer 1 for testing.		
				010	2 = select Channelizer 2 for testing.		
				011	3 = select Channelizer 3 for testing.		
				100	4 = select Channelizer 4 for testing.		
				101	5 = select Channelizer 5 for testing.		
				110	6 = select Channelizer 6 for testing.		
				111	7 = select Channelizer 7 for testing.		
		2	CLR_ERRORS		Clear PRBS Errors. Toggle this bit from 0 to 1 and then back to 0 to clear the PRBS error flags in Register 0x2063.	0x0	R/W
		1	SWAP_ENDIANNESS		Swap endianness (bit reversal).	0x0	R/W
				0	0 = Don't swap endianness.		
				1	1 = reverse the bit order of the PRBS sample checker.		
		0	UPDATE_ERROR_COUNT		Update Error Counter. Toggle this bit from 0 to 1 and the back to 0 to update the PRBS error counter in Register 0x2064 to Register 0x2069.	0x0	R/W
0x2062	SAMPLE_PRBS_CTRL1	[7:5]	RESERVED		Reserved.	0x0	R
		4	PRBS_INV_IMAG		1= invert the data of the imaginary path to the sample prbs checker.	0x0	R/W
		3	PRBS_INV_REAL		1= invert the data of the real path to the sample prbs checker.	0x0	R/W
		[2:0]	PRBS_MODE		Sample PRBS test mode.	0x0	R/W
				000	0 = Pattern checker is off.		
				001	1 = PRBS7.		
				010	2 = PRBS9.		
				011	3 = PRBS15.		
				100	4 = PRBS23.		
				101	5 = PRBS31.		
				Else	Else = Not valid.		
0x2063	SAMPLE_PRBS_STATUS0	[7:4]	RESERVED		Reserved.	0x0	R
		3	PRBS_ERROR_FLAG_Q		Q-data sample PRBS error flag. `JRX_DIGTOP.u_prbs_sample_wrapper.o_error_flag_imag	0x0	R
				0	0 = no errors detected in the Q-data path of the selected channel.		
				1	1 = error(s) detected in the Q-data path of the selected channel.		
		2	PRBS_ERROR_FLAG_I		I-data sample PRBS error flag. `JRX_DIGTOP.u_prbs_sample_wrapper.o_error_flag_real	0x0	R
				0	0 = no errors detected in the I-data path of the selected channel.		
				1	1 = error(s) detected in the I-data path of the selected channel.		
		1	PRBS_INVALID_DATA_FLAG_Q		Q-data sample PRBS invalid data flag. `JRX_DIGTOP.u_prbs_sample_wrapper.o_prbs_invalid_flag_imag	0x0	R

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				0 1	0 = no invalid data detected in the Q-data path of the selected channel. 1 = invalid data detected in the Q-data path of the selected channel.		
		0	PRBS_INVALID_DATA_FLAG_I	0 1	I-data sample PRBS invalid data flag. `JRX_DIGTOP.u_prbs_sample_wrapper.o_prbs_invalid_flag_real 0 = no invalid data detected in the I-data path of the selected channel. 1 = invalid data detected in the I-data path of the selected channel.	0x0	R
0x2064	SAMPLE_PRBS_STATUS1	[7:0]	ERROR_COUNT_I[7:0]		I-data sample PRBS error counter readback. Displays the number of PRBS errors detected on the selected channel (PRBS_CHNL_SEL) when updated using UPDATE_ERROR_COUNT (0x2061[0]).	0x0	R
0x2065	SAMPLE_PRBS_STATUS2	[7:0]	ERROR_COUNT_I[15:8]		I-data sample PRBS error counter readback. Displays the number of PRBS errors detected on the selected channel (PRBS_CHNL_SEL) when updated using UPDATE_ERROR_COUNT (0x2061[0]).	0x0	R
0x2066	SAMPLE_PRBS_STATUS3	[7:0]	ERROR_COUNT_I[23:16]		I-data sample PRBS error counter readback. Displays the number of PRBS errors detected on the selected channel (PRBS_CHNL_SEL) when updated using UPDATE_ERROR_COUNT (0x2061[0]).	0x0	R
0x2067	SAMPLE_PRBS_STATUS4	[7:0]	ERROR_COUNT_Q[7:0]		Q-data sample PRBS error counter readback. Displays the number of PRBS errors detected on the selected channel (prbs_chnL_sel) when updated using update_error_count (0x2061[0]).	0x0	R
0x2068	SAMPLE_PRBS_STATUS5	[7:0]	ERROR_COUNT_Q[15:8]		Q-data sample PRBS error counter readback. Displays the number of PRBS errors detected on the selected channel (prbs_chnL_sel) when updated using update_error_count (0x2061[0]).	0x0	R
0x2069	SAMPLE_PRBS_STATUS6	[7:0]	ERROR_COUNT_Q[23:16]		Q-data sample PRBS error counter readback. Displays the number of PRBS errors detected on the selected channel (prbs_chnL_sel) when updated using update_error_count (0x2061[0]).	0x0	R
0x20D0	DSA_CFG0	[7:0]	DSA_CTRL		The values of DSA_Ctrl are from 0 to 235. 0 equals no attenuation and 235 equals 47dB attenuation (-47dB gain). The codes will be applied to two lookup tables and will control the gain in both analog and digital side.	0x0	R/W
0x20D1	DSA_CFG1	[7:0]	DSA_CUTOVER		This register will contain a code that governs the switch over from analog to digital gain control. All values of total gain below DSA_Cutover will be actuated using analog fullscale current. All values of total gain above DSA_Cutover will be actuated using digital gain adjust.	0x0	R/W
0x20D2	DSA_CFG2	7	EN_DSA_CTRL	1	enable DSA control feature	0x0	R/W
		[6:5]	RESERVED		Reserved.	0x0	R/W
		[4:0]	DSA_BOOST		The DAC can support Full scale currents as high as 40mA, but performance cannot be guaranteed above 26mA. For this case the user will have an	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					optional boost ability to elevate the fullscale current above the 26mA baseline current. The value here can range from 0 – 26mA to 19 - +3.8dB or 40mA). Setting by this bit field.		
0x20D3	DP_GAIN0	[7:0]	DP_GAIN[7:0]		12 bit data path digital gain.	0x0	R
0x20D4	DP_GAIN1	7	GAIN_LOAD_STROBE		12-bit data path digital gain load strobe. When this is applied to '1', then the 12-bit value is applied to the gain block, or else the gain value will not be valid. The design will still use the previous old gain value.	0x0	R/W
		[6:4]	RESERVED		Reserved.	0x0	R
		[3:0]	DP_GAIN[11:8]		12 bit data path digital gain.	0x0	R
0x2100	CUSTOMER_UP_TRANSFER	[7:1]	RESERVED		Reserved.	0x0	R
		0	USER_CTRL_TRANSFER			0x0	R/W
				0	Normal operation.		
				1	If set, update the registers 0x2100 to 0x21DD with the values that have been changed. Self-clearing.		
0x2107	MAX_TEMPERATURE_LSB	7	MAX_TEMPERATURE[0]		LSB of Maximum Temperature word. See TMU section.	0x0	R
		[6:0]	RESERVED		Reserved.	0x0	R
0x2108	MAX_TEMPERATURE_MSB	[7:0]	MAX_TEMPERATURE[8:1]		MSBs of Maximum Temperature word. See TMU section.	0x0	R
0x210B	MIN_TEMPERATURE_LSB	7	MIN_TEMPERATURE[0]		LSB of Minimum Temperature word. See TMU section.	0x0	R
		[6:0]	RESERVED		Reserved.	0x0	R
0x210C	MIN_TEMPERATURE_MSB	[7:0]	MIN_TEMPERATURE[8:1]		MSBs of Minimum Temperature word. See TMU section.	0x0	R
0x2110	NYQUIST_ZONE_SELECT	[7:5]	RESERVED		Reserved.	0x0	R
		4	EVEN_NZ_ADC1_CORE1			0x0	R/W
				0	Odd Nyquist zone operation on ADC3 for AD9081/AD9988/AD9209.		
				1	Even Nyquist zone operation on ADC3 for AD9081/AD9988/AD9209. Requires setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
		3	EVEN_NZ_ADC1_CORE0			0x0	R/W
				0	Odd Nyquist zone operation on ADC2 for AD9081/AD9988/AD9209.		
				1	Even Nyquist zone operation on ADC2 for AD9081/AD9988/AD9209. Requires setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
		2	EVEN_NZ_ADC0_CORE1			0x0	R/W
				0	Odd Nyquist zone operation on ADC1 for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207.		
				1	Even Nyquist zone operation on ADC1 for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207. Requires setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
		1	EVEN_NZ_ADC0_CORE0			0x0	R/W
				0	Odd Nyquist zone operation on ADC0 for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				1	Even Nyquist zone operation on ADC0 for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207. Requires setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
		0	FORCE_NYQUIST_ZONE			0x0	R/W
				0	Do not override chip defaults with setup in 0x2110[4:1].		
				1	Force override of chip defaults with values in 0x2110[4:1].		
0x2111	DATA_INVERSION_DC_COUPLING	[7:4]	RESERVED		Reserved.	0x0	R/W
		3	INVERT_ADC1_CORE1		ADC3 Data Invert for AD9081/AD9988/AD9209.	0x0	R/W
				0	No Inversion.		
				1	Invert ADC3 data Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
		2	INVERT_ADC1_CORE0		ADC2 Data Invert for AD9081/AD9988/AD9209.	0x0	R/W
				0	No Inversion.		
				1	Invert ADC2 data Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
		1	INVERT_ADC0_CORE1		ADC1 Data Invert for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207.	0x0	R/W
				0	No Inversion.		
				1	Invert ADC1 data Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
		0	INVERT_ADC0_CORE0		ADC0 Data Invert for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207.	0x0	R/W
				0	No Inversion.		
				1	Invert ADC0 data Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
0x2112	CALL_FREEZE_GLOBAL	[7:1]	RESERVED		Reserved.	0x0	R
		0	CAL_FREEZE_GLOBAL			0x0	R/W
				0	All ADC Calibrations running.		
				1	Stop all ADC calibrations on all ADC channels of AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207 Does not need setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
0x2114	ADC_FLASH_TSKEW_ADJ	[7:6]	RESERVED		Reserved.	0x0	R/W
		[5:4]	ADC_FLASH_TSKEW		Set to {0, 1, 2, 3} to adjust the ADC core's flash sampling time based on ADC sampling rate; Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).	0x0	R/W
		[3:0]	RESERVED		Reserved.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
0x2115	USER_SETTINGS_FOR_ADC_CAL	[7:1]	RESERVED		Reserved.	0x0	R/W
		0	USER_ADC_CAL_ADJUST		Set to {1} to enable user-defined ADC calibration settings . After setting it, it requires user_ctrl_transfer = 1 (address 0x2100). Setting this bit to 1 is required for Offset, Gain, Timing and Histogram calibrations settings to take effect.	0x0	R/W
0x2116	DISABLE_OFFSET_TIMING_CALIBRATION	[7:4]	RESERVED		Reserved.	0x0	R
		3	USER_ADC_TSKEW_CAL_EN_ADC1_CORE1	0 1	Timing Calibration on ADC3 for AD9081/AD9988/AD9209;. Disable ADC3 timing calibration Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1). Enable (Default).	0x1	R/W
		2	USER_ADC_TSKEW_CAL_EN_ADC1_CORE0	0 1	Timing Calibration on ADC2 for AD9081/AD9988/AD9209;. Disable ADC2 timing calibration Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1). Enable (Default).	0x1	R/W
		1	USER_ADC_TSKEW_CAL_EN_ADC0_CORE1	0 1	Timing Calibration on ADC1 for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207. Disable ADC1 timing calibration Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1). Enable (Default).	0x1	R/W
		0	USER_ADC_TSKEW_CAL_EN_ADC0_CORE0	0 1	Timing Calibration on ADC0 for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207. Disable ADC0 timing calibration Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1). Enable (Default).	0x1	R/W
0x2117	DISABLE_OFFSET_GAIN_CALIBRATION	7	USER_ADC_OS_CAL_EN_ADC1_CORE1	0 1	Offset Calibration on ADC3 for AD9081/AD9988/AD9209;. Disable ADC0 offset calibration Requires setting “user_adc_cal_adjust” (Address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1). Enable (Default).	0x1	R/W
		6	USER_ADC_OS_CAL_EN_ADC1_CORE0	0 1	Offset Calibration on ADC2 for AD9081/AD9988/AD9209;. Disable ADC2 offset calibration Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (Aaddress 0x2100[0] = 1). Enable (Default).	0x1	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		5	USER_ADC_OS_CAL_EN_ADC0_CORE1		Offset Calibration on ADC1 for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207.	0x1	R/W
				0	Disable ADC1 offset calibration Requires setting “user_adc_cal_adjust” (Address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
				1	Enable (Default).		
		4	USER_ADC_OS_CAL_EN_ADC0_CORE0		Offset Calibration on ADC0 for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207.	0x1	R/W
				0	Disable ADC1 offset calibration Requires setting “user_adc_cal_adjust” (Address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
				1	Enable (Default).		
		3	USER_ADC_GAIN_CAL_EN_ADC1_CORE1		Gain Calibration on ADC3 for AD9081/AD9988/AD9209;.	0x1	R/W
				0	Disable ADC3 gain calibration Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (Address 0x2100[0] = 1).		
				1	Enable (Default).		
		2	USER_ADC_GAIN_CAL_EN_ADC1_CORE0		Gain Calibration on ADC2 for AD9081/AD9988/AD9209;.	0x1	R/W
				0	Disable ADC2 gain calibration Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
				1	Enable (Default).		
		1	USER_ADC_GAIN_CAL_EN_ADC0_CORE1		Gain Calibration on ADC1 for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207.	0x1	R/W
				0	Disable ADC1 gain calibration Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
				1	Enable (Default).		
		0	USER_ADC_GAIN_CAL_EN_ADC0_CORE0		Gain Calibration on ADC0 for AD9081/AD9988/AD9209 and AD9082/AD9986/AD9207.	0x1	R/W
				0	Disable ADC0 gain calibration Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
				1	Enable (Default).		
0x2124	HISTOGRAM_TH_ADC_CAL	[7:0]	USER_ADC_HIST_QUAL_THRESH		Adjusts the signal distribution requirements for calibrations. Lower value rejects signals with poorer time-domain sample distribution. Requires setting “user_adc_cal_adjust” (address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).	0x0	R/W
0x212C	ADC_FLASH_TSKEW_ADJ_LOW_SAMP_RATE	[7:4]	RESERVED		Reserved.	0x0	R/W
		3	SPARE_DEBUG		Setting for low ADC sample rates.	0x0	R/W
				0	Default; Sample rate > 2 GSPS.		

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
				1	ADC Sample rare ≤ 2GSPS Extend adc_flash_tskew (register 0x2114[5:4]) to work with ADC sampling rates ≤ 2GSPS; Requires setting “user_adc_cal_adjust” (Address 0x2115[0] = 1), followed by setting “user_ctrl_transfer” (address 0x2100[0] = 1).		
		[2:0]	RESERVED		Reserved.	0x0	R/W
0x21C1	RX_SET_STATE1	7	RX_RESET_STATE	0 1	RX state machine status; Bit self-clears bit for acknowledgment. 0 = JESD204B/C receiver PHY calibration state machine is idle. 1 = Reset JESD204B/C receiver calibration state machine.	0x0	R/W
		[6:5]	RESERVED		Reserved.	0x0	R
		4	RX_FG_CAL_ONLY_RUN		When high, setting 'rx_bg_cal_run' causes the FG/BG cal state machine to only run through the foreground section and exit back to the idle state.	0x0	R/W
		3	RX_BG_CAL_RUN		When high, state machine runs through the foreground / background cal indefinitely until brought back low or the state machine is reset.	0x0	R/W
		[2:0]	RESERVED		Reserved.	0x0	R
0x21C2	RX_SET_STATE2	[7:0]	RX_SET_STATE		JESD204B/C receiver PHY calibration configuration. Must be set to 0x31 to optimize the PHY calibration.	0xF0	R/W
0x21C4	RX_RUN_CAL_MASK	[7:0]	RX_RUN_CAL_MASK		Bit per lane enable for PHY calibration. For example, 0x00 = Calibrate no lanes 0xFF = Calibrate all lanes.	0xFF	R/W
0x21DD	RX_STATE_STATUS	[7:1]	RESERVED		Reserved.	0x0	R/W
		0	RX_AT_IDLE		If high, calibration state machine is currently in the idle state.	0x0	R/W
0x2C58	RXAGC_DSA_SEL	[7:6]	DSA_SEL_3		Selecting any DSA onto particular DSA for AGC-Pinmux.	0x3	R/W
		[5:4]	DSA_SEL_2		Selecting any DSA onto particular DSA for AGC-Pinmux.	0x2	R/W
		[3:2]	DSA_SEL_1		Selecting any DSA onto particular DSA for AGC-Pinmux.	0x1	R/W
		[1:0]	DSA_SEL_0		Selecting any DSA onto particular DSA for AGC-Pinmux.	0x0	R/W
0x37CC	PERI_I_SEL12	[7:0]	PERI_I_SEL12		Selects the pad to which peri_in12 is connected drive bit0 of CDDC NCO channel selection. TxFE GPIO[6] =‘h02 TxFE GPIO[7] = ‘h03 TxFE GPIO[8] = ‘h04 TxFE GPIO[9] = ‘h05 TxFE GPIO[10] = ‘h06 TxFE SYNCINB1_P = ‘h07 TxFE SYNCINB1_N = ‘h08	0x0	R/W
0x37CD	PERI_I_SEL13	[7:0]	PERI_I_SEL13		Selects the pad to which peri_in13 is connected drive bit1 of CDDC NCO channel selection. TxFE GPIO[6] = ‘h02 TxFE GPIO[7] = ‘h03 TxFE GPIO[8] = ‘h04	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					TxFE GPIO[9] = 'h05 TxFE GPIO[10] = 'h06 TxFE SYNCINB1_P = 'h07 TxFE SYNCINB1_N = 'h08		
0x37CE	PERI_I_SEL14	[7:0]	PERI_I_SEL14		Selects the pad to which peri_in14 is connected drive bit2 of CDDC NCO channel selection. TxFE GPIO[6] = 'h02 TxFE GPIO[7] = 'h03 TxFE GPIO[8] = 'h04 TxFE GPIO[9] = 'h05 TxFE GPIO[10] = 'h06 TxFE SYNCINB1_P = 'h07 TxFE SYNCINB1_N = 'h08	0x0	R/W
0x37CF	PERI_I_SEL15	[7:0]	PERI_I_SEL15		Selects the pad to which peri_in15 is connected drive bit3 of CDDC NCO channel selection. TxFE GPIO[6] = 'h02 TxFE GPIO[7] = 'h03 TxFE GPIO[8] = 'h04 TxFE GPIO[9] = 'h05 TxFE GPIO[10] = 'h06 TxFE SYNCINB1_P = 'h07 TxFE SYNCINB1_N = 'h08	0x0	R/W
0x37D0	PERI_I_SEL16	[7:0]	PERI_I_SEL16		Selects the pad to which peri_in16 is connected drive bit1 of the 2-bit select which CDDC NCO is chosen for hopping. TxFE GPIO[6] = 'h02 TxFE GPIO[7] = 'h03 TxFE GPIO[8] = 'h04 TxFE GPIO[9] = 'h05 TxFE GPIO[10] = 'h06 TxFE SYNCINB1_P = 'h07 TxFE SYNCINB1_N = 'h08	0x0	R/W
0x37D1	PERI_I_SEL17	[7:0]	PERI_I_SEL17		Selects the pad to which peri_in17 is connected drive bit0 of the 2-bit select which CDDC NCO is chosen for hopping. TxFE GPIO[6] = 'h02 TxFE GPIO[7] = 'h03 TxFE GPIO[8] = 'h04 TxFE GPIO[9] = 'h05 TxFE GPIO[10] = 'h06 TxFE SYNCINB1_P = 'h07 TxFE SYNCINB1_N = 'h08	0x0	R/W
0x37D4	PERI_I_SEL20	[7:0]	PERI_I_SEL20		Selects the pad to which peri_in20 is connected act as FastDetect enable/Signal Monitor Enable. TxFE GPIO[6] = 'h02 TxFE GPIO[7] ='h03 TxFE GPIO[8] = 'h04 TxFE GPIO[9] = 'h05 TxFE GPIO[10] = 'h06	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
					TxFE SYNCINB1_P = 'h07 TxFE SYNCINB1_N = 'h08		
0x37D5	PERI_I_SEL21	[7:0]	PERI_I_SEL21		Selects the pad to which peri_in21 is connected drive bit 0 of the 2-bit selection among four profiles of Programmable Filter/Fractional Delay/ Cycle Delay. TxFE GPIO[6] = 'h02 TxFE GPIO[7] = 'h03 TxFE GPIO[8] = 'h04 TxFE GPIO[9] = 'h05 TxFE GPIO[10] = 'h06 TxFE SYNCINB1_P = 'h07 TxFE SYNCINB1_N = 'h08	0x0	R/W
0x37D6	PERI_I_SEL22	[7:0]	PERI_I_SEL22		Selects the pad to which peri_in22 is connected drive bit 1 of the 2-bit selection among four profiles of Programmable Filter/Fractional Delay/ Cycle Delay. TxFE GPIO[6] = 'h02 TxFE GPIO[7] = 'h03 TxFE GPIO[8] = 'h04 TxFE GPIO[9] = 'h05 TxFE GPIO[10] = 'h06 TxFE SYNCINB1_P = 'h07 TxFE SYNCINB1_N = 'h08	0x0	R/W
0x37D7	PERI_I_SEL23	[7:0]	PERI_I_SEL23		Selects the pad to act as RXENGP0, whose functions are controlled by registers in the range 0x2CE-0x2D0. TxFE GPIO[6] = 'h02 TxFE GPIO[7] = 'h03 TxFE GPIO[8] = 'h04 TxFE GPIO[9] = 'h05 TxFE GPIO[10] = 'h06 TxFE SYNCINB1_P = 'h07 TxFE SYNCINB1_N = 'h08	0x0	R/W
0x37D8	PERI_I_SEL24	[7:0]	PERI_I_SEL24		Selects the pad to act as RXENGP1, whose functions are controlled by registers in the range 0x2D1-0x2D3. TxFE GPIO[6] = 'h02 TxFE GPIO[7] = 'h03 TxFE GPIO[8] = 'h04 TxFE GPIO[9] = 'h05 TxFE GPIO[10] = 'h06 TxFE SYNCINB1_P ='h07 TxFE SYNCINB1_N = 'h08	0x0	R/W
0x37DA	PERI_I_SEL26	[7:0]	PERI_I_SEL26	0x0 0x1	Enable ADCx_SMONx pin (applicable only to AD9082/AD9986/AD9207). 0x00: disable ADCx_SMONx pin. 0x01: enable ADCx_SMONx pin.	0x0	R/W
0x3D26	UP_CTRL	[7:4]	RESERVED		Reserved.	0x0	R
		3	UP_SPI_EDGE_INTERRUPT		Edge triggered interrupt to uP.	0x0	R/W

REGISTER DETAILS

Table 200. (Continued)

Addr	Name	Bits	Bit Name	Setting	Description	Reset	Access
		2	RESERVED		Reserved.	0x0	R
		1	UP_STATVECTORSEL		uP signal to allow selection of the boot address.	0x0	R/W
		0	UP_BRESET		Synchronous reset pin of the uP.	0x0	R/W

NOTES