

MOSFET – Power, Single P-Channel, **POWERTRENCH®**

-30 V, -6.8 A, 35 mΩ

FDMA530PZ

General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance.

The WDFN6 (MicroFET™ 2 × 2) package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- Max $r_{DS(on)}$ = 35 mΩ at $V_{GS} = -10$ V, $I_D = -6.8$ A
- Max $r_{DS(on)}$ = 65 mΩ at $V_{GS} = -4.5$ V, $I_D = -5.0$ A
- Low Profile – 0.8 mm Maximum – in the New Package WDFN6 (MicroFET 2 × 2 mm)
- HBM ESD Protection Level > 3k V Typical (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- RoHS Compliant

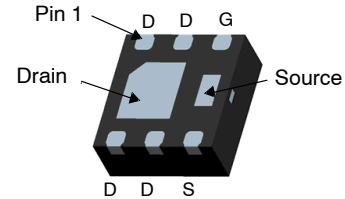
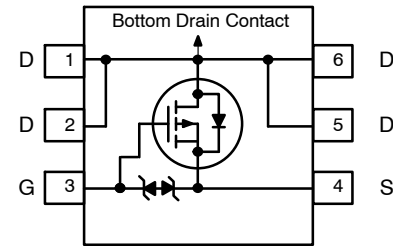
MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{DS}	Drain to Source Voltage		-30	V
V_{GS}	Gate to Source Voltage		±25	V
I_D	Drain Current	Continuous (Note 1a)	-6.8	A
		Pulsed	-24	
P_D	Power Dissipation	(Note 1a)	2.4	W
		(Note 1b)	0.9	
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

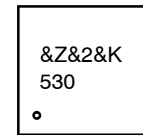
THERMAL CHARACTERISTICS

Symbol	Parameter		Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	52	°C/W
		(Note 1b)	145	



WDFN6 (MicroFET 2 x 2)
CASE 511CZ

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = Date Code
&K = Lot Code
530 = Specific Device Code

ORDERING INFORMATION

Device Marking	Device	Package	Shipping†
530	FDMA530PZ	WDFN6 (MicroFET 2x2)	3000 Units/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDMA530PZ

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C		-23		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V			-1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±25 V, V _{DS} = 0 V			±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-1	-2.1	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C		5.4		mV/°C
r _{DS(on)}	Static Drain to Source on Resistance	V _{GS} = -10 V, I _D = -6.8 A		30	35	mΩ
		V _{GS} = -4.5 V, I _D = -5.0 A		52	65	
		V _{GS} = -10 V, I _D = -6.8 A, T _J = 125°C		43	63	
g _{FS}	Forward Transconductance	V _{DS} = -10 V, I _D = -6.8 A		17		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz		805	1070	pF
C _{oss}	Output Capacitance			155	210	
C _{rss}	Reverse Transfer Capacitance			130	195	
R _g	Gate Resistance	f = 1 MHz	1	18	38	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = -15 V, I _D = -6.8 A, V _{GS} = -10 V, R _{GEN} = 6 Ω		6	12	ns
t _r	Rise Time			21	34	
t _{d(off)}	Turn-Off Delay Time			43	69	
t _f	Fall Time			31	50	
Q _g	Total Gate Charge	V _{GS} = -10 V		16	24	nC
Q _g	Total Gate Charge	V _{GS} = -5 V		9	11	
Q _{gs}	Gate to Source Gate Charge	V _{DD} = -15 V, I _D = -6.8 A		3.1		
Q _{gd}	Gate to Drain "Miller" Charge			4.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

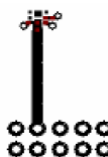
I _S	Maximum Continuous Drain-Source Diode Forward Current				-2	A
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -2 A		-0.8	-1.2	V
t _{rr}	Reverse Recovery Time	I _F = -6.8 A, di/dt = 100 A/μS		24	36	ns
Q _{rr}	Reverse Recovery Charge			19	29	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.



a. 52 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 145 °C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- The diode connected between the gate and the source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

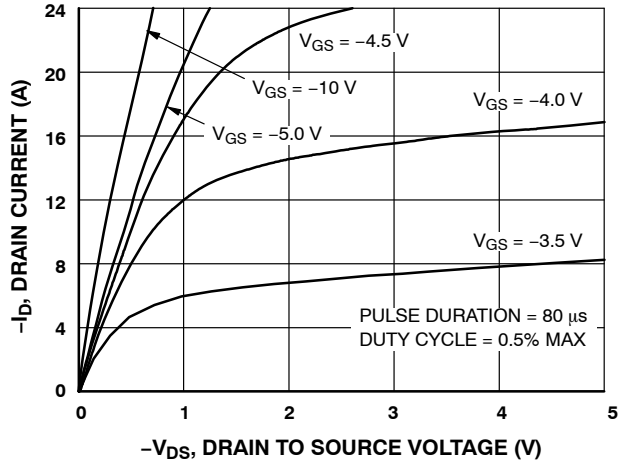


Figure 1. On-Region Characteristics

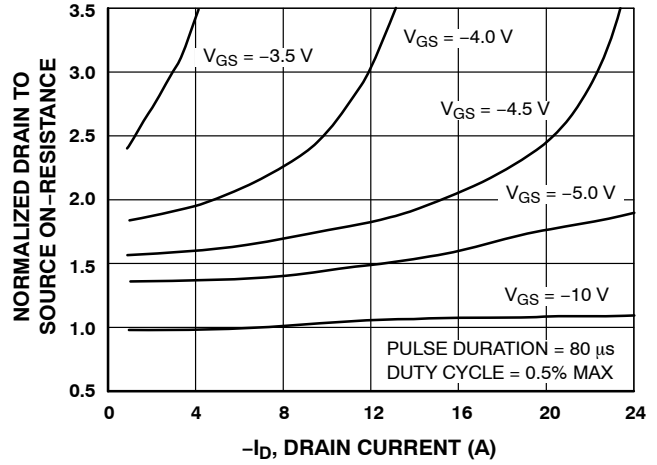


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

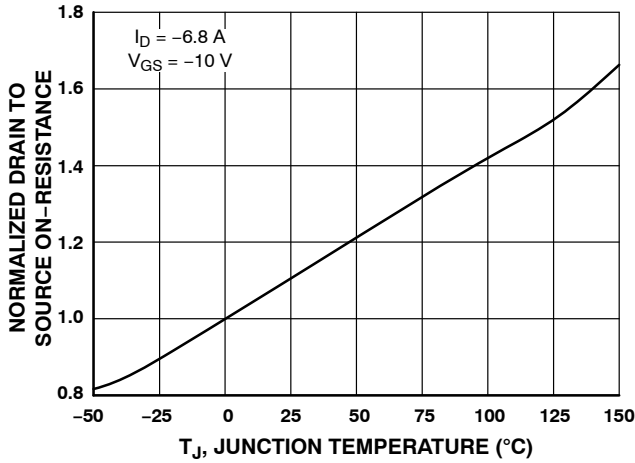


Figure 3. Normalized On-Resistance vs. Junction Temperature

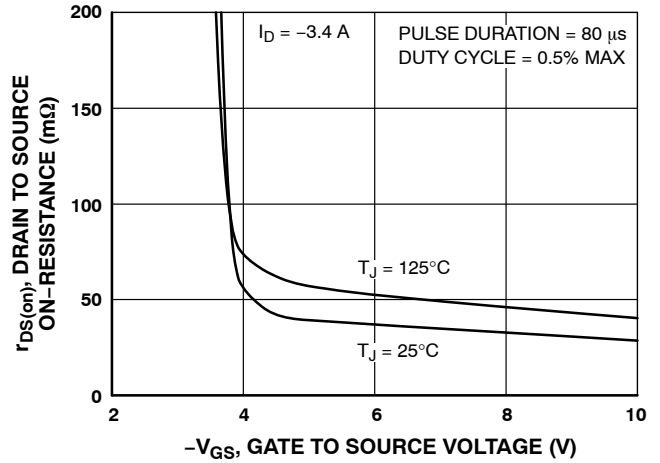


Figure 4. On-Resistance vs. Gate to Source Voltage

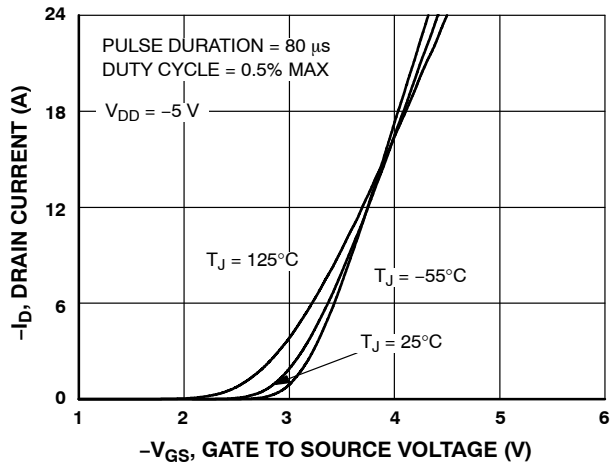


Figure 5. Transfer Characteristics

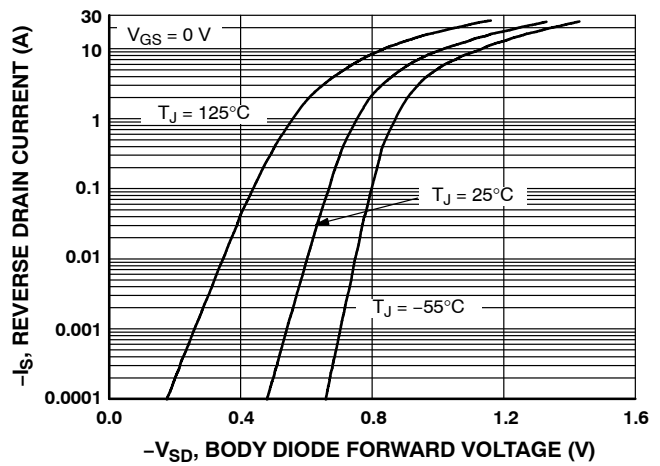


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

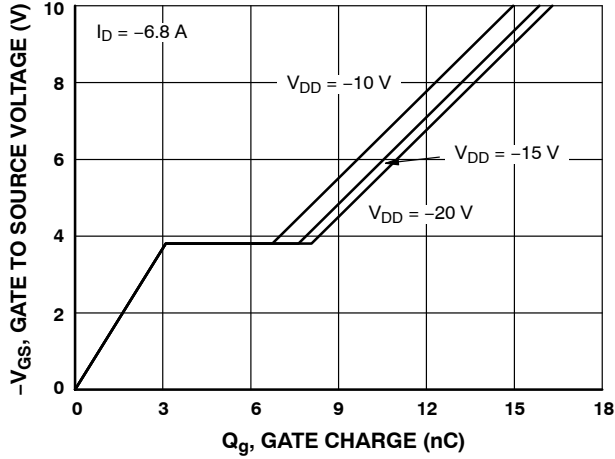


Figure 7. Gate Charge Characteristics

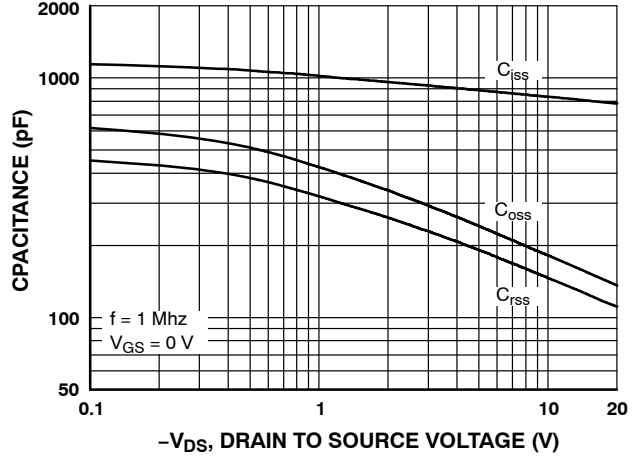


Figure 8. Capacitance vs. Drain to Source Voltage

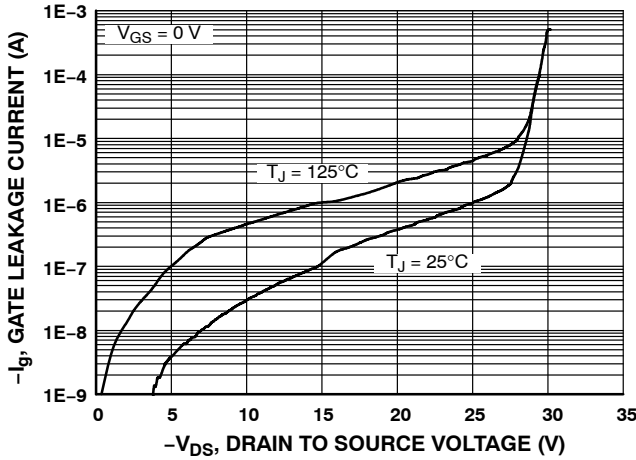


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

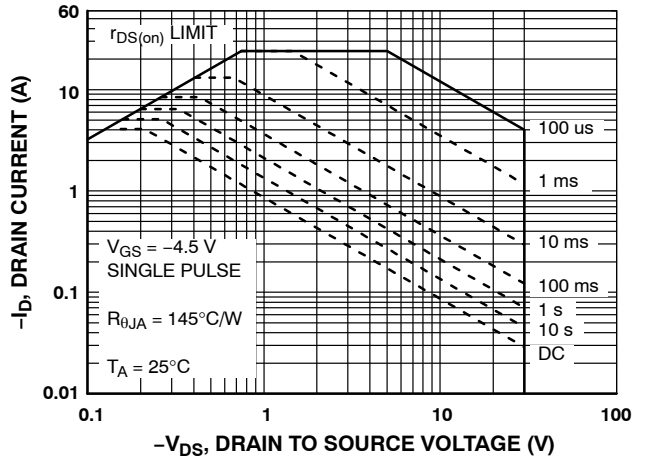


Figure 10. Forward Bias Safe Operating Area

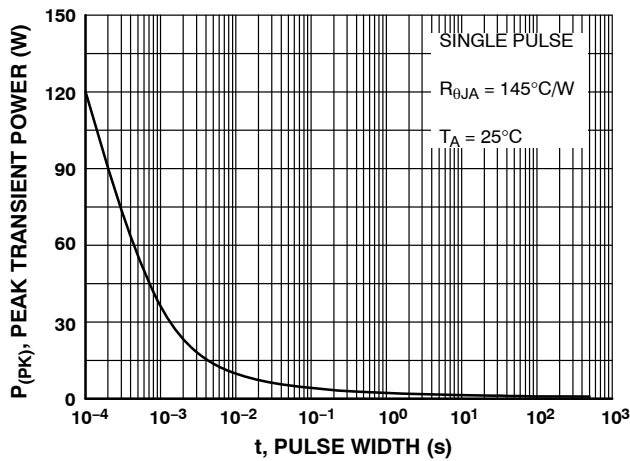


Figure 11. Single Pulse Maximum Power Dissipation

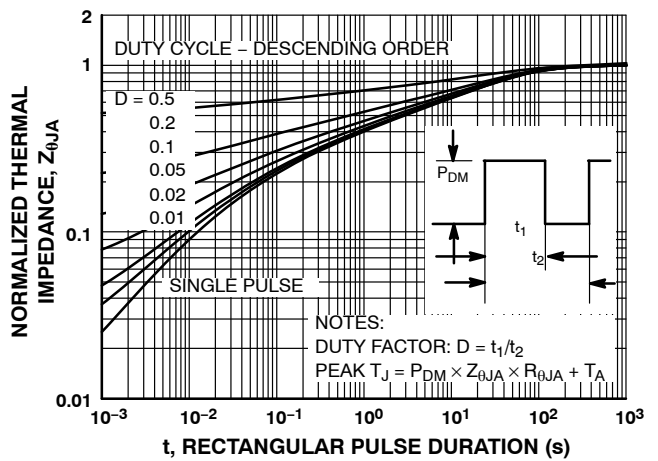


Figure 12. Transient Thermal Response Curve

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MECHANICAL CASE OUTLINE

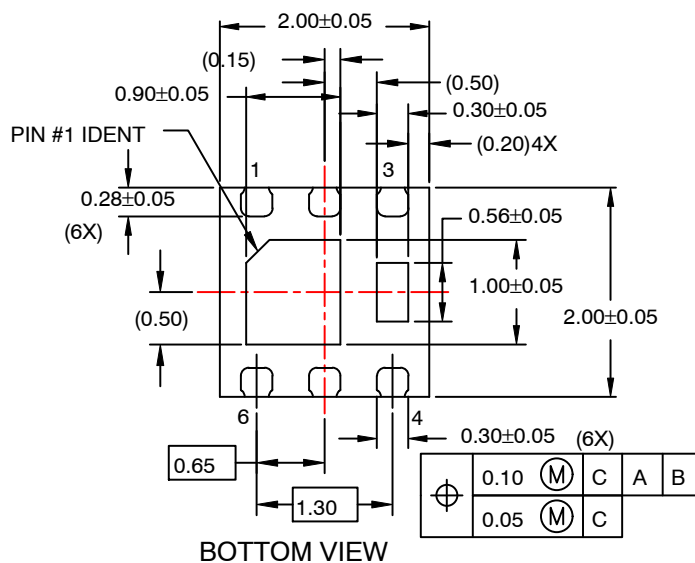
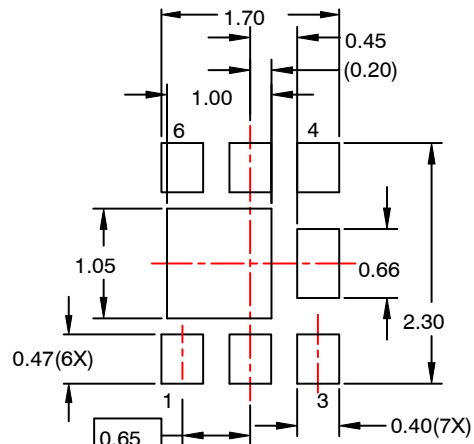
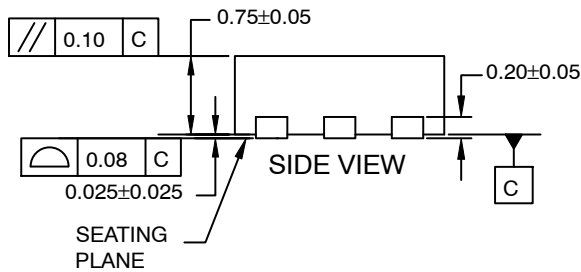
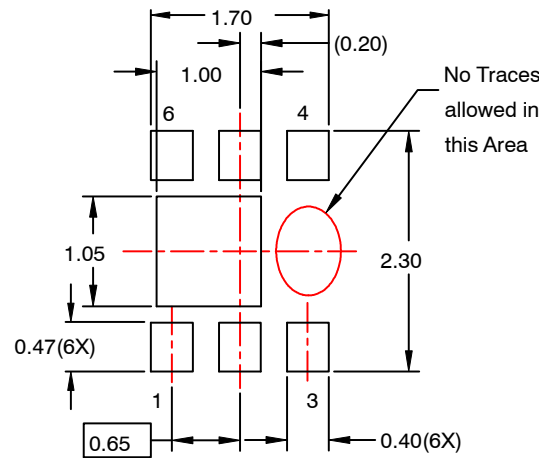
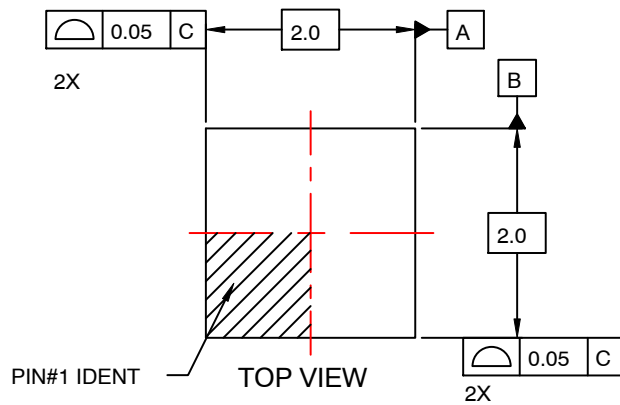
PACKAGE DIMENSIONS

ON Semiconductor®



WDFN6 2x2, 0.65P
CASE 511CZ
ISSUE O

DATE 31 JUL 2016



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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