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S1D13719
Mobile Graphics Engine

Hardware Functional Specification

Document Number: X59A-A-001-01

Status: Revision 1.5

Issue Date: 2012/02/28

Table of Contents

1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13719 Mobile Graphics Engine. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

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1.2 General Description

The S1D13719 is a Mobile Graphics Engine solution designed with support for the digital video revolution in mobile products. The S1D13719 contains an integrated dual port camera interface, hardware JPEG encoder/decoder and can be interfaced to an external MPEG codec. Seamlessly connecting to both direct and indirect CPU interfaces, it provides support for up to two LCD panels. The Mobile Graphics Engine supports all standard TFT panel types and many extended TFT types, eliminating the need for an external timing control IC. The S1D13719, with it’s 512K bytes of embedded SRAM and rich feature set, provides a low cost, low power, single chip solution to meet the demands of embedded markets requiring Digital Video, such as Mobile Communications devices and Palm-size PDAs.

Additionally, products requiring a rotated display can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory, transparent to the software application. The S1D13719 also provides support for “Picture-in-Picture Plus” (a variable size window with overlay functions). Higher performance is provided by the Hardware Acceleration Engine which provides 2D BitBLT functions.

The S1D13719 provides impressive support for cellular and other mobile solutions requiring Digital Video support. However, its impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

2 Features

2.1 Internal Memory

- Embedded 512K byte SRAM used for:
  - Display Buffer
  - JPEG FIFO (up to 512K bytes)
  - JPEG Line Buffer (up to 96K bytes)
- SRAM consists of 5 physical banks (64K/128K/128K/128K/64K bytes)

2.2 Registers

- Registers are memory-mapped
- Asynchronous/synchronous registers (asynchronous registers are accessible during power save mode)
- Special register ports:
  - JPEG FIFO Port (used for JPEG encode/decode/bypass)
  - JPEG Line Buffer Port (used for JPEG encode/decode/bypass)

2.3 Host CPU Interface

- Five Generic Asynchronous CPU interfaces (Mode 80 Type 1, 2, 3 and Mode 68)
- 16-bit serial CPU interface
- 16-bit data bus
  - 16-bit register and FIFO access (when M/R# = 0)
  - 8/16-bit memory access (for direct interface only, when M/R# = 1)
- Hardware configurable at RESET# (using CNF[7:0] pins)
- Indirect / Direct addressing
- Little / Big endian support for parallel interfaces
- Two chip select modes (1CS# or 2CS#) for parallel interfaces
- Memory Rectangular Access for indirect interfaces
- Serial clock polarity mode for serial interface
- Parallel LCD bypass function is not supported when serial interface is selected
  - Bus time-out reset function (interrupt/reset)
  - Cycle time-out function (terminate cycle generation/interrupt)

- Interrupt output
- LCD Bypass Mode (direct control of LCD input by the host CPU)
  - Available for both LCD1/LCD2
  - Supports serial/parallel interface LCD panels
  - Parallel interface LCD panels can be read when LCD panel is bypassed
  - Host CPU control during power save mode

2.4 Display Support

- 9/12/16/18/24-bit RGB Interface Active Matrix TFT displays:
  - Generic TFT interface
  - a-Si TFT interface
  - TFT with u-Wire interface
  - Epson ND-TFD interface
  - Extended TFT interface (Type 2)
- “Direct” support for the Casio TFT LCD (or compatible interfaces)
- “Direct” support for a-TFT Samsung TFT LCD (or compatible interfaces)
- “Direct” support for the Sharp HR-TFT LCD (or compatible interfaces)
  - “Direct” support for Toshiba low power LCDs. Contact your Epson sales representative for details.
- 8/16/18/24-bit Parallel Interface LCD panels with integrated RAM
- 8/9/16/18-bit Serial Interface LCD panels with integrated RAM
- Supports a maximum of 2 panels (LCD1 and LCD2 cannot be refreshed simultaneously)

2.5 Display Modes

- Supports four panel interface modes which each allow two LCDs (LCD1 and LCD2) to be connected to the S1D13719. Only one LCD can be active at a time.
  - Mode 1:
    - LCD1: RGB type panel
    - LCD2: Serial interface panel
  - Mode 2:
    - LCD1: Parallel interface panel
    - LCD2: Serial interface panel
  - Mode 3:
    - LCD1: Parallel interface panel
    - LCD2: Parallel interface panel
  - Mode 4:
    - LCD1: RGB type panel
    - LCD2: Parallel interface panel
- Color Depths:
  - RGB format: 8 bpp/16 bpp/24bpp (can be displayed on Main window or PIP$^+$ window)
  - YUV format: 16bpp (can be displayed only on PIP$^+$ window)
- Look-up table (LUT):
  - LUT1 (for main window): 256 word x 8-bit x 3pcs
  - LUT2 (for PIP$^+$ window): 64 word x 8-bit x 3pcs
  - LUTs can be bypassed

2.6 Display Features

- SwivelView: 90°/180°/270° counter-clockwise hardware rotation of display image
- Mirror Function: Horizontal flip of the display image
- Virtual Display: Displays an image that is larger than the size of the panel using panning and scrolling
- Picture-In-Picture-Plus (PIP$^+$): displays a variable size window overlaid over background image
- Overlay Functions: Average/AND/OR/INV operations using the transparency/key color of PIP$^+$ window
- Overlay can be combined
- Pixel Doubling: Doubles the size of the display image (independent horizontal/vertical)
- Fractional Zoom: Image can be reduced up 1/2x original size or expanded up to 2x original size (Only available for YUV 4:2:2 format)

- Fractional Shrink: Image can be reduced up n/128 (n=1-128) original size (for Capture/View Resizer)
- Video Invert: Data output to the LCD is inverted

2.7 Camera Interface

- Camera interface supports resolution up to a maximum of WUXGA (1920 x 1200) depending on the AC characteristics
- Supports YUV 4:2:2 format
- Supports ITU-R BT.656 format
- 8-bit/16-bit data bus interface
- MPEG Codec interface support on Camera2 interface
- Programmable capture frame
- Timing signal output for strobe control
  - Pulse is programmable and can be output synchronous to the camera input

2.8 JPEG Codec

- Hardware JPEG codec based on the JPEG baseline standard
  - JPEG Encode supports YUV 4:2:2, YUV 4:1:1 formats
  - JPEG Decode supports YUV 4:4:4, YUV 4:2:2, YUV 4:1:1 formats
  - Arithmetic accuracy satisfies the compatibility test of JPEG Part-2 (ISO/IEC10918-2)
  - Software control of image size to maximum of SXGA (1280 x 1024)
  - No gray scale marker support
- JPEG Encode
  - Image data from the camera can be resized and encoded
  - Image data from the LCD can be resized and encoded
  - YUV data from the Host can be encoded
  - Encoded JPEG file is read from the JPEG FIFO
- JPEG Decode
  - Decoded JPEG data is written to the JPEG FIFO
  - JPEG image data can be decoded, resized and then written to the display buffer

2.9 Resizer Functions

- Capture Resizer
  - Resizes image data from the camera
  - Resizes image data for the LCD
  - UV clip function
  - Available trimming and scaling functions (1/2-1/32)
- View Resizer
  - Resizes image data from the camera
  - Resizes JPEG decoded image data
  - UV clip function
  - Available trimming and scaling functions (1/2 - 1/32)
- Pixel Doubling
  - Doubles the image size (i.e. 160x120 can be doubled to 320x240)
  - Independent control of horizontal and vertical
  - Supports both RGB and YUV 4:2:2 formats
- Fractional Capture/View Resizer
  - Camera image data can be reduced from 1x to ½x size in 128 steps
  - JPEG decode data can be reduced from 1x to ½x size in 128 steps
  - Reduction ratios independent of view resize size
- Fractional Zoom
  - YUV 4:2:2 image data can be expanded from 1x to 2x size in 128 steps
  - YUV 4:2:2 image data can be reduced from 1x to 1/2x size in 128 steps
  - Expansion/reduction ratios independent of PIP^+ window size

2.10 Image Data I/O Functions

- YUV data input from camera can be:
  - Resized and written to the display buffer in RGB 5:6:5 format
  - Resized and written to the display buffer in YUV 4:2:2 format
  - Resized, encoded to a JPEG file (YUV 4:2:2, YUV 4:1:1 format), and then output though the JPEG FIFO
  - Resized, converted to YUV 4:2:2 format, and then output through the JPEG FIFO
- JPEG file from the Host CPU can be:

- Input through the JPEG FIFO and decoded by the JPEG codec
- Decoded, resized, and written to the display buffer in RGB 5:6:5 format
- Decoded, resized, and written to the display buffer in YUV 4:2:2 format
- Decoded and output through the JPEG Line Buffer

- LCD Display data (specified rectangular area of display data) can be:
  - Converted to YUV format data
  - Resized, encoded to a JPEG file, and then output through the JPEG FIFO
- YUV data from the Host CPU can be:
  - Input through the JPEG line buffer, resized, and written to the display buffer in RGB 5:6:5 format
  - Input through the JPEG line buffer, resized, and written to the display buffer in YUV 4:2:2 format
  - Input through the JPEG line buffer, encoded, and output through the JPEG FIFO

2.11 Image Data Conversion Functions

- YUV/RGB Converter 1 can:
  - Convert resized image data to RGB 5:6:5 or 8:8:8 format
  - Convert resized image data to YUV 4:2:2 format
  - Use fixed UV data (UV clip)
  - Write a specified rectangular area to the display buffer
  - Set a write prohibit color (RGB)
- YUV/RGB Converter 2 can:
  - Convert YUV 4:2:2 format data in the display buffer to RGB 8:8:8 format
  - Use fixed UV (UV clip)
- RGB/YUV Converter can:
  - Convert RGB format data in a specified area of the display buffer to YUV format
  - Output to LCD panel stop when RGB/YUV converter operates (Parallel/Serial interface LCD panel)
  - Output blank data when RGB/YUV converter operates (RGB interface LCD panel)

2.12 2D BitBLT Accelerator

- Move BitBLT
- Transparent Move BitBLT
- Solid Fill BitBLT
- Read BitBLT (Direct Interface Mode Only)
- Pattern Fill BitBLT

2.13 SD Memory Card Interface

- SD Memory Card interface compatible with the SD Memory Card Physical Layer version 1.0 specification
  - 4-bit or 1-bit interface
  - No security functions
  - Card Detect and Write Protect inputs

2.14 General Purpose I/O Ports

- 22 General Purpose I/O Pins
  - Configurable as inputs or outputs (inputs at reset)
  - Pull-down resistance control for inputs (pull-down resistance is enabled at reset)
  - GPIO pins can be controlled during power save mode

2.15 Clocks

- PLL (requires clock input of 32.768kHz)
  - PLL output range: 48-55MHz
  - PLL output clock period jitter: 3%
  - PLL output stabilization time: 50ms
- PLL bypass mode available

2.16 Power Save Functions

- Software initiated power save mode (internal system clock is stopped)
- Clock supply control for each module
- LCD frame transfer (serial/parallel interface LCD panel)
- LCD auto frame transfer synchronized to camera input (serial/parallel interface LCD panel)
- Pull-down resistance control of general purpose I/O port (default is off for output mode)
- Bypass mode from Host CPU to LCD panel
- The power supply of Camera1 I/F and Camera2 I/F is independent. Only Camera I/F can stop the power supply when the Camera module unused

2.17 Power Supply Voltage

- Logic voltage: 1.95V - 1.65V
- PLL voltage: 1.95V - 1.65V
- Host Interface voltage: 3.25V - 2.75V
- LCD Interface voltage: 3.25V - 2.75V
- Camera Interface voltage: 3.25V - 2.75V
- SD Memory Card Interface voltage: 3.25V - 2.75V

2.18 Package

- PFBGA 180-pin package

3 System Diagrams

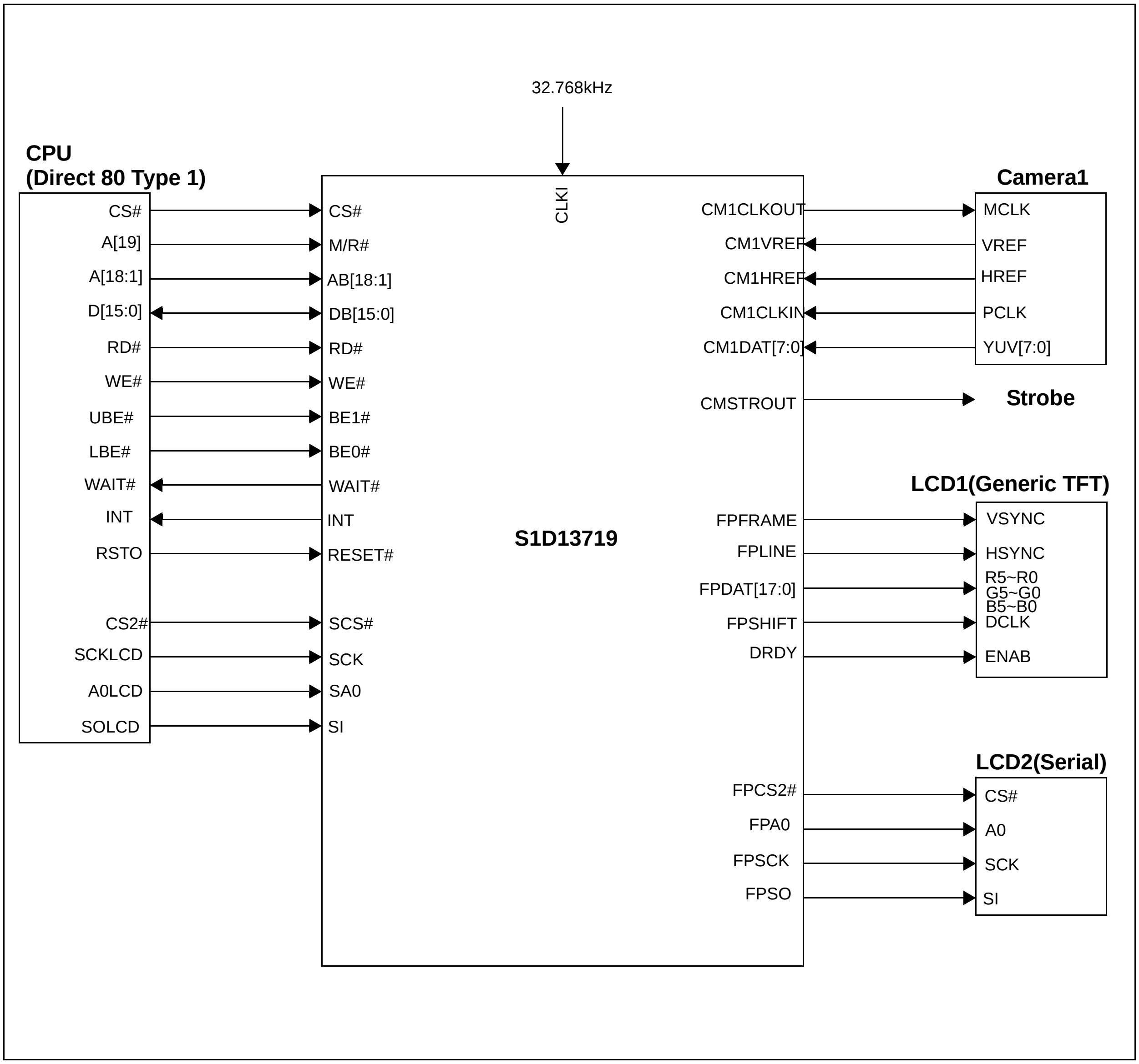

Figure 3-1: Example System Diagram 1

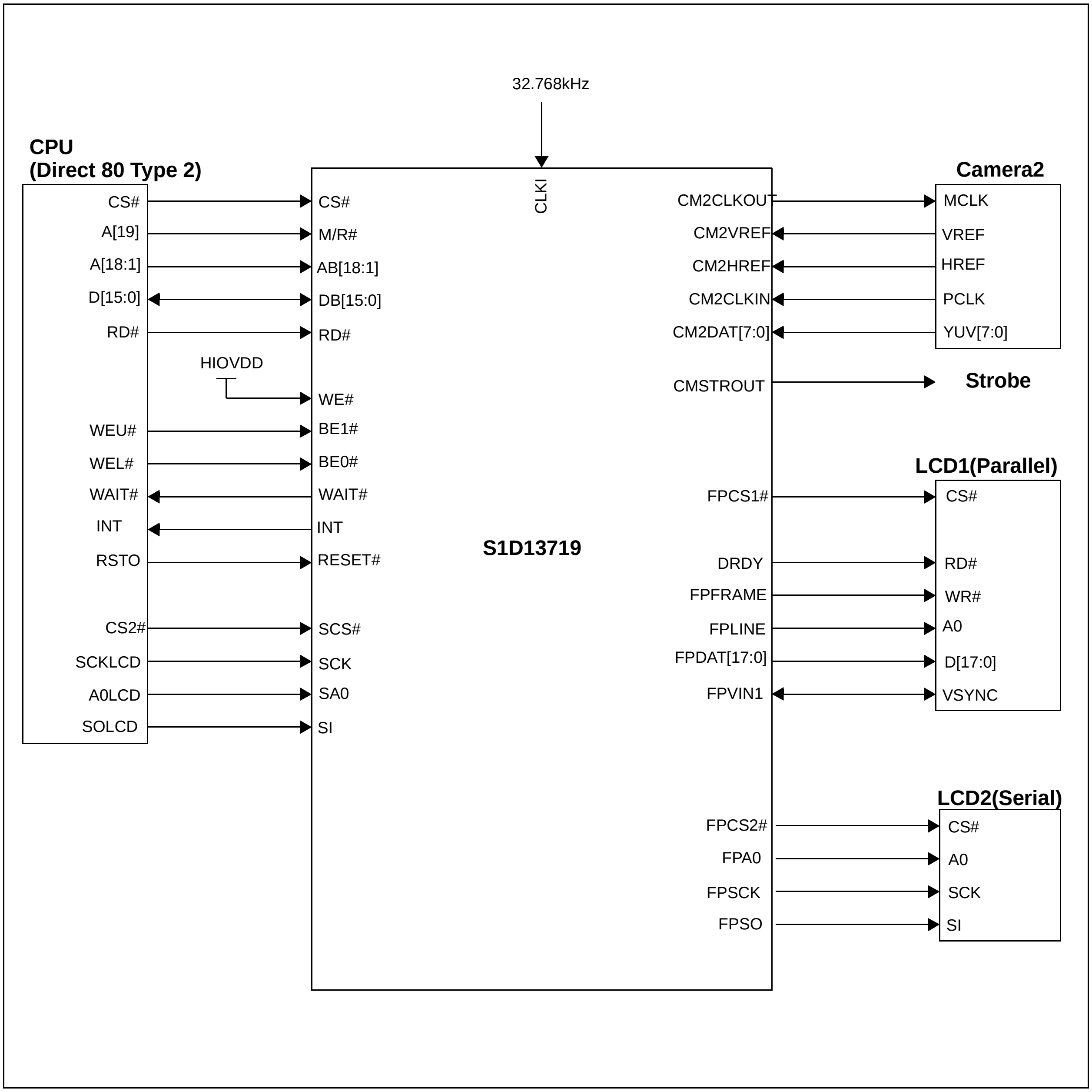

Figure 3-2: Example System Diagram 2

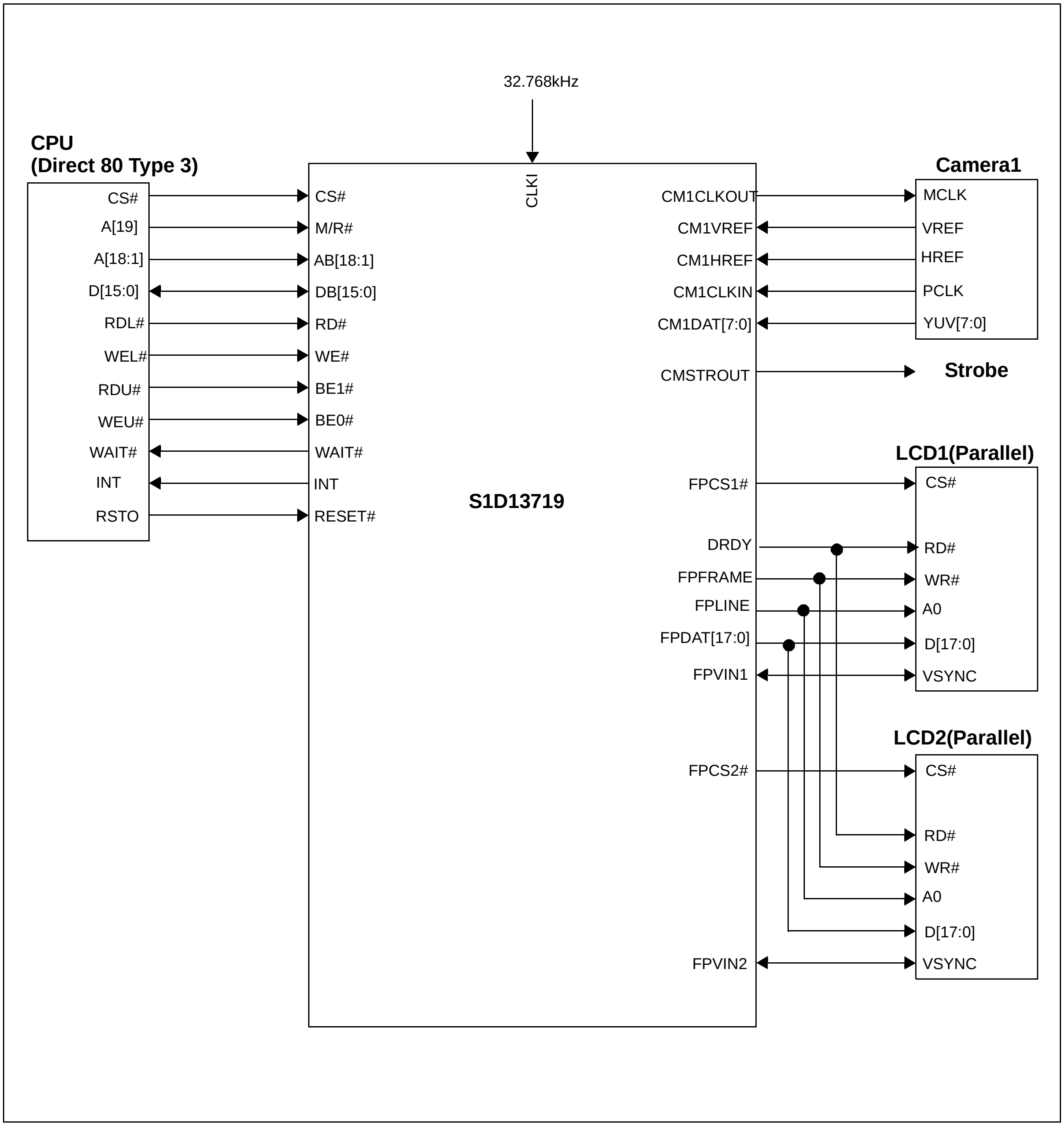

Figure 3-3: Example System Diagram 3

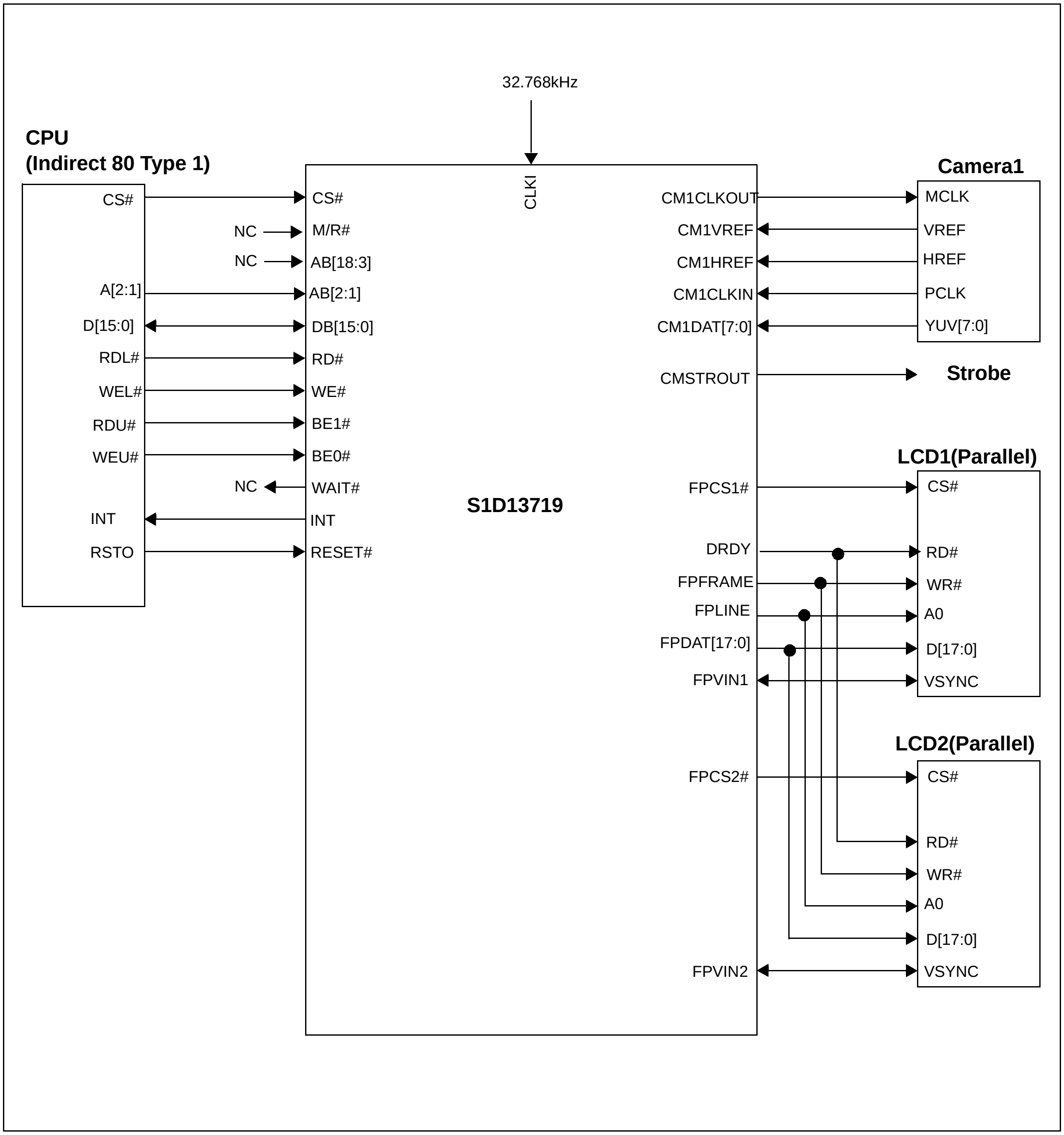

Figure 3-4: Example System Diagram 4

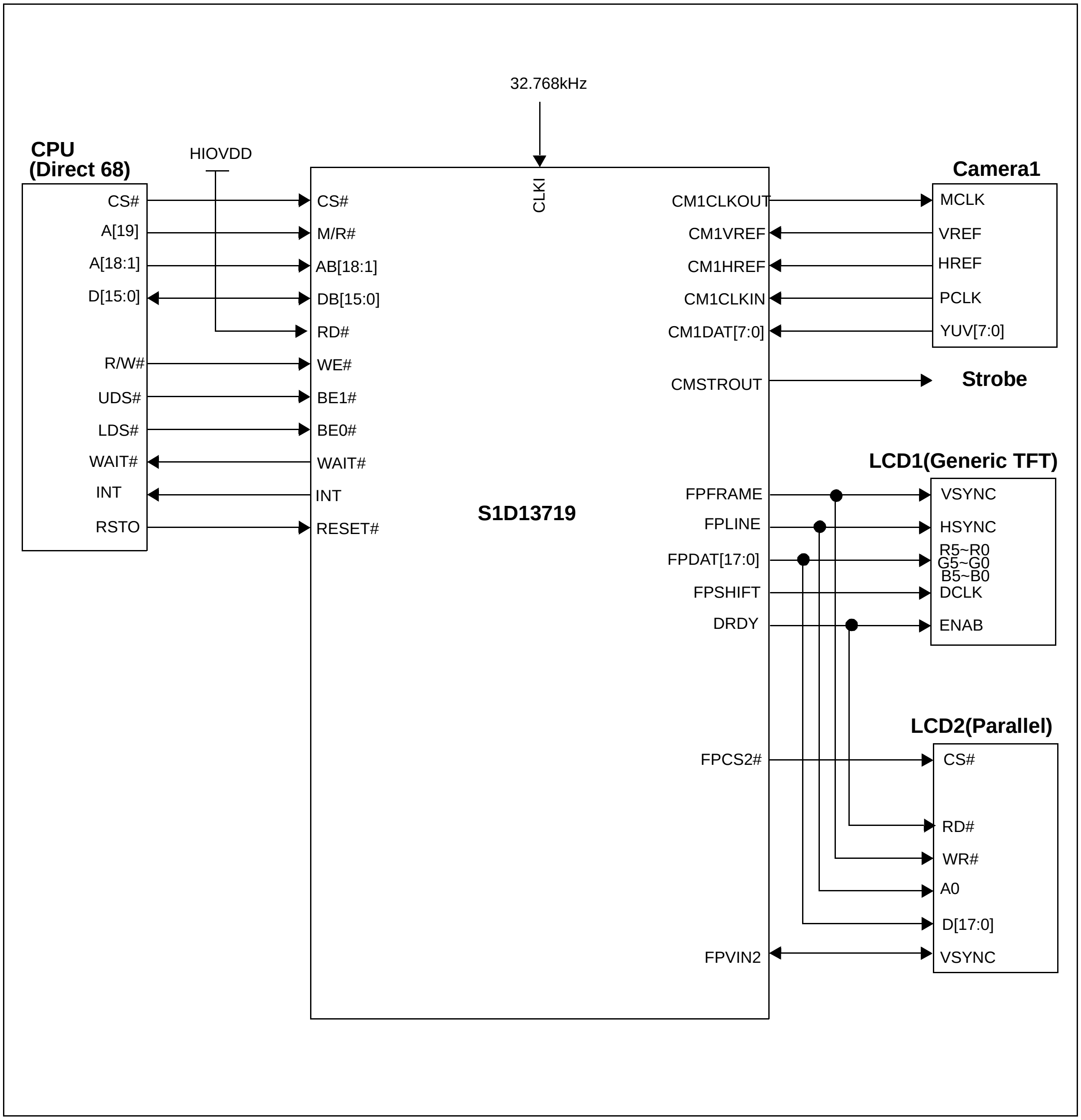

Figure 3-5: Example System Diagram 5

4 Block Diagram

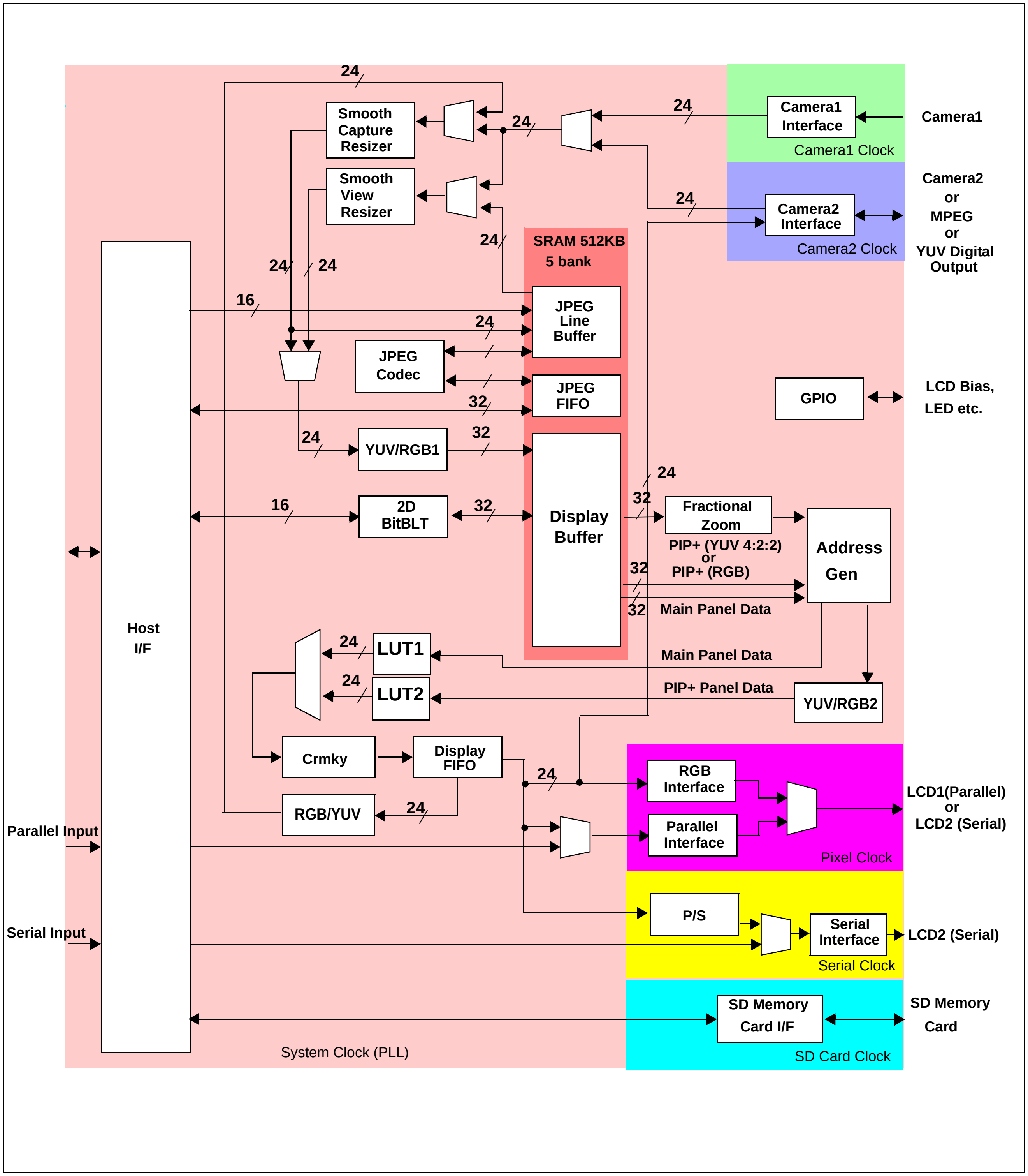

Figure 4-1: S1D13719 Block Diagram

5 Pins

5.1 S1D13719 Pinout Diagram (PFBGA-180)

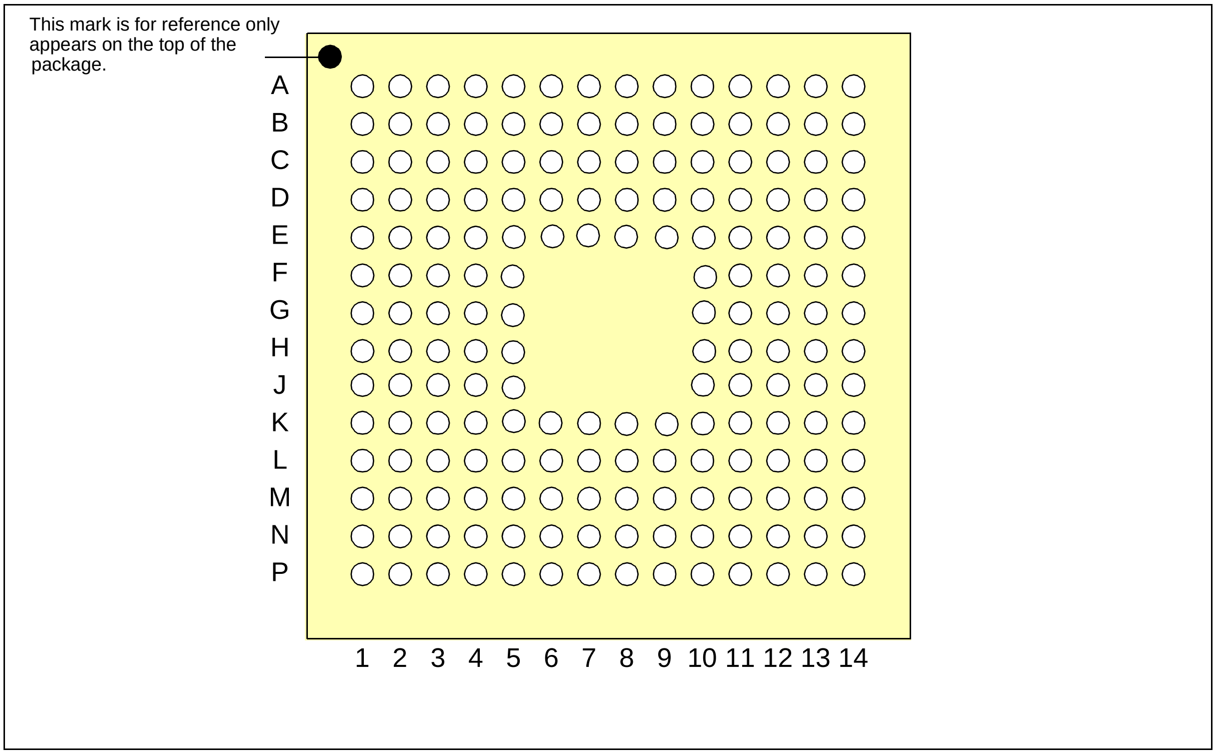

Figure 5-1: S1D13719 PFBGA-180 Pin Mapping (Top View)

Table 5-1: S1D13719 PFBGA-180 Pin Mapping (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	DB[9]	DB[13]	AB[1]	AB[5]	HIOVDD	AB[11]	DB[3]	DB[6]	SCS#	BE1#	CLKI	NC	NC
B	VSS	DB[7]	NC	DB[11]	AB[2]	AB[6]	AB[8]	AB[12]	DB[5]	RD#	BE0#	M/R#	CS#	VSS
C	AB[17]	AB[15]	AB[16]	DB[12]	AB[3]	AB[7]	AB[13]	DB[4]	WAIT#	WE#	NC	PLLVSS	Reserved (GND)	Reserved
D	INT	DB[1]	AB[18]	DB[8]	DB[15]	COREVDD	AB[9]	AB[14]	HIOVDD	SCK	COREVDD	VCP	Reserved (GND)	Reserved
E	RESET#	SA0	DB[2]	DB[0]	DB[10]	AB[4]	AB[10]	COREVDD	COREVDD	VSS	PLLVDD	CM2DAT[1]	CM2DAT[0]	CM2DAT[3]
F	GPIO[19]	GPIO[18]	SI	HIOVDD	DB[14]					CCM2DAT[2]	CM2DAT[4]	NC	CM2DAT[6]	CM2DAT[7]
G	GPIO[15]	GPIO[16]	GPIO[17]	GPIO[11]	SIOVDD					NC	CIO2VDD	CM2DAT[5]	CM2VREF	CM2CLKOUT
H	GPIO[12]	GPIO[13]	GPIO[14]	PIOVDD	CNF[6]					VSS	CM1HREF	CM2HREF	COREVDD	CM2CLKIN
J	NC	VSS	PIOVDD	FPVIN1	CNF[3]					CNF[7]	CIO1VDD	CM1VREF	CM1CLKOUT	NC
K	TESTEN	VSS	FPVIN2	FPDAT[2]	CNF[5]	CNF[0]	FPSCK	COREVDD	CNF[1]	CM1DAT[4]	CM1DAT[0]	CM1DAT[1]	CM1DAT[2]	CM1CLKIN
L	GPIO[0]	FPDAT[8]	FPDAT[0]	SCANEN	CNF[4]	FPDAT[7]	FPDAT[16]	FPDAT[11]	CNF[2]	GPIO[1]	VSS	CM1DAT[5]	CM1DAT[7]	CM1DAT[3]
M	DRDY	FPCS2#	FPDAT[6]	FPDAT[15]	VSS	FPDAT[9]	FPDAT[14]	FPDAT[10]	FPSO	PIOVDD	GPIO[6]	GPIO[5]	GPIO[4]	CM1DAT[6]
N	FPDAT[1]	FPDAT[4]	FPDAT[5]	NC	FPCS1#	FPDAT[17]	NC	FPDAT[13]	NC	GPIO[10]	GPIO[21]	GPIO[8]	GPIO[2]	CMSTROUT
P	NC	FPDAT[3]	FPFRAME	FPLINE	FPSHIFT	PIOVDD	FPA0	FPDAT[12]	VSS	GPIO[9]	GPIO[20]	GPIO[7]	GPIO[3]	NC

5.2 Pin Descriptions

Key:

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
Z	=	High Impedance

Item	Description
IC	LVCMOS[1] input
ICU	LVCMOS input with pull-up resistor (60KΩ@3.0V)
ICD	LVCMOS input with pull-down resistor (60KΩ@3.0V)
IHCS	H System LVCMOS level Schmitt input
ILCS	L System LVCMOS level Schmitt input
OLN35	Low noise output buffer (3.5mA/-3.5mA@3.0V)
OLN35T	Low noise Tri-state output buffer (3.5mA/-3.5mA@3.0V)
BLNC35	Low noise LVCMOS IO buffer (3.5mA/-3.5mA@3.0V)
BLNC35D	Low noise LVCMOS IO buffer (3.5mA/-3.5mA@3.0V) with pull-down resistor (60KΩ@3.0V)
BLNC35DS	Low noise LVCMOS Schmitt IO buffer (3.5mA/-3.5mA@3.0V) with pull-down resistor (60KΩ@3.0V)
ITD	Test mode control input with pull-down resistor (60KΩ@3.0V)
ILTR	Low Voltage Transparent Input
OLTR	Low Voltage Transparent Output
ICDV	LVCMOS input with pull-down resistor (60KΩ@3.0V) and cut-off
BLNCV35D	Low noise LVCMOS IO buffer (3.5mA/-3.5mA@3.0V) with pull-down resistor(60KΩ@3.0V) and cut-off
BLNCV35	Low noise LVCMOS CUT-OFF IO buffer (3.5mA/-3.5mA@3.0V) with cut-off

1. LVCMOS is Low Voltage CMOS (see Section 6, “D.C. Characteristics”).

5.2.1 Host Interface Pins

Many of the host interface pins have different functions depending on the selection of the host bus interface (see configuration of CNF[4:2] pins in Table 5-2: “Summary of Power-On/Reset Options,” on page 39). For a summary of host interface pins, see Table 5-3: “Direct Host Interface Pin Mapping (1 CS# Mode),” on page 407 and Table 5-4: “Indirect Host Interface Pin Mapping (2 CS# Mode),” on page 41.

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
AB[18:3]	I	D3,C1,C3, C2,D8,C7, B8,A7,E7, D7,B7,C6, B6,A5,E6, C5	ICD	HIOVDD	Z	System address bus pins 18-3. • For Direct Host Bus Interfaces, these pins are used for the system address bits 18-3. • For Indirect Host Bus Interfaces, the internal pull-down resistors are enabled and these pins must be left unconnected.
AB[2:1]	I	B5, A4	IC	HIOVDD	Z	System address bus pins 2-1. • For Direct Host Bus Interfaces, these pins are used for the system address bits 2-1. • For Indirect Host Bus Interfaces, these pins are used to index the Indirect Interface Register Ports (see Section 19.3.1, “Indirect Addressing Register Ports”).
DB[15:0]	IO	D5,F5,A3, C4,B4,E5, A2,D4,B2, A9,B9,C8, A8,E3,D2, E4	BLNC35	HIOVDD	Z	System data bus pins 15-0. • For Parallel Host Bus Interfaces, these pins are the System data bus pins 15-0.
CS#	I	B13	IC	HIOVDD	Z	This input pin has multiple functions. • For 1 CS# mode, this pin inputs the chip select signal (CS#). • For 2 CS# mode, this pin inputs the memory chip select signal (CSM#). • When REG[0014h] bit 3 = 1 and the SCS# pin is low, this pin is the LCD parallel bypass chip select.
M/R#	I	B12	ICD	HIOVDD	Z	This input pin has multiple functions. • For 1 CS# mode, this pin selects between the display buffer and register address spaces. When M/R# is set high, the display buffer is accessed and when M/R# is set low the registers are accessed. • For 2 CS# mode, this pin inputs the register chip select (CSR#). Note: For Indirect Host Bus Interfaces, the internal pull-down resistor is enabled and this pin must be left unconnected.
RD#	I	B10	IC	HIOVDD	Z	This input pin has multiple functions. • For Indirect and Direct 68, this pin must be connected to $HIOV_{DD}$. • For Indirect and Direct 80 Type 1 and Type 2, this pin is the read enable signal (RD#). • For Indirect and Direct 80 Type 3, this pin is the DB[7:0] lower byte read enable signal (RDL#).

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
WE#	I	C10	IC	HIOVDD	Z	This input pin has multiple functions. • For Indirect and Direct 68, this pin is the read/write signal (R/W#). • For Indirect and Direct 80 Type 1, this pin is the write enable signal (WE#). • For Indirect and Direct 80 Type 2, this pin must be connected to $HIOV_{DD}$. • For Indirect and Direct 80 Type 3, this pin is the DB[7:0] lower byte write enable signal (WEL#).
BE1#	I	A11	IC	HIOVDD	Z	This input pin has multiple functions. • For Indirect and Direct 68, this pin is the D[15:8] upper data strobe (UDS#). • For Indirect and Direct 80 Type 1, this pin is the D[15:8] upper byte enable signal (UBE#). • For Indirect and Direct 80 Type 2, this pin is the DB[15:8] upper byte write enable signal (WEU#). • For Indirect and Direct 80 Type 3, this pin is the DB[15:8] upper byte read enable signal (RDU#).
BE0#	I	B11	IC	HIOVDD	Z	This input pin has multiple functions. • For Indirect and Direct 68, this pin is the D[7:0] lower data strobe (LDS#). • For Indirect and Direct 80 Type 1, this pin is the D[7:0] lower byte enable signal (LBE#). • For Indirect and Direct 80 Type 2, this pin is the DB[7:0] lower byte write enable signal (WEL#). • For Indirect and Direct 80 Type 3, this pin is the DB[15:8] upper byte write enable signal (WEU#).
WAIT#	O	C9	OLN35T	HIOVDD	Z	During a data transfer, WAIT# is driven active (low) to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. WAIT# is released to a high impedance state after the data transfer is complete. For the indirect host interface, the WAIT# pin is masked.
INT	O	D1	OLN35	HIOVDD	L	Interrupt output. When an internal interrupt occurs, this output pin is driven high. If the Host CPU clears the internal interrupt, this pin is driven low.
RESET#	I	E1	IHCS	HIOVDD	Z	This active low input sets all internal registers to their default state and forces all signals to their inactive states.
SCS#	I	A10	ICU	HIOVDD	1	LCD Serial/Parallel bypass mode chip select input for the Host CPU interface. When Bypass Mode is enabled, the Host CPU can directly control the LCD1 (Parallel) or LCD2 (Serial/Parallel) interface LCD.
SCK	I	D10	ICD	HIOVDD	0	Serial clock input for the Host CPU serial interface. • When Serial Bypass Mode is enabled, the Host CPU can directly control the LCD2 serial interface LCD. • For Parallel Host Bus Interfaces, the internal pull-down resistor is enabled and this pin must be left unconnected.
SA0	I	E2	ICD	HIOVDD	0	Serial/Parallel A0 command input for the Host CPU interface. • When LCD Bypass Mode is enabled, the Host CPU can directly control the LCD2 serial/parallel interface LCD. • For Parallel Host Bus Interfaces, the internal pull-down resistor is enabled and this pin must be left unconnected.

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
SI	I	F3	ICD	HIOVDD	0	Serial data input for the Host CPU serial interface. • When Serial Bypass Mode is enabled, the Host CPU can directly control the LCD2 serial interface LCD. • For Parallel Host Bus Interfaces, the internal pull-down resistor is enabled and this pin must be left unconnected.

5.2.2 LCD Interface Pins

Many of the LCD Interface pins have different functions depending on the configured panel interface mode. See Table 5-5: “LCD Interface Pin Mapping for Mode 1,” on page 42, Table 5-6: “LCD Interface Pin Mapping for Modes 2/3,” on page 43 and Table 5-7: “LCD Interface Pin Mapping for Mode 4,” on page 44 for more details on the pin functions.

- Mode 1 is LCD1: RGB, LCD2: Serial
- Mode 2 is LCD1: Parallel, LCD2: Serial
- Mode 3 is LCD1: Parallel, LCD2: Parallel
- Mode 4 is LCD1: RGB, LCD2: Parallel

For further information on the three panel interface modes, see the bit description for REG[0032h] bits 1-0.

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
FPDAT[17:0]	IO	N6,L7, M4,M7, N8,P8, L8,M8, M6,L2, L6,M3, N3,N2, P2,K4, N1,L3	BLNC35D	PIOVDD	0	These input/output pins are the LCD interface data pins and have multiple functions. • For Mode 1 and Mode 4 RGB interfaces, these pins are the LCD1 RGB data outputs. • For Mode 2 and Mode 3 parallel interfaces, FPDAT[17:0] are the LCD1 parallel interface data outputs. • For Mode 3 and Mode 4 parallel interfaces, FPDAT[17:0] are the LCD2 parallel interface data outputs. • For Parallel Bypass Mode, these pins input/output the Host CPU data. See Table 5-8: “LCD Interface Pin Mapping for Bypass Mode,” on page 45.
FPFRAME	O	P3	OLN35	PIOVDD	0	This output pin has multiple functions. • For Mode 1 and Mode 4 RGB interfaces, this pin is the LCD1 frame pulse output. • For Mode 2 and Mode 3 parallel interfaces, this pin is the LCD1 write command output. • For Mode 3 and Mode 4 parallel interfaces, this pin is the LCD2 write command output. • For Parallel Bypass Mode, this pin outputs the Host CPU XWR signal.

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
FPLINE	O	P4	OLN35	PIOVDD	0	This output pin has multiple functions. • For Mode 1 and Mode 4 RGB interfaces, this pin is the LCD1 line pulse output. • For Mode 2 and Mode 3 parallel interfaces, this pin is the LCD1 command output (A0). • For Mode 3 and Mode 4 parallel interfaces, this pin is the LCD2 command output (A0). • For Parallel Bypass Mode, this pin outputs the Host CPU command signal (A0).
FPSHIFT	O	P5	OLN35	PIOVDD	0	This output pin has multiple functions. • For Mode 1 and Mode 4, this pin is the LCD1 pixel clock output. • For Mode 2 and Mode 3, this pin is not used.
DRDY	O	M1	OLN35	PIOVDD	0	This output pin is the data enable output and has multiple functions. • For Mode 1 and Mode 4, this pin is the LCD1 DRDY output. • For Mode 2 and Mode 3, this pin is not used. • For Parallel Bypass Mode, this pin outputs the XRD signal.
FPCS1#	O	N5	OLN35	PIOVDD	1	This output pin has multiple functions. • For Mode 1 and Mode 4, this pin is the LCD1 serial interface chip select output. • For Mode 2 and Mode 3, this pin is the LCD1 parallel interface chip select output. • For Parallel Bypass Mode, this pin outputs the Host CPU NCS1 signal.
FPCS2#	O	M2	OLN35	PIOVDD	1	This output pin has multiple functions. • For Mode 1 and Mode 2, this pin is the LCD2 serial interface chip select output. When power save is enabled or when serial bypass mode is enabled, this pin outputs the state of the SCS# pin. • For Mode 3 and Mode 4, this pin is the LCD2 parallel interface chip select output. • For Serial or Parallel Bypass Mode, this pin outputs the Host CPU NCS2 signal.
FPSCLK	O	K7	OLN35	PIOVDD	1	This output pin has multiple functions. • For Mode 1, this pin is the LCD1 and LCD2 serial interface clock output. For Mode 4, this pin is the LCD1 serial interface clock output. For LCD2, when power save is enabled or when serial bypass mode is enabled, this pin outputs the state of the SCLK pin. • For Mode 1 and Mode 2, this pin is the LCD2 serial interface clock output. When power save is enabled or when serial bypass mode is enabled, this pin outputs the state of the SCLK pin. • For Mode 3, this pin is not used. • For Serial Bypass Mode, this pin outputs the Host CPU SCK signal.

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
FPA0	O	P7	OLN35	PIOVDD	0	This output pin has multiple functions. • For Mode 1, this pin is the LCD1 and LCD2 serial interface A0 output. For Mode 4, this pin is the LCD1 serial interface A0 output. For LCD2, when power save is enabled or when serial bypass mode is enabled, this pin outputs the state of the SA0 pin. • For Mode 2, this pin is the LCD2 serial interface A0 output. When power save is enabled or when serial bypass mode is enabled, this pin outputs the state of the SA0 pin. • For Mode 3, this pin is not used. • For Serial Bypass Mode, this pin outputs the Host CPU A0 signal.
FPSO	O	M9	OLN35	PIOVDD	0	This output pin has multiple functions. • For Mode 1, this pin is the LCD1 and LCD2 serial interface data output. For Mode 4, this pin is the LCD1 serial interface data output. For LCD2, when power save is enabled or when serial bypass mode is enabled, this pin outputs the state of the SI pin. • For Mode 2, this pin is the LCD2 serial interface data output. When power save is enabled or when serial bypass mode is enabled, this pin outputs the state of the SI pin. • For Mode 3, this pin is not used. • For Serial Bypass Mode, this pin outputs the Host CPU SI signal.
FPVIN1	IO	J4	BLNC35D	PIOVDD	0	This input/output pin has multiple functions. • For Modes 2 and 3, this pin is the parallel interface LCD1 vertical sync input from the LCD panel.
FPVIN2	IO	K3	BLNC35D	PIOVDD	0	This input/output pin has multiple functions. • For Mode 2, this pin is the LCD2 serial interface vertical sync input from the LCD panel. • For Mode 3, this pin is the LCD2 parallel interface vertical sync input from the LCD panel.

5.2.3 Camera Interface Pins

Many of the pins for the 2 Camera Interfaces have different functions depending on the settings for these interfaces. See Table 5-9: “Camera1 Interface Pin Mapping,” on page 46 for details on the connections for the Camera1 Interface. See Table 5-10: “Camera2 Interface Pin Mapping,” on page 46 for details on the connections for the Camera2 Interface.

The Camera1 Interface supports a Type 1 8/16-bit bus Camera interface.

Note
The output functions of the Camera1 Interface pins (CM1DAT[7:0], CM1VREF, CM1HREF, CM1CLKIN) are for testing only.

The Camera2 Interface supports a Type 1 8-bit bus Camera interface. It also supports input from an external MPEG codec.

Note
The output functions of the Camera2 Interface pins (CM2DAT[7:0], CM2CLKIN) are for testing only.

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
CM1DAT[7:0]	I	L13,M14, L12,K10, L14,K13, K12,K11	ICDV	CIO1VDD	0	These input/output pins have multiple functions. • For the Camera1 8-bit interface (REG[0102h] bit 6 = 0), these pins are the 8-bit data input (CAMDAT[7:0]). • For the Camera1 16-bit interface (REG[0102h] bit 6 = 1), these pins are the 8-bit luminance (Y) or chrominance (Cb/Cr) data input (CAMDAT[7:0]). The data type must be set using REG[0102h] bits 4-3.
CM1VREF	I	J12	ICDV	CIO1VDD	0	For the Camera1 interface, this pin is the vertical sync input (VREF).
CM1HREF	I	H11	ICDV	CIO1VDD	0	For the Camera1 interface, this pin is the horizontal sync input (HREF).
CM1CLKOUT	O	J13	OLN35	CIO1VDD	L	For the Camera1 interface, this pin is the Master clock output (CAMMCLK).
CM1CLKIN	I	K14	ICDV	CIO1VDD	0	For the Camera1 interface, this pin is the camera pixel clock input (CAMPCLK).
CM2DAT[7:0]	IO	F14,F13, G12,F11, E14,F10, E12,E13	BLNCV35D	CIO2VDD	0	These input/output pins have multiple functions. • For the Camera1 16-bit interface (REG[0102h] bit 6 = 1), these pins are the 8-bit chrominance (Cb/Cr) or luminance (Y) data input (CAMDAT[15:8]). The data type must be set using REG[0102h] bits 4-3. • For the Camera2 interface, these pins are the 8-bit data input (CAMDAT[7:0]). • For the Camera2 MPEG codec interface, these pins are the 8-bit data input (PXL[7:0]).

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
CM2VREF	IO	G13	BLNCV35D	CIO2VDD	0	This input/output pin has multiple functions. • For the Camera2 interface, this pin is the vertical sync input (VREF). • For the Camera2 MPEG codec interface, this pin is the vertical sync output (nDISPVSYNC).
CM2HREF	IO	H12	BLNCV35D	CIO2VDD	0	This input/output pin has multiple functions. • For the Camera2 interface, this pin is the horizontal sync input (HREF). • For the Camera2 MPEG codec interface, this pin is the horizontal sync output (nDISPHSYNC).
CM2CLKOUT	O	G14	OLN35	CIO2VDD	L	This output pin has multiple functions. • For the Camera2 interface, this pin is the master clock output (CAMMCLK). • For the Camera2 MPEG codec interface, this pin is the clock output (DISPCLK).
CM2CLKIN	IO	H14	BLNCV35D	CIO2VDD	0	This input/output pin has multiple functions. • For the Camera2 interface, this pin is the camera pixel clock input (CAMPCLK). • For the Camera2 MPEG codec interface, this pin is the blanking input (DISPBLK).
CMSTROUT	O	N14	OLN35T	PIOVDD	Z	Strobe signal form MGE Register Trig

5.2.4 SD Card Interface Pins

GPIO[19:11] are used as SD Card Interface when REG[0004h] bit 7=1.

SIOVDD should be supplied to these pins when the SD Card interface is used. PIOVDD should be supplied to these pins when the SD card interface is not used. See Miscellaneous Pins on page 37, GPIO[19:11].

Note
Disable the pull-down resistance of the GPIOs (REG[0308h] bits 19-11) before using the SD Memory Card Interface.

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
SDDAT[3:0]	IO	H3,H2, H1,G4	BLNC35D	SIOVDD	0	This input/output pin has multiple functions. • For SD Card, these pins are used for data IO. • For MMC, the SDDAT0 pin is used for data IO. SDDAT[3:1] must be left unconnected. • When SD Card/MMC is not used, these pins are GPIO[14:12]. See Miscellaneous Pins on page 37, GPIO[14:11].
SDCMD	IO	G1	BLNC35D	SIOVDD	-	This input/output pin has multiple functions. • For SD Card, this pin is the command IO. • For MMC, this pin is the command IO (CMD). • When SD Card is not used, this pin is GPIO15. See Miscellaneous Pins on page 37, GPIO15.
SDCLK	IO	G2	BLNC35D	SIOVDD	-	This input/output pin has multiple functions. • For SD Card, this pin is the clock output. • For MMC, this pin is the clock output (CLK). • When SD Card/MMC is not used, this pin is GPIO16. See Miscellaneous Pins on page 37, GPIO16.
SDCD#	IO	G3	BLNC35D	SIOVDD	-	This input pin has multiple functions. • For SD Card, this pin is the card detect. • For MMC, this pin is the card detect (CD#). • When SD Card/MMC is not used, this pin is GPIO17. See Miscellaneous Pins on page 37, GPIO17.
SDWP	IO	F2	BLNC35D	SIOVDD	-	This input pin has multiple functions. • For SD Card, this pin is the write protection input. • For MMC, this pin is the write protection input (WP). • When SD Card/MMC is not used, this pin is GPIO18. See Miscellaneous Pins on page 37, GPIO18.
SDGPO	IO	F1	BLNC35D	SIOVDD	-	This output pin has multiple functions. • For SD Card, this pin is the general purpose output port. • For MMC, this pin is the general purpose output port (GPO). • When SD Card/MMC is not used, this pin is GPIO19. See Miscellaneous Pins on page 37, GPIO19.

5.2.5 Clock Input Pins

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
CLKI	I	A12	ILCS	HIOVDD	Z	This input pin has multiple functions. • When the internal PLL is used, this pin is the input reference clock for the internal PLL (32.768KHz). • When the PLL is bypassed, this pin is the digital clock input for the system clock (SYSCLK).
Reserved	—	D13	—	—	—	Reserved. This pin must be connected to GND.
Reserved	—	D14	—	—	—	Reserved. This pin must be left unconnected.
Reserved	—	C13	—	—	—	Reserved. This pin must be connected to GND.
Reserved	—	C14	—	—	—	Reserved. This pin must be left unconnected.

5.2.6 Miscellaneous Pins

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
CNF[7:0]	I	J10,H5, K5,L5,J5, L9,K9,K6	IC	PIOVDD	Z	These inputs are used for configuring the S1D13719 and must be connected to either PIOVDD or VSS. The states of these pins are latched at RESET#. For more information, see Table 5-2: “Summary of Power-On/Reset Options,” on page 39.
GPIO[10:0]	IO	N10,P10, N12,P12, M11, M12, M13,P13, N13,L10, L1	BLNC35D	PIOVDD	see note	These pins are general purpose input/output pins. Their default configuration (input or output) is controlled using CNF1. • For various LCD panel settings, GPIO[10:0] are used to output LCD interface signals. See Table 5-5: “LCD Interface Pin Mapping for Mode 1,” on page 42 and Table 5-6: “LCD Interface Pin Mapping for Modes 2/3,” on page 43 for which GPIO pins are available for use as GPIOs for a given LCD panel setting.
GPIO[19:11]	IO	F1,F2, G3,G2, G1,H3, H2,H1, G4	BLNC35D	PIOVDD	see note	These pins are general purpose input/output pins. Their default configuration (input or output) is controlled using CNF1. • For various LCD panel settings (when REG[0004h] bit 7=0), GPIO[13:11] are used to output LCD interface signals. See Table 5-5: “LCD Interface Pin Mapping for Mode 1,” on page 42 and Table 5-6: “LCD Interface Pin Mapping for Modes 2/3,” on page 43 for which GPIO pins are available for use as GPIOs for a given LCD panel setting. • For SD Card/MMC interface (when REG[0004h] bit 7=1), GPIO[19:11] pins are used as the SD/MMC card interface pins. SIOVDD should be used for the signals when the SD Card/MMC interface is used. PIOVDD should be used for the signals when the SD Card/MMC interface is not used. • In serial bypass mode or in power-save mode (when REG[0004h] bit 7=0), GPIO19 inputs the Host CPU serial interface chip select signal (CMCSI#).

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET# State	Description
GPIO[21:20]	IO	N11, P11	BLNC35D	PIOVDD	see note	These pins are general purpose input/output pins. Their default configuration (input or output) is controlled using CNF1. • GPIO20 outputs the strobe control signal when the strobe function is enabled (REG[0124h] bit 3 = 1).
TESTEN	I	K1	ITD	PIOVDD	0	Test Enable input used for production test only. This pin should be left unconnected for normal operation.
SCANEN	I	L4	ICD	PIOVDD	0	Scan Enable input used for production test only. This pin should be left unconnected for normal operation.
VCP	IO	D12	OLTR	COREVDD	Z	PLL output monitor pin used for production test only. This pin should be left unconnected for normal operation.

Note

When CNF1 = 0 (GPIO pins are outputs), the reset state of GPIO[21:3, 0] is 0.
When CNF1 = 1 (GPIO pins default to inputs), the reset state of GPIO[21:3, 0] is 0.
When REG[0056h] bit 13 = 1, or REG[005Eh] bit 13 = 1, the reset state of GPIO[2:1] is always Hi-Z.
When REG[0056h] bit 13 = 0 and REG[005Eh] bit 13 = 0, the reset state of GPIO[2:1] depends on CNF1 as above.

5.2.7 Power and Ground Pins

Pin Name	Type	PFBGA Pin#	Power	RESET# State	Description
HIOVDD	P	F4,A6,D9	P	—	IO power supply for the host interface
PIOVDD	P	J3,H4, P6,M10	P	—	IO power supply for the panel interface
CIO1VDD	P	J11	P	—	IO power supply for the camera1 interface
CIO2VDD	P	G11	P	—	IO power supply for the camera2 interface
SIOVDD	P	G5	P	—	IO power supply for the SD-Card I/F interface
COREVDD	P	D6,D11, E8,E9, K8,H13	P	—	Core power supply
VSS	P	B1,J2, E10,K2, M5,P9, H10,L11, B14	P	—	GND for HIOVDD, PIOVDD, CIO1VDD, CIO2VDD, SIOVDD, and COREVDD
PLLVDD	P	E11	P	—	PLL power supply
PLLVSS	P	C12	P	—	GND for PLLVDD

5.3 Summary of Configuration Options

These pins are used for configuration of the chip and must be connected directly to PIOVDD or VSS. The state of CNF[7:0] are latched on the rising edge of RESET#. Changing state at any other time has no effect.

Table 5-2: Summary of Power-On/Reset Options

Configuration Input	Power-On/Reset State	
	1 (connected to PIOVDD)	**0 (connected to VSS)**
CNF7	Camera2 power supply OFF	Camera2 power supply ON
CNF6	Parallel 2 CS# mode	Parallel 1 CS# mode
CNF5	Big Endian	Little Endian
CNF[4:2]	Selects host bus interface as follows: **CNF4 CNF3 CNF2 Host Bus** 0 0 0 Direct 80 Type 2 0 0 1 Direct 80 Type 3 0 1 0 Indirect 80 Type 2 0 1 1 Indirect 80 Type 3 1 0 0 Direct 80 Type 1 1 0 1 Direct 68 1 1 0 Indirect 80 Type 1 1 1 1 Indirect 68	
CNF1 (see Note)	All GPIO pins (GPIO[21:0]) are configured as inputs. Note: When CNF1=1 at RESET#, REG[0300h]-REG[0302h] can be used to change individual GPIO pins between inputs/outputs.	All GPIO pins (GPIO[21:0] are configured as outputs. Note: When CNF1=0 at RESET#, REG[0300h]-REG[0302h] are ignored and the GPIO pins are always outputs.
CNF0	Camera1 power supply OFF	Camera1 power supply ON

Note

When GPIO pins are used for the SD Card Interface (REG[0004h] bit 7=1) CNF1 has no effect on these pins. See Figure 5.8 “SD Memory Card Interface Pin Mapping,” on page 47 for the GPIO pins used.
When GPIO pins are used for the panel interface CNF1 has no effect on these pins. See Figure 5.5 “LCD Interface Pin Mapping,” on page 42 for the GPIO pins used.

5.4 Host Interface Pin Mapping

The host interface is selected using CNF[4:2]. For information on selecting the following interfaces, see Table 5-2: “Summary of Power-On/Reset Options,” on page 39.

Table 5-3: Direct Host Interface Pin Mapping (1 CS# Mode)

Pin Name	Direct 68	Direct 80 Type 1	Direct 80 Type 2	Direct 80 Type 3
AB[18:3]	A[18:3]	A[18:3]	A[18:3]	A[18:3]
AB[2:1]	AB[2:1]	AB[2:1]	AB[2:1]	AB[2:1]
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]
CS#	CS#	CS#	CS#	CS#
M/R#	Address (1CS#), chip/selection (2CS#)			
RD#	HIOVDD	RD#	RD#	RDL#
WR#	R/W#	WE#	HIOVDD	WEL#
BE1#	UDS#	UBE#	WEU#	RDU#
BE0#	LDS#	LBE#	WEL#	WEU#
WAIT#	WAIT#			
INT	Interrupt Signal			
RESET#	RESET#			
SCS#	-	-	-	-
SCLK	-	-	-	-
SA0	-	-	-	-
SI	-	-	-	-

Table 5-4: Indirect Host Interface Pin Mapping (2 CS# Mode)

Pin Name	Indirect 68	Indirect 80 Type 1	Indirect 80 Type 2	Indirect 80 Type 3
AB[18:3]	Unconnected			
AB[2:1]	AB[2:1]	AB[2:1]	AB[2:1]	AB[2:1]
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]
CS#	CS#	CS#	CS#	CS#
M/R#	Connected to VSS			
RD#	HIOVDD	RD#	RD#	RDL#
WR#	R/W#	WE#	HIOVDD	WEL#
BE1#	UDS#	UBE#	WEU#	RDU#
BE0#	LDS#	LBE#	WEL#	WEU#
WAIT#	Unconnected			
INT	Interrupt Signal			
RESET#	RESET#			
SCS#	-	-	-	-
SCLK	-	-	-	-
SA0	-	-	-	-
SI	-	-	-	-

5.5 LCD Interface Pin Mapping

Table 5-5: LCD Interface Pin Mapping for Mode 1

Pin Name	Mode 1									
	LCD1									LCD2
	Generic TFT	ND-TFD	a-Si TFT	TFT with uWIRE I/F	Sharp HR-TFT	Casio TFT	Samsung α-TFT	Type 2 TFT	SPI	Serial I/F
FPFRAME	VSYNC	VSYNC	VSYNC	VSYNC	SPS	GSRT	STV	STV		
FPLINE	HSYNC	HSYNC	HSYNC	HSYNC	LP	GPCK	STH	STB		
FPSHIFT	DCK	DCK	DCLK	CLK	DCLK	CLK	HCLK	CLK		
DRDY	ENAB	ENAB	ENAB	ENAB	no connect	no connect	no connect	INV		
FPDAT0	R7	R7	R7	R7	R7	R7	R5	R7		
FPDAT1	R6	R6	R6	R6	R6	R6	R4	R6		
FPDAT2	R5	R5	R5	R5	R5	R5	R3	R5		
FPDAT3	G7	G7	G7	G7	G7	G7	G5	G7		
FPDAT4	G6	G6	G6	G6	G6	G6	G4	G6		
FPDAT5	G5	G5	G5	G5	G5	G5	G3	G5		
FPDAT6	B7	B7	B7	B7	B7	B7	B5	B7		
FPDAT7	B6	B6	B6	B6	B6	B6	B4	B6		
FPDAT8	B5	B5	B5	B5	B5	B5	B3	B5		
FPDAT9	R4	R4	R4	R4	R4	R4	R2	R4		
FPDAT10	R3	R3	R3	R3	R3	R3	R1	R3		
FPDAT11	R2	R2	R2	R2	R2	R2	R0	R2		
FPDAT12	G4	G4	G4	G4	G4	G4	G2	G4		
FPDAT13	G3	G3	G3	G3	G3	G3	G1	G3		
FPDAT14	G2	G2	G2	G2	G2	G2	G0	G2		
FPDAT15	B4	B4	B4	B4	B4	B4	B2	B4		
FPDAT16	B3	B3	B3	B3	B3	B3	B1	B3		
FPDAT17	B2	B2	B2	B2	B2	B2	B0	B2		
FPCS1#		XCS	SSTB	LCDCS	SPR				CS	
FPCS2#										NCS2
FPSCLK		SCK	SCLK	SCLK					SCL	SCK
FPA0		A0								A0
FPSO		SI	SDATA	SDO					SDI	SI
FPVIN1									SDO(FPSI)	
FPVIN2										VIN2
GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	PS	POL	CKV	VCLK	GPIO0	GPIO0
GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	CLS	GRES	LD	AP	GPIO1	GPIO1
GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	REV	FRP	INV	POL	GPIO2	GPIO2
GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	SPL	STH	VCOM	STH	GPIO3	GPIO3
GPIO4	R1	R1	R1	R1	R1	R1	GPIO4	R1	GPIO4	GPIO4
GPIO5	R0	R0	R0	R0	R0	R0	GPIO5	R0	GPIO5	GPIO5
GPIO6	G1	G1	G1	G1	G1	G1	GPIO6	G1	GPIO6	GPIO6
GPIO7	G0	G0	G0	G0	G0	G0	GPIO7	G0	GPIO7	GPIO7
GPIO8	B1	B1	B1	B1	B1	B1	GPIO8	B1	GPIO8	GPIO8
GPIO9	B0	B0	B0	B0	B0	B0	GPIO9	B0	GPIO9	GPIO9
GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10
GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11
GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12
GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13
GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21

Table 5-6: LCD Interface Pin Mapping for Modes 2/3

Pin Name	Mode 2		Mode 3	
	LCD1	**LCD2**	**LCD1**	**LCD2**
	Parallel I/F	**Serial I/F**	**Parallel I/F**	**Parallel I/F**
FPFRAME	XWR		XWR	XWR
FPLINE	A0		A0	A0
FPSHIFT				
DRDY				
FPDAT0	D0		D0	D0
FPDAT1	D1		D1	D1
FPDAT2	D2		D2	D2
FPDAT3	D3		D3	D3
FPDAT4	D4		D4	D4
FPDAT5	D5		D5	D5
FPDAT6	D6		D6	D6
FPDAT7	D7		D7	D7
FPDAT8	D8		D8	D8
FPDAT9	D9		D9	D9
FPDAT10	D10		D10	D10
FPDAT11	D11		D11	D11
FPDAT12	D12		D12	D12
FPDAT13	D13		D13	D13
FPDAT14	D14		D14	D14
FPDAT15	D15		D15	D15
FPDAT16	D16		D16	D16
FPDAT17	D17		D17	D17
FPCS1#	NCS1		NCS1	
FPCS2#		NCS2		NCS2
FPSCLK		SCK		
FPA0		A0		
FPSO		SI		
FPVIN1	VIN1/VOUT1		VIN1/VOUT1	
FPVIN2		VIN2		VIN2/VOUT2
GPIO0	GPIO0	GPIO0	GPIO0	GPIO0
GPIO1	GPIO1	GPIO1	GPIO1	GPIO1
GPIO2	GPIO2	GPIO2	GPIO2	GPIO2
GPIO3	GPIO3	GPIO3	GPIO3	GPIO3
GPIO4	D18	GPIO4	D18	D18
GPIO5	D19	GPIO5	D19	D19
GPIO6	D20	GPIO6	D20	D20
GPIO7	D21	GPIO7	D21	D21
GPIO8	D22	GPIO8	D22	D22
GPIO9	D23	GPIO9	D23	D23
GPIO10	GPIO10	GPIO10	GPIO10	GPIO10
GPIO11	GPIO11	GPIO11	GPIO11	GPIO11
GPIO12	GPIO12	GPIO12	GPIO12	GPIO12
GPIO13	GPIO13	GPIO13	GPIO13	GPIO13
GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21

Table 5-7: LCD Interface Pin Mapping for Mode 4

Pin Name	Mode 4									
	LCD1									LCD2
	Generic TFT	ND-TFD	a-Si TFT	TFT with uWIRE I/F	Sharp HRTFT	Casio TFT	Samsung α-TFT	Type 2 TFT	SPI	Parallel I/F
FPFRAME	VSYNC	VSYNC	VSYNC	VSYNC	SPS	GSRT	STV	STV		XWR
FPLINE	HSYNC	HSYNC	HSYNC	HSYNC	LP	GPCK	STH	STB		A0
FPSHIFT	DCK	DCK	DCLK	CLK	DCLK	CLK	HCLK	CLK		
DRDY	ENAB	ENAB	ENAB	ENAB	no connect	no connect	no connect	INV		
FPDAT0	R7	R7	R7	R7	R7	R7	R5	R7		D0
FPDAT1	R6	R6	R6	R6	R6	R6	R4	R6		D1
FPDAT2	R5	R5	R5	R5	R5	R5	R3	R5		D2
FPDAT3	G7	G7	G7	G7	G7	G7	G5	G7		D3
FPDAT4	G6	G6	G6	G6	G6	G6	G4	G6		D4
FPDAT5	G5	G5	G5	G5	G5	G5	G3	G5		D5
FPDAT6	B7	B7	B7	B7	B7	B7	B5	B7		D6
FPDAT7	B6	B6	B6	B6	B6	B6	B4	B6		D7
FPDAT8	B5	B5	B5	B5	B5	B5	B3	B5		D8[1]
FPDAT9	R4	R4	R4	R4	R4	R4	R2	R4		D9[1]
FPDAT10	R3	R3	R3	R3	R3	R3	R1	R3		D10[1]
FPDAT11	R2	R2	R2	R2	R2	R2	R0	R2		D11[1]
FPDAT12	G4	G4	G4	G4	G4	G4	G2	G4		D12[1]
FPDAT13	G3	G3	G3	G3	G3	G3	G1	G3		D13[1]
FPDAT14	G2	G2	G2	G2	G2	G2	G0	G2		D14[1]
FPDAT15	B4	B4	B4	B4	B4	B4	B2	B4		D15[1]
FPDAT16	B3	B3	B3	B3	B3	B3	B1	B3		D16[1]
FPDAT17	B2	B2	B2	B2	B2	B2	B0	B2		D17[1]
FPCS1#		XCS	SSTB	LCDCS	SPR				CS	
FPCS2#										NCS2
FPSCLK		SCK	SCLK	SCLK					SCL	
FPA0		A0								
FPSO		SI	SDATA	SDO					SDI	
FPVIN1									SDO(FPSI)	
FPVIN2										VIN2
GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	PS	POL	CKV	VCLK	GPIO0	GPIO0
GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	CLS	GRES	LD	AP	GPIO1	GPIO1
GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	REV	FRP	INV	POL	GPIO2	GPIO2
GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	SPL	STH	VCOM	STH	GPIO3	GPIO3
GPIO4	R1	R1	R1	R1	R1	R1	GPIO4	R1	GPIO4	D18[1] or GPIO4
GPIO5	R0	R0	R0	R0	R0	R0	GPIO5	R0	GPIO5	D19[1] or GPIO5
GPIO6	G1	G1	G1	G1	G1	G1	GPIO6	G1	GPIO6	D20[1] or GPIO6
GPIO7	G0	G0	G0	G0	G0	G0	GPIO7	G0	GPIO7	D21[1] or GPIO7
GPIO8	B1	B1	B1	B1	B1	B1	GPIO8	B1	GPIO8	D22[1] or GPIO8
GPIO9	B0	B0	B0	B0	B0	B0	GPIO9	B0	GPIO9	D23[1] or GPIO9
GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10	GPIO10
GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11	GPIO11
GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12	GPIO12
GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13	GPIO13
GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21	GPIO14-21

Note

[1] Mode 4 supports 24-bit parallel panels if LCD Bypass Mode is not required. If LCD Bypass Mode is required, the bypass data is only 8-bit.

5.6 LCD Bypass Mode Pin Mapping

Table 5-8: LCD Interface Pin Mapping for Bypass Mode

Pin Name	LCD2		LCD1			LCD2		
	Serial Interface		Parallel Interface					
	Mode A	Mode B	Mode C	Mode D	Mode E	Mode F	Mode G	Mode H
FPFRAME	—	—	WR#[1]	WR#[1]	WR#[1]	WR#[1]	WR#[1]	WR#[1]
FPLINE	—	—	SA0	SA0	SA0	SA0	SA0	SA0
FPSHIFT	—	—	—	—	—	—	—	—
DRDY	—	—	RD#	RD#	RD#	RD#	RD#	RD#
FPDAT0	—	—	DB0	Low/High[2]	Low	DB0	Low/High[2]	Low
FPDAT1	—	—	DB1	DB0	DB0	DB1	DB0	DB0
FPDAT2	—	—	DB2	DB1	DB1	DB2	DB1	DB1
FPDAT3	—	—	DB3	DB2	DB2	DB3	DB2	DB2
FPDAT4	—	—	DB4	DB3	DB3	DB4	DB3	DB3
FPDAT5	—	—	DB5	DB4	DB4	DB5	DB4	DB4
FPDAT6	—	—	DB6	DB5	DB5	DB6	DB5	DB5
FPDAT7	—	—	DB7	DB6	DB6	DB7	DB6	DB6
FPDAT8	—	—	DB8	DB7	DB7	DB8	DB7	DB7
FPDAT9	—	—	DB9	DB8	Low	DB9	DB8	Low
FPDAT10	—	—	DB10	DB9	DB8	DB10	DB9	DB8
FPDAT11	—	—	DB11	DB10	DB9	DB11	DB10	DB9
FPDAT12	—	—	DB12	Low/High[3]	DB10	DB12	Low/High[3]	DB10
FPDAT13	—	—	DB13	DB11	DB11	DB13	DB11	DB11
FPDAT14	—	—	DB14	DB12	DB12	DB14	DB12	DB12
FPDAT15	—	—	DB15	DB13	DB13	DB15	DB13	DB13
FPDAT16	—	—	Low	DB14	DB14	Low	DB14	DB14
FPDAT17	—	—	Low	DB15	DB15	Low	DB15	DB15
FPCS1#	High	SCS#	SCS#	SCS#	SCS#	High	High	High
FPCS2#	SCS#	High	High	High	High	SCS#	SCS#	SCS#
FPSCK	SCK	SCK	—	—	—	—	—	—
FPA0	SA0	SA0	—	—	—	—	—	—
FPSO	SI	SI	—	—	—	—	—	—
FPVIN1	—	—	—	—	—	—	—	—
FPVIN2	—	—	—	—	—	—	—	—

1. WE# depends on the Host CPU type.
2. The output is driven according to the logical AND of DB4 - DB0.
3. The output is driven according to the logical AND of DB15 - DB11.
4. RGB refers to the signals used for RGB panels.

5.7 Camera Interface Pin Mapping

5.7.1 Camera1 Interface Pin Mapping

Table 5-9: Camera1 Interface Pin Mapping

Pin Name	Type 1 Camera
CM1DAT[7:0]	CAMDAT[7:0]
CM1VREF	VREF
CM1HREF	HREF
CM1CLKOUT	CAMMCLK
CM1CLKIN	CAMPCLK
GPIO21	GPIO21
GPIO20	GPIO20

5.7.2 Camera2 Interface Pin Mapping

Table 5-10: Camera2 Interface Pin Mapping

Pin Name	Camera	MPEG Codec Interface
CM2DAT[7:0]	CAMDAT[7:0]	DISPPXL[7:0]
CM2VREF	VREF	DISPVSYNC
CM2HREF	HREF	DISPHSYNC
CM2CLKOUT	CAMMCLK	DISPCLK
CM2CLKIN	CMCLKIN	DISPBLK

5.8 SD Memory Card Interface Pin Mapping

Table 5-11: SD Memory Card Interface Pin Mapping

Pin Name	SD Card I/F	MultiMediaCard (MMC)	Description
GPIO11	SDDAT0	DATA	This input/output pin is the card data IO bit 0.
GPIO12	SDDAT1	n/c	This input/output pin is the SD memory card data IO bit 1.
GPIO13	SDDAT2	n/c	This input/output pin is the SD memory card data IO bit 2.
GPIO14	SDDAT3	n/c	This input/output pin is the SD memory card data IO bit 3.
GPIO15	SDCMD	CMD	This input/output pin is the card command IO.
GPIO16	SDCLK	CLK	This input/output pin is the card clock output.
GPIO17	SDCD#	CD#	This input pin is the card detect.
GPIO18	SDWP	WP	This input pin is the card write protection input.
GPIO19	SDGPO	GPO	This output pin is the card general purpose output port.

Note

SIOVDD should be supplied to these pins when the SD Card/MMC interface is used. PIOVDD should be supplied to these pins when the SD Card/MMC interface is not used.

6 D.C. Characteristics

6.1 Absolute Maximum Ratings

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Core Supply Voltage	V_{SS} - 0.3 ~ 2.5	V
PLL V_{DD}	PLL Supply Voltage	V_{SS} - 0.3 ~ 2.1	V
HIO V_{DD}	Host IO Supply Voltage	Core V_{DD} ~ 4.0	V
PIO V_{DD}	Non-Host IO Supply Voltage	Core V_{DD} ~ 4.0	V
CIO1 V_{DD}	Camera1 IO Supply Voltage	Core V_{DD} ~ 4.0	V
CIO2 V_{DD}	Camera2 IO Supply Voltage	Core V_{DD} ~ 4.0	V
SIO V_{DD}	SD Card IO Supply Voltage	Core V_{DD} ~ 4.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 ~ IO V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 ~ IO V_{DD} + 0.5	V
I_{OUT}	Output Current	± 10	mA

6.2 Recommended Operating Conditions

Table 6-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Core Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
PLL V_{DD}	PLL Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
HIO V_{DD}	Host IO Supply Voltage	V_{SS} = 0 V	2.75	3.0	3.25	V
			2.3	2.5	2.7	
PIO V_{DD}	Non-Host IO Supply Voltage	V_{SS} = 0 V	2.75	3.0	3.25	V
			2.3	2.5	2.7	
CIO1 V_{DD}	Camera IO Supply Voltage	V_{SS} = 0 V	2.75	3.0	3.25	V
			2.3	2.5	2.7	
CIO2 V_{DD}	Camera IO Supply Voltage	V_{SS} = 0 V	2.75	3.0	2.25	V
			2.3	2.5	2.7	
SIO V_{DD}	SD Card IO Supply Voltage	V_{SS} = 0 V	2.75	3.0	3.25	V
			2.3	2.5	2.7	
V_{IN}	Input Voltage	—	V_{SS}	—	IO V_{DD}	V
T_{OPR}	Operating Temperature	—	-40	25	85	°C

6.3 Electrical Characteristics

The following characteristics are for: HIO V_{DD} = PIO V_{DD} = CIO V_{DD} = SIO V_{DD} = IO V_{DD1},
V_{SS} = 0V, T_{OPR} =-25 - 85°C.

Table 6-3: Electrical Characteristics for VDD = 3.0V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDSH}	IO Quiescent Current	Quiescent Conditions		TBD		µA
I_{DDSL}	CORE Quiescent Current	Quiescent Conditions		10		µA
I_{IZ}	Input Leakage Current		-5		5	µA
I_{OZ}	Output Leakage Current		-5		5	µA
$HIOV_{OH}$	High Level Output Voltage	HIOVDD = min I_{OH} = -3.6mA	$HIOV_{DD}$ - 0.4			V
$CIO1V_{OH}$	High Level Output Voltage	CIO1VDD = min I_{OH} = -3.6mA	$CIO1V_{DD}$ - 0.4			V
$CIO2V_{OH}$	High Level Output Voltage	CIO2VDD = min I_{OH} = -3.6mA	$CIO2V_{DD}$ - 0.4			V
$PIOV_{OH}$	High Level Output Voltage	PIOVDD = min I_{OH} = -3.6mA	$PIOV_{DD}$ - 0.4			V
$SIOV_{OH}$	High Level Output Voltage	SIOVDD = min I_{OH} = -3.6mA	$SIOV_{DD}$ - 0.4			V
$HIOV_{OL}$	Low Level Output Voltage	HIOVDD = min I_{OL} = 3.6mA			0.4	V
$CIO1V_{OL}$	Low Level Output Voltage	CIO1VDD = min I_{OL} = 3.6mA			0.4	V
$CIO2V_{OL}$	Low Level Output Voltage	CIO2VDD = min I_{OL} = 3.6mA			0.4	V
$PIOV_{OL}$	Low Level Output Voltage	PIOVDD = min I_{OL} = 3.6mA			0.4	V
$SIOV_{OL}$	Low Level Output Voltage	SIOVDD = min I_{OL} = 3.6mA			0.4	V
$HIOV_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.95			V
$CIO1V_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.95			V
$CIO2V_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.95			V
$PIOV_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.95			V
$SIOV_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.95			V
$HIOV_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.85	V
$CIO1V_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.85	V
$CIO2V_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.85	V
$PIOV_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.85	V
$SIOV_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.85	V

Table 6-3: Electrical Characteristics for VDD = 3.0V typical (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$HIOV_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	1.35		2.5	V
$CIO1V_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	1.35		2.5	V
$CIO2V_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	1.35		2.5	V
$PIOV_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	1.35		2.5	V
$HIOV_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.7		1.6	V
$CIO1V_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.7		1.6	V
$CIO2V_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.7		1.6	V
$PIOV_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.7		1.6	V
R_{PD}	Pull Down Resistance	$V_{IN} = V_{DD}$	30	60	144	kΩ
R_{PU}	Pull Up Resistance	$V_{IN} = V_{DD}$	30	60	144	kΩ
C_I	Input Pin Capacitance	f = 1MHz, V_{DD} = 0V	-	-	8	pF
C_O	Output Pin Capacitance	f = 1MHz, V_{DD} = 0V	-	-	8	pF
C_{IO}	Bi-Directional Pin Capacitance	f = 1MHz, V_{DD} = 0V	-	-	8	pF

1. The pull-down resistance depends on COREVDD.
2. SDCD#, SDWP pin

Table 6-4: Electrical Characteristics for VDD = 2.5V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDSH}	IO Quiescent Current	Quiescent Conditions		TBD		µA
I_{DDSL}	CORE Quiescent Current	Quiescent Conditions		10		µA
I_{IZ}	Input Leakage Current		-5		5	µA
I_{OZ}	Output Leakage Current		-5		5	µA
$HIOV_{OH}$	High Level Output Voltage	HIOVDD = min I_{OH} = -3mA	$HIOV_{DD}$ - 0.4			V
$CIO1V_{OH}$	High Level Output Voltage	CIO1VDD = min I_{OH} = -3mA	$CIO1V_{DD}$ - 0.4			V
$CIO2V_{OH}$	High Level Output Voltage	CIO2VDD = min I_{OH} = -3mA	$CIO2V_{DD}$ - 0.4			V
$PIOV_{OH}$	High Level Output Voltage	PIOVDD = min I_{OH} = -3mA	$PIOV_{DD}$ - 0.4			V
$SIOV_{OH}$	High Level Output Voltage	SIOVDD = min I_{OH} = -3mA	$SIOV_{DD}$ - 0.4			V
$HIOV_{OL}$	Low Level Output Voltage	HIOVDD = min I_{OL} = 3mA			0.4	V
$CIO1V_{OL}$	Low Level Output Voltage	CIO1VDD = min I_{OL} = 3mA			0.4	V
$CIO2V_{OL}$	Low Level Output Voltage	CIO2VDD = min I_{OL} = 3mA			0.4	V
$PIOV_{OL}$	Low Level Output Voltage	PIOVDD = min I_{OL} = 3mA			0.4	V
$SIOV_{OL}$	Low Level Output Voltage	SIOVDD = min I_{OL} = 3mA			0.4	V
$HIOV_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.7			V
$CIO1V_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.7			V

Table 6-4: Electrical Characteristics for VDD = 2.5V typical (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$CIO2V_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.7			V
$PIOV_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.7			V
$SIOV_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.7			V
$HIOV_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.7	V
$CIO1V_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.7	V
$CIO2V_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.7	V
$PIOV_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.7	V
$SIOV_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.7	V
$HIOV_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	0.8		1.9	V
$CIO1V_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	0.8		1.9	V
$CIO2V_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	0.8		1.9	V
$PIOV_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	0.8		1.9	V
$HIOV_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.5		1.3	V
$CIO1V_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.5		1.3	V
$CIO2V_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.5		1.3	V
$PIOV_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.5		1.3	V
R_{PD}	Pull Down Resistance	$V_{IN} = V_{DD}$	35	70	175	kΩ
R_{PU}	Pull Up Resistance	$V_{IN} = V_{DD}$	35	70	175	kΩ
C_I	Input Pin Capacitance	f = 1MHz, V_{DD} = 0V	-	-	8	pF
C_O	Output Pin Capacitance	f = 1MHz, V_{DD} = 0V	-	-	8	pF
C_{IO}	Bi-Directional Pin Capacitance	f = 1MHz, V_{DD} = 0V	-	-	8	pF

1. The pull-down resistance depends on COREVDD.
2. SDCD#, SDWP pin

7 A.C. Characteristics

Conditions: IO V_{DD} = 3.0V ± 0.25V
T_A = -40° C to 85° C
T_{rise} and T_{fall} for all inputs except CLKI must be ≤ 50 ns (10% ~ 90%)
C_L = 15pF (Host Interface)
C_L = 15pF (Camera Interface)
C_L = 30pF (LCD Panel/GPIO Interface)

7.1 Clock Timing

7.1.1 Input Clocks

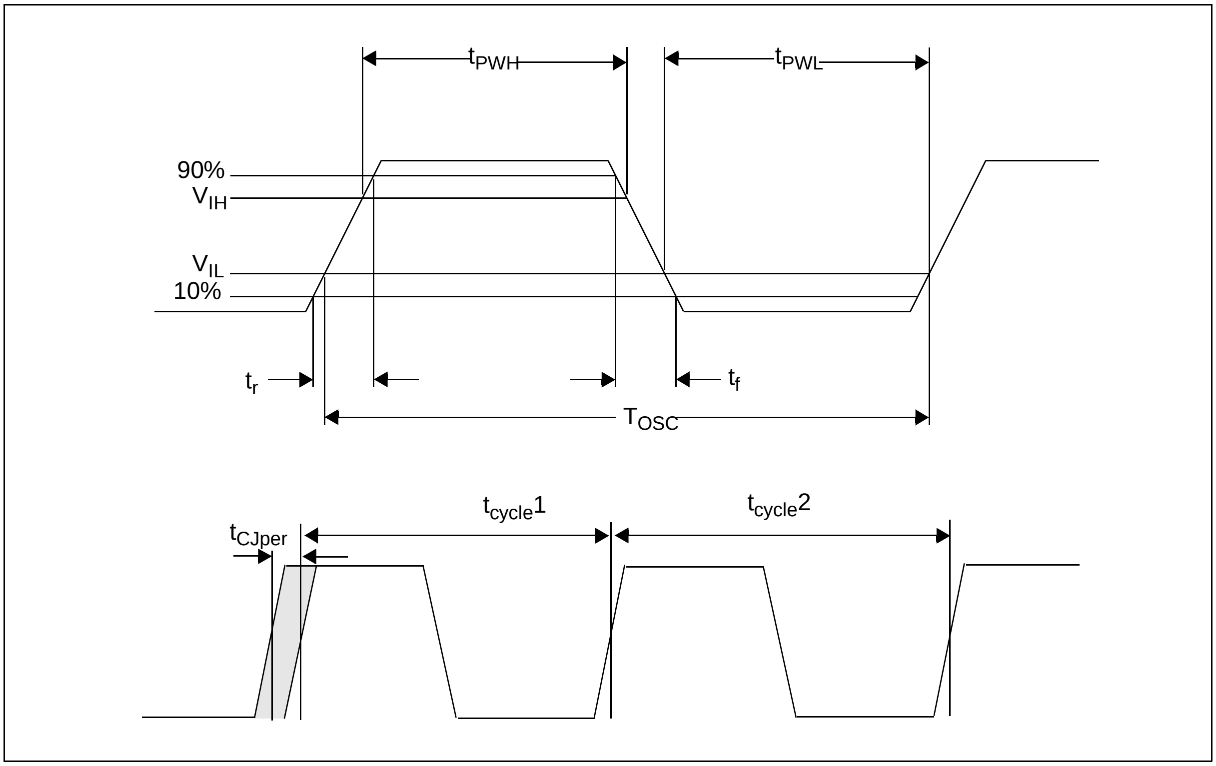

Figure 7-1: Clock Input Required (PLL)

Table 7-1: Clock Input Requirements (PLL)

Symbol	Parameter	Min	Typ	Max	Units
f_{OSC}	Input clock frequency	30	32.768	64	KHz
T_{OSC}	Input clock period	—	$1/f_{OSC}$	—	µs
t_{PWH}	Input clock pulse width high	5	—	—	µs
t_{PWL}	Input clock pulse width low	5	—	—	µs
t_r	Input clock rising time (10% - 90%)		—	5	µs
t_f	Input clock falling time (10% - 90%)		—	5	µs
t_{CJper}	Input clock period jitter (see Notes 2 and 4)	-100	—	100	ns
$t_{CJcycle}$ (Note 1)	Input clock cycle jitter (see Notes 3 and 4)	-100	—	100	ns

1. $t_{CJcycle} = t_{cycle}1 - t_{cycle}2$
2. The input clock period jitter is the displacement relative to the center period (reciprocal of the center frequency).
3. The input clock cycle jitter is the difference in period between adjacent cycles.
4. The jitter characteristics must satisfy both the t_{CJper} and $t_{CJcycle}$ characteristics.

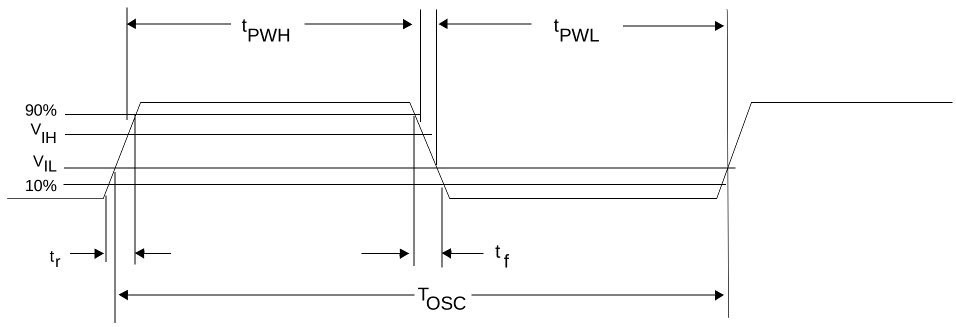

Figure 7-2: Clock Input Requirements (PLL Bypassed)

Table 7-2: Clock Input Requirements (PLL Bypassed)

Symbol	Parameter	Min	Typ	Max	Units
f_{OSCI}	Input Clock Frequency (CLKI)	—	—	55	MHz
T_{OSC}	Input Clock period (CLKI)	$1/f_{OSC}$	—	—	ns
t_{PWH}	Input Clock Pulse Width High (CLKI)	$0.4T_{OSC}$	—	—	ns
t_{PWL}	Input Clock Pulse Width Low (CLKI)	$0.4T_{OSC}$	—	—	ns
t_r	Input clock rising time (10% - 90%)	—	—	5	ns
t_f	Input clock falling time (10% - 90%)	—	—	5	ns

7.1.2 Internal System Clock

Table 7-3: Internal System Clock Requirements

Symbol	Parameter	Min	Max	Units
f_{SYS}	Internal System Clock Frequency	—	55	MHz
T_{SYS}	Internal System Clock Period	$1/f_{SYS}$	—	ns

7.1.3 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.

For example, if noise with a 2KHz frequency modulation is added on PLLVDD, the jitter on the PLL clock output may fluctuate. Measures must be taken to avoid noise within the range of 1KHz to 3KHz.

The specific design should be confirmed to determine the jitter value of a clock. This is because the actual jitter characteristics are affected by a combination of factors, such as the jitter frequency spectrum of the clock, and amplitude and frequency of the noise on the supplied power. If the jitter of a clock exceeds the requirement of a module, an external oscillator should be used instead of using the internal PLL circuitry.

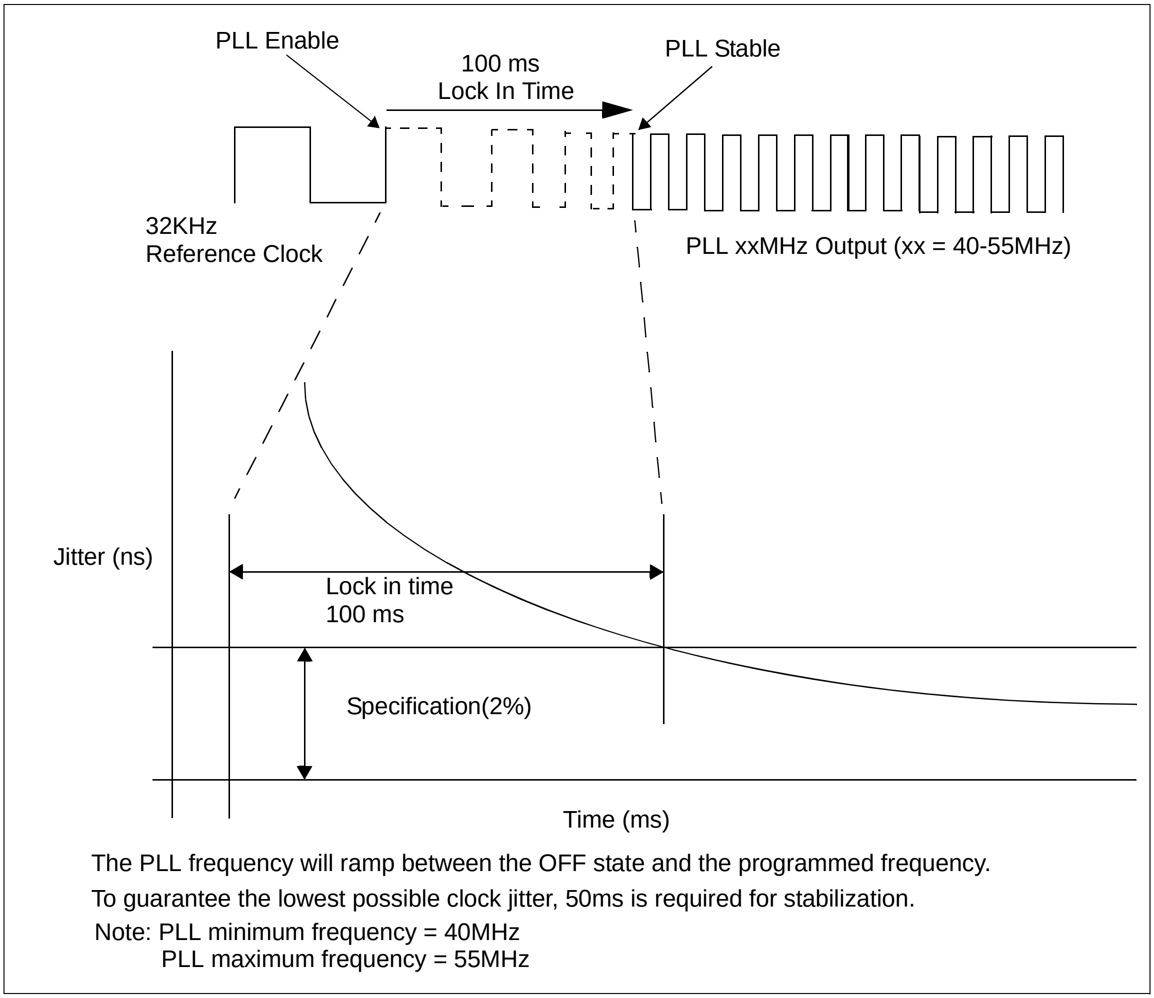

Figure 7-3: PLL Start-Up Time

Table 7-4: PLL Clock Requirements

Symbol	**Parameter**	**Min**	**Max**	**Units**
f_{PLL}	PLL output clock frequency	40	55	MHz
t_{PStal}	PLL output stable time	—	100	ms

7.2 Power Supply Sequence

7.2.1 Power-On Sequence

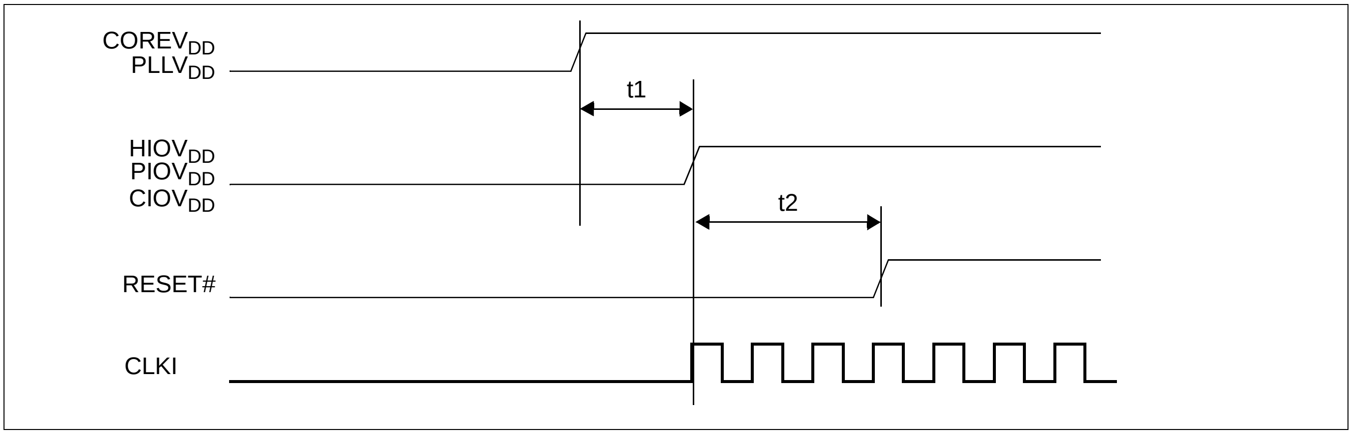

Figure 7-4: Power-On Sequence

Table 7-5: Power-On Sequence

Symbol	Parameter	Min	Max	Units
t1	IOV_{DD} on delay from $COREV_{DD}$ / $PLLV_{DD}$ on	0	—	ns
t2	RESET# width period (Start of CLKI) (Note1)	1	—	CLKI

1. When CLKI can not be input for the reset period, a“Soft Reset” is necessary in the power-on sequence.

7.2.2 Power-Off Sequence

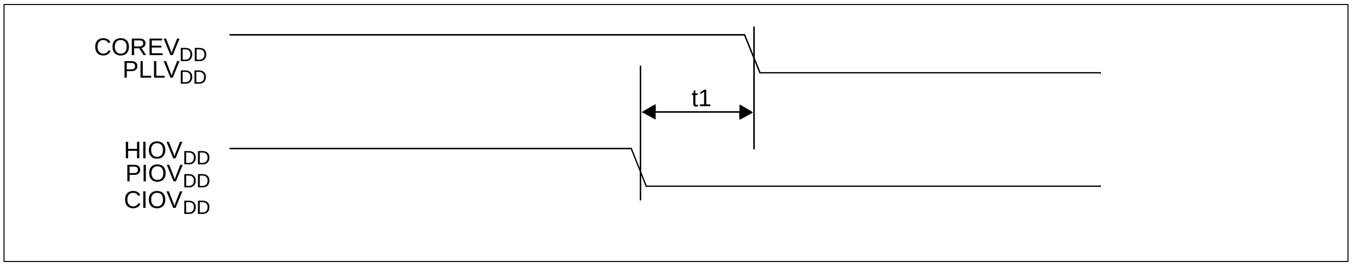

Figure 7-5: Power-Off Sequence

Table 7-6: Power-Off Sequence

Symbol	Parameter	Min	Max	Units
t1	$COREV_{DD}$ / $PLLV_{DD}$ off delay from IOV_{DD} off	0	—	ns

7.3 Host Interface Timing

7.3.1 Direct 80 Type 1

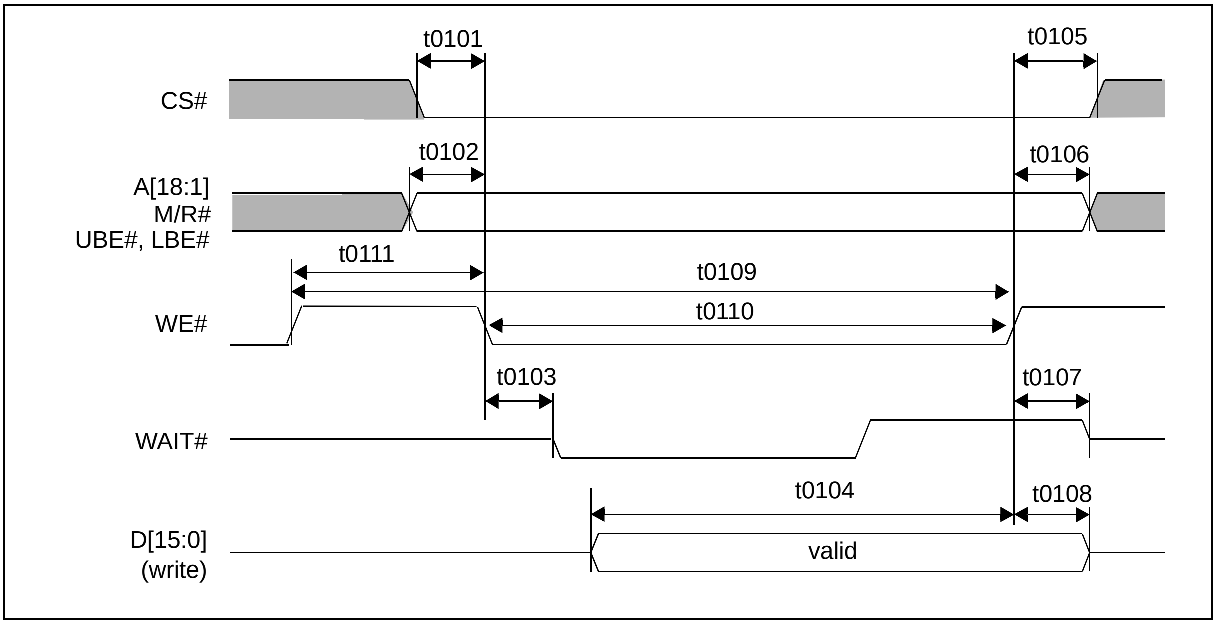

Figure 7-6: Direct 80 Type 1 Interface Write Cycle Timing

Table 7-7: Direct 80 Type 1 Interface Write Cycle Timing

Symbol	Parameter	3.0 Volt		1.8 Volt		Units
		Min	Max	Min	Max	
t0101	CS# setup time	5	—	5	—	ns
t0102	A[18:1], M/R#, UBE#, LBE# setup time	5	—	5	—	ns
t0103	WE# falling edge to WAIT# driven low	—	12		14	ns
t0104	D[15:0] setup time to WE# rising edge	15	—	7	—	ns
t0105	CS# hold time from WE# rising edge	4	—	4	—	ns
t0106	A[18:1], M/R#, UBE#, LBE# hold time from WE# rising edge	4	—	4	—	ns
t0107	WE# rising edge to WAIT# high impedance	—	7		8	ns
t0108	D[15:0] hold time from WE# rising edge.	0	—	0	—	ns
t0109	WE# cycle time	3	—	3	—	Ts
t0110	WE# pulse active time	2	—	2	—	Ts
t0111	WE# pulse inactive time	1	—	1	—	Ts

1. Ts = System clock period.

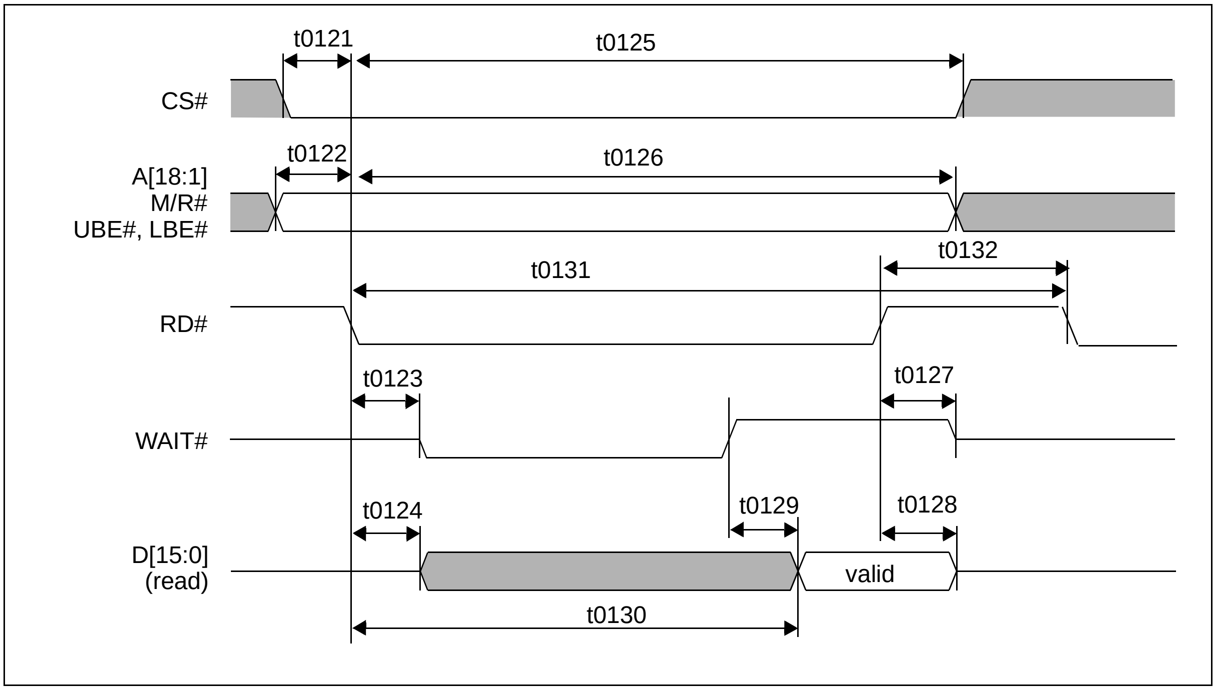

Figure 7-7: Direct 80 Type 1 Interface Read Cycle Timing

Table 7-8: Direct 80 Type 1 Interface Read Cycle Timing

Symbol	Parameter	3.0 Volt		1.8 Volt		Units
		Min	Max	Min	Max	
t0121	CS# setup time	Note2	—	Note2	—	ns
t0122	A[18:1], M/R#, UBE#, LBE# setup time	Note2	—	Note2	—	ns
t0123	RD# falling edge to WAIT# driven low	—	Note2	—	Note2	ns
t0124	RD# falling edge to D[15:0] driven	4	—	4	—	ns
t0125	CS# hold time from RD# falling edge	20	—	20	—	ns
t0126	A[18:1], M/R#, UBE#, LBE# hold time from RD# falling edge	20	—	20	—	ns
t0127	RD# rising edge to WAIT# high impedance	—	8	—	8	ns
t0128	D[15:0] hold time from RD# rising edge	2	8	2	9	ns
t0129	WAIT# rising edge to valid Data if WAIT# is asserted	—	10	—	7	ns
t0130	RD# falling edge to valid Data if WAIT# is NOT asserted	—	Note2	—	Note2	ns
t0131	RD# cycle time	3	—	3	—	Ts
t0132	RD# pulse inactive time	8	—	8	—	ns

1. Ts = System clock period.
2. REG[0006h] bit 9,
   When this bit = 0, t0121min/ t0122min = 5ns, t0123max = 18ns, t0130max = 28ns.
   When this bit = 1, t0121min/ t0122min = 0ns, t0123max = 15ns, t0130max = 25ns.

Table 7-9: Direct 80 Type 1 Interface Truth Table (Little Endian / 1 CS# Mode)

CS#	M/R#	WE#	RD#	UBE#	LBE#	D[15:8]	D[7:0]	Comments
0	1/0	0	1	0	0	valid	valid	16-bit write
0	1	0	1	1	0	—	valid	8-bit write; even address
0	1	0	1	0	1	valid	—	8-bit write; odd address
0	1/0	1	0	0	0	valid	valid	16-bit read
0	1	1	0	1	0	—	valid	8-bit read; even address
0	1	1	0	0	1	valid	—	8-bit read; odd address

Table 7-10: Direct 80 Type 1 Interface Truth Table (Big Endian / 1 CS# Mode)

CS#	M/R#	WE#	RD#	UBE#	LBE#	D[15:8]	D[7:0]	Comments
0	1/0	0	1	0	0	valid	valid	16-bit write
0	1	0	1	1	0	—	valid	8-bit write; odd address
0	1	0	1	0	1	valid	—	8-bit write; even address
0	1/0	1	0	0	0	valid	valid	16-bit read
0	1	1	0	1	0	—	valid	8-bit read; odd address
0	1	1	0	0	1	valid	—	8-bit read; even address

Table 7-11: Direct 80 Type 1 Interface Truth Table (Little Endian / 2 CS# Mode)

CS#	M/R#	WE#	RD#	UBE#	LBE#	D[15:8]	D[7:0]	Comments
0/1	1/0	0	1	0	0	valid	valid	16-bit write
0	1	0	1	1	0	—	valid	8-bit write; even address
0	1	0	1	0	1	valid	—	8-bit write; odd address
0/1	1/0	1	0	0	0	valid	valid	16-bit read
0	1	1	0	1	0	—	valid	8-bit read; even address
0	1	1	0	0	1	valid	—	8-bit read; odd address

Table 7-12: Direct 80 Type 1 Interface Truth Table (Big Endian / 2 CS# Mode)

CS#	M/R#	WE#	RD#	UBE#	LBE#	D[15:8]	D[7:0]	Comments
0/1	1/0	0	1	0	0	valid	valid	16-bit write
0	1	0	1	1	0	—	valid	8-bit write; odd address
0	1	0	1	0	1	valid	—	8-bit write; even address
0/1	1/0	1	0	0	0	valid	valid	16-bit read
0	1	1	0	1	0	—	valid	8-bit read; odd address
0	1	1	0	0	1	valid	—	8-bit read; even address

7.3.2 Direct 80 Type 2

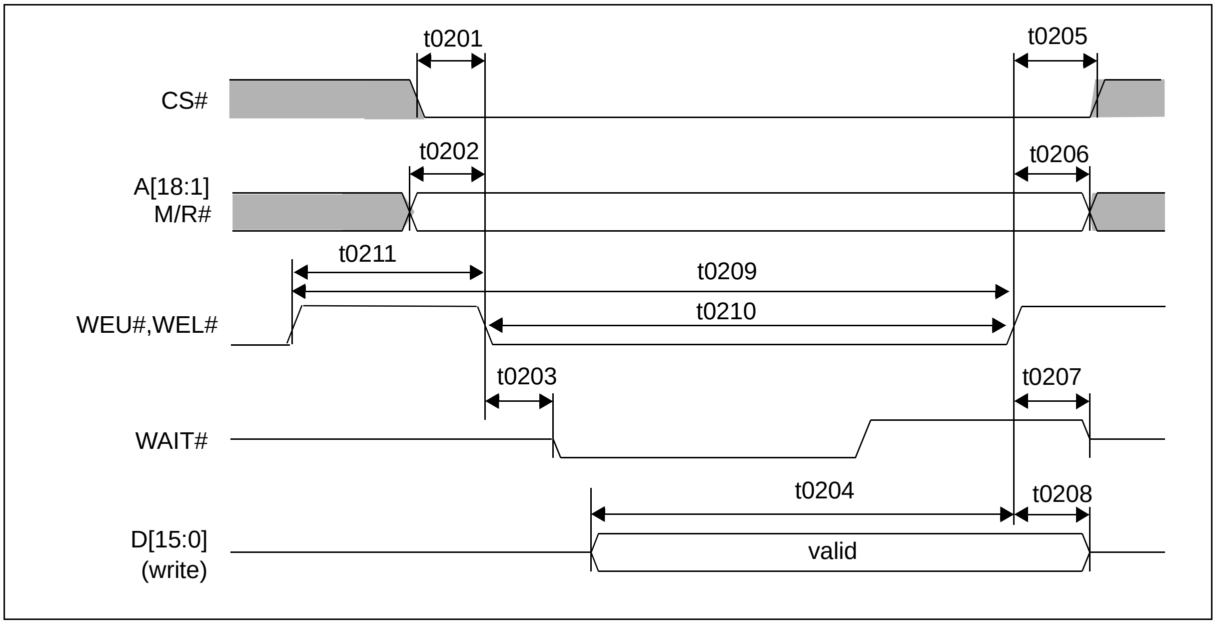

Figure 7-8: Direct 80 Type 2Interface Write Cycle Timing

Table 7-13: Direct 80 Type 2 Interface Write Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0201	CS# setup time	5	—	ns
t0202	A[18:1], M/R# setup time	5	—	ns
t0203	WEU#,WEL# falling edge to WAIT# driven low	—	12	ns
t0204	D[15:0] setup time to WEU#,WEL# rising edge	15	—	ns
t0205	CS# hold time from WEU#,WEL# rising edge	4	—	ns
t0206	A[18:1], M/R# hold time from WEU#,WEL# rising edge	4	—	ns
t0207	WEU#,WEL# rising edge to WAIT# high impedance	—	7	ns
t0208	D[15:0] hold time from WEU#,WEL# rising edge.	0	—	ns
t0209	WEU#,WEL# cycle time	3	—	Ts
t0210	WEU#,WEL# pulse active time	2	—	Ts
t0211	WEU#,WEL# pulse inactive time	1	—	Ts

1. Ts = System clock period.

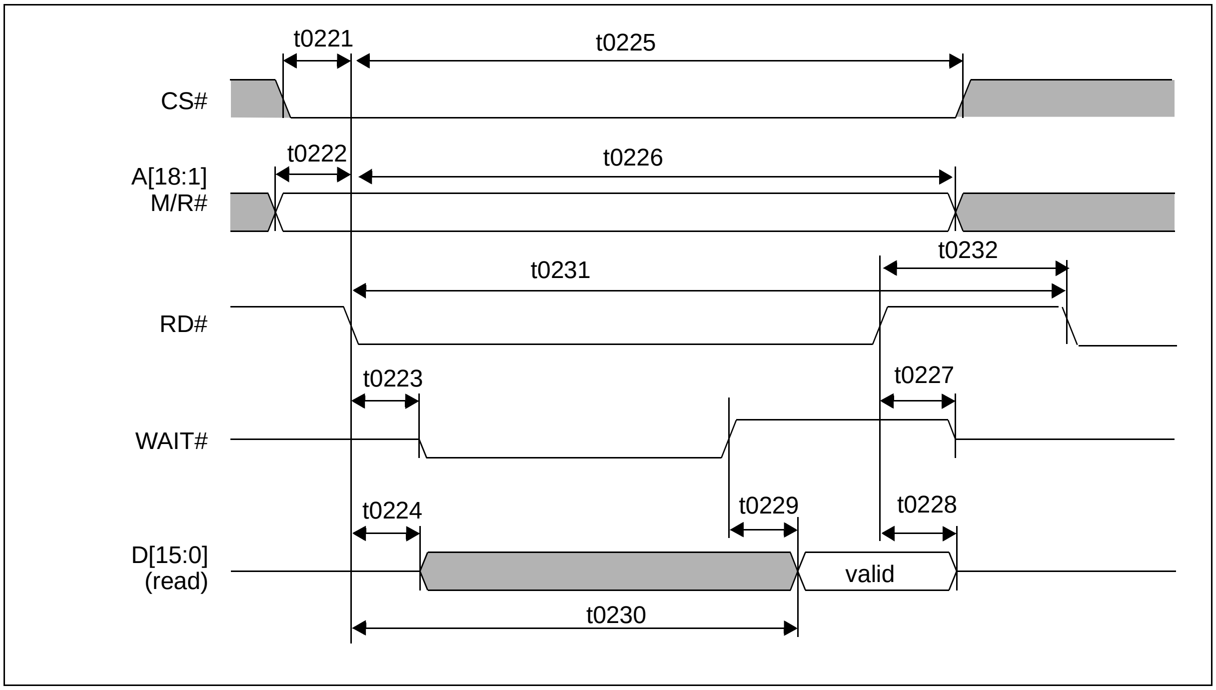

Figure 7-9: Direct 80 Type 2 Interface Read Cycle Timing

Table 7-14: Direct 80 Type 2 Interface Read Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0221	CS# setup time	Note2	—	ns
t0222	A[18:1], M/R# setup time	Note2	—	ns
t0223	RD# falling edge to WAIT# driven low	—	Note2	ns
t0224	RD# falling edge to D[15:0] driven	4	—	ns
t0225	CS# hold time from RD# falling edge	20	—	ns
t0226	A[18:1], M/R# hold time from RD# falling edge	20	—	ns
t0227	RD# rising edge to WAIT# high impedance	—	8	ns
t0228	D[15:0] hold time from RD# rising edge	2	8	ns
t0229	WAIT# rising edge to valid Data if WAIT# is asserted	—	10	ns
t0230	RD# falling edge to valid Data if WAIT# is NOT asserted	—	Note2	ns
t0231	RD# cycle time	3	—	Ts
t0232	RD# pulse inactive time	8	—	ns

1. Ts = System clock period
2. REG[0006h] bit 9,
   When this bit = 0, t0221min/ t0222min = 5ns, t0223max = 18ns, t0230max = 28ns.
   When this bit = 1, t0221min/ t0222min = 0ns, t0223max = 15ns, t0230max = 25ns.

Table 7-15: Direct 80 Type 2 Interface Truth Table (Little Endian / 1 CS# Mode)

CS#	M/R#	RD#	WEU#	WEL#	D[15:8]	D[7:0]	Comments
0	1/0	1	0	0	valid	valid	16-bit write
0	1	1	1	0	—	valid	8-bit write; even address
0	1	1	0	1	valid	—	8-bit write; odd address
0	1/0	0	1	1	valid	valid	16-bit read

Table 7-16: Direct 80 Type 2 Interface Truth Table (Big Endian / 1 CS# Mode)

CS#	M/R#	RD#	WEU#	WEL#	D[15:8]	D[7:0]	Comments
0	1/0	1	0	0	valid	valid	16-bit write
0	1	1	1	0	—	valid	8-bit write; odd address
0	1	1	0	1	valid	—	8-bit write; even address
0	1/0	0	1	1	valid	valid	16-bit read

Table 7-17: Direct 80 Type 2 Interface Truth Table (Little Endian / 2 CS# Mode)

CS#	M/R#	RD#	WEU#	WEL#	D[15:8]	D[7:0]	Comments
0/1	1/0	1	0	0	valid	valid	16-bit write
0	1	1	1	0	—	valid	8-bit write; even address
0	1	1	0	1	valid	—	8-bit write; odd address
0/1	1/0	0	1	1	valid	valid	16-bit read

Table 7-18: Direct 80 Type 2 Interface Truth Table (Big Endian / 2 CS# Mode)

CS#	M/R#	RD#	WEU#	WEL#	D[15:8]	D[7:0]	Comments
0/1	1/0	1	0	0	valid	valid	16-bit write
0	1	1	1	0	—	valid	8-bit write; odd address
0	1	1	0	1	valid	—	8-bit write; even address
0/1	1/0	0	1	1	valid	valid	16-bit read

7.3.3 Direct 80 Type 3

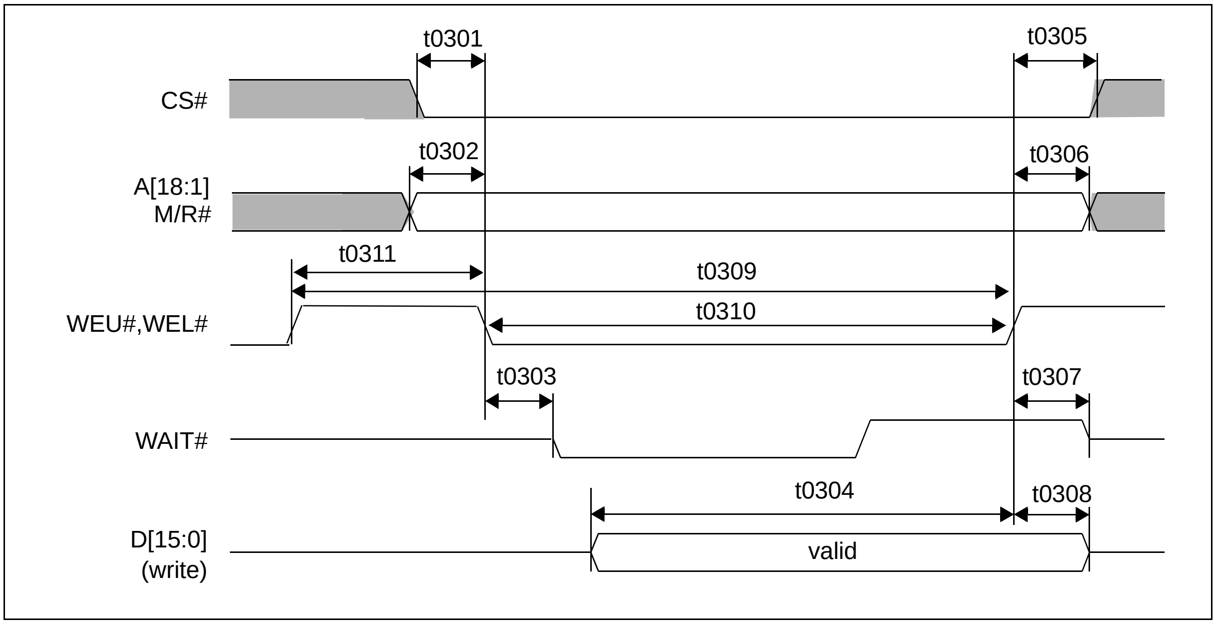

Figure 7-10: Direct 80 Type 3 Interface Write Cycle Timing

Table 7-19: Direct 80 Type 3 Interface Write Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0301	CS# setup time	5	—	ns
t0302	A[18:1], M/R# setup time	5	—	ns
t0303	WEU#, WEL# falling edge to WAIT# driven low	—	12	ns
t0304	D[15:0] setup time to WEU#,WEL# rising edge	15	—	ns
t0305	CS# hold time from WEU#,WEL# rising edge	4	—	ns
t0306	A[18:1], M/R# hold time from WE# rising edge	4	—	ns
t0307	WEU#, WEL# rising edge to WAIT# high impedance	—	7	ns
t0308	D[15:0] hold time from WEU#,WEL# rising edge.	5	—	ns
t0309	WEU#, WEL# cycle time	3	—	Ts
t0310	WEU#, WEL# pulse active time	2	—	Ts
t0311	WEU#, WEL# pulse inactive time	1	—	Ts

1. Ts = System clock period.

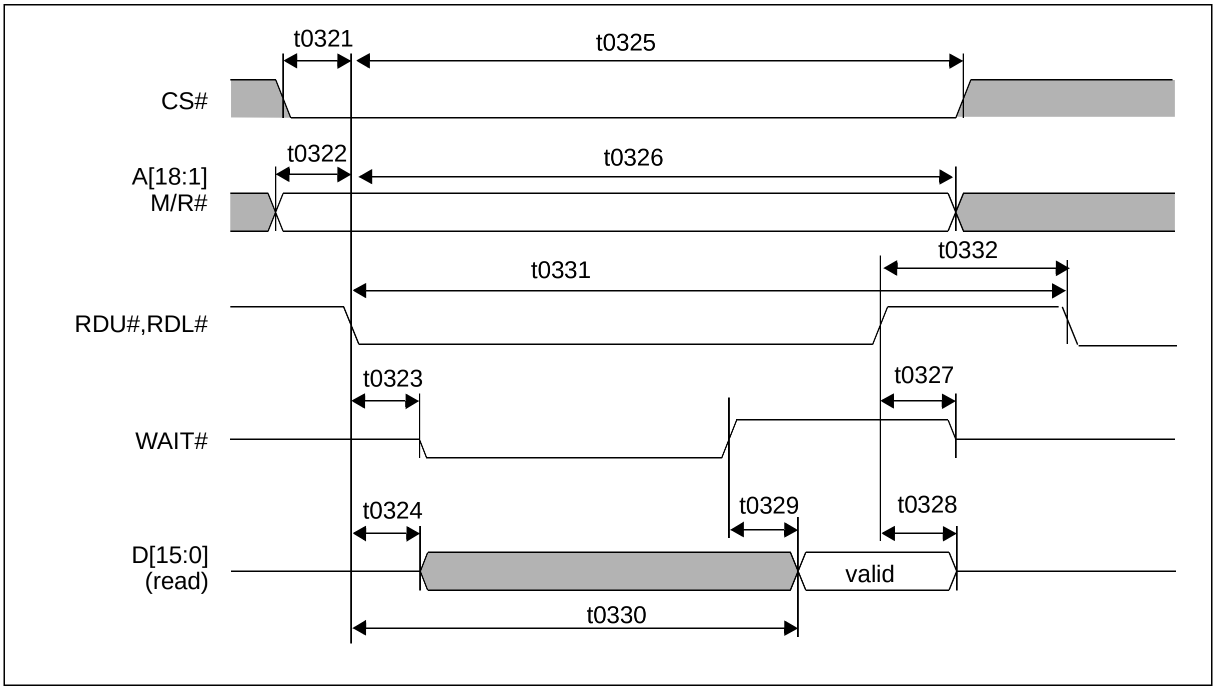

Figure 7-11: Direct 80 Type 3 Interface Read Cycle Timing

Table 7-20: Direct 80 Type 3 Interface Read Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0321	CS# setup time	Note2	—	ns
t0322	A[18:1], M/R# setup time	Note2	—	ns
t0323	RD# falling edge to WAIT# driven low	—	Note2	ns
t0324	RD# falling edge to D[15:0] driven	4	—	ns
t0325	CS# hold time from RD# falling edge	20	—	ns
t0326	A[18:1], M/R# hold time from RD# falling edge	20	—	ns
t0327	RD# rising edge to WAIT# high impedance	--	8	ns
t0328	D[15:0] hold time from RD# rising edge	2	8	ns
t0329	WAIT# rising edge to valid Data if WAIT# is asserted	—	10	ns
t0330	RD# falling edge to valid Data if WAIT# is NOT asserted	—	Note2	ns
t0331	RD# cycle time	3	—	Ts
t0332	RD# pulse inactive time	8	—	ns

1. Ts = System clock period
2. REG[0006h] bit 9,
   When this bit = 0, t0321min/ t0322min = 5ns, t0323max = 18ns, t0330max = 28ns.
   When this bit = 1, t0321min/ t0322min = 0ns, t0323max = 15ns, t0330max = 25ns.

Table 7-21: Direct 80 Type 3 Interface Truth Table (Little Endian / 1 CS# Mode)

CS#	M/R#	WEU#	WEL#	RDU#	RDL#	D[15:8]	D[7:0]	Comments
0	1/0	0	0	1	1	valid	valid	16-bit write
0	1	1	0	1	1	—	valid	8-bit write; even address
0	1	0	1	1	1	valid	—	8-bit write; odd address
0	1/0	1	1	0	0	valid	valid	16-bit read
0	1	1	1	1	0	—	valid	8-bit read; even address
0	1	1	1	0	1	valid	—	8-bit read; odd address

Table 7-22: Direct 80 Type 3 Interface Truth Table (Big Endian / 1 CS# Mode)

CS#	M/R#	WEU#	WEL#	RDU#	RDL#	D[15:8]	D[7:0]	Comments
0	1/0	0	0	1	1	valid	valid	16-bit write
0	1	1	0	1	1	—	valid	8-bit write; odd address
0	1	0	1	1	1	valid	—	8-bit write; even address
0	1/0	1	1	0	0	valid	valid	16-bit read
0	1	1	1	1	0	—	valid	8-bit read; odd address
0	1	1	1	0	1	valid	—	8-bit read; even address

Table 7-23: Direct 80 Type 3 Interface Truth Table (Little Endian / 2 CS# Mode)

CS#	M/R#	WEU#	WEL#	RDU#	RDL#	D[15:8]	D[7:0]	Comments
0/1	1/0	0	0	1	1	valid	valid	16-bit write
0	1	1	0	1	1	—	valid	8-bit write; even address
0	1	0	1	1	1	valid	—	8-bit write; odd address
0/1	1/0	1	1	0	0	valid	valid	16-bit read
0	1	1	1	1	0	—	valid	8-bit read; even address
0	1	1	1	0	1	valid	—	8-bit read; odd address

Table 7-24: Direct 80 Type 3 Interface Truth Table (Big Endian / 2 CS# Mode)

CS#	M/R#	WEU#	WEL#	RDU#	RDL#	D[15:8]	D[7:0]	Comments
0/1	1/0	0	0	1	1	valid	valid	16-bit write
0	1	1	0	1	1	—	valid	8-bit write; odd address
0	1	0	1	1	1	valid	—	8-bit write; even address
0/1	1/0	1	1	0	0	valid	valid	16-bit read
0	1	1	1	1	0	—	valid	8-bit read; odd address
0	1	1	1	0	1	valid	—	8-bit read; even address

7.3.4 Direct 68

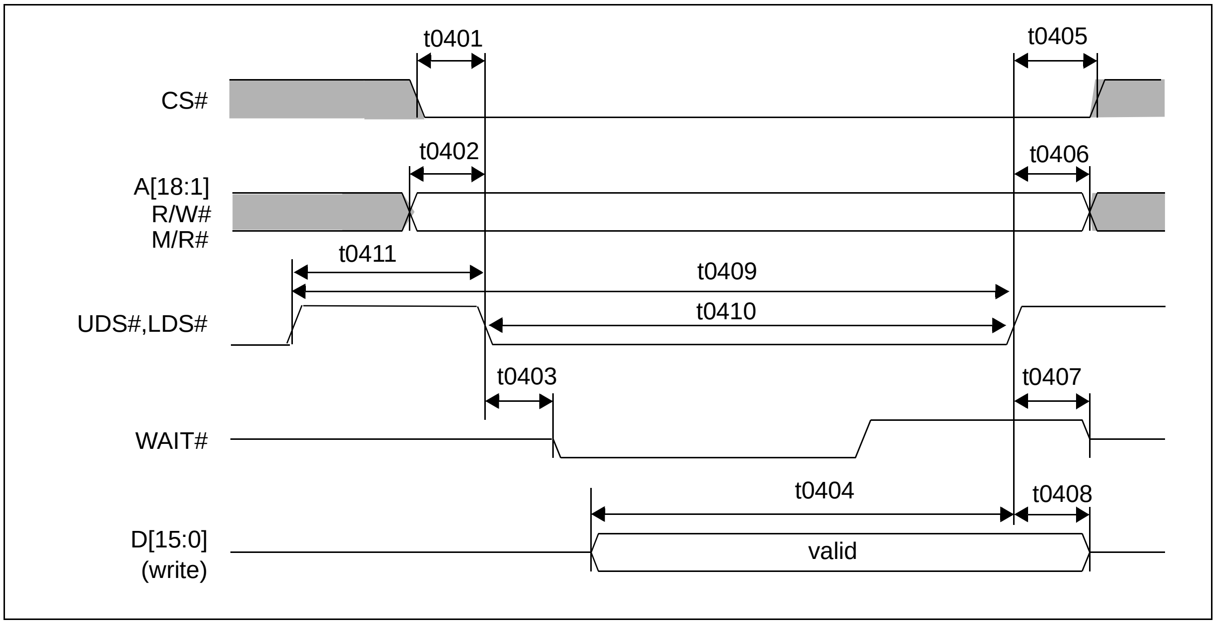

Figure 7-12: Direct 68 Interface Write Cycle Timing

Table 7-25: Direct 68 Interface Write Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0401	CS# setup time	5	—	ns
t0402	A[18:1], R/W#, M/R# setup time	5	—	ns
t0403	UDS#, LDS# falling edge to WAIT# driven low	—	12	ns
t0404	D[15:0] setup time to UDS#, LDS# rising edge	15	—	ns
t0405	CS# hold time from UDS#,LDS# rising edge	4	—	ns
t0406	A[18:1], R/W#, M/R# hold time from UDS#, LDS# rising edge	4	—	ns
t0407	UDS#, LDS# rising edge to WAIT# high impedance	—	7	ns
t0408	D[15:0] hold time from UDS#, LDS# rising edge.	0	—	ns
t0409	UDS#, LDS# cycle time	3	—	Ts
t0410	UDS#, LDS# pulse active time	2	—	Ts
t0411	UDS#, LDS# pulse inactive time	1	—	Ts

1. Ts = System clock period.

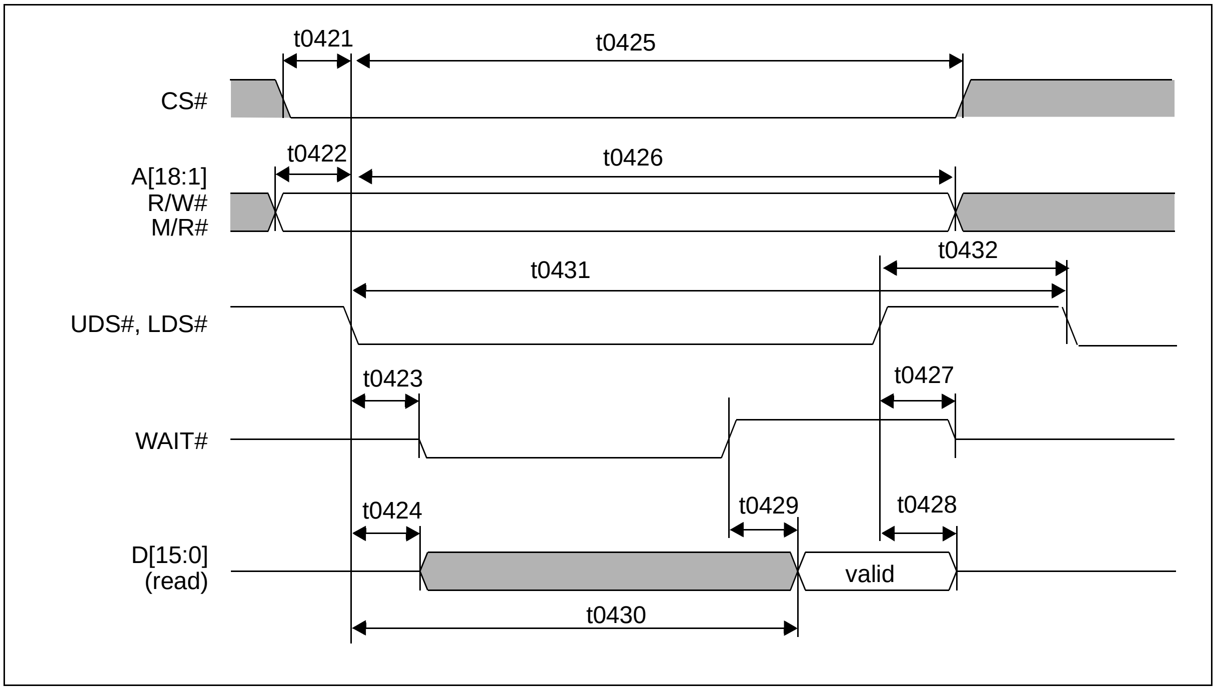

Figure 7-13: Direct 68 Interface Read Cycle Timing

Table 7-26: Direct 68 Interface Read Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	**Max**	
t0421	CS# setup time	Note2	—	ns
t0422	A[18:1], R/W#, M/R# setup time	Note2	—	ns
t0423	UDS#,LDS# falling edge to WAIT# driven low	—	Note2	ns
t0424	UDS#,LDS# falling edge to D[15:0] driven	4	—	ns
t0425	CS# hold time from UDS#,LDS# falling edge	20	—	ns
t0426	A[18:1], R/W#, M/R# hold time from UDS#,LDS# falling edge	20	—	ns
t0427	UDS#,LDS# rising edge to WAIT# high impedance	—	8	ns
t0428	D[15:0] hold time from UDS#, LDS# rising edge	2	8	ns
t0429	WAIT# rising edge to valid Data if WAIT# is asserted	—	10	ns
t0430	UDS#,LDS# falling edge to valid Data if WAIT# is NOT asserted	—	Note2	ns
t0431	UDS#,LDS# cycle time	3	—	Ts
t0432	UDS#,LDS# pulse inactive time	8	—	ns

1. Ts = System clock period
2. REG[0006h] bit 9,
   When this bit = 0, t0421min/ t0422min = 5ns, t0423max = 18ns, t0430max = 28ns.
   When this bit = 1, t0421min/ t0422min = 0ns, t0423max = 15ns, t0430max = 25ns.

7.3.5 Indirect 80 Type 1

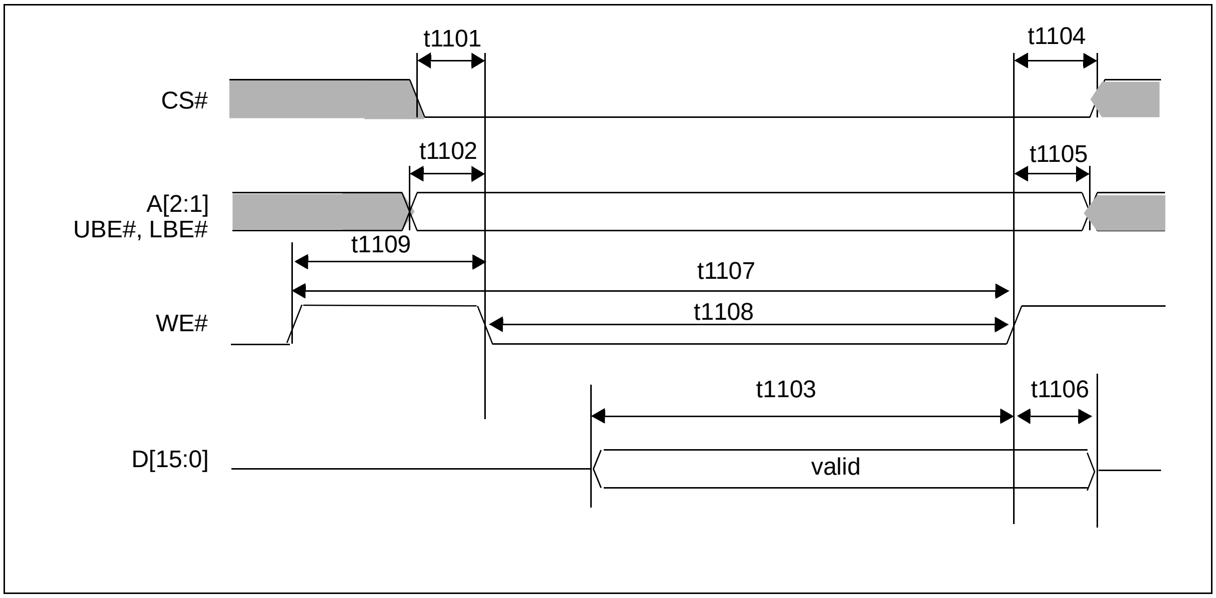

Figure 7-14: Indirect 80 Type 1 Interface Write Cycle Timing

Note
The Indirect 80 Type1 Interface only supports 16-bit access.

Table 7-27: Indirect 80 Type 1 Interface Write Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1101	CS# setup time	5	—	ns
t1102	A[2:1], UBE#, LBE# setup time	5	—	ns
t1103	D[15:0] setup time to WE# rising edge	15	—	ns
t1104	CS# hold time from WE# rising edge	4	—	ns
t1105	A[2:1], UBE#, LBE# hold time from WE# rising edge	4	—	ns
t1106	D[15:0] hold time from WE# rising edge	0	—	ns
t1107	WE# Cycle time	6	—	Ts
t1108	WE# pulse active time	4	—	Ts
t1109	WE# pulse inactive time	2	—	Ts

1. Ts = System Clock Period.

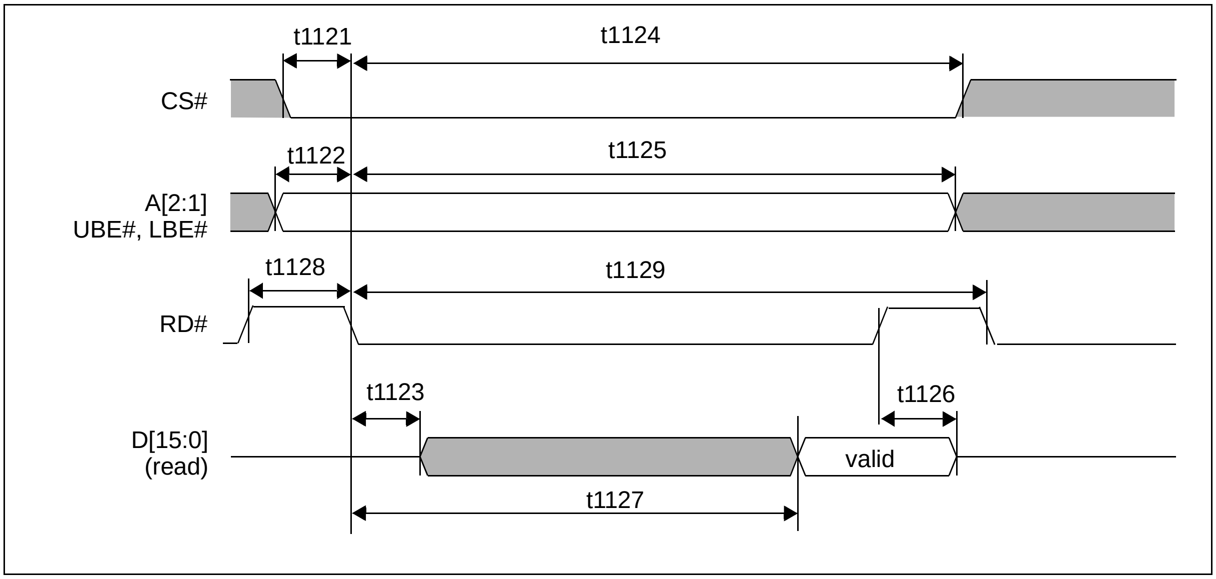

Figure 7-15: Indirect 80 Type 1 Interface Read Cycle Timing

Table 7-28: Indirect 80 Type 1 Interface Read Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1121	CS# setup time	Note2	—	ns
t1122	A[2:1], UBE#, LBE# setup time	Note2	—	ns
t1123	RD# falling edge to D[15:0] driven	4	—	ns
t1124	CS# hold time from RD# falling edge	20	—	ns
t1125	A[2:1], UBE#, LBE# hold time from RD# falling edge	20	—	ns
t1126	D[15:0] hold time from RD# rising edge	2	8	ns
t1127	RD# falling edge to valid Data if there are no internal delayed cycles	—	4Ts+19	ns
t1128	RD# pulse inactive time	8	—	ns
t1129	RD# cycle time	6	—	Ts

1. Ts = System Clock Period.
2. REG[0006h] bit 9
   When this bit = 0, t1121min/ t1122min = 5ns.
   When this bit = 1, t1121min/ t1122min = 0ns.

Table 7-29: Indirect 80 Type 1 Interface Truth Table

CS#	M/R#	A2	A1	WE#	RD#	UBE#	LBE#	Comments
0	0	0	0	1	0	0	0	Index register read
0	0	0	0	0	1	0	0	Index register write
0	0	0	1	1	0	0	0	Status register read
0	0	1	0	1	0	0	0	Data register read
0	0	1	0	0	1	0	0	Data register write

7.3.6 Indirect 80 Type 2

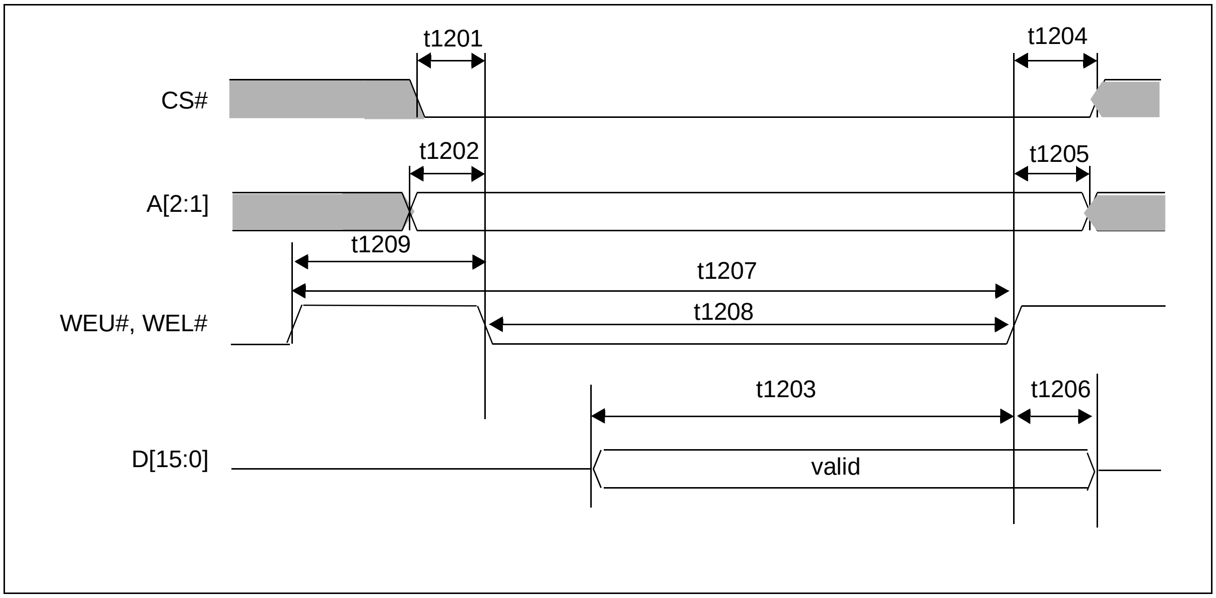

Figure 7-16: Indirect 80 Type 2 Interface Write Cycle Timing

Note
The Indirect 80 Type2 Interface only supports 16-bit access.

Table 7-30: Indirect 80 Type 2 Interface Write Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1201	CS# setup time	5	—	ns
t1202	A[2:1] setup time	5	—	ns
t1203	D[15:0] setup time to WEU#, WEL# rising edge	15	—	ns
t1204	CS# hold time from WEU#, WEL# rising edge	4	—	ns
t1205	A[2:1] hold time from WEU#, WEL# rising edge	4	—	ns
t1206	D[15:0] hold time from WEU#, WEL# rising edge	0	—	ns
t1207	WEU#, WEL# Cycle time	6	—	Ts
t1208	WEU#, WEL# pulse active time	4	—	Ts
t1209	WEU, WEL# pulse inactive time	2	—	Ts

1. Ts = System Clock Period.

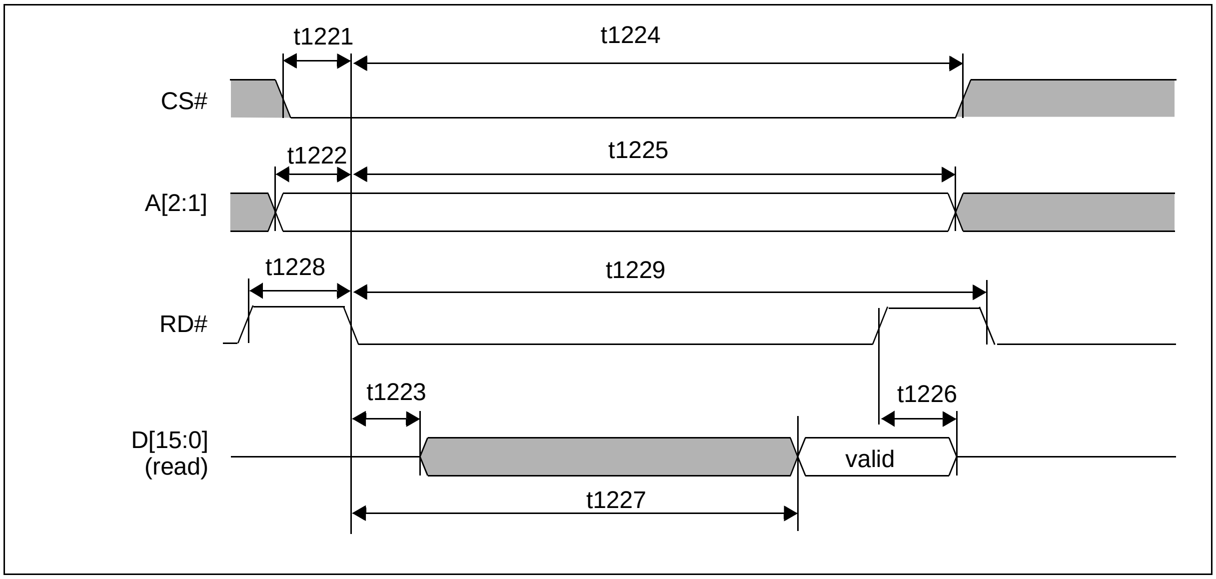

Figure 7-17: Indirect 80 Type 2 Interface Read Cycle Timing

Table 7-31: Indirect 80 Type 2 Interface Read Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1221	CS# setup time	Note2	—	ns
t1222	A[2:1] setup time	Note2	—	ns
t1223	RD# falling edge to D[15:0] driven	4	—	ns
t1224	CS# hold time from RD# falling edge	20	—	ns
t1225	A[2:1] hold time from RD# falling edge	20	—	ns
t1226	D[15:0] hold time from RD# rising edge	2	8	ns
t1227	RD# falling edge to valid Data if there are no internal delayed cycles	—	4Ts+19	ns
t1228	RD# pulse inactive time	8	—	ns
t1229	RD# cycle time	6	—	Ts

1. Ts = System Clock Period.
2. REG[0006h] bit 9
   When this bit = 0, t1221min/ t1222min = 5ns.
   When this bit = 1, t1221min/ t1222min = 0ns.

Table 7-32: Indirect 80 Type 2 Interface Truth Table

CS#	M/R#	A2	A1	WEU#	WEL#	RD#	Comments
0	0	0	0	1	1	0	Index register read
0	0	0	0	0	0	1	Index register write
0	0	0	1	1	1	0	Status register read
0	0	1	0	1	1	0	Data register read
0	0	1	0	0	0	1	Data register write

7.3.7 Indirect 80 Type 3

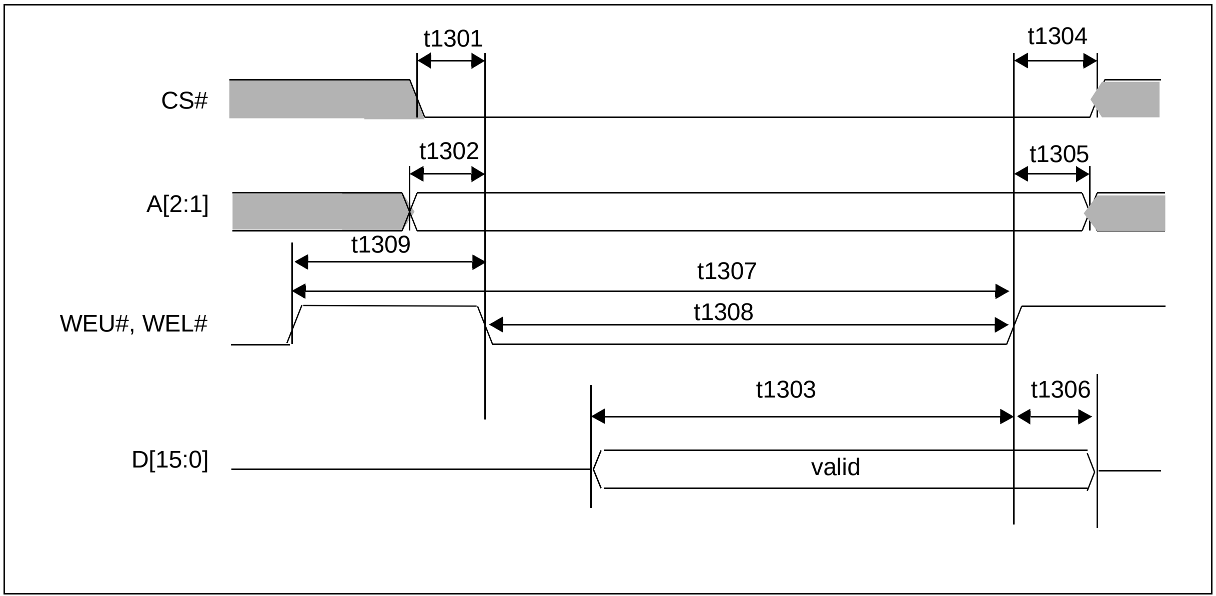

Figure 7-18: Indirect 80 Type 3 Interface Write Cycle Timing

Note
The Indirect 80 Type3 Interface only supports 16-bit access.

Table 7-33: Indirect 80 Type 3 Interface Write Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1301	CS# setup time	5	—	ns
t1302	A[2:1] setup time	5	—	ns
t1303	D[15:0] setup time to WEU#,WEL# rising edge	15	—	ns
t1304	CS# hold time from WEU#,WEL# rising edge	4	—	ns
t1305	A[2:1] hold time from WEU#, WEL# rising edge	4	—	ns
t1306	D[15:0] hold time from WEU#, WEL# rising edge	0	—	ns
t1307	WEU#, WEL# Cycle time	6	—	Ts
t1308	WEU#,WEL# pulse active time	4	—	Ts
t1309	WEU,WEL# pulse inactive time	2	—	Ts

1. Ts = System Clock Period.

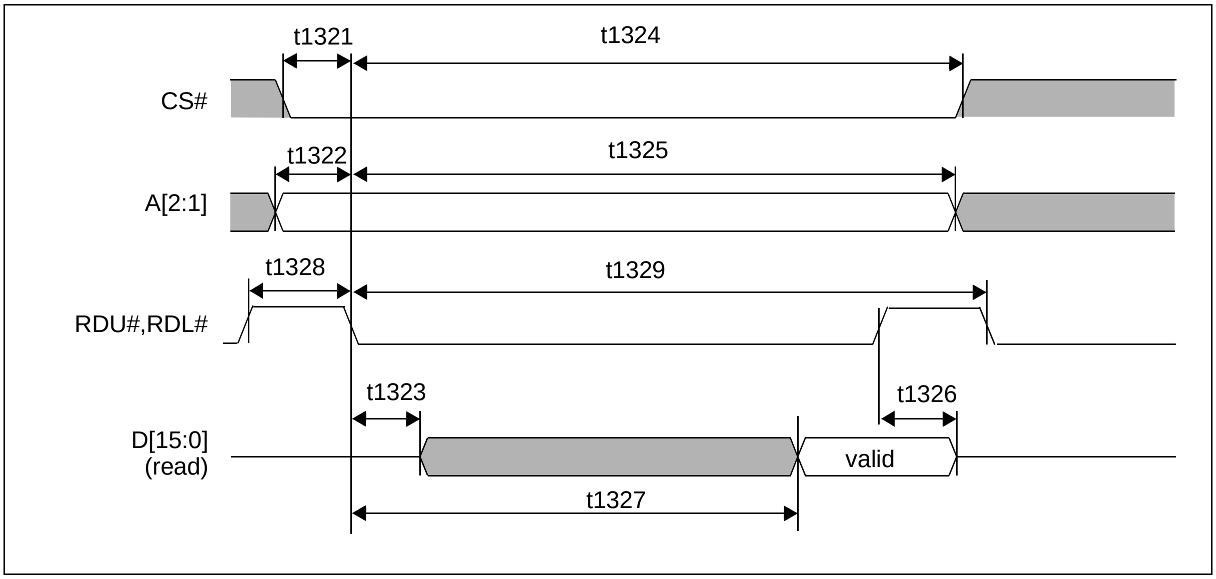

Figure 7-19: Indirect 80 Type 3 Interface Read Cycle Timing

Table 7-34: Indirect 80 Type 3 Interface Read Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	**Max**	
t1321	CS# setup time	Note2	—	ns
t1322	A[2:1] setup time	Note2	—	ns
t1323	RDU,RDL# falling edge to D[15:0] driven	4	—	ns
t1324	CS# hold time from RDU#,RDL# falling edge	20	—	ns
t1325	A[2:1] hold time from RDU#,RDL# falling edge	20	—	ns
t1326	D[15:0] hold time from RDU#,RDL# rising edge	2	8	ns
t1327	RDU#,RDL# falling edge to valid Data if there are no internal delayed cycles	—	4Ts+19	ns
t1328	RDU#,RDL# pulse inactive time	8	—	ns
t1329	RDU#,RDL# cycle time	6	—	Ts

1. Ts = System Clock Period.
2. REG[0006h] bit 9
   When this bit = 0, t1321min/ t1322min = 5ns.
   When this bit = 1, t1321min/ t1322min = 0ns.

Table 7-35: Indirect 80 Type 3 Interface Truth Table

CS#	M/R#	A2	A1	WEU#	WEL#	RDU#	RDL#	Comments
0	0	0	0	1	1	0	0	Index register read
0	0	0	0	0	0	1	1	Index register write
0	0	0	1	1	1	0	0	Status register read
0	0	1	0	1	1	0	0	Data register read
0	0	1	0	0	0	1	1	Data register write

7.3.8 Indirect 68

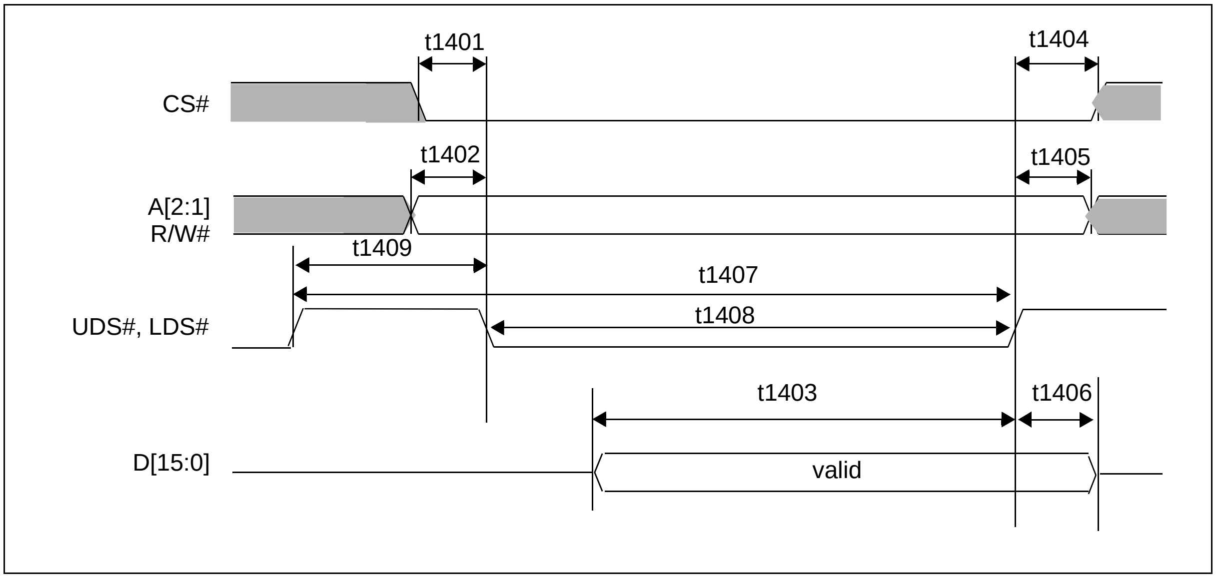

Figure 7-20: Indirect 68 Interface Write Cycle Timing

Note
The Indirect 68 Interface only supports 16-bit access.

Table 7-36: Indirect 68 Interface Write Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1401	CS# setup time	5	—	ns
t1402	A[2:1], R/W# setup time	5	—	ns
t1403	D[15:0] setup time to UDS#,LDS# rising edge	15	—	ns
t1404	CS# hold time from UDS#,LDS# rising edge	4	—	ns
t1405	A[2:1], R/W# hold time from UDS#,LDS# rising edge	4	—	ns
t1406	D[15:0] hold time from UDS#,LDS# rising edge	0	—	ns
t1407	UDS#,LDS# cycle time	6	—	Ts
t1408	UDS#,LDS# pulse active time	4	—	Ts
t1409	UDS#,LDS# pulse inactive time	2	—	Ts

1. Ts = System Clock Period.

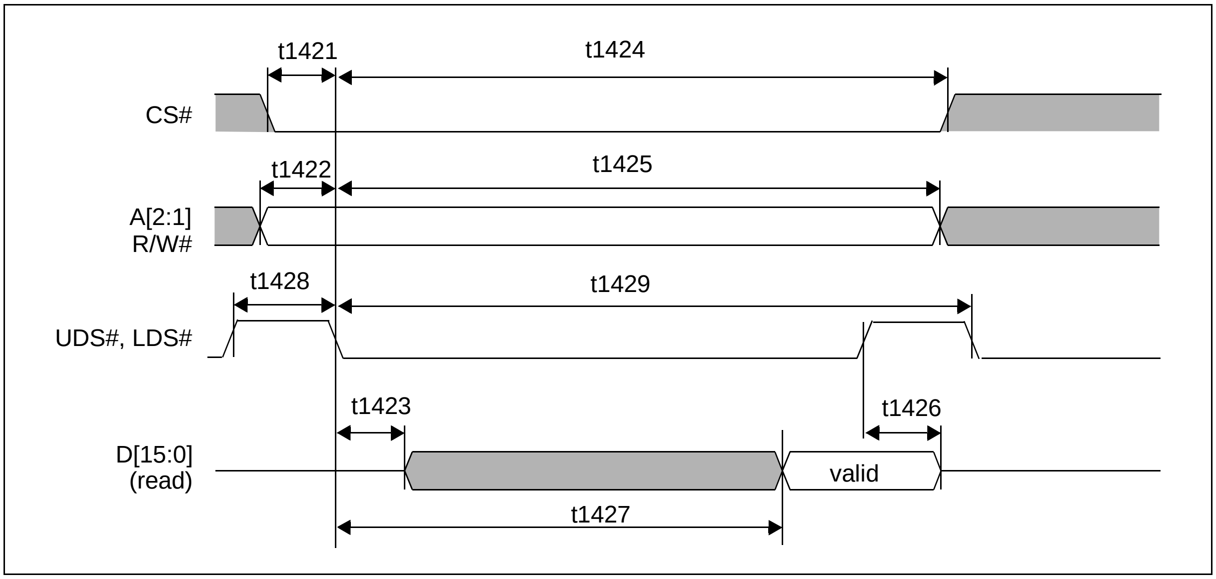

Figure 7-21: Indirect 68 Interface Read Cycle Timing

Table 7-37: Indirect 68 Interface Read Cycle Timing

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1421	CS# setup time	Note2	—	ns
t1422	A[2:1], R/W# setup time	Note2	—	ns
t1423	UDS#, LDS# falling edge to D[15:0] driven	4	—	ns
t1424	CS# hold time from UDS#, LDS# falling edge	20	—	ns
t1425	A[2:1], R/W# hold time from UDS#, LDS# falling edge	20	—	ns
t1426	D[15:0] hold time from UDS#, LDS# rising edge	2	8	ns
t1427	UDS#, LDS# falling edge to valid Data if there are no internal delayed cycles	—	4Ts+17	ns
t1428	UDS#, LDS# pulse inactive time	8	—	ns
t1429	UDS#, LDS# cycle time	6	—	Ts

1. Ts = System Clock Period.
2. REG[0006h] bit 9
   When this bit = 0, t1421min/ t1422min = 5ns.
   When this bit = 1, t1421min/ t1422min = 0ns.

Table 7-38: Indirect 68 Interface Truth Table

CS#	M/R#	A2	A1	R/W#	UDS#	LDS#	Comments
0	0	0	0	1	0	0	Index register read
0	0	0	0	0	0	0	Index register write
0	0	0	1	1	0	0	Status register read
0	0	1	0	1	0	0	Data register read
0	0	1	0	0	0	0	Data register write

7.3.9 LCD Bypass Mode

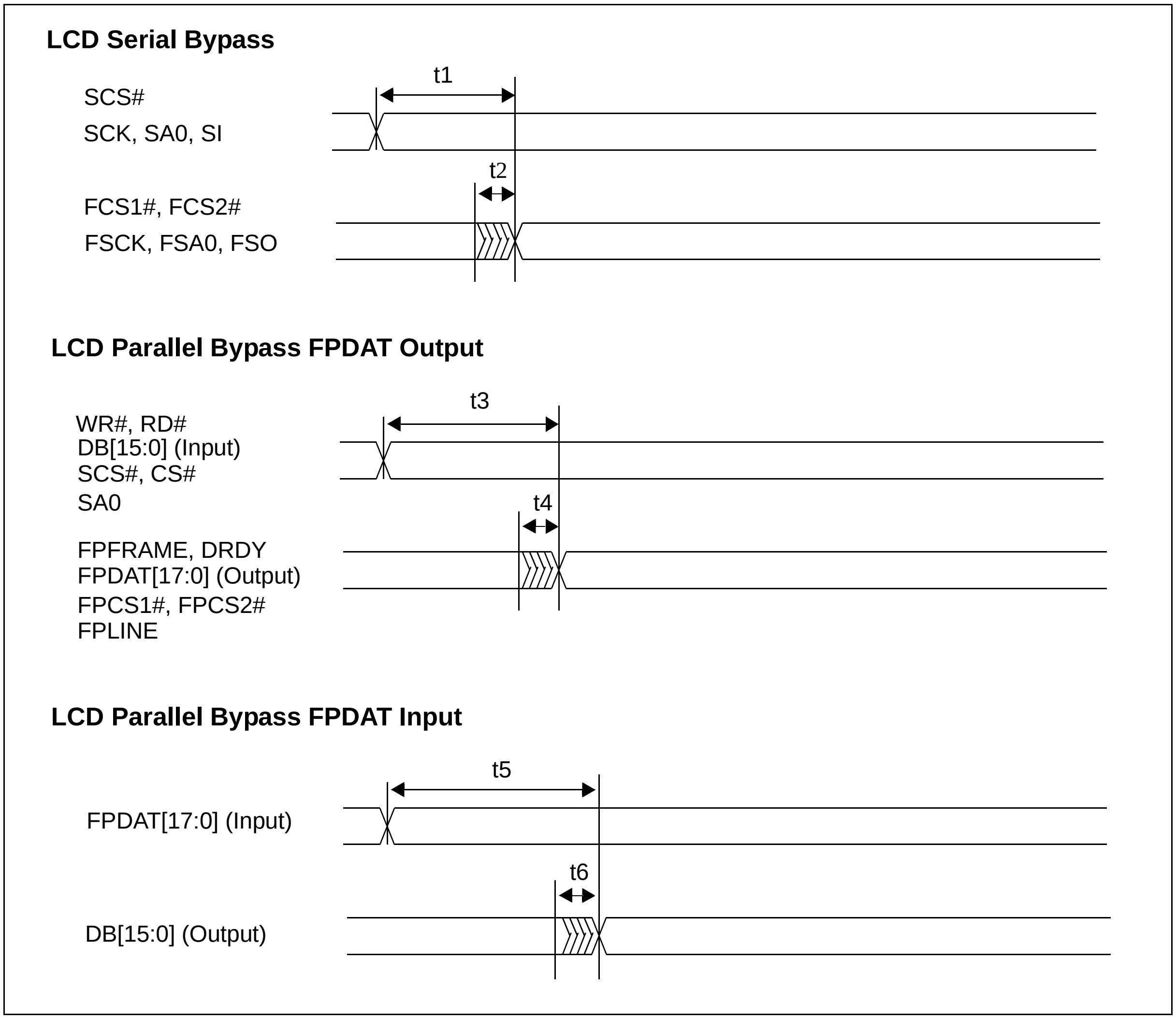

Figure 7-22: LCD Bypass Mode Timing

Table 7-39: LCD Bypass Mode Timing

Symbol	Parameter	Min	Max	Units
t1	LCD serial bypass delay time	3	15	ns
t2	LCD serial bypass stable time	—	4	ns
t3	LCD parallel output bypass delay time	3	20	ns
t4	LCD parallel output bypass stable time	—	5	ns
t5	LCD parallel input bypass delay time	3	20	ns
t6	LCD parallel input bypass stable time	—	4	ns

Table 7-40: LCD Bypass Mode Truth Table

CNF4, 2	WR#	RD#	BE1#	BE0#	Write	Read	Comments
10b	0	—	—	—	Valid	—	80 Type 1 Write
10b	—	0	—	—	—	Valid	80 Type 1 Read
00b	—	—	0	0	Valid	—	80 Type 2 Write
00b	—	0	—	—	—	Valid	80 Type 2 Read
01b	0	—	—	0	Valid	—	80 Type 3 Write
01b	—	0	0	—	—	Valid	80 Type 3 Read
11b	0	—	0	0	Valid	—	68 Write
11b	1	—	0	0	—	Valid	68 Read

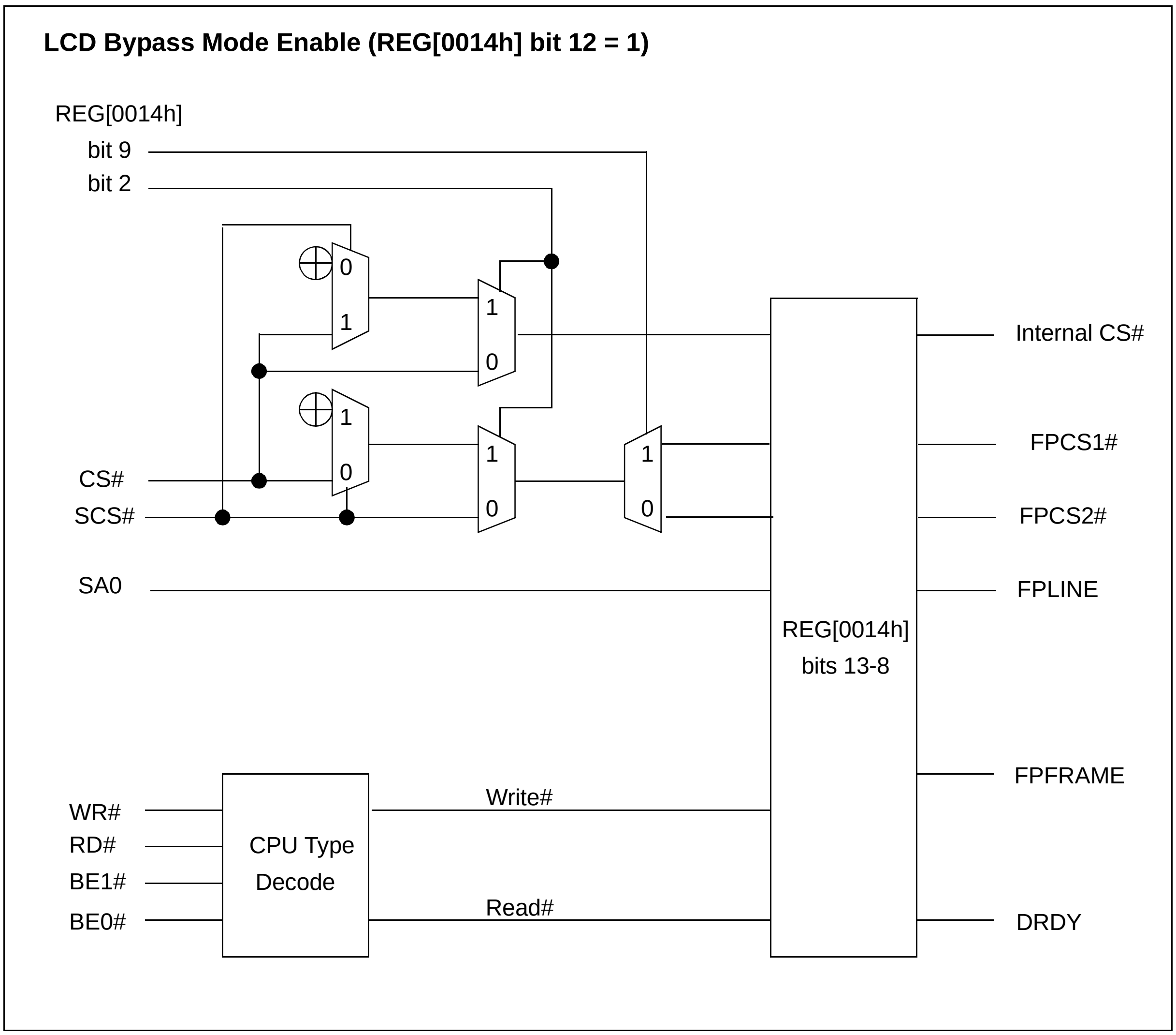

Figure 7-23: LCD Bypass Mode Logic Diagram

7.4 Panel Interface Timing

7.4.1 Generic TFT Panel Timing

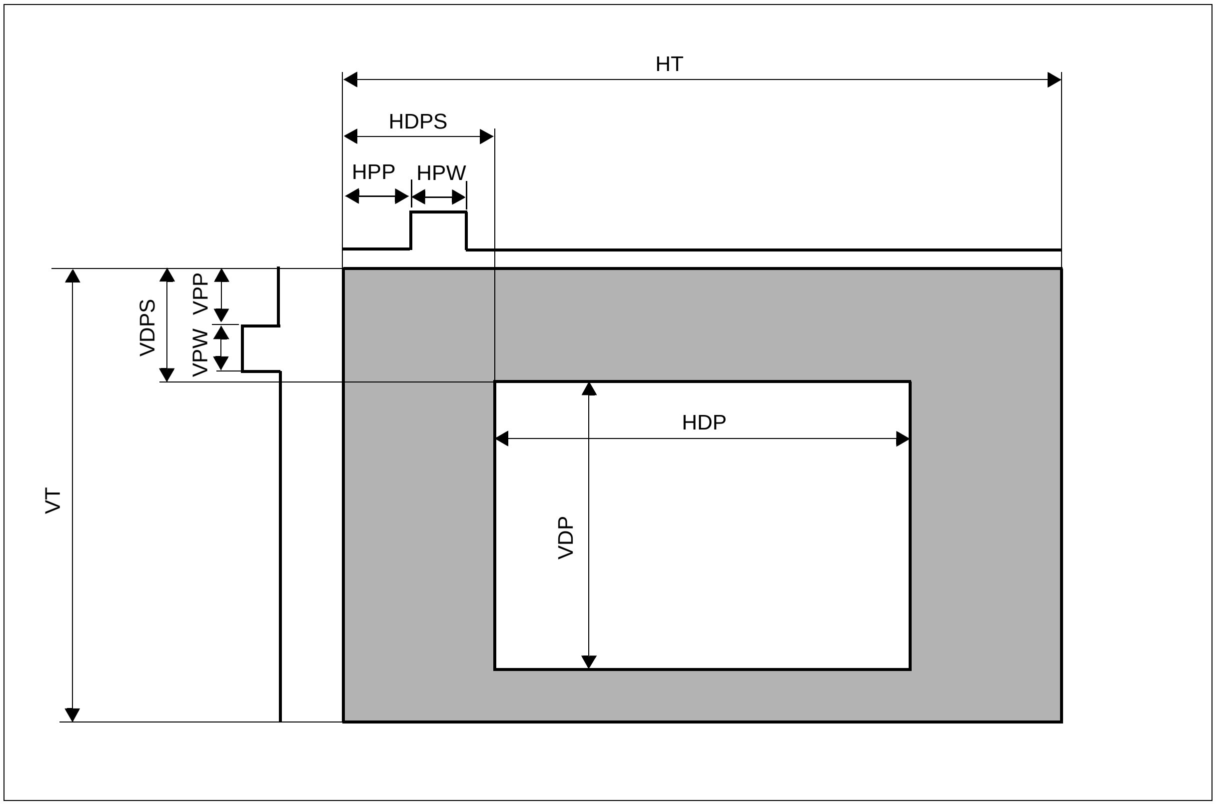

Figure 7-24: Generic TFT Panel Timing

Table 7-41: Generic TFT Panel Timing

Symbol	Description	Derived From	Units
HT	LCD1 Horizontal total	((REG[0040h] bits 6-0) + 1) x 8	
HDP	LCD1 Display Period	((REG[0042h] bits 8-0) + 1) x 2	
HDPS	LCD1 Horizontal Display Period Start Position	((REG[0044h] bits 9-0) + 9	Ts
HPW	LCD1 FPLINE Pulse Width	(REG[0046h] bits 6-0) + 1	
HPP	LCD1 FPLINE Pulse Position (see note 2)	(REG[0048h] bits 9-0) + 1	
VT	LCD1 Vertical Total	(REG[004Ah] bits 9-0) + 1	
VDP	LCD1 Vertical Display Period	(REG[004Ch] bits 9-0) + 1	
VDPS	LCD1 Vertical Display Period Start Position	REG[004Eh] bits 9-0	Lines
VPW	LCD1 FPFRAME Pulse Width	(REG[50h] bits 2-0) + 1	
VPP	LCD1 FPFRAME Pulse Position (see note 2)	REG[0052h] bits 9-0	

1. The following formulas must be valid for all panel timings:
   HDPS + HDP < HT
   VDPS + VDP < VT
2. For generic TFT panel types, the HPP value must be programmed to 1 and the VPP value must be programmed to 0. These values may be used to configure extended TFT types as required.

Generic RGB Type Interface Panel Horizontal Timing

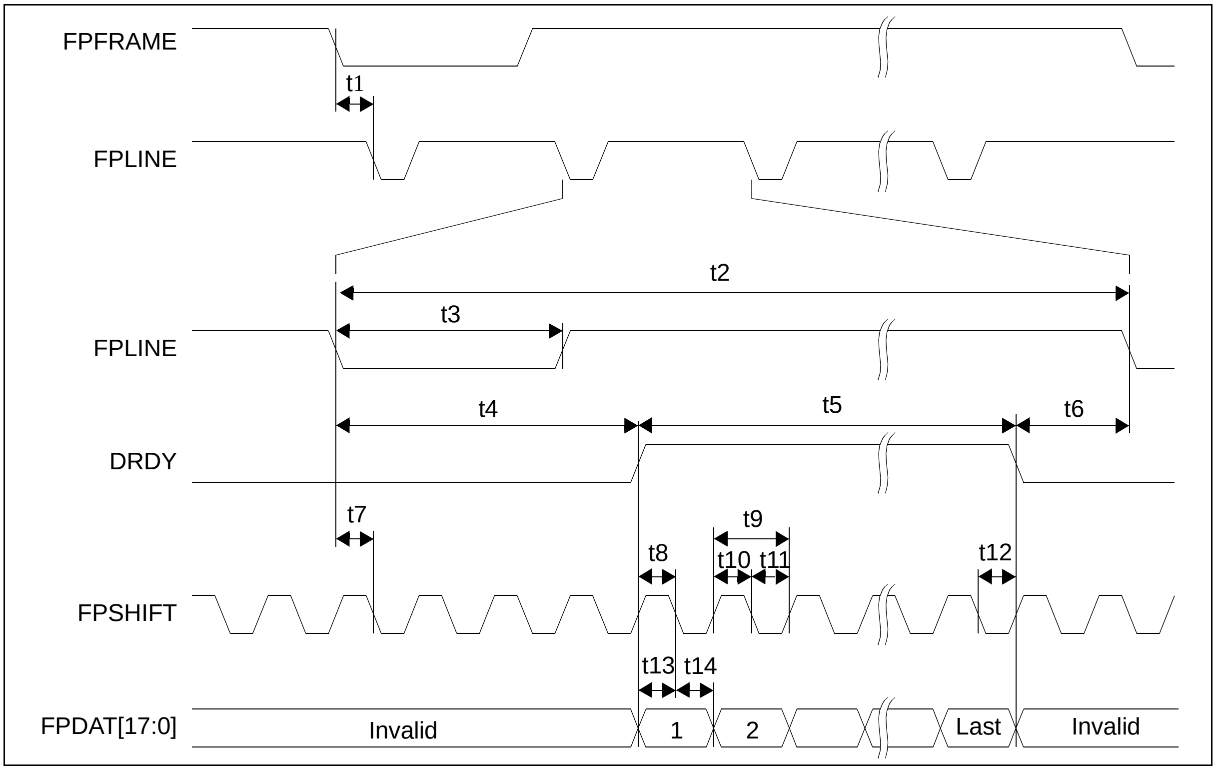

Figure 7-25: Generic RGB Type Interface Panel Horizontal Timing

Table 7-42: Generic RGB Type Interface Panel Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME falling edge to FPLINE falling edge	—	HPP (note 2)	—	Ts (note 1)
t2	Horizontal total period	—	HT	—	Ts
t3	FPLINE pulse width	—	HPW	—	Ts
t4	FPLINE falling edge to DRDY active	—	HDPS	—	Ts
t5	Horizontal display period	—	HDP	—	Ts
t6	DRDY falling edge to FPLINE falling edge	—	note 3	—	Ts
t7	FPLINE setup time to FPSHIFT falling edge	—	0.5	—	Ts
t8	DRDY setup to FPSHIFT falling edge	—	0.5	—	Ts
t9	FPSHIFT period	—	1	—	Ts
t10	FPSHIFT pulse width high	—	0.5	—	Ts
t11	FPSHIFT pulse width low	—	0.5	—	Ts
t12	DRDY hold from FPSHIFT falling edge	—	0.5	—	Ts
t13	Data setup to FPSHIFT falling edge	—	0.5	—	Ts
t14	Data hold from FPSHIFT falling edge	—	0.5	—	Ts

1. Ts = pixel clock period
2. For generic TFT panel types, the HPP value must be programmed to 1 and the VPP value must be programmed to 0. This values may be used to configure extended TFT types as required.
3. t6typ = t2 - t4 - t5

Note

The Generic TFT timings are based on the following:

FPFRAME Pulse Polarity bit is active low (REG[0050h] bit 7 = 0).

FPLINE Pulse Polarity bit is active low (REG[0046h] bit 7 = 0).

Generic RGB Type Interface Panel Vertical Timing

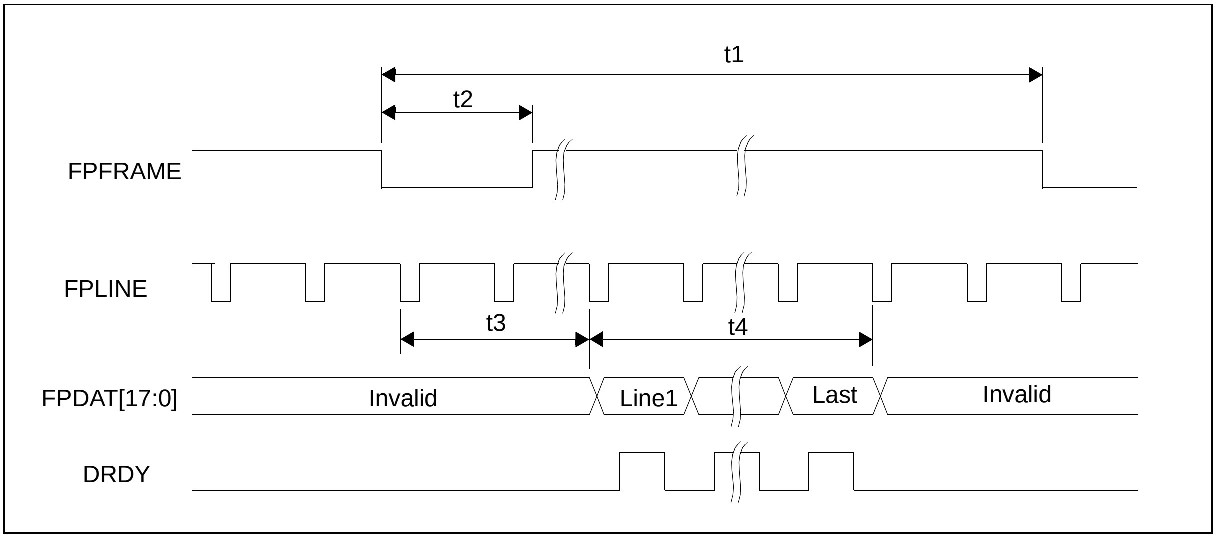

Figure 7-26: Generic RGB Type Interface Panel Vertical timing

Table 7-43: Generic RGB Type Interface Panel Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Vertical total period	—	VT	—	Line
t2	FPFRAME pulse width	—	VPW	—	Line
t3	Vertical display start position (note 1)	—	note 2	—	Line
t4	Vertical display period	—	VDP	—	Line

1. t3 is measured from the first FPLINE pulse at the start of the frame to the last FPLINE pulse before FPDAT is valid.
2. t3typ = VDPS - VPP (For generic TFT panel types, the VPP value must be programmed to 0. This value may be used to configure extended TFT types as required.

7.4.2 HR-TFT Panel Timing

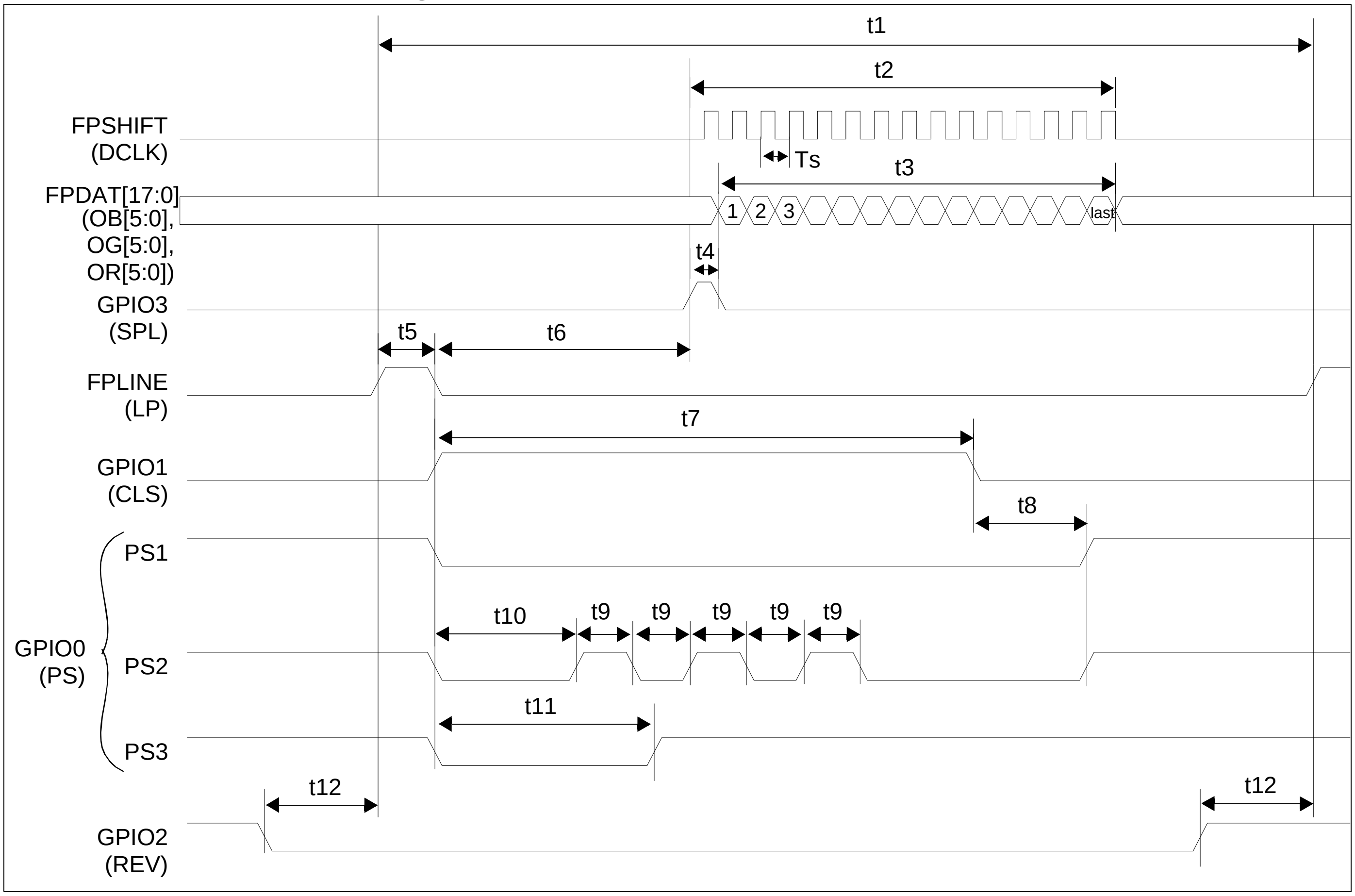

Figure 7-27: HR-TFT Panel Horizontal Timing

Table 7-44: HR-TFT Panel Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Horizontal total period	8	Note 2	1024	Ts (note 1)
t2	FPSHIFT active	9	Note 3	1025	Ts
t3	Horizontal display period	8	Note 4	1024	Ts
t4	GPIO3 pulse width	—	1	—	Ts
t5	FPLINE pulse width	1	Note 5	128	Ts
t6	FPLINE falling edge to GPIO3 rising edge	2	Note 6	—	Ts
t7	GPIO1 pulse width	1	Note 7	511	Ts
t8	GPIO1 falling edge to GPIO0 (PS1) rising edge	0	Note 8	63	Ts
t9	GPIO0 (PS2) toggle width	1	Note 9	127	Ts
t10	GPIO0 (PS2) first falling edge to GPIO0 (PS2) first rising edge	1	Note 10	255	Ts
t11	GPIO0 (PS3) pulse width	1	Note 11	127	Ts
t12	GPIO2 (REV) toggle position to FPLINE rising edge	1	Note 12	31	Ts

1. Ts = pixel clock period
2. t1typ = [(REG[0040h] bits 6-0) + 1] * 8
3. t2typ = [((REG[0042h] bits 8-0) + 1) * 2] + 1
4. t3typ = [(REG[0042h] bits 8-0) + 1] * 2

5. t5typ = (REG[0046h] bits 6-0) + 1
6. t6typ = REG[0044h] bits 9-0 - REG[0046h] bits 6-0 + 2
7. t7typ = (REG[0092h] bits 8-0) > 0
8. t8typ = (REG[0094h] bits 5-0)
9. t9typ = (REG[0098h] bits 6-0) > 0
10. t10typ = (REG[0096h] bits 7-0) > 0
11. t11typ = (REG[009Ah] bits 6-0) > 0
12. t12typ = REG[009Eh] bits 4-0

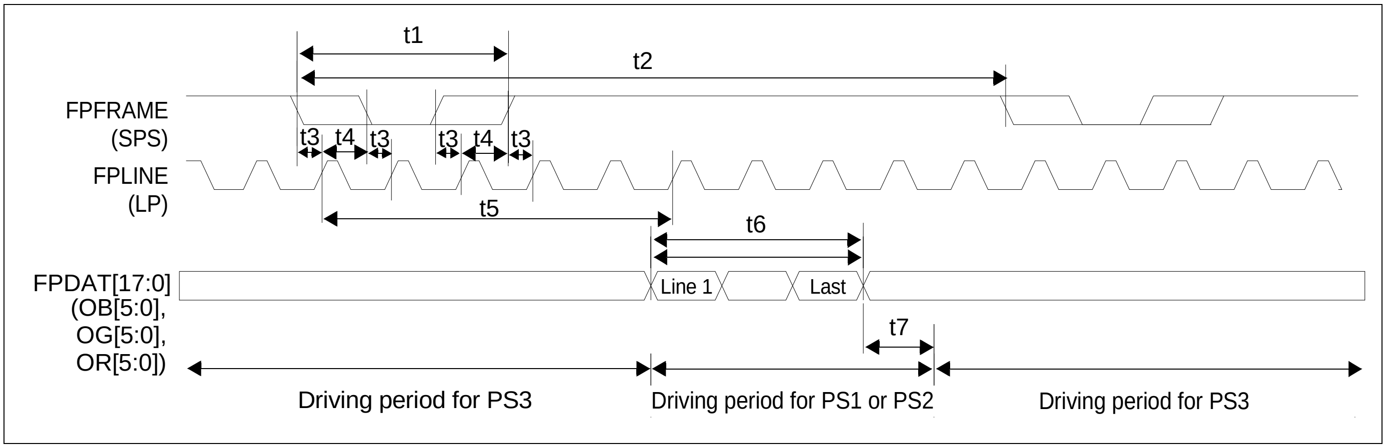

Figure 7-28: HR-TFT Panel Vertical Timing

Table 7-45: HR-TFT Panel Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME pulse width	1	Note 2	8	Lines
t2	Vertical total period	1	Note 3	1024	Lines
t3	FPFRAME rising/falling edge to FPLINE rising edge	—	1 (Note 4)	—	Ts (Note 1)
t4	FPLINE rising edge to FPFRAME rising/falling edge	0	Note 4	1023	Ts
t5	Vertical display start position	0	Note 5	1023	Lines
t6	Vertical display period	1	Note 6	1024	Lines
t7	Extra driving period for PS1/2	0	Note 7	7	Lines

1. Ts = pixel clock period
2. t1typ = (REG[0050h] bits 2-0) + 1
3. t2typ = (REG[004Ah] bits 9-0) + 1
4. t3typ The FPFRAME (SPS) rising/falling edge can occur before or after FPLINE (LP) rising edge depending on the value stored in the FPLINE Pulse Start Position bits (REG[0048h] bits 9-0). To obtain the case indicated by t3, set the FPLINE Pulse Start Position bits to 0 and the FPFRAME (SPS) rising/falling edge will occur 1 Ts before the FPLINE (LP) rising edge. To obtain the case indicated by t4, set the FPLINE Pulse Start Position bits to a value between 1 and the Horizontal Total - 1. Then t4 = (Horizontal Total Period - 1) - (REG[0048h] bits 9-0)
5. When REG[0048h] bits 9-0 > 4, t5typ = REG[004Eh] bits 9-0 - REG[0052h] bits 9-0
   When 0 ≤ REG[0048h] bits 9-0 ≤ 4, t5typ = REG[004Eh] bits 9-0 - REG[0052h] bits 9-0 + 1
6. t6typ = (REG[004Ch] bits 9-0) + 1
7. t7typ = (REG[00A0h] bits 2-0)

7.4.3 Casio TFT Panel Timing

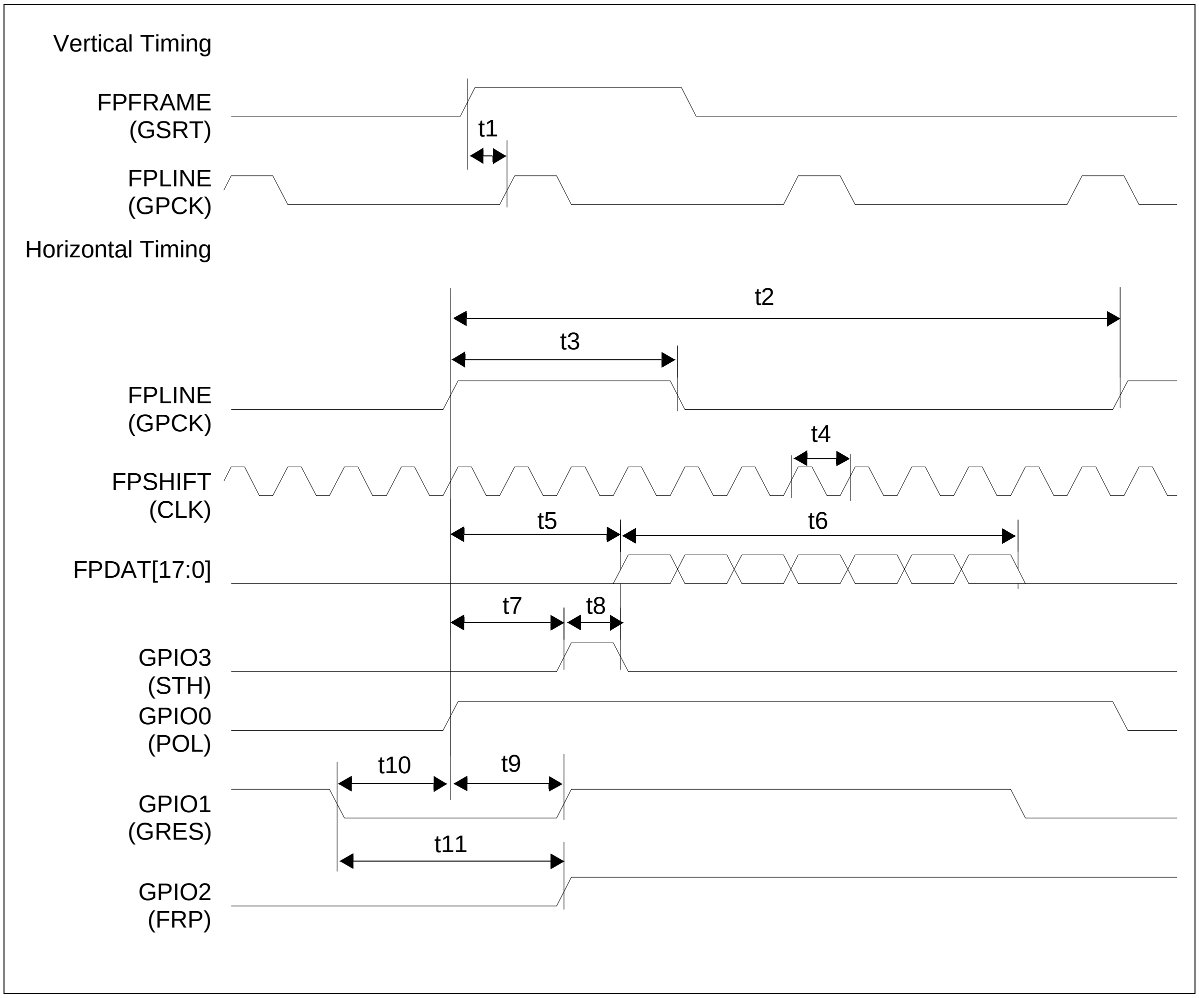

Figure 7-29: Casio TFT Horizontal Timing

Table 7-46: Casio TFT Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Horizontal pulse start position	1	Note 2	1024	Ts
t2	Horizontal total	8	Note 3	1024	Ts
t3	Horizontal pulse width	1	Note 4	128	Ts
t4	Pixel clock period	—	Note 5	—	Ts (Note 1)
t5	Horizontal display period start position	4	Note 6	1027	Ts
t6	Horizontal display period	8	Note 7	1024	Ts
t7	FPLINE rising edge to GPIO3 rising edge	0	Note 8	63	Ts
t8	GPIO3 pulse width	—	1	—	Ts
t9	FPLINE rising edge to GPIO1 rising edge	0	Note 9	63	Ts
t10	GPOIO1 falling edge to FPLINE rising edge	1	Note 10	64	Ts
t11	FPLINE falling edge to GPIO2 toggle point	0	Note 11	127	Ts

1. Ts = Pixel clock period
2. t1typ = [(REG[0048h] bits 9-0) + 1)

3. t2typ = [(REG[0040h] bits 6-0) + 1) * 8
4. t3typ = [(REG[0046h] bits 6-0) + 1
5. t4typ = depends on the pixel clock (PCLK)
6. t5typ = (REG[0044h] bits 9-0) + 4
7. t6typ = [(REG[0042h] bits 8-0) + 1] * 2
8. t7typ = (REG[00A6h] bits 13-8)
9. t9typ = (REG[00A4h] bits 5-0)
10. t10typ = (REG[00A4h] bits 13-8)+1
11. t11typ = (REG[00A6h] bits 6-0)

Note

For Casio Panels set the following:
FPFRAME Pulse Polarity bit to active high (REG[0050h] bit 8 = 1).
FPLINE Pulse Polarity bit to active high (REG[0046h] bit 8 = 1).

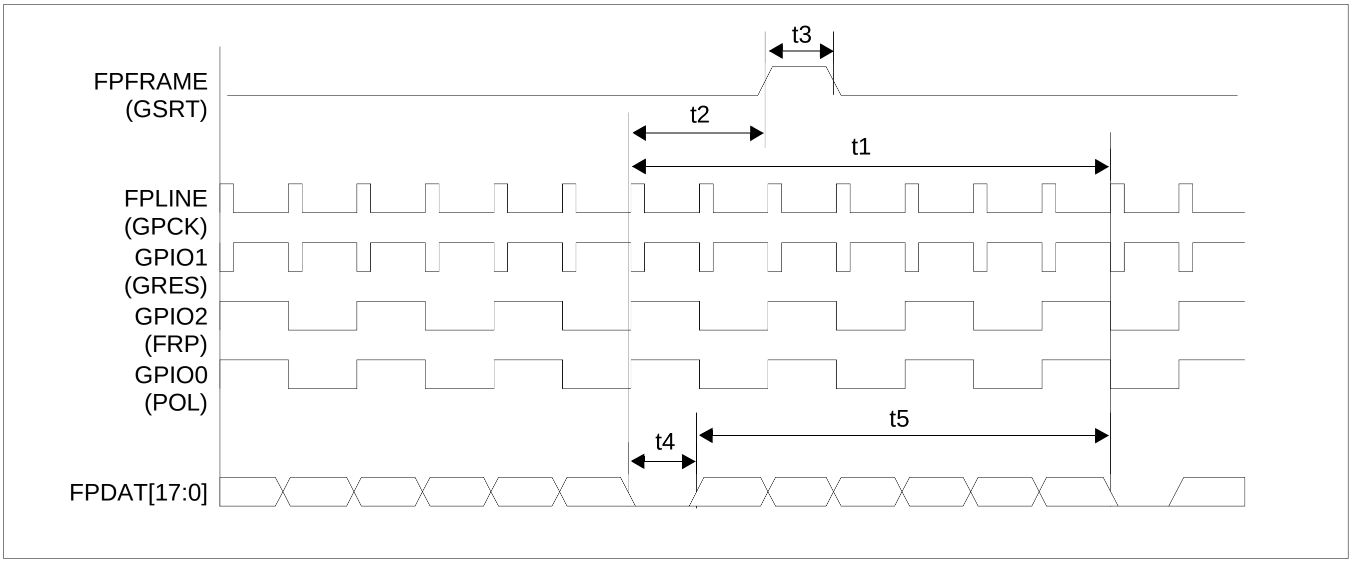

Figure 7-30: Casio TFT Vertical Timing

Table 7-47: Casio TFT Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Vertical total	1	Note 1	1024	Lines
t2	Vertical pulse start	0	Note 2	1023	Lines
t3	Vertical pulse width	1	Note 3	8	Lines
t4	Vertical display period start position	1	Note 4	1024	Lines
t5	Vertical display period	1	Note 5	1024	Lines

1. t1typ = (REG[004Ah] bits 9-0) + 1
2. t2typ = (REG[0052h] bits 9-0) -1
3. t3typ = (REG[0050h] bits 2-0) + 1
4. t4typ = (REG[004Eh] bits 9-0) +1
5. t5typ = (REG[004Ch] bits 9-0) + 1
6. t2 < t4

7.4.4 α-TFT Panel Timing

Note
REG[0044h] bits 9-0 must be set to zero when using the a-TFT panel.

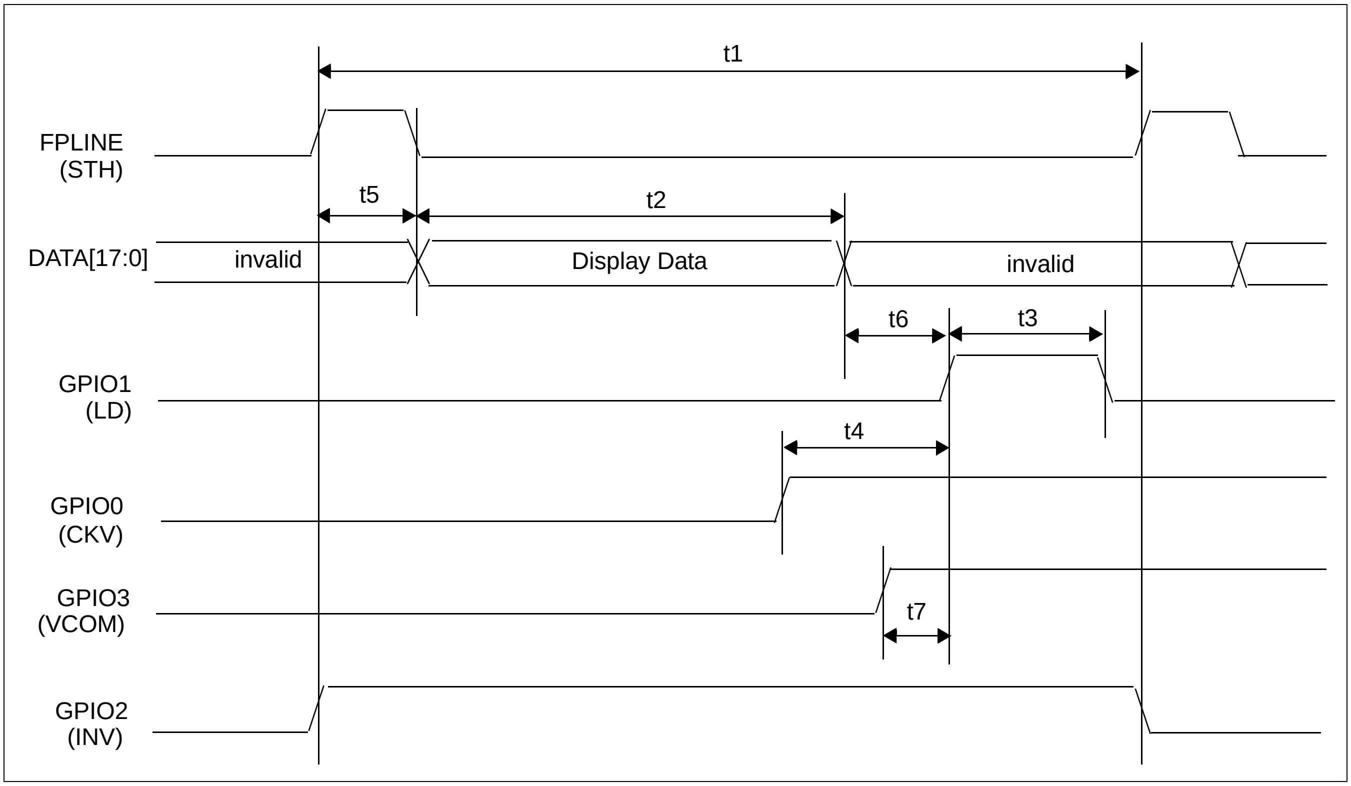

Figure 7-31: α-TFT Panel Horizontal Timing

Table 7-48: α-TFT Panel Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Horizontal total period	—	282 (Note 2)	1024	Ts (Note 1)
t2	Horizontal Display period	—	240 (Note 3)	1014	Ts
t3	GPIO1 (LD) pulse width	1	4 (Note 4)	8	Ts
t4	GPIO0 (CKV) rise edge position	0	28 (Note 5)	127	Ts
t5	FPLINE (STH) pulse width	1	1 (Note 6)	8	Ts
t6	GPIO1 (LD) rising edge	0	1 (Note 7)	3	Ts
t7	GPIO3 (VCOM) rising edge position	0	11 (Note 8)	63	Ts

1. Ts = pixel clock period
2. t1typ = REG[0080h] bits 9-0 + 1

3. t2typ = (REG[0042h] bits 8-0 + 1) x 2
4. t3typ = REG[0088h] bits 10-8 + 1
5. t4typ = t2 + t5 + t6 - (REG[0084h] bits 9-0) + 8
6. t5typ = REG[0088h] bits 2-0 + 1
7. t6typ = (REG[0082h] bits 9-0) - t2 - t5 - 8
8. t7typ = t2 + t5 + t6 - (REG[0086h] bits 9-0) + 8

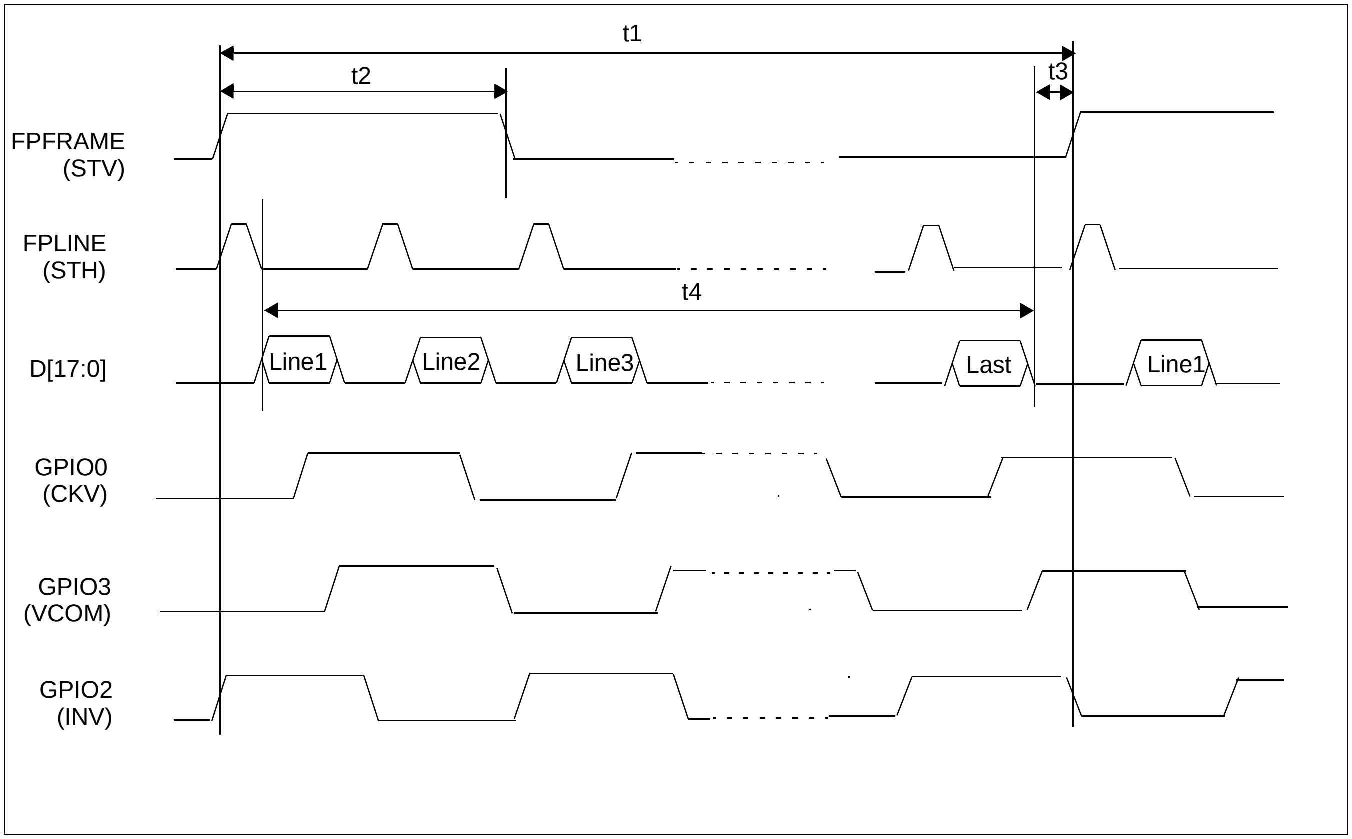

Figure 7-32: α–TFT Panel Vertical Timing

Table 7-49: α–TFT Panel Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Vertical total period	—	327 (Note 1)	1024	Lines
t2	FPFRAME (STV) pulse width	1	2 (Note 2)	—	Lines
t3	FPFRAME Hold Lines	1	7 (Note 3)	—	Lines
t4	Vertical display period	—	320 (Note 4)	1022	Lines

1. t1typ = REG[004Ah] bits 9-0 + 1
2. t2typ = REG[0050h] bits 2-0 + 1
3. t3typ = t1 - t4
4. t4typ = REG[004Ch] bits 9-0 + 1

7.4.5 TFT Type 2 Panel Timing

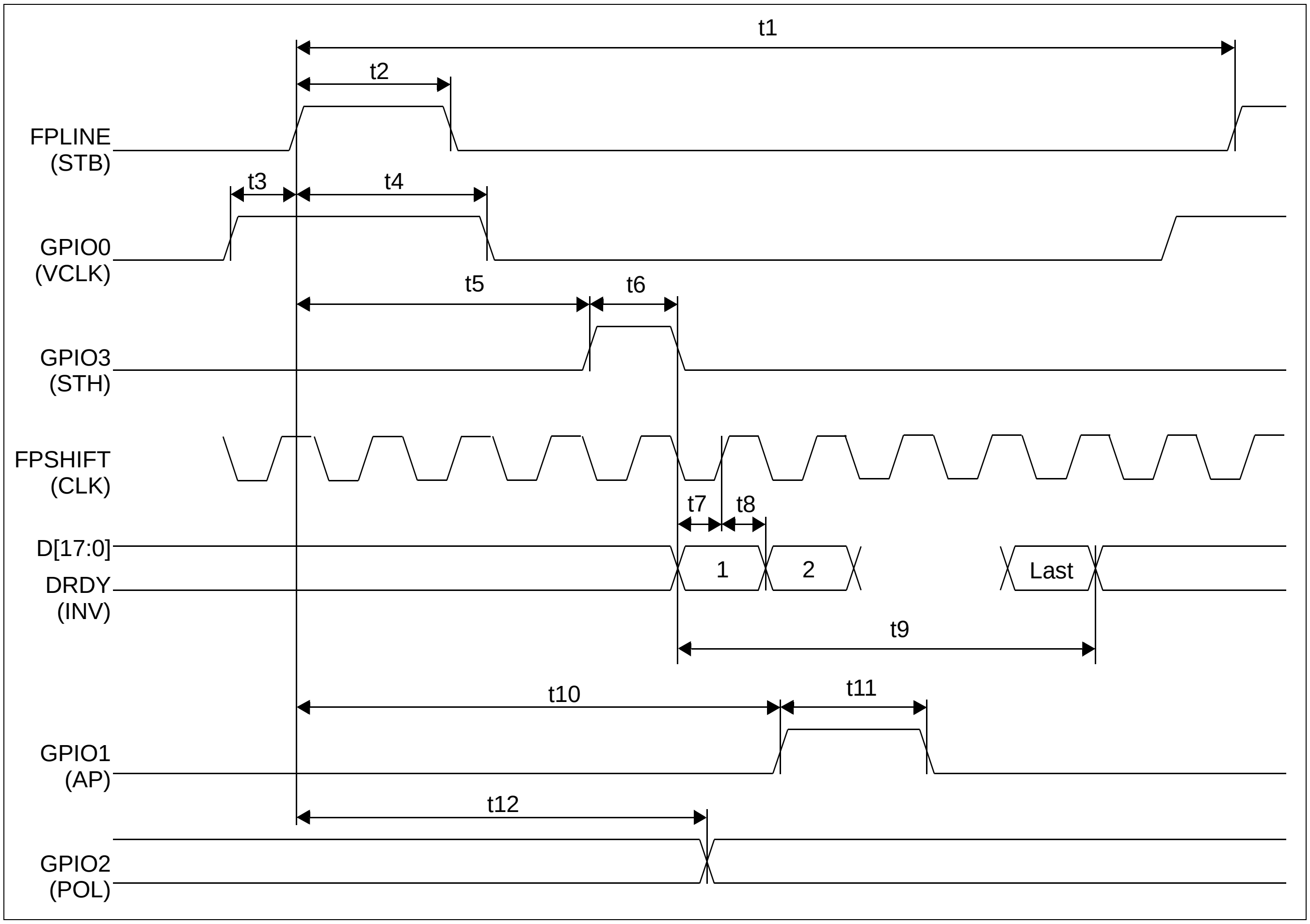

Figure 7-33: TFT Type 2 Horizontal Timing

Table 7-50: TFT Type 2 Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Horizontal total period	16	Note 2	1024	Ts (Note 1)
t2	FPLINE pulse width	—	5	—	Ts
t3	GPIO0 rising edge to FPLINE rising edge	7	Note 3	16	Ts
t4	FPLINE rising edge to GPIO0 falling edge	7	Note 4	16	Ts
t5	FPLINE rising edge to GPIO3 rising edge	—	Note 5	—	Lines
t6	GPIO3 pulse width	—	1	—	Ts
t7	Data setup time	0.5		—	Ts
t8	Data hold time	0.5		—	Ts
t9	Horizontal display period	8	Note 6	1024	Ts
t10	FPLINE rising edge to GPIO1 rising edge	40	Note 7	90	Ts
t11	GPIO1 pulse width	20	Note 8	270	Ts
t12	FPLINE rising edge to GPIO2 toggle position	—	10	—	Ts

1. Ts = pixel clock period
2. t1typ = (REG[0040h] bits 6-0 + 1) x 8
3. t3typ = Selected from 7, 9, 12 or 16 Ts using REG[00A2h bits 1-0
4. t4typ = Selected from 7, 9, 12 or 16 Ts using REG[00A2h] bits 4-3
5. t5typ = REG[0044h] bits 9-0 + 3
6. t9typ = (REG[0042h] bits 8-0 + 1) x 2
7. t10typ = Selected from 40, 52, 68 or 90 Ts using REG[00A2h] bits 9-8
8. t11typ = Selected from 20, 40, 80, 120, 150, 190, 240 or 270 Ts using REG[00A2h] bits 13-11

Note

For TFT Type 2 Panels set the following:
FPFRAME Pulse Polarity bit to active high (REG[0050h] bit 7 = 1).
FPLINE Pulse Polarity bit to active high (REG[0046h] bit 7 = 1).
FPFRAME Pulse Position bits to zero (REG[0052h] bits 9-0 = 000h).

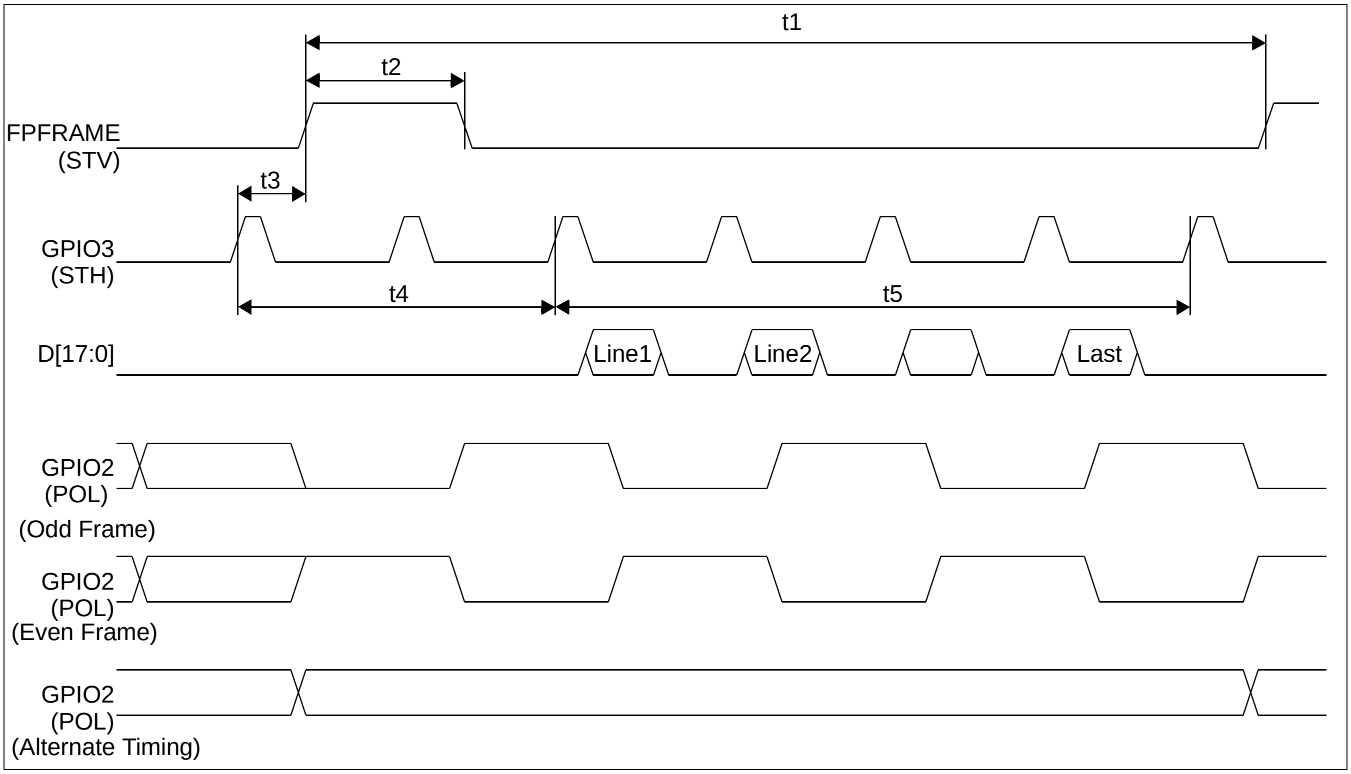

Figure 7-34: TFT Type 2 Vertical Timing

Table 7-51: TFT Type 2 Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Vertical total period	8	Note 2	1024	Lines
t2	FPFRAME pulse width	—	1	—	Lines
t3	GPIO3 rising edge to FPFRAME rising edge	—	0	—	Ts (Note 1)
t4	Vertical display start position	0	Note 3	1024	Lines
t5	Vertical display period	1	Note 4	1024	Ts

1. Ts = pixel clock period
2. t1typ = REG[004Ah] bits 9-0 + 1
3. t4typ = REG[004Eh] bits 9-0
4. t5typ = REG[004Ch] bits 9-0 + 1

7.4.6 LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing

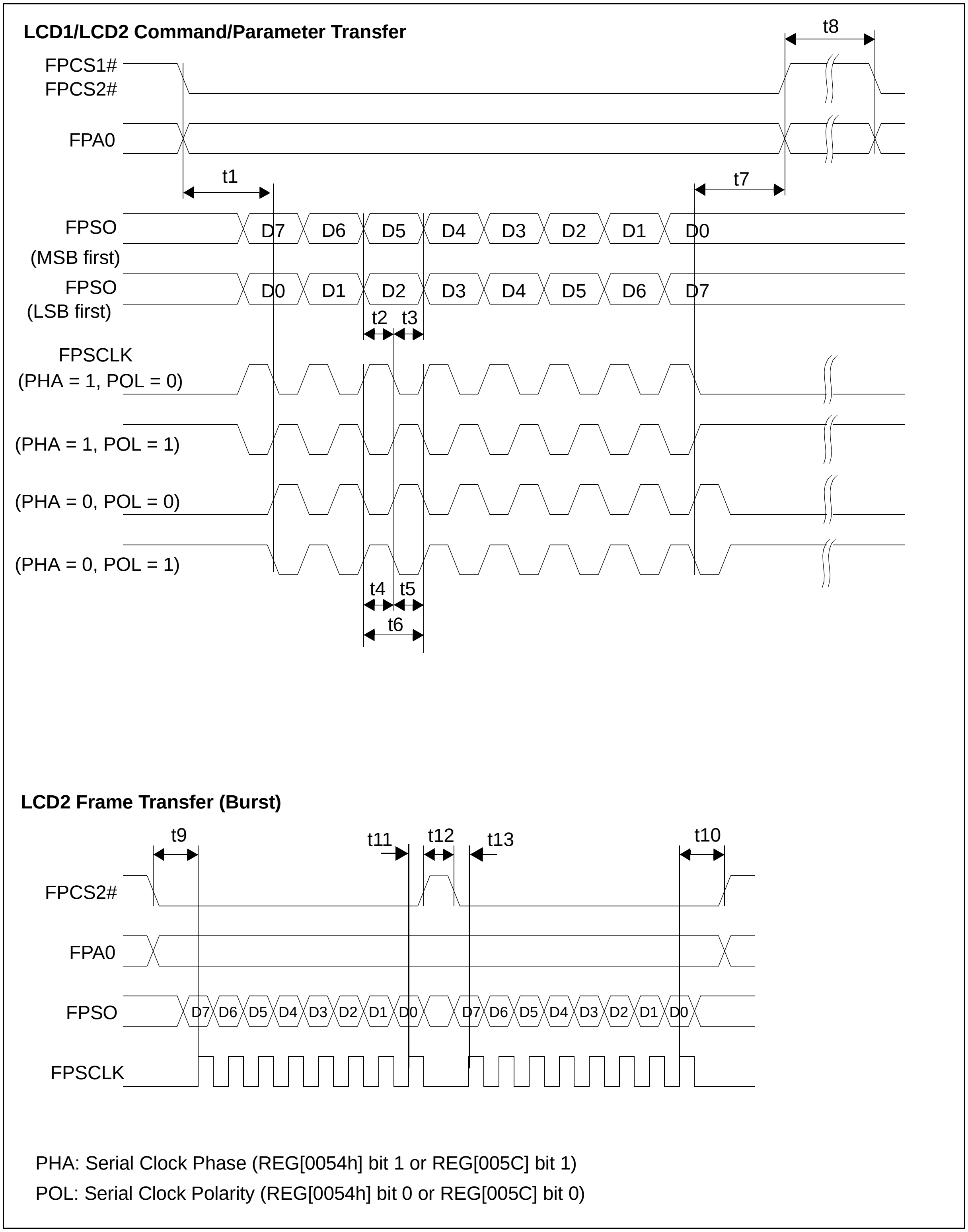

Figure 7-35: LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing

Table 7-52: LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	—	1.5	—	Ts (Note 1)
t2	Data setup time	—	0.5	—	Ts
t3	Data hold time	—	0.5	—	Ts
t4	Serial clock pulse width low (high)	—	0.5	—	Ts
t5	Serial clock pulse width high (low)	—	0.5	—	Ts
t6	Serial clock period	—	1	—	Ts
t7	Chip select hold time for command/parameter transfer	—	1.5	—	Ts
t8	Chip select de-assert to reassert	—	1	—	Ts
t9	Chip select setup time at beginning of burst mode	—	1.5	—	
t10	Chip select hold time at end of burst mode	—	2.5	—	Ts
t11	Chip select hold time during burst mode	—	0.5	—	Ts
t12	Chip select interval in burst mode	—	1	—	Ts
t13	Chip select setup time during burst mode	—	0.5	—	Ts

1. Ts = Serial clock period

7.4.7 LCD1 ND-TFD, LCD2 9-Bit Serial Interface Timing

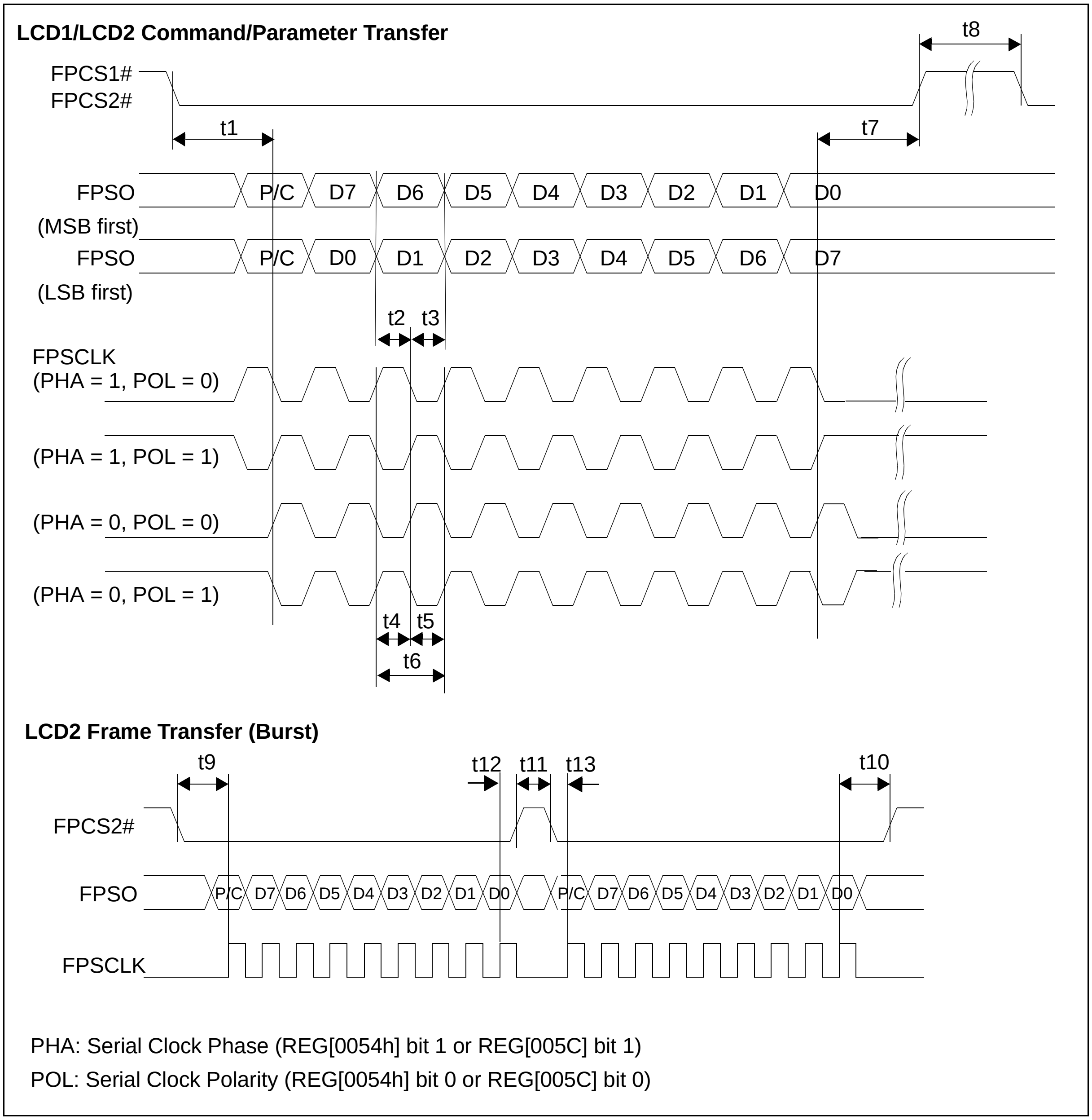

Figure 7-36: LCD1 ND-TFD, LCD2 9-Bit Serial Interface Timing

Table 7-53: LCD1 ND-TFD, LCD2 9-Bit Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	—	1.5	—	Ts (Note 1)
t2	Data setup time	—	0.5	—	Ts
t3	Data hold time	—	0.5	—	Ts
t4	Serial clock pulse width low (high)	—	0.5	—	Ts
t5	Serial clock pulse width high (low)	—	0.5	—	Ts
t6	Serial clock period	—	1	—	Ts
t7	Chip select hold time	—	1.5	—	Ts
t8	Chip select de-assert to reassert	—	1	—	Ts
t9	Chip select setup time at beginning of burst mode	—	1.5	—	
t10	Chip select hold time at end of burst mode	—	2.5	—	Ts
t11	Chip select interval in burst mode	—	1	—	Ts
t12	Chip select hold time during burst mode	—	0.5	—	Ts
t13	Chip select setup time during burst mode	—	0.5	—	Ts

1. Ts = Serial clock period

7.4.8 LCD1 a-Si TFT Serial Interface Timing

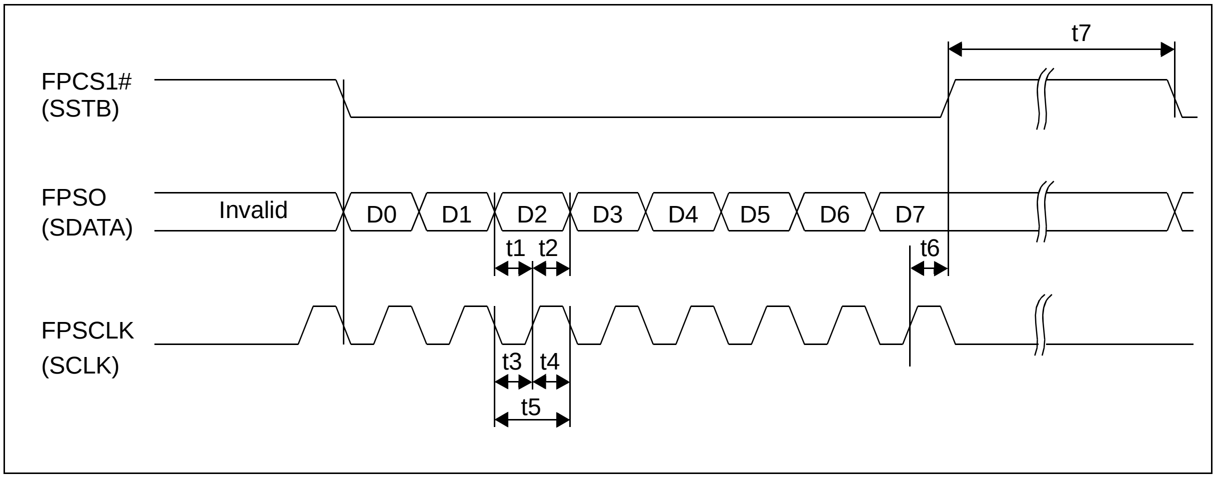

Figure 7-37: LCD1 a-Si TFT Serial Interface Timing

Table 7-54: LCD1 a-Si TFT Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Data Setup Time	—	0.5	—	Ts (Note 1)
t2	Data Hold Time	—	0.5	—	Ts
t3	Serial clock plus low period	—	0.5	—	Ts
t4	Serial clock pulse high period	—	0.5	—	Ts
t5	Serial clock period	—	1	—	Ts
t6	Chip select hold time	—	1.5	—	Ts
t7	Chip select de-assert to reassert	—	Note 2	—	Ts

1. Ts = Serial clock period
2. This setting depends on software

7.4.9 LCD1 uWIRE Serial Interface Timing

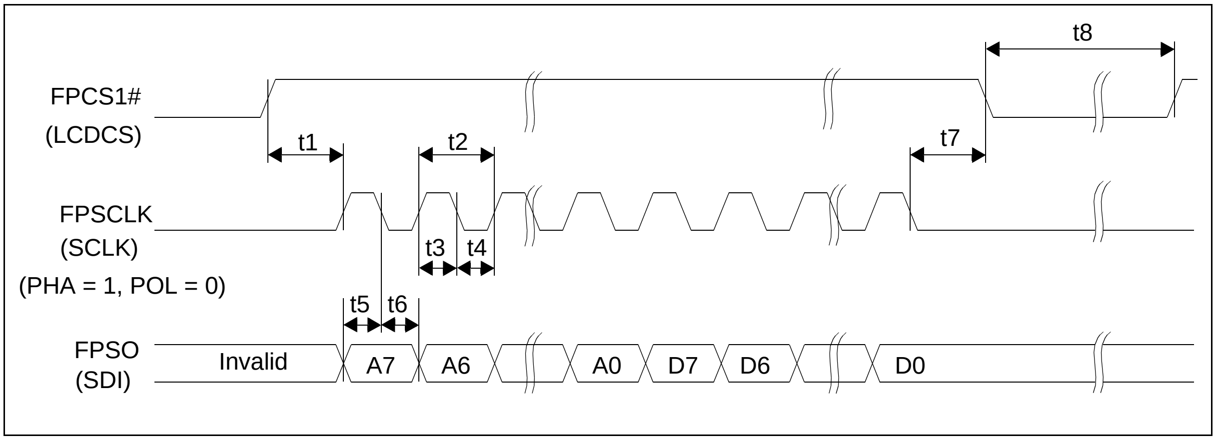

Figure 7-38: LCD1 uWIRE Serial Interface Timing

Table 7-55: LCD1 uWIRE Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	—	1	—	Ts (Note 1)
t2	Serial Clock Period	—	1	—	Ts
t3	Serial clock pulse width low	—	0.5	—	Ts
t4	Serial clock pulse width high	—	0.5	—	Ts
t5	Data setup time	—	0.5	—	Ts
t6	Data hold time	—	0.5	—	Ts
t7	Chip select hold time	—	1.5	—	Ts
t8	Chip select de-assert to reassert	—	Note 2	—	Ts

1. Ts = Serial clock period
2. This setting depends on software

Note

When a uWire panel is selected (REG[0054h] bits 7-5 = 10x), FPCS1# idles high until the first uWire transfer is started. After the first transfer, FPCS1# idles low.

7.4.10 LCD1 SPI Serial Interface Timing

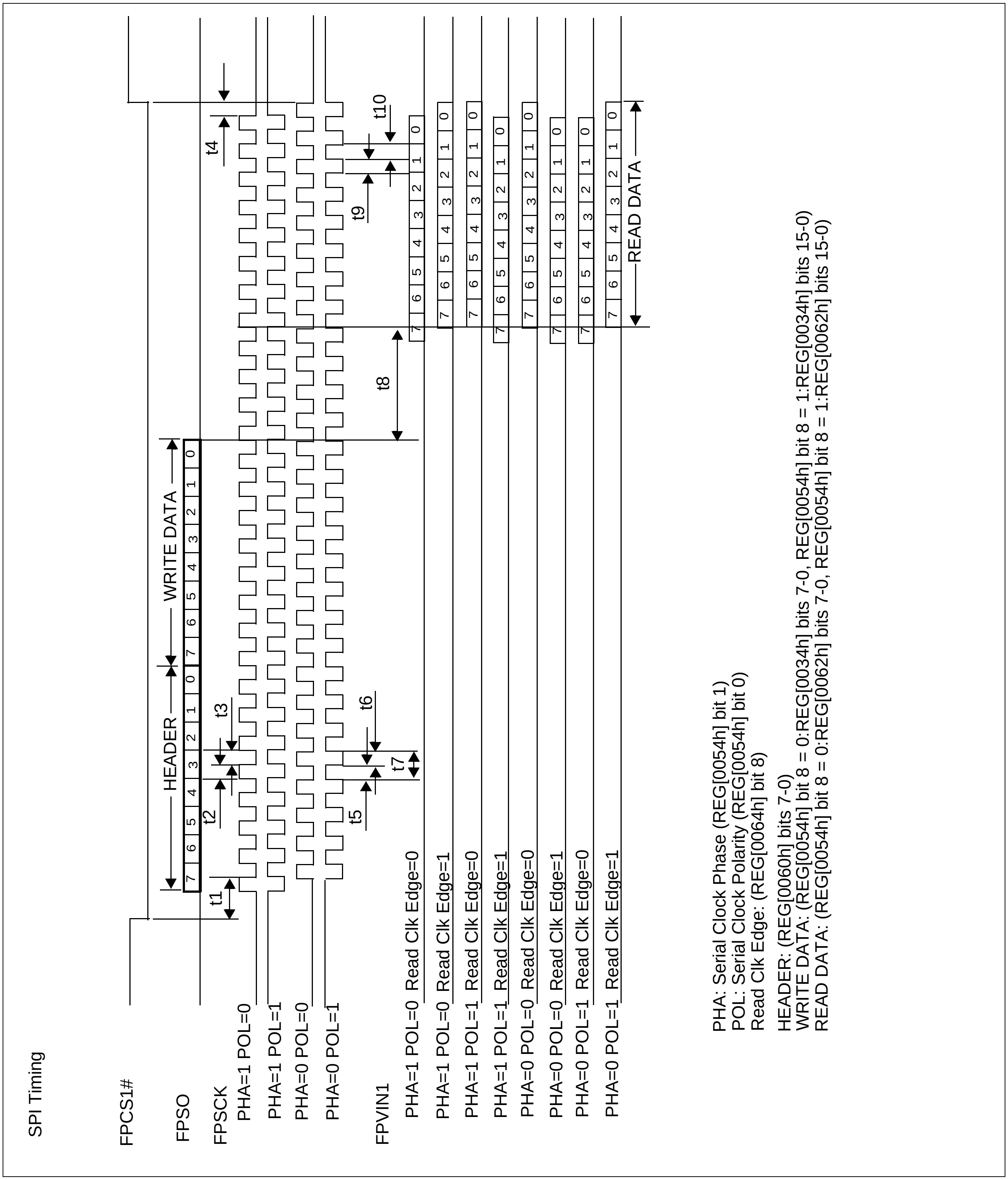

Figure 7-39: LCD1 SPI Serial Interface Timing

Table 7-56: LCD1 SPI Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	—	1.5	—	Ts (Note 1)
t2	Header/ Write data setup time	—	0.5	—	Ts
t3	Header/ Write data hold time	—	0.5	—	Ts
t4	Chip select hold time	—	0.5	—	Ts
t5	Serial clock pulse width high (low)	—	0.5	—	Ts
t6	Serial clock pulse width low (high)	—	0.5	—	Ts
t7	Serial clock period	—	1	—	Ts
t8	Write data output to Read data input	—	Note 2	—	Ts
t9	Read data setup time	TBD	—	—	ns
t10	Read data hold time	TBD	—	—	ns

1. Ts = Pixel clock period
2. t8typ = REG[0064h] bits 4-0

7.4.11 LCD1, LCD2 Parallel Interface (80)

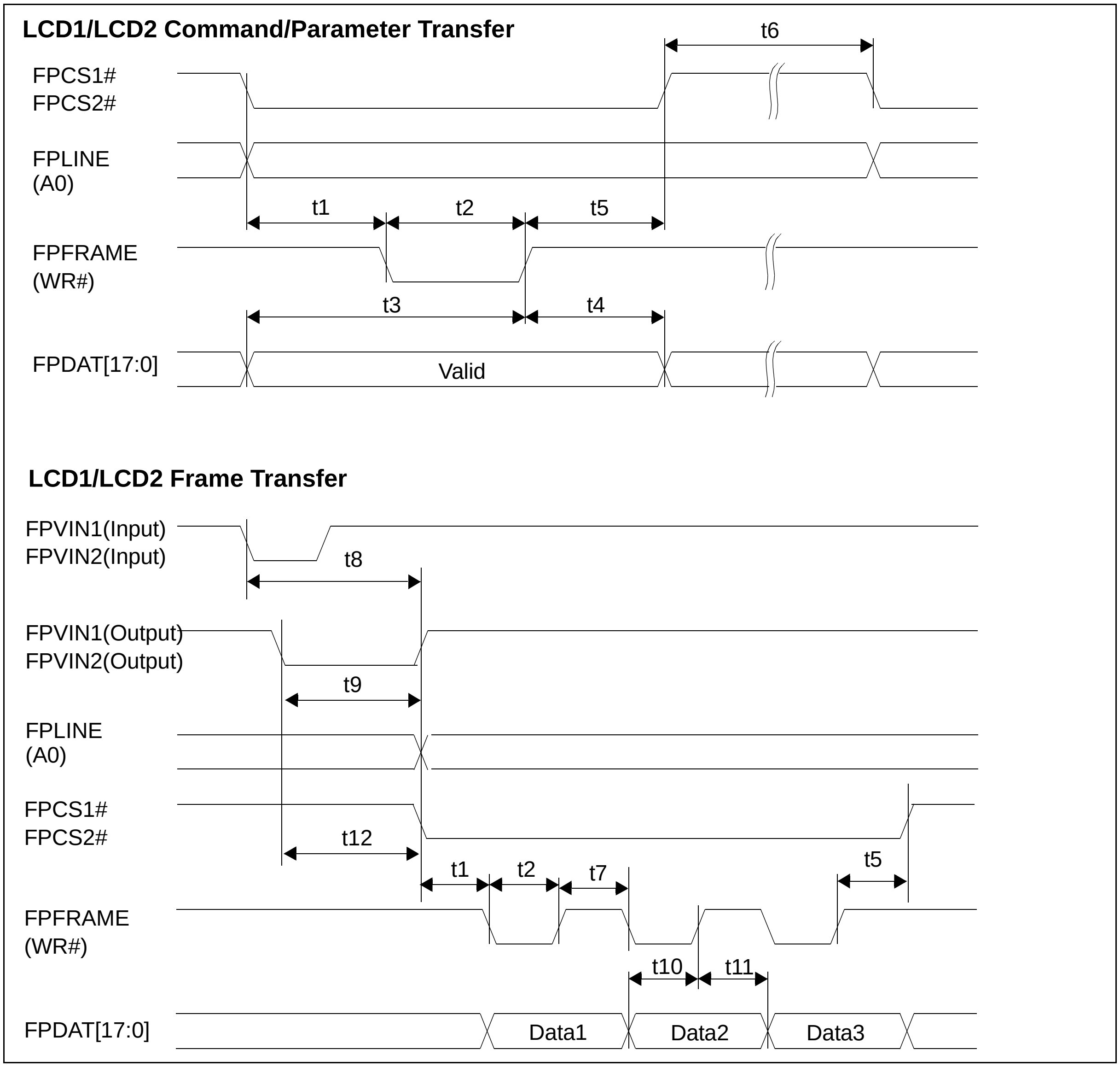

Figure 7-40: LCD1, LCD2 Parallel Interface Timing (80)

Table 7-57: LCD1, LCD2 Parallel Interface Timing (80)

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select falling edge to FPFRAME falling edge	—	1	—	Tp
t2	FPFRAME low period	—	1	—	Tp
t3	Data setup time	—	2	—	Tp
t4	Data hold time	—	1	—	Tp
t5	Write signal rising edge to chip select rising edge	—	1	—	Tp
t6	Chip select de-assert to reassert	—	0	—	Tp
t7	Write signal high period in burst cycle	—	1	—	Tp
t8	FPVIN (input) falling edge to chip select falling edge	—	—	51	Tp
t9	FPVIN (output) low period	—	Note 2	—	
t10	Data setup time in burst cycle	—	1	—	Tp
t11	Data hold time in burst cycle	—	1	—	Tp
t12	FPVIN (output) falling edge to FPCS# falling edge	—	Note 2	—	

1. Tp = Pixel clock period
2. t9 for LCD1 = REG[0068] bits [15:8]
   for LCD2 = REG[006A] bits [15:0]

7.4.12 LCD1, LCD2 Parallel Interface (68)

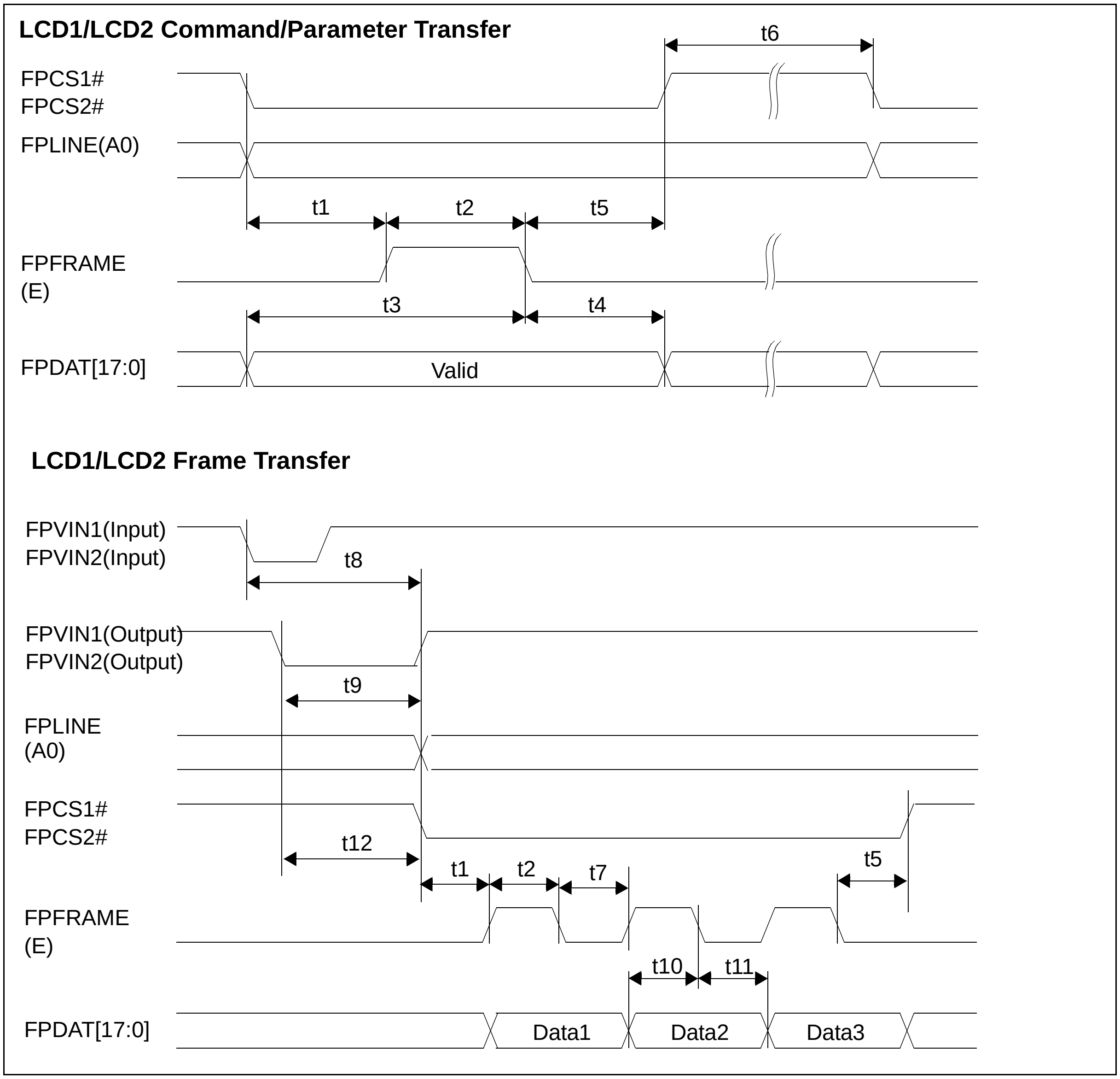

Figure 7-41: LCD1, LCD2 Parallel Interface Timing (68)

Table 7-58: LCD1, LCD2 Parallel Interface Timing (68)

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select falling edge to FPFRAME rising edge	—	1	—	Tp
t2	FPFRAME high period	—	1	—	Tp
t3	Data setup time	—	2	—	Tp
t4	Data hold time	—	1	—	Tp
t5	FPFRAME falling edge to Chip select rising edge	—	1	—	Tp
t6	Chip select deassert to reassert	—	0	—	Tp
t7	Enable signal low period in burst cycle	—	1	—	Tp
t8	FPVIN (input) falling edge to chip select falling edge	—	—	51	Tp
t9	FPVIN (output) low period	—	Note 2	—	Tp
t10	Data setup time in burst cycle	—	1	—	Tp
t11	Data hold time in burst cycle	—	1	—	Tp
t12	FPVIN (output) falling edge to FPCS# falling edge	—	Note 2	—	

1. Tp = Pixel clock period
2. t9 for LCD1 = REG[0068] bits [15:8]
   for LCD2 = REG[006A] bits [15:0]

7.5 Camera Interface Timing

7.5.1 Camera Interface Timing

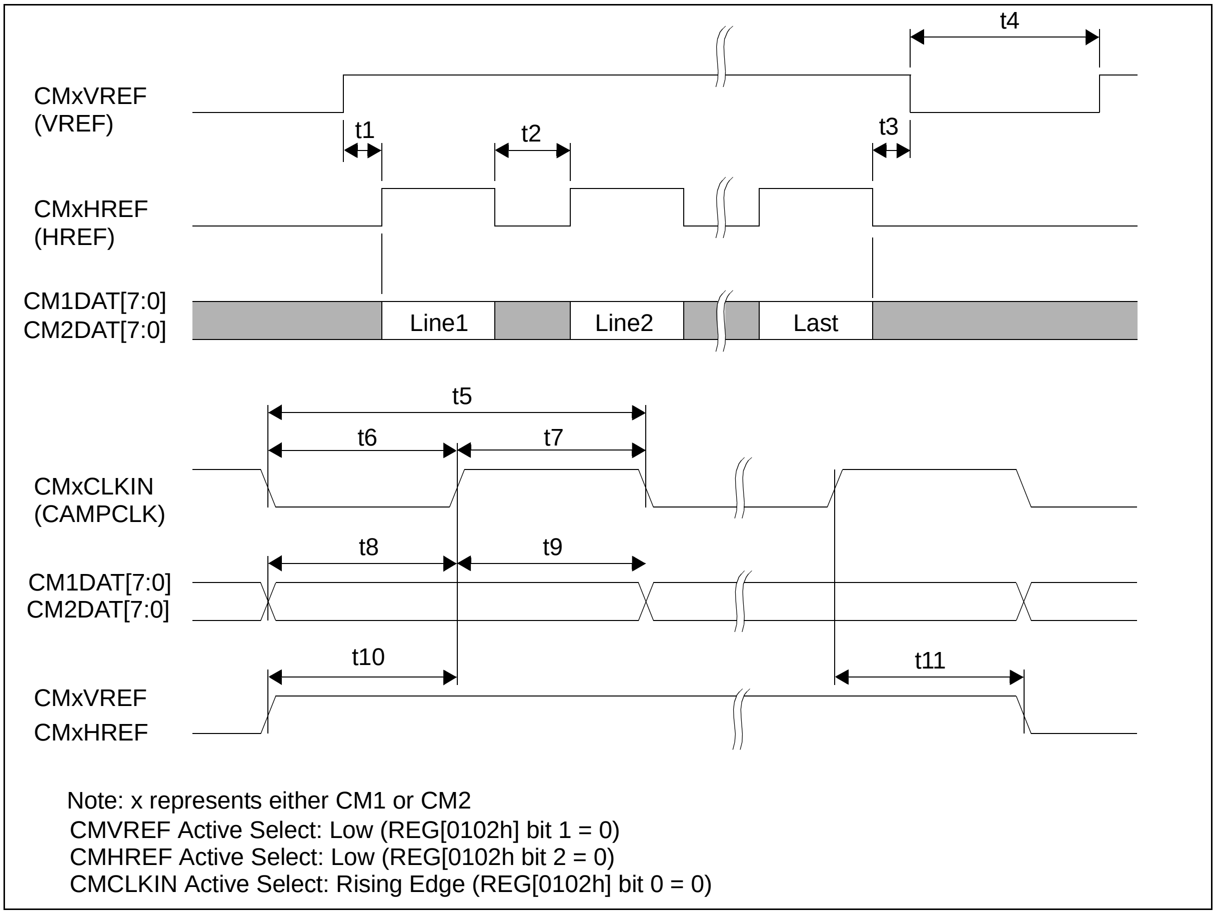

Figure 7-42: Camera Interface Timing

Table 7-59: Camera Interface Timing

Symbol	Parameter	Min	Max	Units
t1	CMxVREF rising edge to CMxHREF rising edge	0	—	Tc (note 1)
t2	Horizontal blank period	4	—	Tc
t3	CMxHREF falling edge to CMxVREF falling edge	0	—	Tc
t4	Vertical blank period	1	—	Line
t5	Camera input clock period, fast mode (REG[0110h] bit 10 = 1 (note 3))	1Ts+2ns	—	Ts (note 2)
t6	Camera input clock pulse width low, normal mode (REG[0110h] bit 10 = 0)	1Ts+2ns	—	Ts
t7	Camera input clock pulse width high, normal mode (REG[0110h] bit 10 = 0)	1Ts+2ns	—	Ts
t8	Data setup time	2	—	ns
t9	Data hold time	4	—	ns
t10	CMxVREF, CMxHREF setup time	2	—	ns
t11	CMxVREF, CMxHREF hold time	4	—	ns

1. Ts = System clock period
2. Tc = Camera block input clock period
3. When REG[0110h] bit 10 = 0, the camera clock is protected from noise by internal circuits.
   When REG[0110h] bit 10 = 1, the camera clock is not protected from noise by internal circuits.

7.5.2 Camera Clock Output

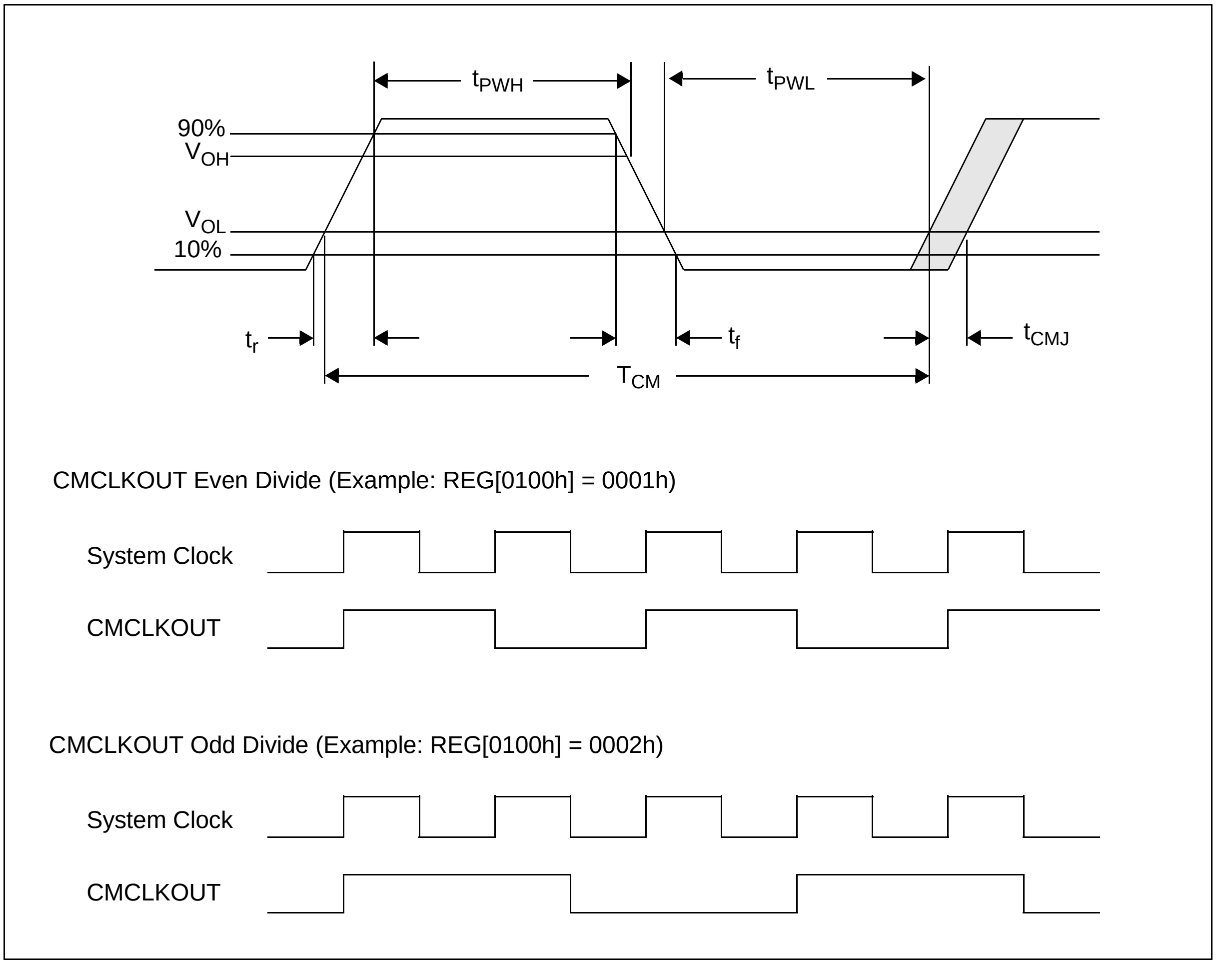

Figure 7-43: Camera Clock Output Timing

Table 7-60: Camera Clock Output Timing

Symbol	Parameter	Min	Typ	Max	Units
f_{CM}	CMCLKOUT frequency	—	—	27.5 (Note 1)	MHz
T_{CM}	CMCLKOUT period	—	$1/f_{CM}$	—	ns
T_{CMJ}	CMCLKOUT jitter	-2	—	2	%
T_{CMDUTY}	CMCLKOUT duty cycle	-10	—	10	%
CIO1/2 VDD = 3.0V, C_L = 30pF					
t_{PWH}	CMCLKOUT width high	9	—	—	ns
t_{PWL}	CMCLKOUT width low	9	—	—	ns
t_r	CMCLKOUT rising time (10% - 90%)	—	—	8.5	ns
t_f	CMCLKOUT falling time (10% - 90%)	—	—	8.5	ns
CIO1/2 VDD = 2.5V, C_L = 30pF					
t_{PWH}	CMCLKOUT width high	8	—	—	ns
t_{PWL}	CMCLKOUT width low	8	—	—	ns
t_r	CMCLKOUT rising time (10% - 90%)	—	—	10	ns
t_f	CMCLKOUT falling time (10% - 90%)	—	—	7.5	ns

1. If it is necessary for a Camera Output higher than 27.5 MHz, contact your EPSON representative.

Note

Refer to the information on PLL jitter in Section 7.1.3, “PLL Clock”.

7.5.3 Strobe Control Output

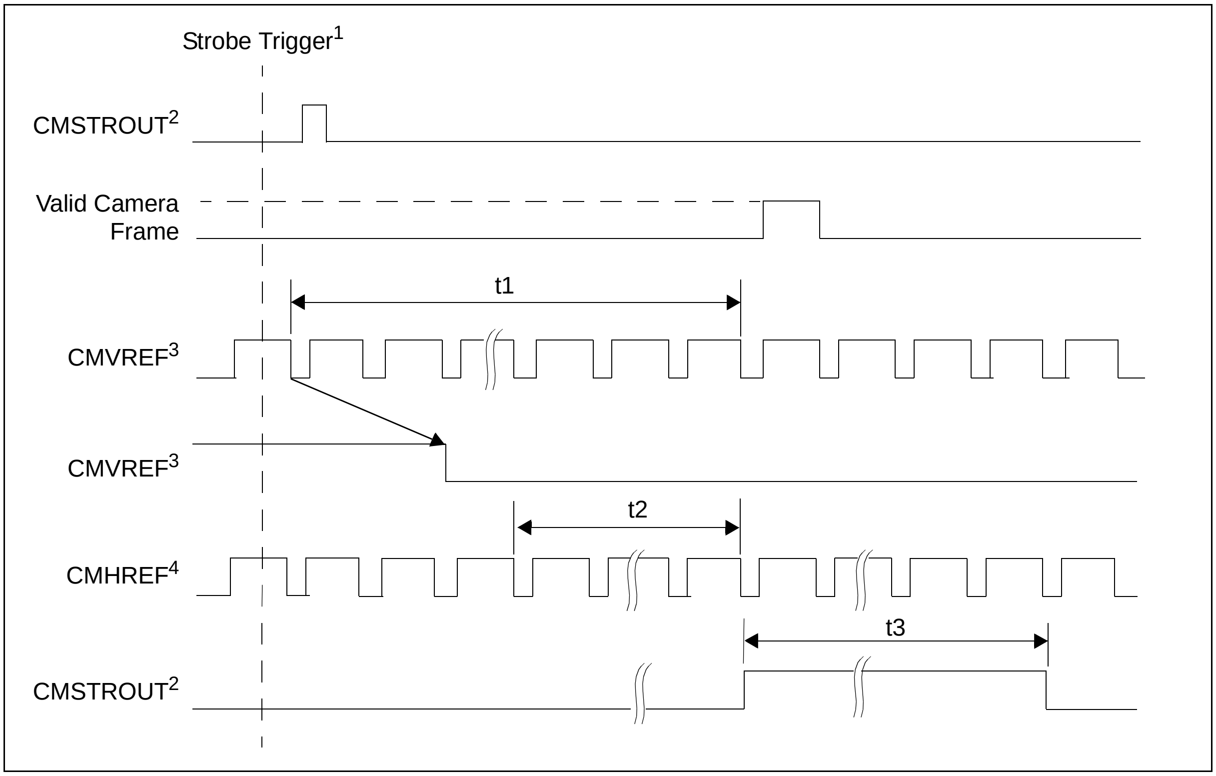

Figure 7-44: Strobe Control Output Timing

Note

1. For more information on the strobe trigger, see the bit description for REG[0124h] bits 7-4 and Section 21.3, “Strobe Control Signal”.
2. CMSTROUT Active Select: High (REG[0124h] bits 3-0 = 1011b)
3. CMVREF Active Select: Low (REG[0102h] bit 1 = 0)
4. CMHREF Active Select: Low (REG[0102h] bit 2 = 0)

Table 7-61: Strobe Control Output Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	CMVREF delay from first CMVREF falling edge (rising edge if active high) after the strobe trigger	—	Note 1	—	Tcmv
t2	CMHREF delay from first CMHREF falling edge (rising edge if active high) after CMVREF active	—	Note 2	—	Tcmh
t3	CMSTROUT active pulse width	—	Note 3	—	Tcmh

1. t1typ = REG[0124h] bits 7-4 (t1 is always 0 for single frame capture mode (REG[0112h] bit 6 = 1) and REG[0124h] bits 7-4 are ignored)
2. t2typ = REG[0120h] bits 15-0
3. t3typ = REG[0122h] bits 15-0
4. Tcmv = CMVREF period
5. Tcmh = CMHREF period

7.5.4 MPEG Codec Interface Timing

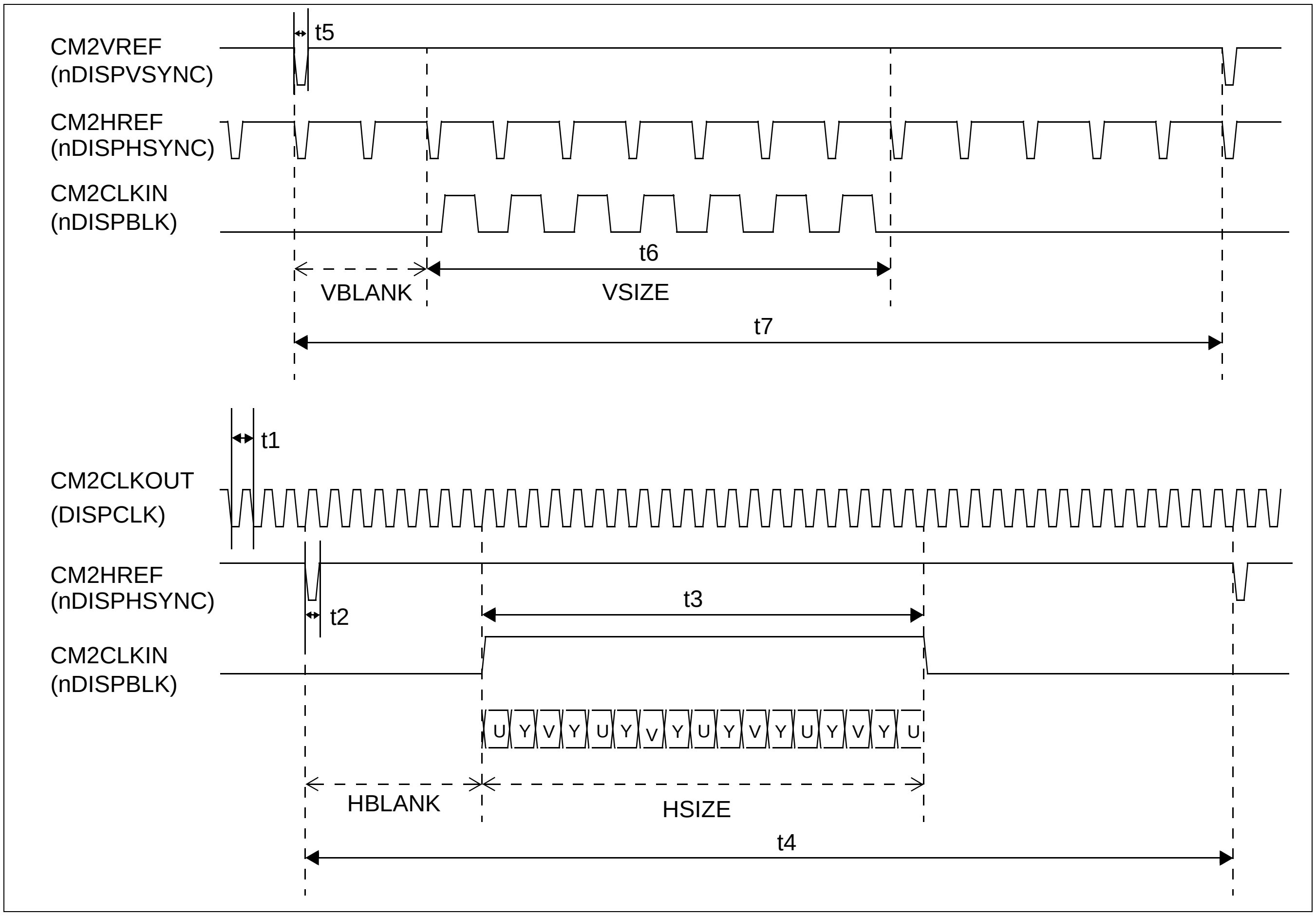

Figure 7-45: MPEG Codec Interface Timing

Table 7-62: MPEG Codec Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Camera Clock Cycle	4	—	32	Ts (Note 1)
t2	Horizontal Sync Pulse Width	—	1	—	Tc (Note 2)
t3	Horizontal Display Period	1	—	1024	Pixel
t4	Horizontal Total	—	REG[012Ah] bits 9-0 + 1	—	Pixel
t5	Vertical Sync Pulse Width	—	1	—	Tc
t6	Vertical Display Period	1	—	512	Line
t7	Vertical Total	—	REG[0128h] bits 9-0 + 1	—	Line

1. Ts = System clock period
2. Tc = Camera block input clock period
3. Tc should be equal or more than 4Ts
4. Tc = t1
5. 1Pixel = 2Tc

7.6 SD Memory Card Interface

7.6.1 SD Memory Card Access

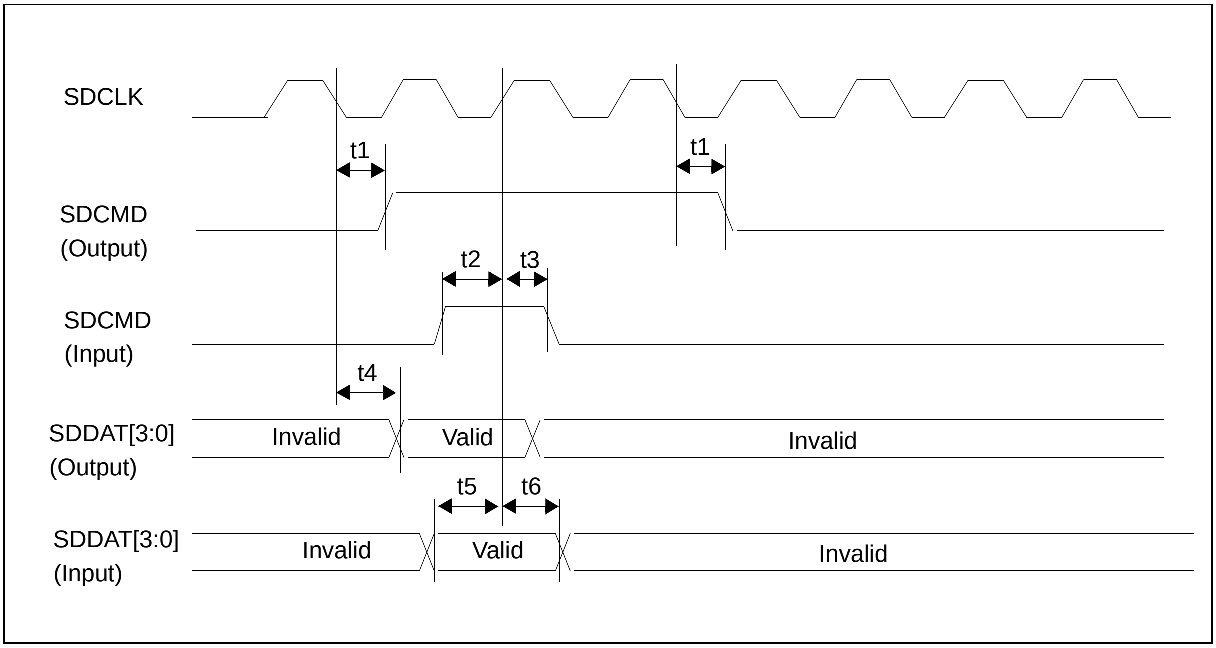

Figure 7-46: SD Memory Card Access Timing

Table 7-63: SD Memory Card Access Timing

Symbol	Parameter	Min	Max	Units
t1	SDCMD output delay time	—	20	ns
t2	SDCMD input setup time	10	—	ns
t3	SDCMD input hold time	5	—	ns
t4	SDDAT[3:0] output delay time	—	20	ns
t5	SDDAT[3:0] input setup time	10	—	ns
t6	SDDAT[3:0] input hold time	5	—	ns

7.6.2 SD Memory Card Clock Output

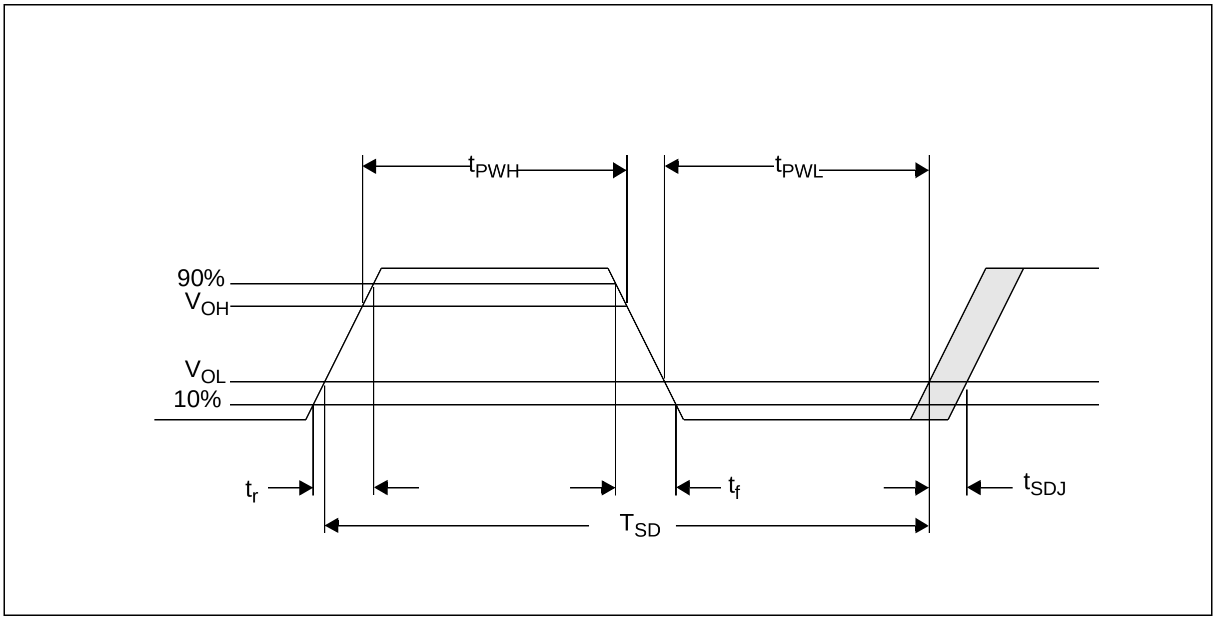

Figure 7-47: SD Memory Card Clock Output Timing

Table 7-64: SD Memory Card Clock Output Timing

Symbol	Parameter	Min	Typ	Max	Units
f_{SD}	SDCLK frequency	—	—	13.75	MHz
T_{SD}	SDCLK period	—	$1/f_{SD}$	—	ns
t_{PWH}	SDCLK width high	10	—	—	ns
t_{PWL}	SDCLK width low	10	—	—	ns
t_r	SDCLK rising time (10% - 90%)	—	—	10	ns
t_f	SDCLK falling time (10% - 90%)	—	—	10	ns
t_{SDJ}	SDCLK jitter	-3	—	3	%
t_{SDD}	SCLK clock duty	45	—	55	%

Note

Refer to the information on PLL jitter in Section 7.1.3, “PLL Clock”.

8 Memory Map

8.1 Physical Memory

The S1D13719 includes 512K byte of embedded SRAM. The SRAM consists of four banks composed of 64K/128K/128K/128K/64K bytes as shown in Figure 8-1: "Physical Memory," on page 111. Each bank is mapped at consecutive addresses.

The memory is used for the Display Buffer, JPEG Line Buffer and JPEG FIFO.

The display buffer contains Main window and PIP+ window image data for LCD1 and image data for LCD2.

Please secure the JPEG decode image or the camera image for the buffer for the display when you use JPEG.

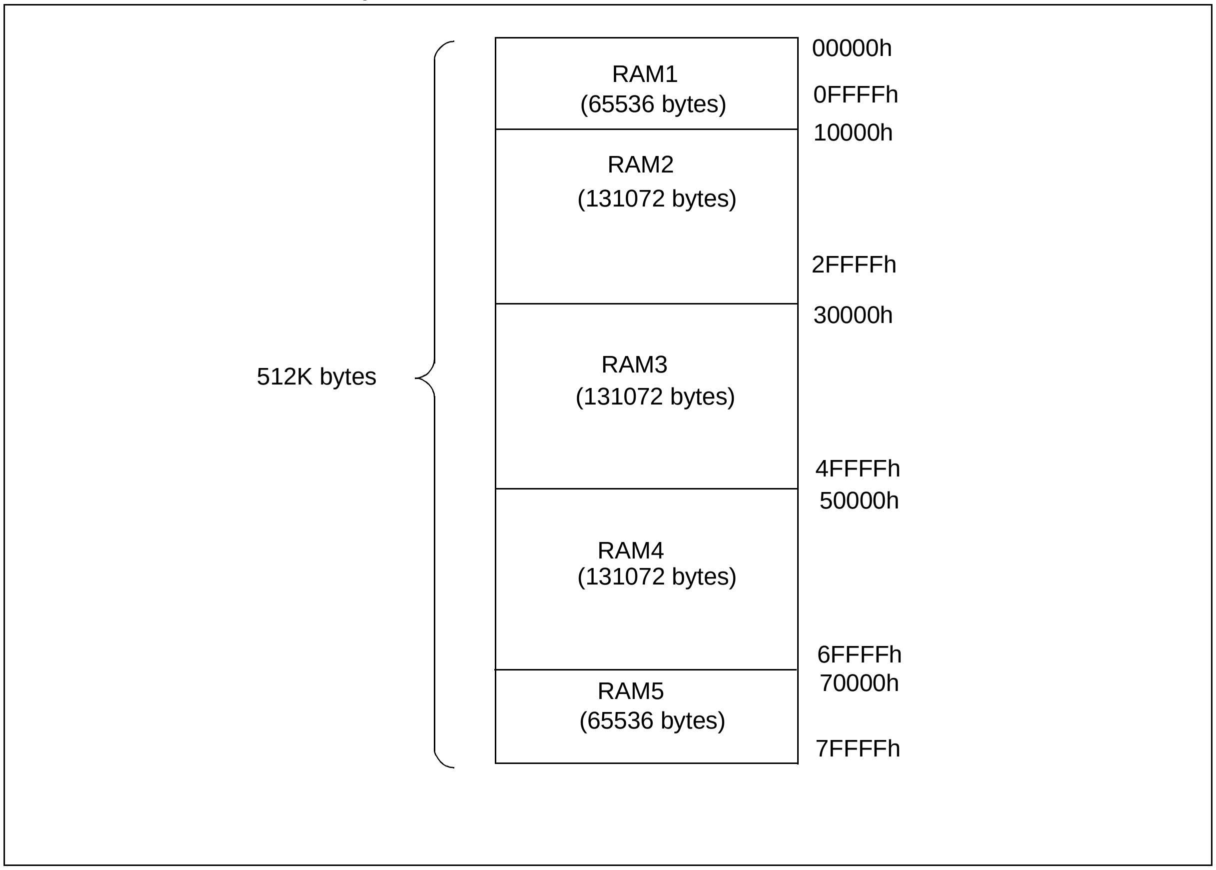

Figure 8-1: Physical Memory

8.2 Memory Map Example

Recommended for: JPEG 1280 x1024

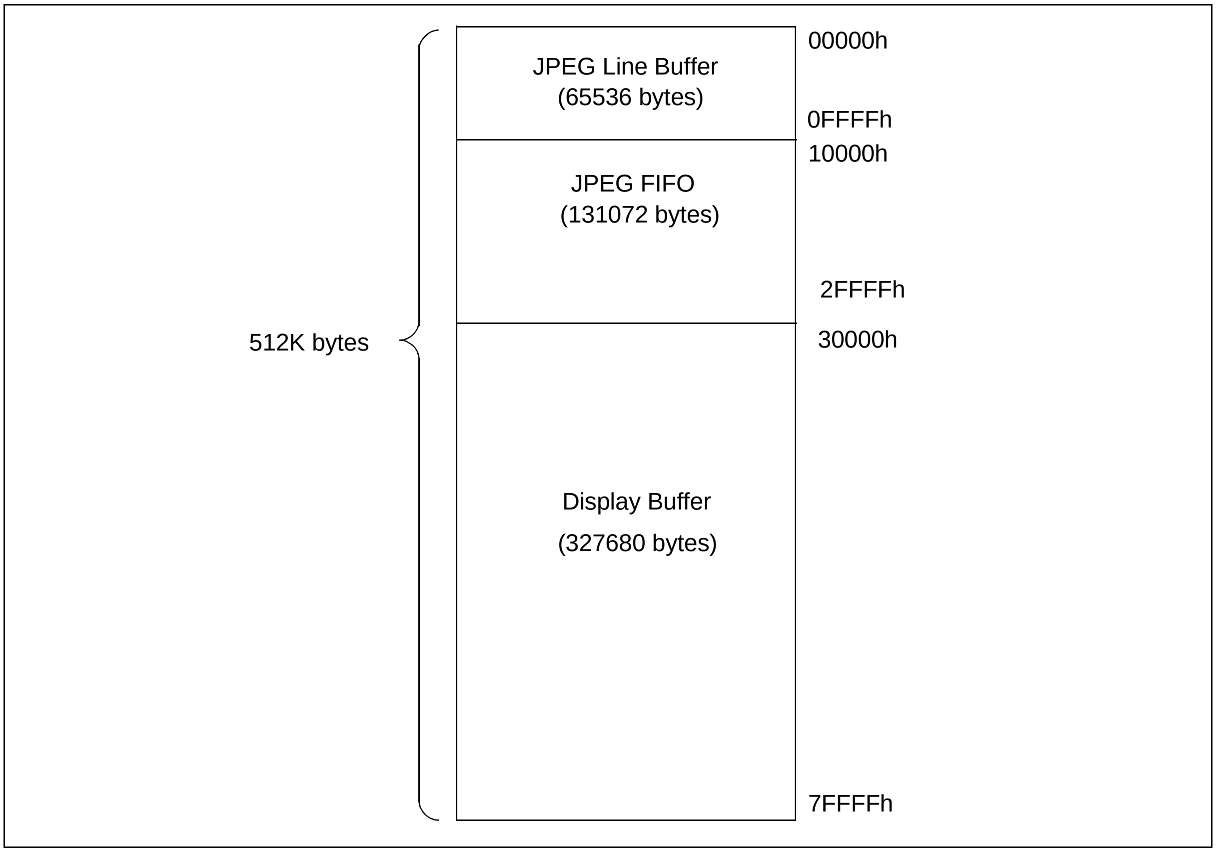

Figure 8-2: Memory Map Example 1

- Memory start address settings:
  - Display Buffer start address: 20000h
  - JPEG Line Buffer start address: 00000h (REG[0F02h] bits 2-0 = 000b, REG[09D2h] bit 5 = 0)
  - JPEG FIFO starting address: 10000h (REG[09BCh] bits 8-0 = 040h)
- Memory size settings:
  - JPEG Line Buffer size: 64K bytes (REG[09D0h] bits 1-0 = 11b)
  - JPEG FIFO size: 64K bytes (REG[09A4h] bits 4-0 = 01111b)
- Display Buffer usage:
  - Image data for LCD1 main window
  - Image data for LCD1 PIP$^+$ window (JPEG decode image or camera image)
  - Image data for LCD2 display

9 Clocks

9.1 Clock Diagram

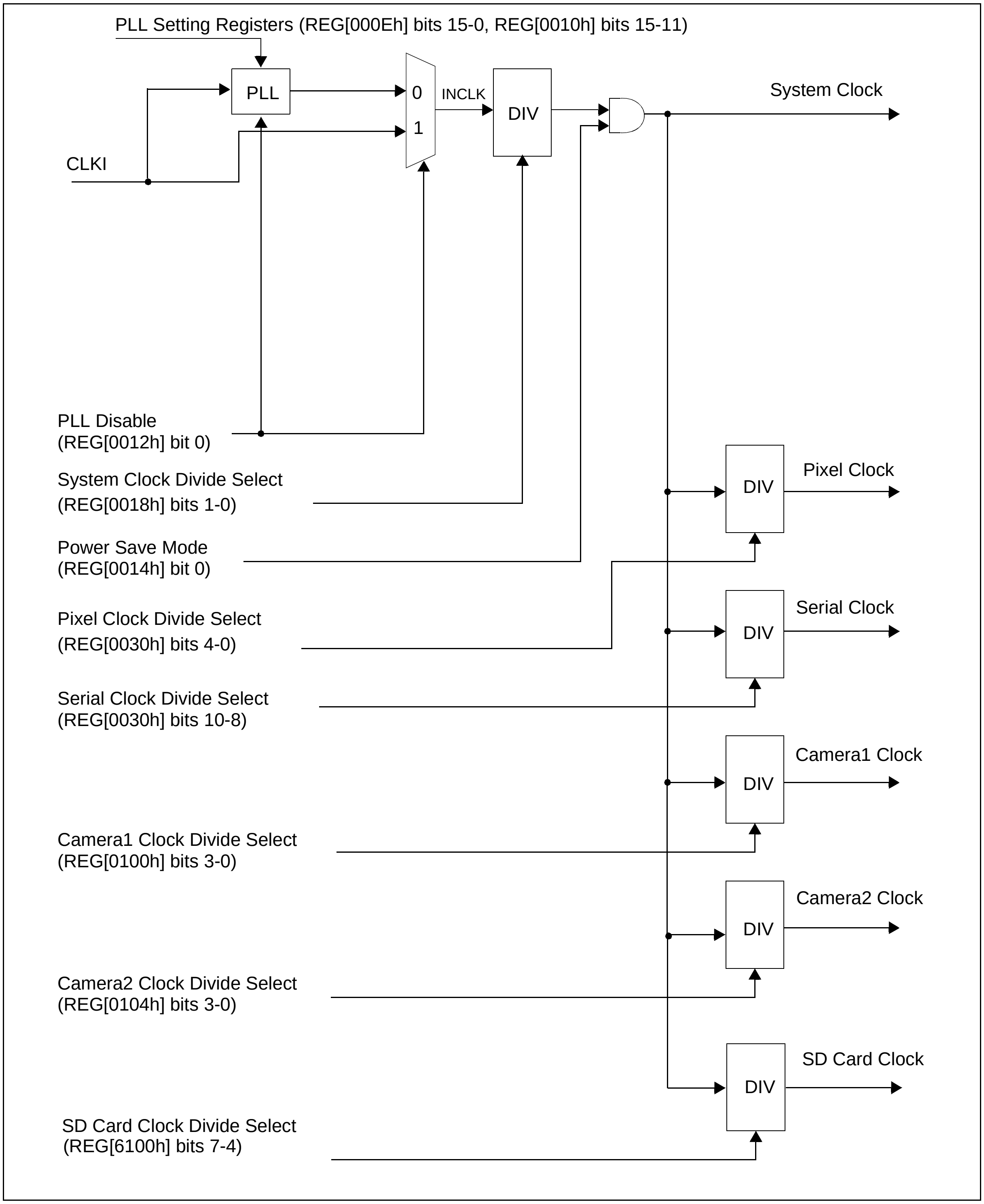

Figure 9-1: Clock Diagram

9.2 Clocks

9.2.1 System Clock

System clock (SYSCLK) is used for the S1D13719 internal main clock. The system clock source can be selected (REG[0012h] bits 2 and 0) from either the internal PLL, or an external clock input (CLKI). The System Clock Divide Select bits (REG[0018h] bits 1-0) control this clock division. The system clock can be a divided down version of the output of the PLL or the input of CLKI.

9.2.2 Pixel Clock

Pixel clock (PCLK) is used for the LCD1 shift clock of a RGB type panel and for the LCD1/LCD2 parallel interface timing. The pixel clock source is always the system clock and can be divided using the Pixel Clock Divide Select bits (REG[0030h] bits 4-0).

9.2.3 Serial Clock

Serial clock (SCLK) is used for the LCD1 and LCD2 serial interfaces. The serial clock source is always the system clock and can be divided using the Serial Clock Divide Select bits (REG[0030h] bits 10-8).

9.2.4 Camera1 Clock

Camera1 clock (CAM1CLK) is used for the Camera1 interface. The camera1 clock source is always the system clock and can be divided using the Camera1 Clock Divide Select bits (REG[0100h] bits 3-0).

Note

This clock can be output on the CM1CLKOUT pin to be used as the master clock of an external camera module attached to the Camera1 interface.

9.2.5 Camera2 Clock

Camera2 clock (CAM2CLK) is used for the Camera2 interface. The camera2 clock source is always the system clock and can be divided using the Camera2 Clock Divide Select bits (REG[0104h] bits 3-0). CAM2CLK is also used for the MPEG Codec interface.

Note

This clock can be output on the CM2CLKOUT pin to be used as the master clock of an external camera module attached to the Camera2 interface.

9.2.6 SD Memory Card Clock

The SD Memory Card clock is output to the external SD Memory Card as the SD Card Clock. The SD memory card clock source is always the system clock and can be divided using the SD Memory Card Clock Divide Select bits (REG[6100h] bits 7-4).

10 Registers

10.1 Register Mapping

The S1D13719 registers are memory-mapped. When the system decodes the input pins as CS# = 0 and M/R# = 0, the registers may be accessed. The register space is decoded by AB[18:1] and BE#[1:0], and is mapped as follows.

Table 10-1: S1D13719 Register Mapping

M/R#	Address	Function
1	00000h to 7FFFFh	SRAM memory
0	0000h to 0007h	System Configuration Registers
0	000Eh to 0019h	Clock Setting Registers
0	0020h to 002Dh	Indirect Interface Registers
0	0030h to 003Dh	LCD Panel Interface Setting Registers
0	0040h to 0057h	LCD1 Setting Registers
0	0058h to 005Fh	LCD2 Setting Registers
0	0060h to 00FFh	Extended Panel Registers
0	0100h to 0131h	Camera Interface Registers
0	0200h to 0281h	Display Mode Setting Registers
0	0300h to 030Fh	GPIO Registers
0	0310h to 0329h	Overlay Registers
0	0400h to 08FFh	Look-Up Table Registers
0	0930h to 096Fh	Resizer Operation Registers
0	0980h to 098Fh	JPEG Module Registers
0	09B0h to 09BBh	JPEG FILE Setting Registers
0	09C0h to 09E1h	JPEG Line Buffer Setting Registers
0	0A00h to 0A41h	Interrupt Control Registers
0	0F00h	JPEG Encode Performance register
0	1000h to 17A3h	JPEG Codec Registers
0	6000h to 613Fh	SD Card Interface Registers
0	8000h to 10001h	2D BitBLT Registers

10.2 Register Set

The S1D13719 registers are listed in the following table.

Table 10-2: S1D13719 Register Set

Register	Pg	Register	Pg
System Configuration Registers			
REG[0000h] Product Information Register	123	REG[0002h] Configuration Pins Status Register	123
REG[0004h] SD Memory Card Interface Enable Register	124	REG[0006h] Bus Timeout Setting Register	124
Clock Setting Registers			
REG[000Eh] PLL Setting Register 0	126	REG[0010h] PLL Setting Register 1	128
REG[0012h] PLL Setting Register 2	129	REG[0014h] Miscellaneous Configuration Register	130
REG[0016h] Software Reset Register	133	REG[0018h] System Clock Setting Register	133
Indirect Interface Registers			
REG[0020h] Indirect Interface Memory Rectangular Address Offset Register	134	REG[0022h] Indirect Interface Memory Address Register 0	134
REG[0024h] Indirect Interface Memory Address Register 1	134	REG[0026h] Indirect Interface Memory Rectangular Width Register	135
REG[0028h] Indirect Interface Memory Access Port Register	135	REG[002Ch] Indirect Interface JPEG Status Register	135
LCD Panel Interface Generic Setting Register			
REG[0030h] LCD Interface Clock Setting Register	137	REG[0032h] LCD Interface Configuration Register	139
REG[0034h] LCD Interface Command Register	141	REG[0036h] LCD Interface Parameter Register	141
REG[0038h] LCD Interface Status Register	142	REG[003Ah] LCD Interface Frame Transfer Register	142
REG[003Ch] LCD Interface Transfer Setting Register	143		
LCD1 Setting Register			
REG[0040h] LCD1 Horizontal Total Register	144	REG[0042h] LCD1 Horizontal Display Period Register	145
REG[0044h] LCD1 Horizontal Display Period Start Position Register	145	REG[0046h] LCD1 FPLINE Register	146
REG[0048h] LCD1 FPLINE Pulse Position Register	146	REG[004Ah] LCD1 Vertical Total Register	147
REG[004Ch] LCD1 Vertical Display Period Register	147	REG[004Eh] LCD1 Vertical Display Period Start Position Register	148
REG[0050h] LCD1 FPFRAME Register	148	REG[0052h] LCD1 FPFRAME Pulse Position Register	148
REG[0054h] LCD1 Serial Interface Setting Register	149	REG[0056h] LCD1 Parallel Interface Setting Register	150
LCD2 Setting Registers			
REG[0058h] LCD2 Horizontal Display Period Register	153	REG[005Ah] LCD2 Vertical Display Period Register	153
REG[005Ch] LCD2 Serial Interface Setting Register	153	REG[005Eh] LCD2 Parallel Interface Setting Register	155

Table 10-2: S1D13719 Register Set

Register	Pg	Register	Pg
Extended Panel Registers			
REG[0060h] SPI Header Data Register	158	REG[0062h] SPI Read Data Register	158
REG[0064h] SPI Read Wait Time Register	158	REG[0068h] LCD1 Vsync Output Register	158
REG[006Ah] LCD2 Vsync Output Register	159	REG[0080h] Samsung a-TFT Horizontal Total Register	160
REG[0082h] Samsung a-TFT LD Rising Edge Register	160	REG[0084h] Samsung a-TFT CKV Toggle Point Register	160
REG[0086h] Samsung a-TFT VCOM Toggle Point Register	161	REG[0088h] Samsung a-TFT Pulse Width Register	161
REG[008Ah] through REG[008Eh] are Reserved	161	REG[0090h] HR-TFT Configuration Register	162
REG[0092h] HR-TFT CLS Width Register	162	REG[0094h] HR-TFT PS1 Rising Edge Register	162
REG[0096h] HR-TFT PS2 Rising Edge Register	163	REG[0098h] HR-TFT PS2 Toggle Width Register	163
REG[009Ah] HR-TFT PS3 Signal Width Register	164	REG[009Eh] HR-TFT REV Toggle Point Register	164
REG[00A0h] HR-TFT PS1/2 End Register	164	REG[00A2h] Type 2 TFT Configuration Register 0	165
REG[00A4h] Casio TFT Timing Register 0	166	REG[00A6h] Casio TFT Timing Register 1	167
REG[00A8h] Type 2 TFT Configuration Register 1	167	REG[00AAh] through REG[00ECh] are Reserved	167
REG[00EEh] Partial Drive Area0 Start Line Register	168	REG[00F0h] Partial Drive Area0 End Line Register	169
REG[00F2h] Partial Drive Area1 Start Line Register	170	REG[00F4h] Partial Drive Area1 End Line Register	170
REG[00F6h] through REG[00FCh] are Reserved	171	REG[00FEh] LCD Interface ID Register	171
Camera Interface Setting Register			
REG[0100h] Camera1 Clock Setting Register	172	REG[0102h] Camera1 Signal Setting Register	172
REG[0104h] Camera2 Clock Divide Select Register	174	REG[0106h] Camera2 Input Signal Format Select Register	175
REG[0108h] through REG[010Eh] are Reserved	176	REG[0110h] Camera Mode Setting Register	176
REG[0112h] Camera Frame Setting Register	179	REG[0114h] Camera Control Register	181
REG[0116h] Camera Status Register	182	REG[0120h] Strobe Line Delay Register	184
REG[0122h] Strobe Pulse Width Register	184	REG[0124h] Strobe Control Register	185
REG[0128h] MPEG Interface VSYNC Width register	186	REG[012Ah] MPEG Interface HSYNC Width register	186
REG[012Ch] through REG[012Fh] are Reserved	186	REG[0130h] CIOVDD Control register	187
Display Mode Setting Register			
REG[0200h] Display Mode Setting Register 0	188	REG[0202h] Display Mode Setting Register 1	192
REG[0204h] Transparent Overlay Key Color Red Data Register	195	REG[0206h] Transparent Overlay Key Color Green Data Register 195	
REG[0208h] Transparent Overlay Key Color Blue Data Register	196	REG[0210h] Main Window Display Start Address Register 0	196
REG[0212h] Main Window Display Start Address Register 1	196	REG[0214h] Main Window Start Address Status Register	197
REG[0216h] Main Window Line Address Offset Register	198	REG[0218h] PIP+ Display Start Address Register 0	199
REG[021Ah] PIP+ Display Start Address Register 1	199	REG[021Ch] PIP+ Window Start Address Status Register	200
REG[021Eh] PIP+ Window Line Address Offset Register	201	REG[0220h] PIP+ X Start Positions Register	203
REG[0222h] PIP+ Y Start Positions Register	203	REG[0224h] PIP+ X End Positions Register	203
REG[0226h] PIP+ Y End Positions Register	204	REG[0228h] is Reserved	204
REG[022Ah] Back Buffer1 Display Start Address Register 0	205	REG[022Ch] Back Buffer1 Display Start Address Register 1	205
REG[022Eh] Back Buffer2 Display Start Address Register 0	205	REG[0230h] Back Buffer2 Display Start Address Register 1	205
REG[0234h] YUV Display Control Register	206	REG[0236h] YUV Display Size Register	207
REG[0238h] YUV Display Start Offset Register	207	REG[023Ah] Fractional Zoom Register	208
REG[023Ch] YRC2 Translate Mode Register	210	REG[023Eh] YRC2 UV Data Fix Register	211
REG[0240h] YRC1 Translate Mode Register	211	REG[0242h] YRC1 Write Start Address 0 Register 0	215
REG[0244h] YRC1 Write Start Address 0 Register 1	215	REG[0246h] YRC1 Write Start Address 1 Register 0	216
REG[0248h] YRC1 Write Start Address 1 Register 1	216	REG[024Ah] YRC1 Write Start Address 2 Register 0	216
REG[024Ch] YRC1 Write Start Address 2 Register 1	216	REG[024Eh] YRC1 UV Data Fix Register	217
REG[0250h] YRC1 Rectangle Pixel Width Register	217	REG[0252h] YRC1 Rectangular Line Address Offset Register	217
REG[0254h] YRC1 Memory Configuration Register	218	REG[0260h] RGB/YUV Converter Configuration Register	219
REG[0262h] is Reserved	219	REG[0264h] Memory Image JPEG Encode Horizontal Display Period Register	220
REG[0266h] Memory Image JPEG Encode Vertical Display Period Register	220	REG[0268h] is Reserved	220

Table 10-2: S1D13719 Register Set

Register	Pg	Register	Pg
REG[0266h] Memory Image JPEG Encode Vertical Display Period Register	220	REG[0270h] Host Image JPEG Encode Control Register	221
REG[0272h] Host Image JPEG Encode Horizontal Pixel Count Register	222	REG[0274h] Host Image JPEG Encode Vertical Line Count Register	222
REG[0276h] Host Image JPEG Encode RGB Data Register 0	223	REG[0278h] Host Image JPEG Encode RGB Data Register 1	223
REG[0280h] is Reserved	223		
GPIO Registers			
REG[0300h] GPIO Configuration Register 0	224	REG[0302h] GPIO Configuration Register 1	224
REG[0304h] GPIO Input Enable Register 0	224	REG[0306h] GPIO Input Enable Register 1	224
REG[0308h] GPIO Pull Down Control Register 0	225	REG[030Ah] GPIO Pull Down Control Register 1	225
REG[030Ch] GPIO Status Register 0	225	REG[030Eh] GPIO Status Register 1	225
Overlay Registers			
REG[0310h] Average Overlay Key Color Red Data Register	226	REG[0312h] Average Overlay Key Color Green Data Register	227
REG[0314h] Average Overlay Key Color Blue Data Register	227	REG[0316h] AND Overlay Key Color Red Data Register	228
REG[0318h] AND Overlay Key Color Green Data Register	228	REG[031Ah] AND Overlay Key Color Blue Data Register	229
REG[031Ch] OR Overlay Key Color Red Data Register	229	REG[031Eh] OR Overlay Key Color Green Data Register	230
REG[0320h] OR Overlay Key Color Blue Data Register	230	REG[0322h] INV Overlay Key Color Red Data Register	231
REG[0324h] INV Overlay Key Color Green Data Register	231	REG[0326h] INV Overlay Key Color Blue Data Register	232
REG[0328h] Overlay Miscellaneous Register	232		
LUT1 (Main Window)			
REG[0400 - 07FCh] LUT1 Data Register 0	235	REG[0402 - 07FEh] LUT1 Data Register 1	235
LUT2 (PIP+ Window)			
REG[0800 - 08FCh] LUT2 Data Register 0	236	REG[0802 - 08FEh] LUT2 Data Register 1	236
Resizer Operation Registers			
REG[0930h] Global Resizer Control Register	237	REG[0932h] through REG[093Eh] are Reserved	239
REG[0940h] View Resizer Control Register	240	REG[0944h] View Resizer Start X Position Register	240
REG[0946h] View Resizer Start Y Position Register	241	REG[0948h] View Resizer End X Position Register	241
REG[094Ah] View Resizer End Y Position Register	241	REG[094Ch] View Resizer Operation Setting Register 0	242
REG[094Eh] View Resizer Operation Setting Register 1	244	REG[0960h] Capture Resizer Control Register	245
REG[0964h] Capture Resizer Start X Position Register	246	REG[0966h] Capture Resizer Start Y Position Register	247
REG[0968h] Capture Resizer End X Position Register	247	REG[096Ah] Capture Resizer End Y Position Register	247
REG[096Ch] Capture Resizer Operation Setting Register 0	248	REG[096Eh] Capture Resizer Operation Setting Register 1	250
JPEG Module Registers			
REG[0980h] JPEG Control Register	251	REG[0982h] JPEG Status Flag Register	256
REG[0984h] JPEG Raw Status Flag Register	260	REG[0986h] JPEG Interrupt Control Register	263
REG[0988h] is Reserved	265	REG[098Ah] JPEG Code Start/Stop Control Register	265
REG[098Ch] through REG[098Eh] are Reserved	265		
JPEG FIFO Setting Register			
REG[09A0h] JPEG FIFO Control Register	266	REG[09A2h] JPEG FIFO Status Register	268
REG[09A4h] JPEG FIFO Size Register	269	REG[09A6h] JPEG FIFO Read/Write Port Register	270
REG[09A8h] JPEG FIFO Valid Data Size Register	270	REG[09AAh] JPEG FIFO Read Pointer Register	271
REG[09ACh] JPEG FIFO Write Pointer Register	271	REG[09B0h] Encode Size Limit Register 0	272
REG[09B2h] Encode Size Limit Register 1	272	REG[09B4h] Encode Size Result Register 0	272
REG[09B6h] Encode Size Result Register 1	272	REG[09B8h] JPEG File Size Register 0	273
REG[09BAh] JPEG File Size Register 1	273	REG[09BCh] JPEG FIFO Address Offset Register	273
JPEG Line Buffer Setting Register			
REG[09C0h] JPEG Line Buffer Status Flag Register	274	REG[09C2h] JPEG Line Buffer Raw Status Flag Register	275
REG[09C4h] JPEG Line Buffer Raw Current Status Register	275	REG[09C6h] JPEG Line Buffer Interrupt Control Register	276
REG[09C8h] through REG[09CEh] are Reserved	276	REG[09D0h] JPEG Line Buffer Configuration Register	277
REG[09D2h] JPEG Line Buffer Address Offset Register	277	REG[09D4h] through REG[09DEh] are Reserved	277

Table 10-2: S1D13719 Register Set

Register	Pg	Register	Pg
REG[09E0h] JPEG Line Buffer Read/Write Port Register	278		
Interrupt Control Registers			
REG[0A00h] Interrupt Status Register	279	REG[0A02h] Interrupt Control Register 0	280
REG[0A04h] Interrupt Control Register 1	281	REG[0A06h] Debug Status Register	282
REG[0A08h] Interrupt Control for Debug Register	283	REG[0A0Ah] Host Cycle Interrupt Status Register	284
REG[0A0Ch] Host Cycle Interrupt Control Register	284	REG[0A0Eh] Cycle Time Out Control Register	285
REG[0A10h] is Reserved	285	REG[0A20h] Indirect Interface Interrupt Flag Register	286
REG[0A22h] Indirect Interface Interrupt Control Register	287	REG[0A40h] Interrupt Request Status Register	288
JPEG Encode Performance Register			
REG[0F00h] JPEG Encode Performance Register	289	REG[0F02h] JPEG Extended Address Register	289
JPEG Codec Registers			
REG[1000h] Operation Mode Setting Register	291	REG[1002h] Command Setting Register	292
REG[1004h] JPEG Operation Status Register	293	REG[1006h] Quantization Table Number Register	293
REG[1008h] Huffman Table Number Register	294	REG[100Ah] DRI Setting Register 0	295
REG[100Ch] DRI Setting Register 1	295	REG[100Eh] Vertical Pixel Size Register 0	296
REG[1010h] Vertical Pixel Size Register 1	296	REG[1012h] Horizontal Pixel Size Register 0	297
REG[1014h] Horizontal Pixel Size Register 1	297	REG[1016h] Through REG[101Ah] are Reserved	297
REG[101Ch] RST Marker Operation Setting Register	298	REG[101Eh] RST Marker Operation Status Register	298
REG[1020 - 1066h] Insertion Marker Data Register	299	REG[1200 - 127Eh] Quantization Table No. 0 Register	299
REG[1280 - 12FEh] Quantization Table No. 1 Register	300	REG[1400 - 141Eh] DC Huffman Table No. 0 Register 0	300
REG[1420 - 1436h] DC Huffman Table No. 0 Register 1	300	REG[1440 - 145Eh] AC Huffman Table No. 0 Register 0	301
REG[1460 - 15A2h] AC Huffman Table No. 0 Register 1	301	REG[1600 - 161Eh] DC Huffman Table No. 1 Register 0	303
REG[1620 - 1636h] DC Huffman Table No. 1 Register 1	303	REG[1640 - 165Eh] AC Huffman Table No. 1 Register 0	304
REG[1660 - 17A2h] AC Huffman Table No. 1 Register 1	304		
SD Memory Card Interface Registers			
REG[6000h] SD Memory Card Configuration Register 0	306	REG[6004h] SD Memory Card Configuration Register 2	306
REG[6008h] SD Memory Card Interrupt Flag Register	308	REG[600Ah] SD Memory Card Interrupt Enable Register	309
REG[600Ch] SD Memory Card Interrupt Clear Register	310	REG[6100h] SD Memory Card Control Register 0	311
REG[6102h] SD Memory Card Control Register 1	313	REG[6104h] SD Memory Card Function Register	314
REG[6106h] SD Memory Card Status Register	316	REG[6108h] SD Memory Card Data Length Register 0	317
REG[610Ah] SD Memory Card Data Length Register 1	317	REG[610Ch] SD Memory Card Command Register	317
REG[610Eh] SD Memory Card Timer Register	318	REG[6110h] SD Memory Card Parameter Register 0	318
REG[6112h] SD Memory Card Parameter Register 1	318	REG[6114h] SD Memory Card Parameter Register 2	318
REG[6116h] SD Memory Card Parameter Register 3	319	REG[6118h - 611Eh] SD Memory Card Data Registers	319
REG[6120h] SD Memory Card Response Register 0	319	REG[6122h] SD Memory Card Response Register 1	320
REG[6124h] SD Memory Card Response Register 2	320	REG[6126h] SD Memory Card Response Register 3	320
REG[6128h] SD Memory Card Response Register 4	320	REG[612Ah] SD Memory Card Response Register 5	321
REG[612Ch] SD Memory Card Response Register 6	321	REG[612Eh] SD Memory Card Response Register 7	321
REG[6130h] SD Memory Card Response Register 8	321	REG[6132h] SD Memory Card Response Register 9	322
REG[6134h] SD Memory Card Response Register A	322	REG[6136h] SD Memory Card Response Register B	322
REG[6138h] SD Memory Card Response Register C	322	REG[613Ah] SD Memory Card Response Register D	323
REG[613Ch] SD Memory Card Response Register E	323	REG[613Eh] SD Memory Card Response Register F	323

Table 10-2: S1D13719 Register Set

Register	Pg	Register	Pg
2D BitBLT Registers			
REG[8000h] BitBLT Control Register 0	324	REG[8002h] BitBLT Control Register 1	324
REG[8004h] BitBLT Status Register 0	325	REG[8006h] is Reserved	326
REG[8008h] BitBLT Command Register 0	326	REG[800Ah] BitBLT Command Register 1	327
REG[800Ch] BitBLT Source Start Address Register 0	328	REG[800Eh] BitBLT Source Start Address Register 1	328
REG[8010h] BitBLT Destination Start Address Register 0	329	REG[8012h] BitBLT Destination Start Address Register 1	329
REG[8014h] BitBLT Memory Address Offset Register	329	REG[8018h] BitBLT Width Register	329
REG[801Ch] BitBLT Height Register	330	REG[8020h] BitBLT Background Color Register	330
REG[8024h] BitBLT Foreground Color Register	330	REG[8030h] BitBLT Interrupt Status Register	330
REG[8032h] BitBLT Interrupt Control Register	331	REG[10000h] 2D BitBLT Data Memory Mapped Region Register	331

10.3 Register Restrictions

All reserved bits must be set to 0 unless otherwise specified. Writing a value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect.

Some registers are only accessible when certain conditions exist. Any attempts to read/write in-accessible registers are invalid. The following restrictions apply.

- REG[0000h] through REG[0018h] and REG[0300h] through REG[030Eh] are always accessible.
- REG[0000h] through REG[0018h] and REG[0300h] through REG[030Eh] are not reset by a Software Reset.
- When power save mode is enabled (REG[0014h] bit 0 = 1), REG[0030h] through REG[0A0Eh] except REG[0300h] through REG[030Eh] are not accessible.
- When the JPEG Codec is disabled (REG[0980h] bit 0 = 0), REG[1000h] through REG[17A2h] are not accessible.
- When the SD Memory Card Interface is disabled (REG[6000h] bit 0 = 0), REG[6100h] through REG[613Eh] are not accessible.

10.4 Register Description

10.4.1 System Configuration Registers

REG[0000h] Product Information Register Default = 8070h							Read Only
Display Buffer Size bits 7-0							
15	14	13	12	11	10	9	8
Product Code bits 5-0						Revision Code bits 1-0	
7	6	5	4	3	2	1	0

bits 15-8 Display Buffer Size bits [7:0] (Read Only)
These bits indicate the size of the SRAM display buffer measured in 4K byte increments. The S1D13719 display buffer is 512K bytes and these bits return a value of 128 (80h).

REG[0000h] bits 15-8 = display buffer size ÷ 4K bytes
= 512K bytes ÷ 4K bytes
= 128 (80h)

bits 7-2 Product Code bits [5:0] (Read Only)
These bits indicate the product code. The product code for the S1D13719 is 011100b (1Ch).

bits 1-0 Revision Code bits [1:0] (Read Only)
These bits indicate the revision code. The revision code is 00b.

REG[0002h] Configuration Pins Status Register Default = 0000h							Read Only
n/a							
15	14	13	12	11	10	9	8
CNF[7:0] Status							
7	6	5	4	3	2	1	0

bits 7-0 CNF[7:0] Status (Read Only)
These status bits return the status of the configuration pins CNF[7:0]. CNF[7:0] are latched at the rising edge of RESET#. For a functional description of each configuration bit (CNF[7:0]), see Section 5.3, “Summary of Configuration Options”.

REG[0004h] SD Memory Card Interface Enable Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
SD Memory Card Interface Enable	n/a			AB[18:3] Pull-down Control	n/a		

bit 7 SD Memory Card Interface Enable
When this bit = 0, the SD memory card interface is disabled.
When this bit = 1, the SD memory card interface is enabled.GPIO[19-11] pins are assigned for the card interface.

bit 3 AB[18:3] Pull-down Control
This bit controls the pull-down resistance for the AB[18:3] pins when the indirect interface is selected. When the direct interface is selected, this bit has no effect and the pull-down resistance is disabled.
When this bit = 0, the pull-down resistance is enabled (default).
When this bit = 1, the pull-down resistance is disabled.

REG[0006h] Bus Timeout Setting Register
Default = 0000h — Read/Write

15	14	13	13	11	10	9	8
n/a						Host I/F Setup Timing Control	Reserved

7	6	5	4	3	2	1	0
n/a					Bus Timeout Reset Interrupt Status (RO)	Bus Timeout Reset Disable	Bus Timeout Reset Interrupt Disable

bit 9 Host I/F Setup Timing Control
When this bit = 0, the setup timing of read mode is 5ns (default).
When this bit = 1, the setup timing of read mode is 0ns.

bit 8 Reserved.
The default value for this bit is 0.

bit 2 Bus Timeout Reset Interrupt Status (Read Only).
This is the status bit for the bus timeout reset function. Bus timeout reset occurs when the WAIT# signal is active for 2 or 3 cycles.
This is the status bit for the bus timeout function.
When this bit = 0, a bus timeout has not occurred.
When this bit = 1, a bus timeout has occurred.

This flag is cleared by the Bus Timeout Reset Interrupt Disable bit (REG[0006h] bit 0).

bit 1 Bus Timeout Reset Disable
This bit controls the Bus Timeout Reset function of the S1D13719. If a bus timeout occurs, the Bus Timeout Reset Interrupt Status is set (REG[0006h] bit 2) and the chip is reset.
When this bit = 0, the bus timeout reset function is enabled (default).
When this bit = 1, the bus timeout reset function is disabled.

Note

When the internal PLL is disabled (REG[0012h] bit 0 = 1), the Bus Timeout function must be disabled (REG[0006h] bit 1 = 1).

bit 0 Bus Timeout Reset Interrupt Disable
This bit controls the bus timeout reset interrupt and is used to clear the Bus Timeout Reset Interrupt Status (REG[0006h] bit 2).
When this bit = 0, the Bus Timeout Interrupt is enabled (default).
When this bit = 1, the Bus Timeout Interrupt is disabled.

When this bit is written as 1, the Bus Timeout Flag (REG[0006h] bit 2) is cleared.

10.4.2 Clock Setting Registers

REG[000Eh] PLL Setting Register 0
Default = 1BE8h Read/Write

N-Counter bits 3-0				L-Counter bits 9-6			
15	14	13	12	11	10	9	8
L-Counter bits 5-0						V-Divider bits 1-0	
7	6	5	4	3	2	1	0

Note
Before setting this register, power save mode must be enabled (REG[0014h] bit 0 = 1) and the PLL must be disabled (REG[0012h] bit 0 = 1). For more information, see Figure 11-1: "Power-On/Power-Off Sequence," on page 332 or Figure 11-2: "Power Modes," on page 333.

bits 15-12 N-Counter bits [3:0]
bits 11-2 L-Counter bits [9:0]
These bits are used together to configure the PLL Output (in MHz) and must be set according to the following formula.

PLL Output = (N-Counter +1) x (L-Counter +1) x CLKI
= NN x LL x CLKI

Where:
PLL Output is the desired PLL output frequency in MHz (55MHz max)
N-Counter is the value in bits 15-12
L-Counter is the value in bits 11-2
CLKI is the PLL reference frequency (should always be 32.768kHz)

Table 10-3: PLL Setting Example

Target Freq. (MHz)	NN	LL	NN x LL	REG[000Eh]	POUT (MHz)
40	4	305	1220	34C0h	39.98
45	6	229	1374	5390h	45.02
48.76	16	93	1488	F194h	48.76
50	15	122	1830	E1E4h	49.97
54	16	103	1648	F198h	54.00
55	2	839	1678	1D18h	54.98

Note
To optimize power consumption, use the largest NN value possible.

bits 1-0 V-Divider bits [1:0]
These bits are used to fine tune the PLL output jitter. The V-Divider bits represent a value as shown in the following table. The V-Divider bits must be set such that the following formula is valid.

$$100\text{MHz} \leq \text{PLL Output x V-Divider} \leq 410\text{MHz}$$

Table 10-4: V-Divider

REG[000Eh] bits 1-0	V-Divider
00	see note
01	2
10	4
11	8

Where:
PLL Output in MHz (55MHz max) generated by bits 15-12 (N-Counter) and bits 11-2 (L-Counter)
V-Divide is the value from Table 10-4:

Note
Setting the V-Divider value to 00 provides the lowest possible power consumption, but the most jitter. Specific system design requirements should be considered to achieve the optimal setting.

REG[0010h] PLL Setting Register 1 Default = 0000h							Read/Write
VCO Kv Set bits 3-0				n/a			
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0

Note

Before setting this register, power save mode must be enabled (REG[0014h] bit 0 = 1) and the PLL must be disabled (REG[0012h] bit 0 = 1). For more information, see Figure 11-1: "Power-On/Power-Off Sequence," on page 332 or Figure 11-2: "Power Modes," on page 333.

bits 15-12 VCO Kv Set bits [3:0]

These bits are used to fine tune the PLL output jitter. These bits should be set as follows.

If 100MHz ≤ (PLL Output x V-Divider) ≤ 200MHz, set these bits to 0010.
If 200MHz < (PLL Output x V-Divider) ≤ 300MHz, set these bits to 0101.
If 300MHz < (PLL Output x V-Divider) ≤ 410MHz, set these bits to 0111.
All other non-zero values for these bits are reserved.

Where:

PLL Output is the desired PLL output frequency in MHz and is generated using REG[000Eh] bits 15-12 and REG[000Eh] bits 11-2
V-Divide is the value from Table 10-4: and is controlled by REG[000Eh] bits 1-0

Note

Setting the value of these bits to 0000b provides the lowest possible power consumption, but the most jitter. Specific system design requirements should be considered to achieve the optimal setting.

REG[0012h] PLL Setting Register 2 Default = 0001h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a					Reserved	Reserved	PLL Disable
7	6	5	4	3	2	1	0

Note
For more information on the PLL and clock structure, see Section 9, "Clocks".

bit 2 Reserved.
The default value for this bit is 0.

bit 1 Reserved.
The default value for this bit is 0.

bit 0 PLL Disable
This bit controls the internal PLL. The PLL must be configured using PLL Setting Register 0 (REG[000Eh]) and PLL Setting Register 1 (REG[0010h]) before enabling this bit.
When this bit = 0, the PLL is enabled. When this option is selected, the PLL output is the source for the system clock divider.
When this bit = 1, the PLL is disabled (default). When this option is selected, the external clock, CLKI, is the source for the system clock divider.

Note
There may be up to a 100ms delay before the PLL output becomes stable. The S1D13719 must not be accessed during this time.

REG[0014h] Miscellaneous Configuration Register Default = 04D1h							Read/Write
Reserved	Parallel Bypass Pull-down Control	Parallel Bypass Direction Control	LCD Bypass Enable	LCD Bypass Mode select bits 3-0			
15	14	13	12	11	10	9	8
VNDP Status (RO)	Memory Power Save Status (RO)	n/a	Bypass Input Pull-up/down Control	Parallel Bypass Chip Select Mode	Reserved	Reserved	Power Save Mode Enable
7	6	5	4	3	2	1	0

bit 15 Reserved
The default value for this bit is 0.

bit 14 Parallel Bypass Pull-down Control
This bit controls the pull-down resistance for the FPDAT[17:0] pins when they are configured as inputs during Parallel Bypass mode (see REG[0014h] bit 13). When the FPDAT[17:0] pins are configured as outputs, this bit has no effect and the pull-down resistance is disabled.
When this bit = 0, the pull-down resistance is disabled (default).
When this bit = 1, the pull-down resistance is enabled.

Note
When LCD Bypass Mode is enabled (REG[0014h] bit 12 = 1), the DB[15:0] inputs must not be left floating or Hi-Z.

bit 13 Parallel Bypass Direction Control
When Parallel Bypass mode is enabled, the FPDAT[17:0] pins may be configured as inputs or outputs as controlled by this bit.
When this bit = 0, the pins are configured as outputs (default).
When this bit = 1, the pins are configured as inputs.

bit 12 LCD Bypass Enable
This bit controls LCD Bypass mode. All LCD Bypass settings should be configured before enabling LCD Bypass mode.
When this bit = 0, LCD Bypass mode is disabled (default).
When this bit = 1, LCD Bypass mode is enabled.

Note
This bit must not be enabled if the LCD interface is busy (REG[0038h] = 1).

bits 11-8 LCD Bypass Mode Select bits [3:0]l
These bits select the LCD Bypass Mode as follows.

Table 10-5: LCD Bypass Mode Selection

REG[0014h] bits 11-8	Bypass Mode	LCD Panel	Interface	Data Terminal
0000b	F	LCD2	Parallel	FPDAT[15:0]
0001b	G	LCD2	Parallel	FPDAT[17:0]
0010b	C	LCD1	Parallel	FPDAT[15:0]
0011b	D	LCD1	Parallel	FPDAT[17:0]
0100b (default)	A	LCD2	Serial	FSO
0101b	Reserved			
0110b	B	LCD1	Serial	FSO
0111b - 1000b	Reserved			
1001b	H	LCD2	Parallel	FPDAT[17:10], FPDAT[8:1]
1010b	Reserved			
1011b	E	LCD1	Parallel	FPDAT[17:10], FPDAT[8:1]
1100b - 1111b	Reserved			

bit 7 Vertical Non-Display Period Status (Read Only)
If an RGB interface panel is selected for LCD1 (Mode 1/Mode 4, see REG[0032h] bits 1-0), this status bit indicates whether the panel is in a Vertical Non-Display Period. This bit has no effect when Mode 2 or Mode 3 is selected.
When this bit = 0, the LCD panel output is in a Vertical Display Period.
When this bit = 1, the LCD panel output is in a Vertical Non-Display Period.

bit 6 Memory Power Save Status (Read Only)
This bit indicates the status of the memory controller and must be checked before enabling Power Save Mode (REG[0014h] bit 0) or disabling the PLL (REG[0012h] bit 0). For further information on using this bit, see Figure 7-4: “Power-On Sequence,” on page 57 and Figure 7-5: “Power-Off Sequence,” on page 57.
When this bit = 0, the memory controller is powered up.
When this bit = 1, the memory controller is idling and the system clock source can be disabled.

bit 4 Bypass Input Pull-up/down Control
This bit controls the active pull-up/pull-down resistors on the host serial/parallel input pins (SCS#, SCLK, SA0, SI). When the serial/parallel input port is unused (Hi-Z), set this bit to 1.
When this bit = 0, the pull-up/pull-down resistors are inactive.
When this bit = 1, the pull-up/pull-down resistors are active and the pins are affected as follows (default).

Table 10-6: Serial/Parallel Pull-up/Pull-down Resistors

Pin	Type
SCS#	Pull-up
SCLK	Pull-down
SA0	Pull-down
SI	Pull-down

bit 3 Parallel Bypass Chip Select Mode
This bit controls the chip select mode used when Parallel Bypass mode is enabled.

Table 10-7: Parallel Bypass Chip Select Mode

REG[0014h] bit 3	Chip Select Mode	SCS# Function	CS# Function
0	SCS# Mode	LCD Parallel Bypass	Memory/Register
1	CS# Mode	1 input	Memory/Register
		0 input	LCD Parallel Bypass

bit 2 Reserved
The default value of this bit is 0.

bit 1 Reserved
The default value of this bit is 0.

bit 0 Power Save Mode Enable
This bit controls the state of the software initiated power save mode. When power save mode is disabled, the S1D13719 is operating normally. When power save mode is enabled, the S1D13719 is in a power efficient state. For more information on the S1D13719 condition during Power Save Mode, see Section 11, “Power Save Modes”.
When this bit = 0, power save mode is disabled.
When this bit = 1, power save mode is enabled (default).

Note

Before enabling power save mode, the Display Output Port must be turned off (REG[0202h] bits 12-10 = 000b) **and** the Memory Controller Idle Status bit (REG[0014h] bit 6) must return a 1.

REG[0016h] Software Reset Register							
Default = not applicable							Write Only
Software Reset bits 15-8							
15	14	13	12	11	10	9	8
Software Reset bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Software Reset bits [15:0] (Write Only)
When any value is written to these bits, **all registers are reset to their default values**. A software reset via this register **does not clear the display buffer**. For further information on software reset, see Section 11.1.2, “Reset”.

REG[0018h] System Clock Setting Register							
Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a						System Clock Divide Select bits 1-0	
7	6	5	4	3	2	1	0

bits 1-0 System Clock Divide Select bits [1:0]
These bits determine the divide ratio for the system clock. The source is selectable, using REG[0012h] bit 0, between either the PLL output (see REG[000Eh]-REG[0012h]) or an external clock source (CLKI).

Table 10-8: System Clock Divide Ratio Selection

REG[0018h] bits 1-0	System Clock Divide Ratio
00b	1:1
01b	2:1
10b	3:1
11b	4:1

Note
For more information on clocks, see Section 9, “Clocks”.

10.4.3 Indirect Interface Registers

These registers are used for the Indirect Interface modes only. The indirect interface is selected at RESET# using the configuration bits CNF[4:2] (see Table 5-2: “Summary of Power-On/Reset Options,” on page 39).

REG[0020h] Indirect Interface Memory Rectangular Address Offset Register
Default = 0000h Read/Write

n/a					Indirect Interface Memory Rectangular Address Offset bits 10-8		
15	14	13	12	11	10	9	8
Indirect Interface Memory Rectangular Address Offset bits 7-1							n/a
7	6	5	4	3	2	1	0

bits 10-1 Indirect Interface Memory Rectangular Address Offset bits [10:1]
These bits are used for Indirect Interface modes only.
These bits determine the memory address offset for the indirect interface when rectangular memory address mode is selected (REG[0024h] bit 15 = 1).
REG[0020h] bits 10-1 = Memory Rectangular Address Offset - 1 word

REG[0022h] Indirect Interface Memory Address Register 0
Default = 0000h Read/Write

Indirect Interface Memory Address bits 15-8							
15	14	13	12	11	10	9	8
Indirect Interface Memory Address bits 7-1							Indirect Interface Read/Write Cycle
7	6	5	4	3	2	1	0

REG[0024h] Indirect Interface Memory Address Register 1
Default = 0000h Read/Write

Memory Address Mode	n/a						
15	14	13	12	11	10	9	8
n/a					Indirect Interface Memory Address bits 18-16		
7	6	5	4	3	2	1	0

REG[0024h] bits 2-0
REG[0022h] bits 15-1 Indirect Interface Memory Address bits [18:1]
These bits are used for Indirect Interface modes only.
These bits determine the memory start address for each memory access. After a completed memory access, this register is incremented automatically.

Note
Please set REG[0022h] after setting REG[0024h].

REG[0022h] bit 0 Indirect Interface Read/Write Cycle
This bit is used for Indirect Interface modes only.
This bit determines whether a memory read or write operation takes place.
When this bit = 0, a write operation takes place (default).
When this bit = 1, a read operation takes place.

REG[0024h] bit 15 Memory Address Mode
This bit is used for Indirect Interface modes only.
This bit selects the memory address mode used for the indirect interface.
When this bit = 0, linear memory address mode is selected (default).
When this bit = 1, rectangular memory address mode is selected.

REG[0026h] Indirect Interface Memory Rectangular Width Register Default = 0000h					Read/Write		
n/a					Indirect Interface Memory Rectangular Width bits 10-8		
15	14	13	12	11	10	9	8
Indirect Interface Memory Rectangular Width bits 7-1							n/a
7	6	5	4	3	2	1	0

bits 10-1 Indirect Interface Memory Rectangular Width bits [10:1]
These bits are used for Indirect Interface modes only.
These bits determine the memory rectangular width for the indirect interface when rectangular memory address mode is selected (REG[0024h] bit 15 = 1).
REG[0026h] bits 10-1 = Memory Rectangular Width - 1 word

REG[0028h] Indirect Interface Memory Access Port Register Default = not applicable							Read/Write
Indirect Interface Memory Access Port bits 15-8							
15	14	13	12	11	10	9	8
Indirect Interface Memory Access Port bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Indirect Interface Memory Access Port bits [15:0]
This register is used for Indirect Interface modes only.
These bits are the memory read/write port for the Indirect Interface.

REG[002Ch] Indirect Interface JPEG Status Register Default = 0000h							Write Only
Reserved	JPEG LB Receive Buffer Clear (WO)	Reserved			JPEG LB Transmit Buffer Clear (WO)	Reserved	
15	14	13	12	11	10	9	8
Reserved	JPEG FIFO Receive Buffer Clear (WO)	Reserved			JPEG FIFO Transmit Buffer Clear (WO)	Reserved	
7	6	5	4	3	2	1	0

Note
This register is used for Indirect Interface modes only and must not be accessed when using Direct Interface modes.

bit 15 Reserved
The default value of this bit is 0.

bit 14 — JPEG Line Buffer Receive Buffer Clear (Write Only)
This bit clears the receive buffer portion of the JPEG Line Buffer. The buffer should be cleared before starting the JPEG operation because when a JPEG Line Buffer read error occurs corrupted data may remain in the buffer. See REG[0A20h] and REG[0A22h] for information on the JPEG Line Buffer Error Interrupts.
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit clears the receive buffer.

bits 13-11 — Reserved
The default value for these bits is 0.

bit 10 — JPEG Line Buffer Transmit Buffer Clear (Write Only)
This bit clears the transmit buffer portion of the JPEG Line Buffer. The buffer should be cleared before starting the JPEG operation because when a JPEG Line Buffer write error occurs corrupted data may remain in the buffer. See REG[0A20h] and REG[0A22h] for information on the JPEG Line Buffer Error Interrupts.
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit clears the transmit buffer.

bits 9-7 — Reserved
The default value for these bits is 0.

bit 6 — JPEG FIFO Receive Buffer Clear (Write Only)
This bit clears the receive buffer portion of the JPEG FIFO. The buffer should be cleared before starting the JPEG operation because when a JPEG FIFO read error occurs corrupted data may remain in the buffer. See REG[0A20h] and REG[0A22h] for information on the JPEG FIFO Error Interrupts.
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit clears the receive buffer.

bits 5-3 — Reserved
The default value for these bits is 0.

bit 2 — JPEG FIFO Transmit Buffer Clear (Write Only)
This bit clears the transmit buffer portion of the JPEG FIFO. The buffer should be cleared before starting the JPEG operation because when a JPEG FIFO write error occurs corrupted data may remain in the buffer. See REG[0A20h] and REG[0A22h] for information on the JPEG FIFO Error Interrupts.
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit clears the transmit buffer.

bits 1-0 — Reserved
The default value for these bits is 0.

10.4.4 LCD Panel Interface Generic Setting Register

REG[0030h] LCD Interface Clock Setting Register Default = 0000h							Read/Write
n/a					Serial Clock Divide Select bits 2-0		
15	14	13	12	11	10	9	8
n/a			Pixel Clock Divide Select bits 4-0				
7	6	5	4	3	2	1	0

bits 10-8 Serial Clock Divide Select bits [2:0]
These bits specify the divide ratio for the serial clock. The clock source for the serial clock is the system clock (see Figure 9-1: "Clock Diagram," on page 113). If LCD1 or LCD2 is not a serial interface type LCD panel (REG[0032h] bits 1-0) or if Serial Port Bypass is enabled (REG[0032h] bit 8 = 1), these bits are ignored.

Table 10-9: Serial Clock Divide Ratio Selection

REG[0030h] bits 10-8	Serial Clock Divide Ratio
000b	2:1
001b	4:1
010b	6:1
011b	8:1
100b	10:1
101b	12:1
110b	14:1
111b	16:1

bits 4-0 Pixel Clock Divide Select bits [4:0]
These bits specify the divide ratio for the pixel clock. The clock source for the pixel clock is the system clock (see Figure 9-1: “Clock Diagram,” on page 113). When LCD1 is an RGB type panel (REG[0032h] bits 1-0 = 00b or 01b), the pixel clock is the same as the shift clock. When LCD1 or LCD2 is a parallel interface type panel (REG[0032h] bits 1-0 = 10b or 11b), the pixel clock is used for the parallel data output timing clock.

Table 10-10: Pixel Clock Divide Selection

REG[0030h] bits 4-0	Pixel Clock Divide Ratio
00000b	2:1 (see Note)
00001b	4:1
00010b	6:1
00011b	8:1
00100b	10:1
00101b	12:1
00110b	14:1
00111b	16:1
01000b	18:1
01001b	20:1
01010b	22:1
01011b	24:1
01100b	26:1
01101b	28:1
01110b	30:1
01111b	32:1
10000b	34:1
10001b	36:1
10010b	38:1
10011b	40:1
10100b	42:1
10101b	44:1
10110b	46:1
10111b	48:1
11000b - 11111b	Reserved

Note

SwivelView should not be used when the 2:1 Pixel Clock Divide Ratio is used (REG[0202h] bits 5-4 = 00b and bits 1-0 = 00b).

<table>
<tr><td colspan="8">REG[0032h] LCD Interface Configuration Register
Default = 0000h — Read/Write</td></tr>
<tr><td colspan="6">RGB Panel Type bits 5-0</td><td>DRDY Polarity Select</td><td>FPCS1# Polarity Select</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>FPSHIFT Polarity Select</td><td colspan="3">RGB Interface Panel Data Bus Width bits 2-0</td><td colspan="2">n/a</td><td colspan="2">Panel Interface bits 1-0</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
</table>

bits 15-10 RGB Panel Type bits [5:0]
When the panel interface for LCD1 is RGB (REG[0032h] bits 1-0 = 00b), these bits determine the RGB panel type. When LCD1 is not an RGB interface (REG[0032h] bits 1-0 = 10b or 11b), these bit are ignored.

Table 10-11: RGB Panel Type Selection

REG[0032h] bits 15-10	RGB Panel Type (LCD1)
000000b	Generic TFT, ND-TFD
000001b	HR-TFT
000010b	Casio TFT
000011b	TFT Type 2
000100b	TFT Type 3
000101b - 101111b	Reserved
110000b	α-TFT
110001b - 111111b	Reserved

bit 9 DRDY Polarity Select
This bit sets the active polarity of the data ready signal for RGB type panels.
When this bit = 0, DRDY is active high.
When this bit = 1, DRDY is active low.

bit 8 FPCS1# Polarity Select
This bit sets the active polarity of the LCD1 interface chip select for parallel and serial type panels.
When this bit = 0, FPCS1# is active low.
When this bit = 1, FPCS1# is active high.

bit 7 FPSHIFT Polarity Select
This bit sets the polarity of the shift clock for RGB type panels (inverts FPSHIFT).
When this bit = 0, all panel interface signals change at the rising edge of FPSHIFT.
When this bit = 1, all panel interface signals change at the falling edge of FPSHIFT.

bits 6-4 RGB Interface Panel Data Bus Width bits [2:0]
These bits only have an effect when a RGB interface panel is selected (REG[0032h] bits 1-0 = 00b or 01b). These bits determine the RGB Interface Panel Data Bus size. Unused FPDAT[17:0] pins are forced low and unused GPIO[9:4] pins are used as GPIOs.

Table 10-12: RGB Interface Panel Data Bus Width Selection

REG[0032h] bits 6-4	RGB Interface Panel Data Bus Width (LCD1)
000b	9-bit
001b	12-bit
010b	16-bit
011b	18-bit
100b	24-bit
101b - 111b	Reserved

bits 1-0 Panel Interface bits [1:0]
These bits determine the LCD1 and LCD2 interface types.

Table 10-13: Panel Interface Selection

REG[0032h] bits 1-0	Mode	LCD1 Panel Interface	LCD2 Panel Interface
00b	1	RGB Interface	Serial Interface (RAM integrated)
01b	4	RGB Interface	Parallel Interface (RAM integrated)
10b	2	Parallel Interface (RAM integrated)	Serial Interface (RAM integrated)
11b	3	Parallel Interface (RAM integrated)	Parallel Interface (RAM integrated)

REG[0034h] LCD Interface Command Register Default = 0000h							Read/Write
LCD Interface Command Register bits 15-8							
15	14	13	12	11	10	9	8
LCD Interface Command Register bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 LCD Interface Command Register bits [15:0]
These bits are only for parallel/serial interface panels on LCD1 or LCD2 and have no effect for RGB type panels. These bits form the command register for the LCD1/LCD2 parallel/serial interfaces. For 8-bit parallel or serial interfaces, only the lower byte is used. When the LCD interface is busy (REG[0038h] bit 0 = 1), this register must not be written. When the LCD interface is not busy (REG[0038h] bit 0 = 0), the command transfer starts when this register is written. When the command transfer starts, the FPA0 pin is driven low or high depending on the state of the P/C Polarity Invert Enable bit (REG[003Ch] bit 7).

Note
If the LCD1 serial data type is set to uWIRE (REG[0054h] bits 7-5 = 10xb) , the upper byte of REG[0034h] is used for A[7:0] and the lower byte is used for D[7:0].

REG[0036h] LCD Interface Parameter Register Default = 0000h							Read/Write
LCD Interface Parameter Register bits 15-8							
15	14	13	12	11	10	9	8
LCD Interface Parameter Register bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 LCD Interface Parameter Register bits [15:0]
These bits are only for parallel/serial interface panels on LCD1 or LCD2 and have no effect for RGB type panels. These bits form the parameter register for the LCD1/LCD2 parallel/serial interfaces. For 8-bit parallel or serial interfaces, only the lower byte is used. When the LCD interface is busy (REG[0038h] bit 0 = 1), this register must not be written. When the LCD interface is not busy (REG[0038h] bit 0 = 0), data transfer starts when this register is written. When the data transfer starts, the FPA0 pin is driven high or low depending on the state of the P/C Polarity Invert Enable bit (REG[003Ch] bit 7).

Note
If the LCD1 serial data type is set to uWIRE (REG[0054h] bits 7-5 = 10xb) , the upper byte of REG[0034h] is used for A[7:0] and the lower byte is used for D[7:0].

REG[0038h] LCD Interface Status Register Default = 0000h							Read Only
n/a							
15	14	13	12	11	10	9	8
n/a							LCD Interface Status
7	6	5	4	3	2	1	0

bit 0 LCD Interface Status (Read Only)
This bit indicates the status of the LCD1 or LCD2 serial/parallel interface.
When this bit = 0, the LCD1 or LCD2 serial/parallel interface is not busy (or ready).
When this bit = 1, the LCD1 or LCD2 serial/parallel interface is busy.

REG[003Ah] LCD Interface Frame Transfer Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a							LCD Interface Frame Transfer Trigger
7	6	5	4	3	2	1	0

bit 0 LCD Interface Frame Transfer Trigger
This bit is only for parallel/serial interface panels on LCD1 or LCD2 and has no effect for RGB type panels. This bit is the trigger to transfer 1 frame of data to the LCD interface.
When this bit is set to 1 and the LCD interface is busy (REG[0038h] bit 0 = 1), the frame transfer request is ignored. Once the LCD interface is no longer busy, this bit is cleared without transferring any data.
When this bit is set to 1 and the LCD interface status is not busy (REG[0038h] bit 0 = 0), 1 frame of data is transferred to the LCD interface. When the data transfer is finished, this bit is cleared automatically.

Note

When LCD Interface Auto Transfer is enabled (REG[003Ch] bit 0 = 1), this bit remains high (1).

REG[003Ch] LCD Interface Transfer Setting Register
Default = 0000h Read/Write

n/a						Reserved	
15	14	13	12	11	10	9	8
P/C Polarity Invert Enable	n/a						LCD Interface Auto Frame Transfer Enable
7	6	5	4	3	2	1	0

bits 9-8 Reserved
The default value for these bits is 0.

bit 7 Parameter/Command Polarity Invert Enable
This bit is only for parallel/serial interface panels on LCD1 or LCD2 and has no effect for RGB type panels. During an LCD Interface Command (REG[0034h]) or LCD Interface Parameter (REG[0036h]) transfer, FPA0 is driven high or low based on the setting of this bit. When LCD1 is a ND-TFD 9-bit panel (REG[0054h] bits 7-5 = 001b) or LCD2 is a 9-bit serial panel (REG[005Ch] bit 5 = 1), this bit determines the MSB of the 9-bit data on FPSO.

Table 10-14: Parameter/Command Invert Setting

REG[003Ch] bit 7	FPA0 Signal Output	
	Command	Parameter
0	Low	High
1	High	Low

bit 0 LCD Interface Auto Frame Transfer Enable
This bit is only for parallel/serial interface panels on LCD1 or LCD2 and has no effect for RGB type panels. This bit controls the automatic frame transfer of one frame of display memory to the LCD interface. The frame transfer is triggered and synchronized by the camera interface vertical sync signal (CM1VREF or CM2VREF). All camera input signals are required to trigger the frame transfer.
When this bit = 0, auto frame transfer is disabled.
When this bit = 1, auto frame transfer is enabled.

When this bit = 1, the LCD Interface Status bit (REG[0038h] bit 0) is always busy. When busy, command/parameter and frame transfers cannot be sent manually. This bit should be disabled before camera input is disabled.

Note
While auto transfer is enabled, the following condition must be met or no frame transfers will take place.

1 Frame transfer cycle (time) < 1 CMVREF period (time)

Note
While auto transfer is enabled, do not vary the PCLK and CM1CLKOUT/CM2CLKOUT frequencies

10.4.5 LCD1 Setting Register

REG[0040h] LCD1 Horizontal Total Register Default = 0001h							Read/Write
n/a						Reserved	
15	14	13	12	11	10	9	8
Reserved	LCD1 Horizontal Total bits 6-0						
7	6	5	4	3	2	1	0

bits 9-7 Reserved
These bits default to 0

bits 6-0 LCD1 Horizontal Total bits [6:0]
These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the LCD1 Horizontal Total period, in 8 pixel resolution. The Horizontal Total is the sum of the Horizontal Display Period and the Horizontal Non-Display Period. The maximum Horizontal Total is 1024 pixels. These bits must not be set to 0.

REG[0040h] bits 6-0 = (Horizontal Total in pixels ÷ 8) - 1

Note

This register must be programmed such that the following formula is valid.

HT ≥ HDP + HNDP

REG[0042h] LCD1 Horizontal Display Period Register Default = 0000h							Read/Write
n/a							LCD1 HDP bit 8
15	14	13	12	11	10	9	8
LCD1 Horizontal Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 8-0 LCD1 Horizontal Display Period bits [8:0]
These bits specify the LCD1 Horizontal Display Period, in 2 pixel resolution. The Horizontal Display Period must be less than the Horizontal Total to allow for a sufficient Horizontal Non-Display Period.
REG[0042h] bits 8-0 = (Horizontal Display Period in pixels ÷ 2) - 1

Note

For Parallel interface panels (see REG[0032h] bits 1-0), the following formula must be valid.
HDP x VDP ≥ 40 pixels.

REG[0044h] LCD1 Horizontal Display Period Start Position Register Default = 0000h							Read/Write
n/a						LCD1 HDP bits 9-8	
15	14	13	12	11	10	9	8
LCD1 Horizontal Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 LCD1 Horizontal Display Period Start Position bits [9:0]
These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the LCD1 Horizontal Display Period Start Position in 1 pixel resolution.
REG[0044h] bits 9-0 = Horizontal Display Period Start Position in pixels - 9

REG[0046h] LCD1 FPLINE Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
FPLINE Polarity	FPLINE Pulse Width bits 6-0						
7	6	5	4	3	2	1	0

bit 7 FPLINE Pulse Polarity
This bit is for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and has no effect when a serial or parallel interface panel is selected. This bit selects the polarity of the horizontal sync signal (FPLINE).
When this bit = 0, the horizontal sync signal (FPLINE) is active low.
When this bit = 1, the horizontal sync signal (FPLINE) is active high.

Note
This bit does have an effect in Mode 1 LCD 2 configuration.

bits 6-0 FPLINE Pulse Width bits [6:0]
These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the width of the horizontal sync signal (FPLINE), in 1 pixel resolution.
REG[0046h] bits 6-0 = FPLINE Pulse Width in pixels - 1

REG[0048h] LCD1 FPLINE Pulse Position Register Default = 0000h							Read/Write
n/a						FPLINE Pulse Position bits 9-8	
15	14	13	12	11	10	9	8
FPLINE Pulse Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 FPLINE Pulse Position bits [9:0]
These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the position of the FPLINE pulse.
REG[0048h] bits 9-0 = FPFRAME edge to FPLINE edge in pixels - 1

REG[004Ah] LCD1 Vertical Total Register Default = 0000h							Read/Write
n/a						LCD1 Vertical Total bits 9-8	
15	14	13	12	11	10	9	8
LCD1 Vertical Total bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 LCD1 Vertical Total bits [9:0]
These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the LCD1 Vertical Total period, in 1 line resolution. The Vertical Total is the sum of the Vertical Display Period and the Vertical Non-Display Period. The maximum Vertical Total is 1024 lines.

REG[004Ah] bits 9-0 = Vertical Total in lines - 1

REG[004Ch] LCD1 Vertical Display Period Register Default = 0000h							Read/Write
n/a						Vertical Display Period bits 9-8	
15	14	13	12	11	10	9	8
Vertical Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 Vertical Display Period bits [9:0]
These bits specify the LCD1 Vertical Display period, in 1 line resolution. The Vertical Display Period must be less than the Vertical Total to allow for a sufficient Vertical Non-Display period.

REG[004Ch] bits 9-0 = Vertical Display Period in lines - 1

Note

For Parallel interface panels (see REG[0032h] bits 1-0), the following formula must be valid.

HDP x VDP $\geq$ 40 pixels

REG[004Eh] LCD1 Vertical Display Period Start Position Register Default = 0000h							Read/Write
n/a						Vertical Display Period Start Position bits 9-8	
15	14	13	12	11	10	9	8
Vertical Display Period Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 LCD1 Vertical Display Period Start Position bits [9:0]
These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the LCD1 Vertical Display Period Start Position in 1 line resolution.

REG[0050h] LCD1 FPFRAME Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
FPFRAME Polarity	n/a			Reserved	FPFRAME Pulse Width bits 2-0		
7	6	5	4	3	2	1	0

bit 7 FPFRAME Pulse Polarity
This bit is for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and has no effect when a serial or parallel interface panel is selected. This bit selects the polarity of the vertical sync signal (FPFRAME).
When this bit = 0, the vertical sync signal (FPFRAME) is active low.
When this bit = 1, the vertical sync signal (FPFRAME) is active high.

Note
This bit does have an effect in Mode 1 LCD 2 configuration.

bits 3 Reserved
The default value for these bits is 0.

bits 2-0 FPFRAME Pulse Width bits [2:0]
These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the width of the panel vertical sync signal (FPFRAME), in 1 line resolution.
REG[0050h] bits 2-0 = FPFRAME Pulse Width in lines - 1

REG[0052h] LCD1 FPFRAME Pulse Position Register Default = 0000h							Read/Write
n/a						FPFRAME Pulse Position bits 9-8	
15	14	13	12	11	10	9	8
FPFRAME Pulse Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 FPFRAME Pulse Position bits [9:0]
These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the start position of the FPFRAME signal, in 1 line resolution.

REG[0054h] LCD1 Serial Interface Setting Register
Default = 0001h — Read/Write

n/a							SPI Data Bus Width
15	14	13	12	11	10	9	8
LCD1 Serial Data Type bits 2-0			LCD1 Serial Data Direction	n/a		LCD1 Serial Clock Phase	LCD1 Serial Clock Polarity
7	6	5	4	3	2	1	0

bit 8 — SPI Data Bus Width Select
When this bit = 0, the SPI data bus width is 8-bit.
When this bit = 1, the SPI data bus width is 16-bit.

bits 7-5 — LCD1 Serial Data Type bits [2:0]
These bits determine the LCD1 Serial Data Type.

Table 10-15: LCD1 Serial Data Type Selection

REG[0054h] bits 7-5	LCD1 Serial Data Type
000b	ND-TFD 4 pins (8-bit Serial)
001b	ND-TFD 3 pins (9-bit Serial)
01xb	a-Si TFT (8-bit Serial)
10xb	uWIRE (16-bit Serial)
110b	SPI (8 or 16-bit Serial)
111b	Reserved

Note
For Mode 2 and Mode 3 configurations (see REG[0032h] bits 1-0), these bits must be set to 000b.

bit 4 — LCD1 Serial Data Direction
This bit determines the LCD1 serial data direction.
When this bit = 0, the MSB is first.
When this bit = 1, the LSB is first.

bit 1 — LCD1 Serial Clock Phase
This bit specifies the serial clock phase. See Table 10-16: “LCD1 Serial Clock Polarity and Phase Selection”.

Note
For details on timing, see Section 7.4.6, “LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing”.

bit 0 LCD1 Serial Clock Polarity
This bit determines the LCD1 serial data format.

Table 10-16: LCD1 Serial Clock Polarity and Phase Selection

REG[0054h] bit 1	REG[0054h] bit 0	Serial Data Output Changes	Idling Status of Clock
0	0	falling edge of Serial Clock	Low
	1	rising edge of Serial Clock	High
1	0	rising edge of Serial Clock	Low
	1	falling edge of Serial Clock	High

Note
For details on timing, see Section 7.4.6, “LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing”.

REG[0056h] LCD1 Parallel Interface Setting Register
Default = 0400h Read/Write

FPVIN1 Pin Type Select	FPVIN1 Polarity	n/a			FPVIN1 Pull-down Control	Reserved	
15	14	13	12	11	10	9	8
LCD1 VSYNC Input Enable	LCD1 Parallel Type Select	LCD1 Parallel Command/Parameter Pin bits 1-0		LCD1 Parallel Data Format bits 3-0			
7	6	5	4	3	2	1	0

bit 15 FPVIN1 Pin Type Select
This bit selects the FPVIN1 pin type. When an output is selected, the vertical synchronizing signal outputs it from FPVIN1.
When this bit = 0, FPVIN1 is configured as an input (default).
When this bit = 1, FPVIN1 is configured as an output.

bit 14 FPVIN1 Polarity
This bit is effects both the input vertical sync and Output vertical sync (REG[0056h] bit 15).
When this bit = 0, FPVIN1 is active low (default)
When this bit = 1, FPVIN1 is active high

bit 10 FPVIN1 Pull-down Control
This bit controls the internal pull-down resistance on FPVIN1 when it is configured as an input (REG[0056h] bit 15 = 0).
When this bit = 0, the pull-down resistance is disabled.
When this bit = 1, the pull-down resistance is enabled (default).

bits 9-8 Reserved
These bits are reserved and default to 0.

bit 7 LCD1 VSYNC Input Enable
This bit is not used for RGB type panels.
This bit allows the transfer of a frame of data synced to an external VSYNC input (FPVIN1).
When this bit = 0, the LCD1 data output is independent of an external VSYNC input.
When this bit = 1, the LCD1 data output is synchronous with an external VSYNC input.

Note
The FPVIN1 signal period must be longer than the time it takes to transfer a frame of data. If the FPVIN1 period is shorter than the time it takes to transfer a complete frame to the panel, the current frame transfer is interrupted at the next FPVIN1 falling edge.

Note
Once a manual frame transfer has been initiated (REG[003Ah] bit 0 = 1), the LCD1 VSYNC Input Enable bit must not be disabled before the next VSYNC signal has occurred or the LCD interface will always be busy and subsequent transfers will not occur.

bit 6 LCD1 Parallel Type Select
This bit determines the LCD1 parallel interface type.
When this bit = 0, the parallel interface is type 80.
When this bit = 1, the parallel interface is type 68.

bits 5-4 LCD 1 Parallel Command/Parameter Pin bits [1:0]
These bits determine which FPDAT[17:0] pins are used for the parallel panel command/parameter..

Table 10-17: LCD1 Parallel Command/Parameter Pin Mapping

REG[0056h] bits 5-4	Command/Parameter Pin Mapping
00b (default)	FPDAT[15:0]
01b	FPDAT[17:10], FPDAT[8:1]
10b	FPDAT[17:13], FPDAT[11:1]
11b	Reserved

bits 3-0 LCD1 Parallel Data Format bits [3:0]
These bits determine the LCD1 parallel data format. **These bits are not used for RGB Type Panels (REG[0032h] bits 1-0 = 00b or 01b)**. For further information on available parallel data formats, see Section 12, “Display Modes”.

Table 10-18: LCD1 Parallel Data Format Selection

REG[0056h] bits 2-0	LCD1 Parallel Data Format	
	Data Bus Width	**Data Format**
0000b	8-bit	RGB = 3:3:2 (1 cycle/pixel)
0001b		RGB = 4:4:4 (3 cycle / 2 pixel)
0010b	16-bit	RGB = 8:8:8 (3 cycle/2 pixel)
0011b	8-bit	RGB = 8:8:8 (3 cycle/pixel)
0100b	24-bit	RGB = 8:8:8 (1 cycle/pixel)
0101b	16-bit	RGB = 4:4:4 (1 cycle/pixel)
0110b		RGB = 5:6:5 (1 cycle/pixel)
0111b	18-bit	RGB = 6:6:6 (1 cycle/pixel)
1xxxb	8-bit	REG = 5:6:5 (2 cycle/pixel)

10.4.6 LCD2 Setting Registers

REG[0058h] LCD2 Horizontal Display Period Register Default = 0000h							Read/Write
n/a							LCD2 HDP bit 8
15	14	13	12	11	10	9	8
LCD2 Horizontal Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 8-0 LCD2 Horizontal Display Period bits [8:0]
These bits specify the LCD2 Horizontal Display Period, in 2 pixel resolution.
REG[0058h] bits 8-0 = (Horizontal Display Period in pixels ÷ 2) - 1

Note
For Parallel and Serial interface panels (see REG[0032h] bits 1-0), the following formula must be valid.
HDP x VDP ≥ 40 pixels.

REG[005Ah] LCD2 Vertical Display Period Register Default = 0000h							Read/Write
n/a						LCD2 Vertical Display Period bits 9-8	
15	14	13	12	11	10	9	8
LCD2 Vertical Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 Vertical Display Period bits [9:0]
These bits specify the LCD2 Vertical Display Period, in 1 line resolution.
REG[005Ah] bits 9-0 = Vertical Display Period in lines - 1

Note
For Parallel and Serial interface panels (see REG[0032h] bits 1-0), the following formula must be valid.
HDP x VDP ≥ 40 pixels.

REG[005Ch] LCD2 Serial Interface Setting Register Default = 0001h							Read/Write
n/a							
15	14	13	12	11	10	9	8
LCD2 Serial Bit Type Select	n/a	LCD2 Serial Data Type Select	LCD2 Serial Data Direction	LCD2 Serial Data Format bits 1-0		LCD2 Serial Clock Phase	LCD2 Serial Clock Polarity
7	6	5	4	3	2	1	0

bit 7 LCD2 Serial Bit Type Select
This bit selects the panel data width type for LCD2 serial interface mode.
When this bit = 0, the serial panel data width is 8/9-bit.
When this bit = 1, the serial panel data width is 16/17-bit.

bit 5 LCD2 Serial Data Type Select
This bit selects the data type for LCD2 serial interface mode and determines whether the serial interface uses 4 pins or 3 pins.
When this bit = 0, the LCD2 serial interface uses 4 pins (8/16-bit data transfer mode).
When this bit = 1, the LCD2 serial interface uses 3 pins (9/17-bit data transfer mode).

This bit, in conjunction with the most significant bit of the LCD2 Serial Data Format bits (REG[005Ch] bit 7), determines the serial data transfer mode used by the LCD2 port.

Table 10-19: LCD2 Serial Data Transfer Mode Selection

REG[005Ch] bit 7	REG[005Ch] bit 5	LCD2 Serial Data Transfer Mode
0	0	8-bit serial
0	1	9-bit serial
1	0	16-bit serial
1	1	17-bit serial

bit 4 LCD2 Serial Data Direction
This bit determines the LCD2 serial data direction.
When this bit = 0, the MSB is sent first.
When this bit = 1, the LSB is sent first.

bits 3-2 LCD2 Serial Data Format bits [1:0]
These bits determine the LCD2 serial data format. For further information on available serial data formats, see Section 12, “Display Modes”.

Table 10-20: LCD2 Serial Data Format Selection

<table>
<tr><th rowspan="2">REG[005Ch] bits 3-2</th><th rowspan="2">REG[005Ch] bit 7</th><th colspan="2">LCD2 Serial Data Format</th></tr>
<tr><th>Data Length</th><th>Data Format</th></tr>
<tr><td rowspan="2">00b</td><td>0</td><td>8-bit</td><td>RGB 3:3:2
(1 cycle/pixel)</td></tr>
<tr><td>1</td><td>16-bit</td><td>REG 4:4:4
(LSB unused)</td></tr>
<tr><td rowspan="2">01b</td><td>0</td><td>8-bit</td><td>RGB 4:4:4
(3 cycles/2 pixel)</td></tr>
<tr><td>1</td><td>16-bit</td><td>RGB 4:4:4
(MSB unused)</td></tr>
<tr><td>10b</td><td rowspan="2">x</td><td>16-bit</td><td>RGB 5:6:5</td></tr>
<tr><td>11b</td><td>16-bit</td><td>RGB 3:3:2
(1 cycle/2pixel)</td></tr>
</table>

bit 1 LCD2 Serial Clock Phase
This bit specifies the LCDSCLK phase and is used in conjunction with the LCD2 LCDSCLK Polarity bit to configure LCDSCLK which is used for the LCD2 serial panel interface. For a summary of the possible settings, see Table 10-21: “LCD2 Serial Clock Polarity and Phase Selection”.

Note

For details on timing, see Section 7.4.6, “LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing”.

bit 0 LCD2 Serial Clock Polarity
This bit specifies the LCDSCLK polarity and is used in conjunction with the LCD2 LCDSCLK Phase bit to configure LCDSCLK which is used for the LCD2 serial panel interface. The following table summarizes the phase and polarity settings for LCDSCLK.

Table 10-21: LCD2 Serial Clock Polarity and Phase Selection

REG[005Ch] bit 1	REG[005Ch] bit 0	Serial Data Output Changes	Clock Idling Status
0	0	falling edge of Serial Clock	Low
	1	rising edge of Serial Clock	High
1	0	rising edge of Serial Clock	Low
	1	falling edge of Serial Clock	High

Note
For details on timing, see Section 7.4.6, “LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing”.

REG[005Eh] LCD2 Parallel Interface Setting Register Default = 0100h							Read/Write
FPVIN2 Pin Type Select	FPVIN2 Polarity Select	n/a		Monochrome Source Color Select	Reserved	Monochrome mode Enable	FPVIN2 Pull-down Control
15	14	13	12	11	10	9	8
LCD2 VSYNC Input Enable	LCD2 Parallel Type Select	LCD2 Parallel Command/Parameter Pin bits 1-0		LCD2 Parallel Data Format bits 3-0			
7	6	5	4	3	2	1	0

bit 15 FPVIN2 Pin Type Select
This bit selects the FPVIN2 pin type. When an output is selected, the vertical synchronizing signal outputs it from FPVIN2.
When this bit = 0, FPVIN2 is configured as an input (default).
When this bit = 1, FPVIN2 is configured as an output.

bit 14 FPVIN2 Polarity Select
This bit is affects both the input vertical sync and output vertical sync (REG[005Eh] bit 15).
When this bit = 0, FPVIN2 is configured as active low
When this bit = 1, FPVIN2 is configured as active high

bit 11 Monochrome Source Color Select
This bit selects the source color for Monochrome Mode.
When this bit = 0, the source for monochrome display is RGB Data
When this bit = 1, the source for monochrome display is Green Data

bit 10 Reserved
The default value for this bit is 0.

bit 9 Monochrome Mode Enable
When this bit = 1, RGB data is converted to monochrome data and transferred to the LCD panel. Monochrome Mode is effective only 1cycle/2pixel Parallel Panel Type.

bit 8 FPVIN2 Pull-down Control
This bit controls the internal pull-down resistance on FPVIN2 when it is configured as an input (REG[005Eh] bit 15 = 0).
When this bit = 0, the pull-down resistance is disabled.
When this bit = 1, the pull-down resistance is enabled (default).

bit 7 LCD2 VSYNC Input Enable
This bit allows the transfer of a frame of data synced to an external VSYNC input (FPVIN2).
When this bit = 0, the LCD2 data output is independent of an external VSYNC input.
When this bit = 1, the LCD2 data output is synchronous with an external VSYNC input.

Note
The FPVIN2 signal period must be longer than the time it takes to transfer a frame of data. If the FPVIN2 period is shorter than the time it takes to transfer a complete frame to the panel, the current frame transfer is interrupted at the next FPVIN2 falling edge.

bit 6 LCD2 Parallel Type Select
This bit determines the LCD2 parallel interface type.
When this bit = 0, the parallel interface is type 80.
When this bit = 1, the parallel interface is type 68.

bits 5-4 LCD 2 Parallel Command/Parameter Pin bits [1:0]
These bits determine which FPDAT[17:0] pins are used for the parallel panel command/parameter..

Table 10-22: LCD2 Parallel Command/Parameter Pin Mapping

REG[0056h] bits 5-4	Command/Parameter Pin Mapping
00b (default)	FPDAT[15:0]
01b	FPDAT[17:10], FPDAT[8:1]
10b	FPDAT[17:13], FPDAT[11:1]
11b	Reserved

bits 3-0 LCD2 Parallel Data Format bits [3:0]
These bits determine the LCD2 Parallel Data Format. For further information on available parallel data formats, see Section 12, “Display Modes”.

Table 10-23: LCD2 Parallel Data Format Selection

REG[005Eh] bits 2-0	LCD2 Parallel Data Format	
	Data Bus Width	**Data Format**
0000b	8-bit	RGB=3.3.2 (1 cycle/pixel)
0001b		RGB=4.4.4 (3 cycle / 2 pixel)
0011b		RGB=8.8.8 (3 cycle/pixel)
0101b	16-bit	RGB=4.4.4 (1 cycle/pixel)
0110b		RGB=5.6.5 (1 cycle/pixel)
0111b	18-bit	RGB=6.6.6 (1 cycle/pixel)
0010b	16-bit	RGB=8.8.8 (3 cycle/2 pixel)
0100b	24-bit	RGB=8.8.8 (1 cycle/1 pixel)
1xxxb	8-bit	RGB=5.6.5 (2 cycle/pixel)

10.4.7 Extended Panel Registers

REG[0060h] SPI Header Data Register Default = 0001h							Read/Write
n/a							
15	14	13	12	11	10	9	8
SPI Header Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 SPI Header Data bits [7:0]
These bits specify the SPI header data.

REG[0062h] SPI Read Data Register Default = 0000h							Read Only
n/a							
15	14	13	12	11	10	9	8
SPI Read Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 SPI Read Data bits [7:0]
These bits return the data from a SPI read.

REG[0064h] SPI Read Wait Time Register Default = 0000h							Read/Write
n/a							SPI Read CLK Edge Select
15	14	13	12	11	10	9	8
n/a			SPI Read Wait Time bits 4-0				
7	6	5	4	3	2	1	0

bit 8 SPI Read CLK Edge Select
This bit selects which clock edge data is read on.
When this bit = 0, the SPI is read on the rising FPSCLK edge.
When this bit = 1, the SPI is read on the falling FPSCLK edge.

bits 4-0 SPI Read Wait Time bits [4:0]
These bits determine the wait time for a SPI read, in FPSCLKs.

REG[0068h] LCD1 Vsync Output Register Default = 0000h							Read/Write
Vsync Width bits 7-0							
15	14	13	12	11	10	9	8
Vsync Position bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 Vsync Width bits [7:0]
These bits are used only when FPVIN1 (LCD1 VSYNC) is configured as an output, REG[0056h] bit 15 = 1.
These bits determine the width of VSYNC for LCD1.

VSYNC Width = REG[0068] bits [15:8] / 2 PCLKs

bits 7-0 Vsync Position bits [7:0]
These bits are used only when FPVIN1 (LCD1 VSYNC) is configured as an output, REG[0056h] bit 15 = 1.
These bits determine the position of VSYNC for LCD1.

VSYNC Position = REG[0068] bits [7:0] / 2 PCLKs

REG[006Ah] LCD2 Vsync Output Register
Default = 0000h Read/Write

Vsync Width bits 7-0							
15	14	13	12	11	10	9	8
Vsync Position bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 Vsync Width bits [7:0]
These bits are used only when FPVIN2 (LCD2 VSYNC) is configured as an output, REG[0056Eh] bit 15 = 1.
These bits determine the width of VSYNC for LCD2

VSYNC Width = REG[006A] bits [15:8] / 2 PCLKs

bits 7-0 Vsync Position bits [7:0]
These bits are used only when FPVIN2 (LCD2 VSYNC) is configured as an output, REG[005Eh] bit 15 = 1.
These bits determine the position of VSYNC for LCD2.

VSYNC Position = REG[006A] bits [7:0] / 2 PCLKs

REG[0070h] is Reserved

This register is Reserved and should not be written.

REG[0080h] Samsung α-TFT Horizontal Total Register Default = 0000h							Read/Write
n/a						α-TFT Horizontal Total bits 9-8	
15	14	13	12	11	10	9	8
α-TFT Horizontal Total bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 α-TFT Horizontal Total bits [9:0]
These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 = 110000b) and have no effect for any other panel type. These bits specify the Horizontal Total period for Samsung a-TFT panels as follows.

REG[0080] Bits [9:0] = α-TFT Horizontal Total - 1
and must have a value greater than 8.

REG[0082h] Samsung α-TFT LD Rising Edge Register Default = 0000h							Read/Write
n/a						α-TFT LD Rising Edge bits 9-8	
15	14	13	12	11	10	9	8
α-TFT LD Rising Edge bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 α-TFT LD Rising Edge bits [9:0]
These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 = 110000b) and have no effect for any other panel type. These bits specify the LD rising edge position from the STH rising edge.

LD Rising Edge Position = (STH Pulse Width + HDP + LD Rising Edge) + 8

REG[0084h] Samsung α-TFT CKV Toggle Point Register Default = 0000h							Read/Write
n/a						α-TFT CKV Toggle Point bits 9-8	
15	14	13	12	11	10	9	8
α-TFT CKV Toggle Point bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 α-TFT CKV Toggle Point bits [9:0]
These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 = 110000b) and have no effect for any other panel type. These bits specify the CKV toggle point from the STH rising edge.

CKV Toggle Position = (STH Pulse Width + HDP + LD Rising Edge - (CKV Toggle Position to LD Rising Edge period)) + 8

Note

CKV Toggle Position to LD Rising Edge period is shown in Section 7.4.4, “a-TFT Panel Timing”.

REG[0086h] Samsung α-TFT VCOM Toggle Point Register Default = 0000h							Read/Write
n/a						α-TFT VCOM Toggle Point bits 9-8	
15	14	13	12	11	10	9	8
α-TFT VCOM Toggle Point bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 α-TFT VCOM Toggle Point bits [9:0]
These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 = 110000b) and have no effect for any other panel type. These bits specify the VCOM toggle point from the STH rising edge.

VCOM Rising Edge Position = (STH Pulse Width + HDP + LD Rising Edge - (VCOM Toggle Position to LD Rising Edge period) + 8

Note
VCOM Toggle Position to LD Rising Edge period is shown in Section 7.4.4, "a-TFT Panel Timing".

REG[0088h] Samsung α-TFT Pulse Width Register Default = 0000h							Read/Write
n/a					α-TFT LD Pulse Width bits 2-0		
15	14	13	12	11	10	9	8
n/a					α-TFT STH Pulse Width bits 2-0		
7	6	5	4	3	2	1	0

bits 10-8 α-TFT LD Pulse Width bits [2:0]
These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 = 110000b) and have no effect for any other panel type. These bits specify the LD pulse width.

LD Pulse Width = (REG[0088h] bits 10-8) - 1

bits 2-0 α-TFT STH Pulse Width bits [2:0]
These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 bits 1-0 = 110000b) and have no effect for any other panel type. These bits specify the STH pulse width.

STH Pulse Width = (REG[0088h] bits 2-0) - 1

REG[008Ah] through REG[008Eh] are Reserved

These registers are Reserved and should not be written.

REG[0090h] HR-TFT Configuration Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a					Reserved	HR-TFT PS Mode	Reserved
7	6	5	4	3	2	1	0

bit 2 Reserved
The default value for this bit is 0.

bit 1 HR-TFT PS Mode
This bit is for HR-TFT panels only (REG[0032h] bits 15-10 = 000001b) and has no effect for any other panel type. This bit selects the timing used for the PS signal. The alternate PS timings (PS1, PS2, PS3) result in additional power saving on the HR-TFT Panel.
When this bit = 0, the PS signal uses PS1 timing.
When this bit = 1, the PS signal uses PS2 timing.

bit 0 Reserved
The default value for this bit is 0.

REG[0092h] HR-TFT CLS Width Register Default = 012Ch							Read/Write
n/a							CLS Pulse Width bit 8
15	14	13	12	11	10	9	8
CLS Pulse Width bits 7-0							
7	6	5	4	3	2	1	0

bits 8-0 CLS Pulse Width bits [8:0]
These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001b) and have no effect for any other panel type. This register determines the width of the CLS signal in PCLKs.

Note
This register must be programmed such that the following formula is valid.
(REG[0092h] bits 8-0) > 0

REG[0094h] HR-TFT PS1 Rising Edge Register Default = 0032h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a		PS1 Rising Edge bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 PS1 Rising Edge bits [5:0]
These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001b) and have no effect for any other panel type. This register determines the number of PCLKs between the CLS falling edge and the PS1 rising edge.

REG[0096h] HR-TFT PS2 Rising Edge Register
Default = 0064h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
PS2 Rising Edge bits 7-0							

bits 7-0 PS2 Rising Edge bits [7:0]
These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001b) and have no effect for any other panel type. This register determines the number of PCLKs between the LP falling edge and the first PS2 rising edge.

Note
This register must be programmed such that the following formula is valid.
(REG[0096h] bits 7-0) > 0

REG[0098h] HR-TFT PS2 Toggle Width Register
Default = 000Ah — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a	PS2 Toggle Width bits 6-0						

bits 6-0 PS2 Toggle Width bits [6:0]
These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001b) and have no effect for any other panel type. This register determines the width of the PS2 signal before toggling (in PCLKs).

Note
This register must be programmed such that the following formula is valid.
(REG[0098h] bits 6-0) > 0

REG[009Ah] HR-TFT PS3 Signal Width Register Default = 0064h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a	PS3 Signal Width bits 6-0						
7	6	5	4	3	2	1	0

bits 6-0 PS3 Signal Width bits [6:0]
These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001b) and have no effect for any other panel type. This register determines the width of the PS3 signal in PCLKs.

Note
This register must be programmed such that the following formula is valid.
(REG[009Ah] bits 6-0) > 0

REG[009Eh] HR-TFT REV Toggle Point Register Default = 000Ah							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a			REV Toggle bits 4-0				
7	6	5	4	3	2	1	0

bits 4-0 REV Toggle bits [4:0]
These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001b) and have no effect for any other panel type. This register determines the width in PCLKs to toggle the REV signal prior to the LP rising edge.
REG[009E] bits [4:0] = REV toggle position in PCLKs

REG[00A0h] HR-TFT PS1/2 End Register Default = 0007h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a					PS1/2 End bits 2-0		
7	6	5	4	3	2	1	0

bits 2-0 PS1/2 End bits [2:0]
These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001b) and have no effect for any other panel type. This register allows the PS signal to continue into the vertical non-display period (in lines).

Note
This register must be programmed such that the following formula is valid.
VT > (REG[00A0h] bits 2-0) + VDP + VPS + 1

REG[00A2h] Type 2 TFT Configuration Register 0 Default = 0000h							Read/Write
POL Type	n/a	AP Pulse Width bits 2-0			n/a	AP Rising Position bits 1-0	
15	14	13	12	11	10	9	8
n/a			VCLK Hold bits 1-0		n/a	VCLK Setup bits 1-0	
7	6	5	4	3	2	1	0

bit 15 POL Type
This bit is for Type 2 TFT panels only (REG[0032h] bits 15-10 = 000011b) and has no effect for any other panel type. This bit selects how often the POL signal is toggled. The GPIO2 pin controls the POL signal used for the TFT Type 2 Interface.
When this bit = 0, the POL signal is toggled every line.
When this bit = 1, the POL signal is toggled every frame.

bits 13-11 AP Pulse Width bits [2:0]
These bits are for Type 2 TFT panels only (REG[0032h] bits 15-10 = 000011b) and have no effect for any other panel type. These bits specify the AP Pulse Width used for the TFT Type 2 Interface. The GPIO1 pin controls the AP signal for the TFT Type 2 Interface.

Table 10-24: AP Pulse Width

REG[00A2h] bits 13-11	AP Pulse Width (in PCLKs)
000b	20
001b	40
010b	80
011b	120
100b	150
101b	190
110b	240
111b	270

bits 9-8 AP Rising Position bits [1:0]
These bits are for Type 2 TFT panels only (REG[0032h] bits 15-10 = 000011b) and have no effect for any other panel type. These bits specify the TFT Type 2 AC timing parameter from the rising edge of FPLINE (STB) to the rising edge of GPIO1 (AP). The parameter is selected as follows.

Table 10-25: AP Rising Position

REG[00A2h] bits 9-8	AP Rising Position (in PCLKs)
00b	40
01b	52
10b	68
11b	90

bits 4-3 VCLK Hold bits [1:0]
These bits are for Type 2 TFT panels only (REG[0032h] bits 15-10 = 000011b) and have no effect for any other panel type. These bits specify the TFT Type 2 AC timing parameter from the rising edge of FPLINE (STB) to the falling edge of GPIO0 (VCLK). The parameter is selected as follows.

Table 10-26: VCLK Hold

REG[00A2h] bits 4-3	VCLK Hold (in PCLKs)
00b	7
01b	9
10b	12
11b	16

bits 1-0 VCLK Setup bits [1:0]
These bits are for Type 2 TFT panels only (REG[0032h] bits 15-10 = 000011b) and have no effect for any other panel type. These bits specify the TFT Type 2 AC timing parameter from the rising edge of GPIO0 (VCLK) to the rising edge of FPLINE (STB). The parameter is selected as follows.

Table 10-27: VCLK Setup

REG[00A2h] bits 1-0	VCLK Setup (in PCLKs)
00b	7
01b	9
10b	12
11b	16

REG[00A4h] Casio TFT Timing Register 0 Default = 0E09h							Read/Write
n/a		GRES Falling Edge to GPCK Rising Edge bits 5-0					
15	14	13	12	11	10	9	8
n/a		GPCK Rising Edge to GRES Rising Edge bits 5-0					
7	6	5	4	3	2	1	0

bits 13-8 GRES Falling Edge to GPCK Rising Edge bits [5:0]
These bits are for Casio TFT panels only (REG[0032h] bits 15-10 = 000010b) and have no effect for any other panel type. These bits determine the number of PCLKs from GRES falling edge to GPCK rising edge.
GRES falling edge to GPCK rising edge = (REG[00A4h] bits 13-8) + 1

bits 5-0 GPCK Rising Edge to GRES Rising Edge bits [5:0]
These bits are for Casio TFT panels only (REG[0032h] bits 15-10 = 000010b) and have no effect for any other panel type. These bits determine the number of PCLKs from GPCK rising edge to GRES rising edge.

REG[00A6h] Casio TFT Timing Register 1 Default = 0918h							Read/Write
n/a		GPCK Rising Edge to STH Pulse bits 5-0					
15	14	13	12	11	10	9	8
n/a	GRES Falling Edge to FRP Toggle Point bits 6-0						
7	6	5	4	3	2	1	0

bits 13-8 GPCK Rising Edge to STH Pulse bits [5:0]
These bits are for Casio TFT panels only (REG[0032h] bits 15-10 = 000010b) and have no effect for any other panel type. These bits determine the number of PCLKs from GPCK rising edge to STH pulse.

bits 6-0 GRES Falling Edge to FRP Toggle Point bits [6:0]
These bits are for Casio TFT panels only (REG[0032h] bits 15-10 = 000010b) and have no effect for any other panel type. These bits determine the number of PCLKs from GRES falling edge to FRP Toggle point.

REG[00A8h] Type 2 TFT Configuration Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a							Data Compare Invert Enable
7	6	5	4	3	2	1	0

bit 0 Data Compare Invert Enable
This bit can be used to lower power consumption for TFT Type 2 Interfaces. The Data Compare and Invert function reduces the amount of data toggled by counting the number of bits that are changed (1 to 0 **or** 0 to 1) from the previous pixel data. If more than half of the bits are changed the data is inverted and the lesser amount of bits are toggled. For all other panel interfaces it has no effect.
When this bit = 0, the Data Compare and Invert functions are disabled.
When this bit = 1, the Data Compare and Invert functions are enabled.

REG[00AAh] through REG[00ECh] are Reserved

These registers are Reserved and should not be written.

REG[00EEh] Partial Drive Area0 Start Line Register Default = 0000h							Read/Write
Partial Drive Enable	Reserved	Reserved	Reserved	n/a	Partial Drive Area0 Enable	Partial Drive Area0 Start Line bits 9-8	
15	14	13	12	11	10	9	8
Partial Drive Area0 Start Line bits 7-0							
7	6	5	4	3	2	1	0

bit 15 Partial Drive Enable
When this bit = 0, normal mode is enabled (partial drive is disabled).
When this bit = 1, a Partial Drive cycle starts from the next frame.

bit 14 Reserved
The default value for this bit is 0.

bit 13 Reserved
The default value for this bit is 0.

bit 12 Reserved
The default value for this bit is 0.

bit 10 Partial Drive Area0 Enable
The Partial Drive Enable bit (REG[00EEh] bit 15) must be set to 1 before Partial Drive Area0 can be enabled.
When this bit = 1, Partial Drive Area0 is enabled.
When this bit = 0, Partial Drive Area0 is disabled.

bits 9-0 Partial Drive Area0 Start Line bits [9:0]
These bits specify the Partial Drive Area0 Start Line number in 1 line resolution.
REG[00EEh] bits 9-0 = Partial Drive Start Line in lines

Note
Partial Drive Area0 Start Line must be set as smaller than Partial Drive Area1 Start Line Address.

Note
These bits must be programmed such that the following formulas are valid:
REG[00EEh] bits 9-0 > REG[004Eh] bits 9-0
REG[00EEh] bits 9-0 = Partial Area0/1 Display Start in lines + REG[004Eh]
REG[00EEh] bits 9-0 ≠ REG[0052h] bits 8-0

REG[00F0h] Partial Drive Area0 End Line Register Default = 0000h							Read/Write
n/a		Reserved	Reserved	n/a		Partial Drive Area0 End Line bits 9-8	
15	14	13	12	11	10	9	8
Partial Drive Area0 End Line bits 7-0							
7	6	5	4	3	2	1	0

bit 13 Reserved
The default value for this bit is 0.

bit 12 Reserved
The default value for this bit is 0.

bits 9-0 Partial Drive Area0 End Line bits [9:0]
These bits specify the Partial Drive Area0 End Line in 1 line resolution.
REG[00F0h] bits 9-0 = Partial Drive Area0 End Line in lines

Note
The Partial Drive Area0 End Line must be set at least 1 line smaller than the Partial Drive Area1 Start Line Address.

Note
The Partial Drive End Line bits indicate the line at which the partial area will end. For example, to display 30 lines at the beginning of the display, set the Start to 1 and the End to 29.

REG[00F2h] Partial Drive Area1 Start Line Register
Default = 0000h — Read/Write

n/a					Partial Drive Area1 Enable	Partial Drive Area1 Start Line bits 9-8	
15	14	13	12	11	10	9	8
Partial Drive Area1 Start Line bits 7-0							
7	6	5	4	3	2	1	0

bit 10 — Partial Drive Area1 Enable
The Partial Drive Enable bit (REG[00EEh] bit 15) must be set to 1 before Partial Drive Area1 can be enabled.
When this bit = 0, Partial Drive Area1 is disabled.
When this bit = 1, Partial Drive Area1 is enabled.

bits 9-0 — Partial Drive Area1 Start Line bits [9:0]
These bits specify the Partial Drive Area1 Start Line number in 1 line resolution.
REG[00F2h] bits 9-0 = Partial Drive Start Line in lines

Note
The Partial Drive Area1 Start Line must be set at least 1 line larger than the Partial Drive Area0 End Line Address.

Note
These bits must be programmed such that the following formulas are valid:
REG[00F2h] bits 9-0 > REG[004Eh] bits 9-0
REG[00F2h] bits 9-0 = Partial Area0/1 Display Start in lines + REG[004Eh]
REG[00F2h] bits 9-0 ≠ REG[0052h] bits 8-0

REG[00F4h] Partial Drive Area1 End Line Register
Default = 0000h — Read/Write

n/a						Partial Drive Area1 End Line bits 9-8	
15	14	13	12	11	10	9	8
Partial Drive Area1 End Line bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 — Partial Drive Area1 End Line bits [9:0]
These bits specify the Partial Drive Area1 End Line number in 1 line resolution.
REG[00F4h] bits 9-0 = Partial Drive Area1 End Line Number in Lines

Note
The Partial Drive Area0 End Line must be set at least 3 lines smaller than the Partial Drive Area1 Start Line Address.

Note
The Partial Drive End Line bits indicate the line at which the partial area will end. For example, to display 30 lines at the beginning of the display set the Start to 1 and the End to 29.

REG[00F6h] through REG[00FCh] are Reserved

These registers are Reserved and should not be written.

REG[00FEh] LCD Interface ID Register Default = 0001h							Read/Write
LCD Interface Address ID bits 7-0							
15	14	13	12	11	10	9	8
LCD Interface Data ID bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 LCD Interface Address ID bits [7:0]
These bits, along with REG[0034h] bits 15-8, indicate the address for the serial command interface of the TFT Type 5 panel.

bits 7-0 LCD Interface Data ID bits [7:0] (default = 01h)
These bits, along with REG[0034h] bits 7-0, indicate the data for the serial command interface of the TFT Type 5 panel.

Note

The serial command interface consists of four bytes of data as follows:

1. Identify register address (REG[00FEh] bits 15-8).
2. Register address (REG[0034h] bits 15-8).
3. Identify register data (REG[00FEh] bits 7-0).
4. Register data (REG[0034h] bits 7-0).

REG[00FEh] is written first, then REG[0034h]. The command transfer is started after writing REG[0034h].

10.4.8 Camera Interface Setting Register

REG[0100h] Camera1 Clock Setting Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a			Camera1 Clock Divide Select bits 4-0				
7	6	5	4	3	2	1	0

bits 4-0 Camera1 Clock Divide Select bits [4:0]
These bits specify the divide ratio used to generate the Camera1 Clock from the System Clock.

Table 10-28: Camera1 Clock Divide Ratio Selection

REG[0100h] bits 4-0	Camera1 Clock Divide Ratio	REG[0100h] bits 4-0	Camera1 Clock Divide Ratio
00000b	1:1	10000b	17:1
00001b	2:1	10001b	18:1
00010b	3:1	10010b	19:1
00011b	4:1	10011b	20:1
00100b	5:1	10100b	21:1
00101b	6:1	10101b	22:1
00110b	7:1	10110b	23:1
00111b	8:1	10111b	24:1
01000b	9:1	11000b	25:1
01001b	10:1	11001b	26:1
01010b	11:1	11010b	27:1
01011b	12:1	11011b	28:1
01100b	13:1	11100b	29:1
01101b	14:1	11101b	30:1
01110b	15:1	11110b	31:1
01111b	16:1	11111b	32:1

Note
1:1 camera clock JPEG encode should be limited to a maximum resolution of 800x600.

REG[0102h] Camera1 Signal Setting Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a	Camera1 Interface Select	Camera1 Clock Mode Select	Camera1 YUV Data Format Select bits 1-0		Camera1 HSYNC Active Select	Camera1 VSYNC Active Select	Camera1 Valid Input Clock Edge
7	6	5	4	3	2	1	0

bit 6 Camera1 Interface Select
This bit specifies the Camera1 Interface type.
When this bit = 0, the Camera1 interface is configured for YUV 4:2:2 8-bit.
When this bit = 1, the Camera1 interface is configured for YUV 4:2:2 16-bit.

bit 5 Camera1 Clock Mode Select
This bit determines the source of the clock used to sample incoming YUV data on the Camera1 interface.
When this bit = 0, the external input clock (CM1CLKIN) from the camera interface is used to sample incoming YUV data (default).
When this bit = 1, the internally divided system clock is used to sample incoming YUV data.

bits 4-3 Camera1 YUV Data Format Select bits [1:0]
These bits specify the YUV data format for the Camera1 interface, in bytes.

Table 10-29: YUV Data Format Selection

REG[0102h] bits 4-3	YUV Data Format (8-bit format)	YUV Data Format (16-bit format)
00b	(1st) UYVY (last)	(1st cam1) U V (last) (1st cam2) Y Y (last)
01b	(1st) VYUY (last)	(1st cam1) V U (last) (1st cam2) Y Y (last)
10b	(1st) YUYV (last)	(1st cam1) Y Y (last) (1st cam2) U V (last)
11b	(1st) YVYU (last)	(1st cam1) Y Y (last) (1st cam2) V U (last)

bit 2 Camera1 HSYNC Active Select
This bit defines HYSNC for the Camera1 interface.
When this bit = 0, the Camera1 hsync (CM1HREF) is active low and CM1HREF high means data is valid.
When this bit = 1, the Camera1 hsync (CM1HREF) is active high and CM1HREF low means data is valid.

bit 1 Camera1 VSYNC Active Select
This bit defines VYSNC for the Camera1 interface.
When this bit = 0, the Camera1 vsync (CM1VREF) is active low and CM1VREF high means data is valid.
When this bit = 1, the Camera1 vsync (CM1VREF) is active high and CM1VREF low means data is valid.

bit 0 Camera1 Valid Input Clock Edge
This bit determines the edge at which Camera1 data is latched.
When this bit = 0, the S1D13719 latches input data at the rising edge of the clock (CM1CLKIN).
When this bit = 1, S1D13719 latches input data at the falling edge of the clock (CM1CLKIN).

REG[0104h] Camera2 Clock Divide Select Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a			Camera2 Clock Divide Select bits 4-0				
7	6	5	4	3	2	1	0

bits 4-0 Camera2 Clock Divide Select bits [4:0]
These bits specify the divide ratio used to generate the Camera2 Clock from the System Clock.

Table 10-30: Camera2 Clock Divide Ratio Selection

REG[0102h] bits 4-0	Camera2 Clock Divide Ratio	REG[0102h] bits 4-0	Camera2 Clock Divide Ratio
00000b	1:1	10000b	17:1
00001b	2:1	10001b	18:1
00010b	3:1	10010b	19:1
00011b	4:1	10011b	20:1
00100b	5:1	10100b	21:1
00101b	6:1	10101b	22:1
00110b	7:1	10110b	23:1
00111b	8:1	10111b	24:1
01000b	9:1	11000b	25:1
01001b	10:1	11001b	26:1
01010b	11:1	11010b	27:1
01011b	12:1	11011b	28:1
01100b	13:1	11100b	29:1
01101b	14:1	11101b	30:1
01110b	15:1	11110b	31:1
01111b	16:1	11111b	32:1

Note
1:1 camera clock JPEG encode should be limited to a maximum resolution of 800x600.

REG[0106h] Camera2 Input Signal Format Select Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Camera2 Interface Select bits 1-0		Camera2 Clock Mode Select	Camera2 YUV Data Format Select bits 1-0		Camera2 HSYNC Active Select	Camera2 VSYNC Active Select	Camera2 Valid Input Clock Edge
7	6	5	4	3	2	1	0

bits 7-6 Camera2 Interface Select bits [1:0]
These bits specify the Camera2 Interface type.

Table 10-31: YUV Data Format Selection

REG[0106h] bits 7-6	YUV Format
00b	Camera Interface
01b	MPEG Codec Interface
10b	Reserved
11b	Reserved

bit 5 Camera2 Clock Mode Select
This bit determines the source of the clock used to sample incoming YUV data on the Camera2 interface.
When this bit = 0, the external input clock from the camera interface is used to sample incoming YUV data (default).
When this bit = 1, the internally divided system clock (CM2CLKIN) is used to sample incoming YUV data.

bits 4-3 Camera2 YUV Data Format Select bits [1:0]
These bits specify the YUV data format for the Camera2 interface, in bytes.

Table 10-32: YUV Data Format Selection

REG[0106h] bits 4-3	YUV Format
00b	(1st) UYVY (last)
01b	(1st) VYUY (last)
10b	(1st) YUYV (last)
11b	(1st) YVYU (last)

bit 2 Camera2 HSYNC Active Select
This bit defines HYSNC for the Camera2 interface.
When this bit = 0, the Camera2 HSYNC (CM2HREF) is active low and CM2HREF high means data is valid.
When this bit = 1, the Camera2 HSYNC (CM2HREF) is active high and CM2HREF low means data is valid.

bit 1 Camera2 VSYNC Active Select
This bit defines VYSNC for the Camera2 interface.
When this bit = 0, the Camera2 VSYNC (CM2VREF) is active low and CM2VREF high means data is valid.
When this bit = 1, the Camera2 VSYNC (CM2VREF) is active high and CM2VREF low means data is valid.

bit 0 Camera2 Valid Input Clock Edge
This bit determines the edge at which Camera2 data is latched.
When this bit = 0, the S1D13719 latches input data at the rising edge of the clock (CM2CLKIN).
When this bit = 1, S1D13719 latches input data at the falling edge of the clock (CM2CLKIN).

REG[0108h] through REG[010Eh] are Reserved

These registers are Reserved and should not be written.

REG[0110h] Camera Mode Setting Register
Default = 0000h Read/Write

Reserved	Reserved	Camera2 Active Pull-down Disable	Camera1 Active Pull-down Disable	n/a	Fast Sampling Mode Enable	Reserved	YUV/YUV Offset Enable
15	14	13	12	11	10	9	8
ITU-R BT656 Enable	Camera Mode Select bits 2-0			Clock Output Port Select bits 2-0			Camera Module Enable
7	6	5	4	3	2	1	0

bit 15 Reserved
The default value for this bit is 0.bit 14Reserved
The default value for this bit is 0.

bit 13 Camera2 Active Pull-down Disable
This bit controls the active pull-down resistors on the Camera2 interface.
When this bit = 0, the active pull-down resistors on the Camera2 interface are enabled.
When this bit = 1, the active pull-down resistors on the Camera2 interface are disabled.

bit 12 Camera1 Active Pull-down Disable
This bit controls the active pull-down resistors on the Camera1 interface.
When this bit = 0, the active pull-down resistors on the Camera1 interface are enabled.
When this bit = 1, the active pull-down resistors on the Camera1 interface are disabled.

bit 10 Fast Sampling Mode Enable
When this bit = 0, the Fast Sampling Mode is disabled
When this bit = 1, the Fast Sampling Mode is enabled.

Note
This bit should be set when the following is true:
½ * (Internal System Clock Frequency) < Camera Clock Frequency

Note
For Camera clock divides of 1:1 and 2:1, the fast camera sampling rate must be set (REG[0110h] bit 10 = 1).

bit 9 Reserved
The default value for this bit is 0.

bit 8 YUV/YUV Offset Enable
This bit determines whether the incoming U and V data from the camera interface is internally offset. Typically, camera modules output in YUV or YCbCr offset format, therefore this bit is cleared or set to 0. If the camera data is intended for viewing after the YUV/RGB Converter (YRC), or encoding through the JPEG codec, the resulting YUV data format should be YUV or YCbCr offset.
When this bit = 0, no offset is applied to the incoming U and V camera (UV values are unmodified).
When this bit = 1, an offset is applied to the incoming U and V camera data, the incoming U and V camera data MSB are inverted.

Table 10-33: YUV/YUV Offset Enable

REG[0110h] bits 8	YUV/YUV Offset	Input Data Range	Output Data Range
0	No offset is applied	0 ≤ Y ≤ 255	Same as Input
		-128 ≤ U ≤ 127	
		-128 ≤ V ≤ 127	
		16 ≤ Y ≤ 235	
		-113 ≤ U ≤ 112	
		-113 ≤ V ≤ 112	
1	Camera format: YUV Straight range converted to YUV Offset range	0 ≤ Y ≤ 255	0 ≤ Y ≤ 255
		0 ≤ U ≤ 255	-128 ≤ U ≤ 127
		0 ≤ V ≤ 255	-128 ≤ V ≤ 127
	Camera format: YCbCr Straight range converted to YCbCr Offset range	16 ≤ Y ≤ 235	16 ≤ Y ≤ 235
		16 ≤ U ≤ 240	-113 ≤ U ≤ 112
		16 ≤ V ≤ 240	-113 ≤ V ≤ 112

bit 7 ITU-R BT656 Enable
This bit controls the active camera interface type and is valid when the interface type is YUV 4:2:2 8-bit (see REG[0102h] bit 6).
When this bit = 0, the normal camera interface is active. In this mode the hsync, vsync, clock, and data signals are independent.
When this bit = 1, the ITU-R BT656 camera interface is active. In this mode the hsync and vsync signals are mixed with the data signals.

bits 6-4 Camera Mode Select bits [2:0]
These bits select the active camera mode.

Table 10-34: Camera Mode Selection

REG[0110h] bits 6-4	Active Camera Mode
000b	Camera1 Interface Input is Active
001b	Camera2 Interface Input is Active
010b (see note)	Camera1 Interface Input is Active and Camera2 Interface Output is Active
011b - 111b	Reserved

Note

This camera mode must not be selected when any of the following interfaces are selected because the Camera2 data pins are already allocated.

- Camera1 interface is set for 16-bit YUV 4:2:2 (REG[0102h] bit 6 = 1)
- Camera2 interface is set for MPEG Codec Interface (REG[0106h] bits 7-6 = 10b)

bits 3-1 Clock Output Select bits [2:0]
These bits select the active clock output ports.

Table 10-35: Clock Output Port Selection

REG[0110h] bits 3-1	Active Clock Output Port
000b	Same Active Port as selected by REG[0110h] bits 6-4
001b	Camera1 Output Port Active Only
010b	Camera2 Output Port Active Only
011b	Both Camera1 and Camera2 Output Port Active
100b	Clock Output Inactive
101b - 111b	Reserved

bit 0 Camera Module Enable
This bit controls the camera module.
When this bit = 0, the camera module and clock output (CM1CLKOUT/CM2CLKOUT) are disabled.
When this bit = 1, the camera module and clock output (CM1CLKOUT/CM2CLKOUT) are enabled.

REG[0112h] Camera Frame Setting Register Default = 0000h							Read/Write
n/a							Raw Capture Mode Enable
15	14	13	12	11	10	9	8
Camera Frame Capture Interrupt Control	Camera Single Frame Capture Enable	Camera Frame Capture Interrupt Status Always Active	Frame Sampling Control bits 2-0			Camera Frame Capture Interrupt Polarity	Camera Frame Capture Interrupt Enable
7	6	5	4	3	2	1	0

bit 8 Raw Capture Mode Enable
This bit controls raw capture mode. When JPEG encoded data is captured, this bit must be set to 1.
When this bit = 0, raw capture mode is disabled.
When this bit = 1, raw capture mode is enabled.

Note

1. This bit reflects while VBLANK and data capture are stopped. VSYNC does not trigger.

2. The strobe function (REG[0120h]-[0124h]) cannot be used when this function is enabled.

bit 7 Camera Frame Capture Interrupt Control
This bit controls when the camera frame capture interrupt is asserted and depends on the setting of the Camera Single Frame Capture Mode bit (REG[0112h] bit 6) as follows.

For continuous frame capture mode (REG[0112h] bit 6 = 0):
When this bit = 0, the interrupt is generated when a valid frame is captured. This result also depends on the Camera Frame Capture Interrupt Status Always Active bit (REG[0112h] bit 5).
When this bit = 1, the interrupt is generated after a valid frame is captured and the capture is stopped.

For single frame capture mode (REG[0112h] bit 6 = 1):
When this bit = 0, the interrupt is generated when a valid frame is captured. This result also depends on the Camera Frame Capture Interrupt Status Always Active bit (REG[0112h] bit 5).
When this bit = 1, the interrupt is generated when a valid frame is captured.

Note

When this bit = 1, the Camera Frame Capture Interrupt Status Always Active bit (REG[0112h] bit 5) has no effect on camera frame interrupt generation.

bit 6 Camera Single Frame Capture Enable
This bit controls the camera frame capture mode of the camera interface. This bit **must not** be changed while the camera module is enabled (REG[0110h] bit 0 = 1).
When this bit = 0, frames from the camera interface are continuously captured.
When this bit = 1, the next frame from the camera interface is captured when a camera frame capture start command is issued (REG[0114h] bit 2 = 1). The camera frame capture stops after a single frame is captured.

bit 5 Camera Frame Capture Interrupt Status Always Active
When Camera Frame Capture Interrupts are enabled (REG[0112h] bit 0 = 1) this bit enables triggering of the camera frame capture interrupt on all captured camera frames. This bit has no effect if Camera Frame Capture Interrupts are disabled

When this bit = 0, the camera frame capture interrupt flag is only active when the JPEG Start/Stop Control bit is on, REG[098Ah] bit 0 = 1.
When this bit = 1, the camera frame capture interrupt flag is active on all captured camera frames.

bits 4-2 Frame Sampling Control Bits [2:0]
These bits control the camera data sampling rate in frames.

Table 10-36: Frame Sampling Control Selection

REG[0112h] bits 4-2	Frame Sampling Mode
000b	Every Frame is sampled
001b	1 Frame is sampled for every 2 Frames
010b	1 Frame is sampled for every 3 Frames
011b	1 Frame is sampled for every 4 Frames
100b	1 Frame is sampled for every 5 Frames
101b	1 Frame is sampled for every 6 Frames
110b	1 Frame is sampled for every 7 Frames
111b	Reserved

bit 1 Camera Frame Capture Interrupt Trigger Polarity
This bit controls the assertion timing of the camera frame capture interrupt.
When this bit = 0, the Camera Frame Capture Interrupt is asserted when VSYNC is active.
When this bit = 1, the Camera Frame Capture Interrupt is asserted when VSYNC is inactive.

bit 0 Camera Frame Capture Interrupt Enable
This bit controls whether a camera frame capture interrupt is generated or not.
When this bit = 0, the camera frame capture interrupt is disabled.
When this bit = 1, the camera frame capture interrupt is enabled.

REG[0114h] Camera Control Register Default = 0000h							Write Only
n/a						ITU-R BT656 Error Flag 1 Clear	ITU-R BT656 Error Flag 0 Clear
15	14	13	12	11	10	9	8
n/a				Camera Frame Capture Stop	Camera Frame Capture Start	Camera Frame Interrupt Status Clear	Camera Module Software Reset
7	6	5	4	3	2	1	0

bit 9 ITU-R BT656 Error Flag 1 Clear (Write Only)
This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).
Writing a 1 to this bit clears the ITU-R BT656 Error Flag 1 (REG[0116h] bit 9).
Writing a 0 to this bit has no hardware effect.

bit 8 ITU-R BT656 Error Flag 0 Clear (Write Only)
This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).
Writing a 1 to this bit clears the ITU-R BT656 Error Flag 0 (REG[0116h] bit 8).
Writing a 0 to this bit has no hardware effect.

Note
Both ITU-R BT656 Error Flags (bit 9 and bit 8) cannot be cleared at the same time by writing 0Ch to REG[0114h].

bit 3 Camera Frame Capture Stop (Write Only)
This bit stops image frame capturing from the camera interface.
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit stops image frame capturing.

bit 2 Camera Frame Capture Start (Write Only)
This bit starts image frame capturing from the camera interface.
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit starts image frame capturing.

bit 1 Camera Frame Interrupt Status Clear (Write Only)
This bit clears the Camera Frame Interrupt Status bit (REG[0116h] bit 1).
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit clears the Camera Frame Interrupt Status.

bit 0 Camera Module Software Reset (Write Only)
This bit initializes the camera module logic. Camera interface registers are not affected.
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit initializes the camera module.

REG[0116h] Camera Status Register
Default = 0044h Read Only

n/a						ITU-R BT656 Error Flag 1	ITU-R BT656 Error Flag 0
15	14	13	12	11	10	9	8
n/a	Camera Vsync	Effective Strobe Frame Status	Effective Frame Status	Camera Frame Capture Busy Status	Camera Frame Capture Start/Stop Flag	Camera Frame Capture Interrupt Status	n/a
7	6	5	4	3	2	1	0

bit 9 ITU-R BT656 Error Flag 1 (Read Only)
This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).
When this bit = 0, no error has occurred.
When this bit = 1, a 2-bit error is detected on the reference decode operation.

To clear this bit, see REG[0114h] bit 9.

bit 8 ITU-R BT656 Error Flag 0 (Read Only)
This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).
When this bit = 0, no error has occurred.
When this bit = 1, a 1-bit error is detected on the reference decode operation.

To clear this bit, see REG[0114h] bit 8.

bit 6 Camera VSYNC (Read Only)
This bit indicates the current condition of VSYNC from the camera interface.
When this bit = 0, VSYNC is not currently occurring.
When this bit = 1, VSYNC is currently occurring.

bit 5 Effective Strobe Frame Status (Read Only)
This bit indicates the status of the valid data captured when the strobe is enabled (REG[0124h] bit 0 = 1). This bit goes high when the valid frame for the strobe pulse is captured. It will only remain high for one frame and then go low.
This bit returns a 1, when the valid frame for the strobe pulse is captured. It remains high for only one frame and then goes low.
This bit returns a 0, when there is no valid data.

bit 4 — Effective Frame Status (Read Only)
This bit indicates whether the current frame from the camera interface is an "effective" frame based on the Frame Sampling Control bits (REG[0112h] bits 4-2).
When this bit = 0, an effective frame is not occurring.
When this bit = 1, an effective frame is occurring.

The following diagram shows an example of the Effective Frame Status bit where the Frame Sampling Control bits are set for 1 frame sampled for every 3 frames (REG[0112h] bits 4-2 = 010b).

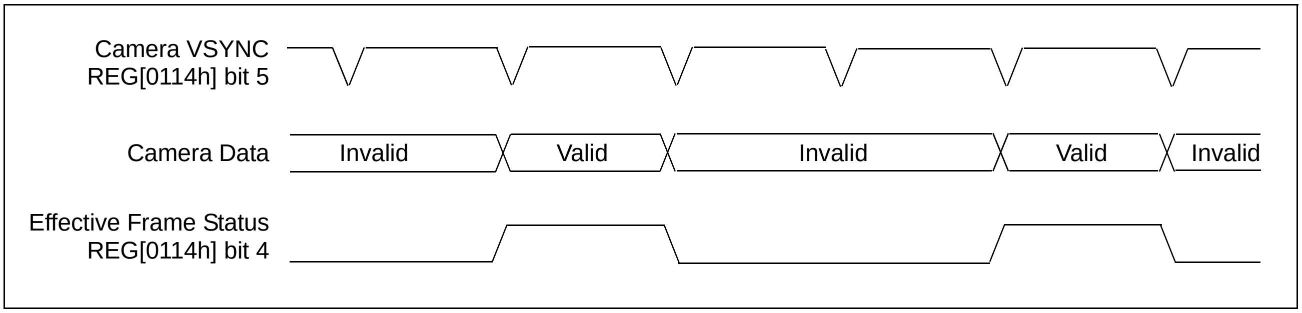

Figure 10-1: Effective Frame Status Bit Example

bit 3 — Camera Frame Capture Busy Status (Read Only)
This bit indicates the status of frame capturing from the camera interface.
When this bit = 0, frames are not being captured.
When this bit = 1, frames are being captured.

bit 2 — Camera Frame Capture Start/Stop Flag (Read Only)
This bit indicates the current state of the camera frame capture setting in relation to the setting of the Camera Frame Capture Start/Stop bits (REG0114h] bits 3-2).
When this bit = 0, camera frame capturing has been stopped.
When this bit = 1, the camera frame capturing start command has been asserted.

bit 1 — Camera Frame Capture Interrupt Status (Read Only)
This bit indicates when a Camera Frame Capture Interrupt has taken place.
When this bit = 0, a camera frame capture interrupt has not occurred.
When this bit = 1, a camera frame capture interrupt has occurred.

Note
When the Camera Frame Capture Interrupt is enabled (REG[0112h] bit 0 = 1) and the Camera Frame Capture Interrupt Status Always Active is enabled (REG[0112h] bit 5 = 0), the camera frame capture interrupt flag is only set at the first camera VREF if continuous capture mode is selected (REG[0112h] bit 6 = 0).

Note
This bit is set regardless of whether the resizers are enabled. Therefore, the Camera Frame Capture Interrupt Status bit cannot be used as an indication that a camera frame has been written to the embedded memory or the JPEG Codec.

REG[0120h] Strobe Line Delay Register Default = 0000h							Read/Write
Strobe Line Delay bits 15-8							
15	14	13	12	11	10	9	8
Strobe Line Delay bits 7-0							
7	6	5	4	3	2	1	0

bit 15-0 Strobe Line Delay bits [15:0]
When the strobe is enabled (REG[0124h] bit 0 = 1), these bits specify the delay, in lines of the camera interface, from the VSYNC input to the beginning of the Strobe Control Signal. For details on the Strobe Control Signal, see Section 21.3, “Strobe Control Signal”.

REG[0122h] Strobe Pulse Width Register Default = 0000h							Read/Write
Strobe Pulse Width bits 15-8							
15	14	13	12	11	10	9	8
Strobe Pulse Width bits 7-0							
7	6	5	4	3	2	1	0

bit 15-0 Strobe Pulse Width bits [15:0]
When the strobe is enabled (REG[0124h] bit 0 = 1), these bits specify the pulse width of the Strobe Control Signal, in lines of the camera interface. For details on the Strobe Control Signal, see Section 21.3, “Strobe Control Signal”.

Strobe Pulse Width = REG[0122] bits [15:0] + 1 in CMHREF lines

REG[0124h] Strobe Control Register
Default = 0000h — Read/Write

n/a							Reserved
15	14	13	12	11	10	9	8
Strobe Capture Delay Control bits 3-0				Strobe Port Enable	Reserved	Strobe Control Signal Polarity	Strobe Enable
7	6	5	4	3	2	1	0

bit 8 — Reserved
The default value for this bit is 0.

bits 7-4 — Strobe Capture Delay Control bits [3:0]
When the strobe is enabled (REG[0124h] bit 0 = 1), these bits specify the number of frames delayed from the strobe control signal output to the valid camera frame capture (for JPEG encoding).

This register has no effect when the strobe is disabled.

Table 10-37: Strobe Capture Delay Control

REG[0124h] bits 7-4	Delay Value
0000b	No Delay
0001b	1 Frame
0010b	2 Frames
0011b	3 Frames
0100b	4 Frames
0101b	5 Frames
0110b	6 Frames
0111b	7 Frames
1000b	8 Frames
1001b	9 Frames
1010b	10 Frames
1011b	11 Frames
1100b	12 Frames
1101b	13 Frames
1110b	14 Frames
1111b	15 Frames

bit 3 — Strobe Port Enable
This bit controls the strobe control signal (CMSTROUT) used for the Strobe Control Signal.
When this bit = 0, the strobe is disabled and CMSTROUT is Hi-Z (default).
When this bit = 1, the strobe is enabled and CMSTROUT is actively driven (high/low).

bit 2 — Reserved
The default value for this bit is 0.

bit 1 Strobe Control Signal Polarity
This bit determines the active polarity of the Strobe Control Signal and only has an effect when the output mode of the strobe port is configured for the strobe function (REG[0124h] bit 0 = 1). Setting this bit will change the inactive state of the CMSTROUT pin immediately.
When this bit = 0, the strobe control signal is active low.
When this bit = 1, the strobe control signal is active high.

bit 0 Strobe Enable
This bit configures the output mode of the Strobe Port (CMSTROUT).
When this bit = 0, the strobe port is a general purpose output port (default). In this mode CMSTROUT can be used for general purpose data output.
When this bit = 1, the strobe port is configured for the strobe (or flash) function. For further information on this function, see Section 21.3, “Strobe Control Signal”. In this mode CMSTROUT outputs a strobe pulse triggered by:

- The JPEG Start/Stop Control bit (REG[098Ah] bit 0 = 1)
- The Frame Capture Stop bit for repeat capture mode (REG[0114h] bit 2 = 1)
- The Frame Capture Start bit for single frame capture mode (REG[0114h] bit 3 = 1)

REG[0128h] MPEG Interface VSYNC Width register Default = 0000h							Read/Write
n/a						MPEG Interface VSYNC Width bits 9-8	
15	14	13	12	11	10	9	8
MPEG Interface VSYNC Width bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 MPEG Interface VSYNC Width bits [9:0]
When the MPEG interface is enabled, these bits specify the Vertical Total Period for a MPEG interface chip.

REG[0128h] bits 9-0 = Vertical Total -1 in horizontal lines (CM2HREF period)

REG[012Ah] MPEG Interface HSYNC Width register Default = 0000h							Read/Write
n/a						MPEG Interface HSYNC Width bits 9-8	
15	14	13	12	11	10	9	8
MPEG Interface HSYNC Width bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 MPEG Interface HSYNC Width bits [9:0]
When the MPEG interface is enabled, these bits specify the Horizontal Total Period for MPEG interface chip.

REG[012Ah] bits 9-0 = Horizontal Total -1 in pixels where 1 pixel is 2 CM2CLKOUTs

REG[012Ch] through REG[012Fh] are Reserved

These registers are Reserved and should not be written.

REG[0130h] CIOVDD Control register Default Determined by CNF0							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a			CIO2VDD Software Control	n/a			CIO1VDD Software Control
7	6	5	4	3	2	1	0

bit 4 CIO2VDD Software Control

This bit is the software control for the Camera2 input buffers. The default state of this bit is directly controlled by CNF0.

When this bit = 0, CIO2VDD can be safely turned off without damaging the S1D13719, or causing excessive current drain on the Camera2 input buffers.
When this bit = 1, CIO2VDD is expected to be powered and the camera2 input pins should be driven.

This bit, when 0, causes internal input buffers of the S1D13719 for the Camera2 interface to be grounded to prevent floating inputs to the S1D13719 when CIO2VDD is turned off.

The power-off sequence is:

1. Turn off the power to CIO2VDD
2. Set REG[0130h] bit 4= 0

The power-on sequence is:

1. Set REG[0130h] bit 4= 1
2. Turn on the power to CIO2VDD

bit 0 CIO1VDD Software Control

This bit is the software control for the Camera1 input buffers. The default state of this bit is directly controlled by CNF0.

When this bit = 0, CIO1VDD can be safely turned off without damaging the S1D13719, or causing excessive current drain on the Camera1 input buffers.
When this bit = 1, CIO1VDD is expected to be powered and the Camera1 input pins should be driven.

This bit, when 0, causes internal input buffers of the S1D13719 for the Camera1 interface to be grounded to prevent floating inputs to the S1D13719 when CIO1VDD is turned off.

The power-off sequence is:

1. Turn off the power to CIO1VDD
2. Set REG[0130h] bit 1= 0

The power-on sequence is:

1. Set REG[0130h] bit 1= 1
2. Turn on the power to CIO1VDD

10.4.9 Display Mode Setting Register

REG[0200h] Display Mode Setting Register 0

Default = 0000h — Read/Write

R/B Color Interpolation	Reserved	Double/Triple Buffer Window Select	Buffer Mode Select		Memory Image JPEG Encode Status (RO)	Display Mode Select bits 1-0	
15	14	13	12	11	10	9	8
LCD Software Reset (WO)	LCD Memory Image JPEG Enable	LUT2 Bypass Enable	LUT1 Bypass Enable	PIP+ Window Bpp Select bits 1-0		Main Window Bpp Select bits 1-0	
7	6	5	4	3	2	1	0

bit 15 — R/B color Interpolate when use the LUT2 Bypass mode.
When this bit = 0, RGB565 is not interpolated.
When this bit = 1, RGB565->RGB666

bit 14 — Reserved
The default value for this bit is 0.

bit 13 — Double/Triple Buffer Window Select
This bit controls which window (Main or PIP$^+$) is affected when Double/Triple Buffer Mode is enabled (REG[0200h] bits 12-11).
When this bit = 0, the PIP$^+$ window area is Double/Triple buffered.(RGB only)
When this bit = 1, the Main window area is Double/Triple buffered.

bits 12-11 — Buffer Mode Select
These bits control buffer mode select. Double or Triple buffer mode can be used to enhance the performance of the camera interface, allowing the display to be refreshed from one or two buffer while the camera interface is writing data to the other buffer. When double or triple buffer mode is enabled it applies to the window as selected by the Double/Triple Buffer Window Select bit (see REG[0200h] bit 13).

When double buffer mode is enabled, the window to be double buffered must be selected using the Double/Triple Buffer Window Select bit (REG[0200h] bit 13). The corresponding Main/PIP$^+$ window area settings, such as the Display Start Address and the Line Address Offset registers, specify the front buffer display start address and line address offset. The back buffer uses the same line address offset as the front buffer, however it's display start address is now controlled by the Back1 Buffer Display Start Address registers (REG[022Ch]-[022Ah]). The following table summarizes the possible address and offset configurations.

When triple buffer mode is enabled, the window to be triple buffered must be selected using the Double/Triple Buffer Window Select bit (REG[0200h] bit 13). The corresponding Main/PIP$^+$ window area settings, such as the Display Start Address and the Line Address Offset registers, specify the front buffer display start address and line address offset. The back buffer uses the same line address offset as the front buffer, however it's display start address is now controlled by the Back1 and Back2 Buffer Display Start Address registers (REG[022Ch]-[022Ah] and REG[0230]-[022Eh]). The following table summarizes the possible address and offset configurations.

When these bits = 00b, single buffer writing mode is selected. (Default)
When these bits = 01b, double buffer writing mode is selected.
When these bits = 10b, triple buffer writing mode is selected.
When these bits = 11b, Reserved.

Note
REG[0240] bits 13-12 must be set to the same mode as these bits or only the last back buffer image will be displayed.

Table 10-38: Double Buffer Address Registers

Double Buffer Window Select (REG[0200h] bit 13)	Front Buffer		Back Buffer	
	Start Address	Offset (RGB Only)	Start Address	Offset (RGB Only)
double buffer = Main	REG[0212h]-[0210h]	REG[0216h]	REG[022Ch]-[022Ah]	REG[0216h]
double buffer = PIP$^+$	REG[021Ah]-[0218h]	REG[021Eh]	REG[022Ch]-[022Ah]	REG[021Eh]

Note
When double buffer mode is enabled (REG[0200h] bits 12-11 = 01b), but double write buffer mode is disabled (REG[0240h] bits 13-12 = 00b), then only the back buffer memory window is displayed on the selected window (REG[0200h] bit 13).

Table 10-39: Triple Buffer Address Registers

Triple Buffer Window Select (REG[0200h] bit 13)	Front Buffer		Back1 Buffer		Back2 Buffer	
	Start Address	Offset (RGB Only)	Start Address	Offset (RGB Only)	Start Address	Offset (RGB Only)
triple buffer = Main	REG[0212h] - [0210h]	REG[0216h]	REG[022Ch] - [022Ah]	REG[0216h]	REG[0230h] - [022Eh]	REG[0216h]
triple buffer = PIP$^+$	REG[021Ah] - [0218h]	REG[021Eh]	REG[022Ch] - [022Ah]	REG[021Eh]	REG[0230h] - [022Eh]	REG[021Eh]

Note
When triple buffer mode is enabled (REG[0200h] bits 12-11 = 10b), but triple write buffer mode is disabled (REG[0240h] bits 13-12 = 00b), then only the back buffer 2 memory window is displayed on the selected window (REG[0200h] bit 13).

bit 10 — Memory Image JPEG encode Status (Read Only)
When this bit = 0, the memory image RGB to YUV convert process has finished or the memory image JPEG encode mode is not enabled.
When this bit = 1, the memory image (or display frame) JPEG encode process is in progress.

bits 9-8 — Display Mode Select bits [1:0]
These bits determine the display mode for either LCD1 or LCD2 depending on the setting of the LCD Output Port Select bits (REG[0202h] bits 12-10).

Table 10-40: Display Mode Selection

REG[0200h] bits 9-8	Display Mode
00b	Main Window only
01b	Main Window and PIP^+
10b	Reserved
11b	Main Window and PIP^+ with Overlay

bit 7 — LCD Software Reset (Write Only)
When this bit is set to 1, a software reset is performed on the LCD and RGB/YUV Converter for both LCD and Memory Image JPEG Encode modes.
When this bit is set to 0, there is no hardware effect.

bit 6 — LCD Memory Image JPEG encode Enable
This bit controls the LCD memory image RGB to YUV convert function. In this mode the memory image from the panel is sent to the JPEG encoder. For panels without ram, data is sent to the JPEG encoder with the first updated frame after the mode is enabled (REG[0200h] bit 6 = 1). For panels with ram, data is sent to the JPEG encoder using a frame forwarding trigger according to the panel type.
When this bit = 0, LCD memory image JPEG encode is disabled.
When this bit = 1, LCD memory image JPEG encode is enabled.

bit 5 — LUT2 Bypass Enable
LUT2 is associated with the PIP^+ Window. This bit determines if LUT2 is used for output to the PIP^+ Window. For more information on the display format when LUT2 is used or bypassed, see Section 12, “Display Modes”.
When this bit = 0, LUT2 is used.
When this bit = 1, LUT2 is bypassed.

Note
When YRC2(24bpp) is used, LUT2 is bypassed.

bit 4 — LUT1 Bypass Enable
LUT1 is associated with the Main Window. This bit determines if LUT1 is used for output to the Main Window. For more information on the display format when LUT1 is used or bypassed, see Section 12, “Display Modes”.
When this bit = 0, LUT1 is used.
When this bit = 1, LUT1 is bypassed.

bits 3-2 PIP+ Window Bits-per-pixel Select bits [1:0]
These bits determine the color depth for the PIP+ Window. For more information, see Section 12, “Display Modes”.

Table 10-41: LUT2 (PIP^{+} Window) Color Mode Selection

REG[0200h] bits 3-2	Color Depth	LUT2 Bypass Enable	Color
00b	8 bpp	0	LUT2 color format
		1	Data is handled as follows: R_data={r2, r1, r0, r2, r2, r2, r2, r2} G_data={g2, g1, g0, g2, g2, g2, g2, g2} B_data={b1, b0, b1, b1, b1, b1, b1, b1}
01b	16 bpp	0	LUT2 color format
		1	Data is handled as follows: R_data={r4, r3, r2, r1, r0, r4, r4, r4} G_data={g5, g4, g3, g2, g1, g0, g5, g5} B_data={b4, b3, b2, b1,b0, b4, b4, b4}
10b	Reserved	0	Reserved
		1	
11b	32 bpp	0	Reserved
		1	Same as Input Data Format

bits 1-0 Main Window Bits-per-pixel Select bits [1:0]
These bits determine the color depth for the Main Window. For more information, see Section 12, “Display Modes”.

Table 10-42: LUT1 (Main Window) Color Mode Selection

REG[0200h] bits 1-0	Color Depth	LUT1 Bypass Enable	Color
00b	8 bpp	0	LUT1 color format
		1	Data is handled as follows: R_data={r2, r1, r0, r2, r2, r2, r2, r2} G_data={g2, g1, g0, g2, g2, g2, g2, g2} B_data={b1, b0, b1, b1, b1, b1, b1, b1}
01b	16 bpp	0	LUT1 color format
		1	Data is handled as follows: R_data={r4, r3, r2, r1, r0, r4, r4, r4} G_data={g5, g4, g3, g2, g1, g0, g5, g5} B_data={b4, b3, b2, b1,b0, b4, b4, b4}
10b	Reserved	0	Reserved
		1	
11b	32 bpp	0	Reserved
		1	Same as Input Data Format

<table>
<tr><td colspan="8">REG[0202h] Display Mode Setting Register 1
Default = 0000h   Read/Write</td></tr>
<tr><td colspan="3">Active LCD Port Status bits 2-0 (RO)</td><td colspan="3">LCD Output Port Select bits 2-0</td><td>SW Video Invert</td><td>Display Blank</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>PIP+ Window Mirror Enable</td><td>Reserved</td><td colspan="2">PIP+ Window SwivelView Mode Select bits 1-0</td><td>Main Window Mirror Enable</td><td>n/a</td><td colspan="2">Main Window SwivelView Mode Select bits 1-0</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
</table>

bits 15-13 Active LCD Port Status bits [2:0] (Read Only)
These bits indicate the selected output port is active. Before sending any commands, parameters, or image data to the port, confirm that the desired port is active.

Note
These bits are read only and are only changed using the LCD Output Port Select bits 2-0 (REG[0202h] bits 12-10).

Table 10-43: Active LCD Port Status

REG[0202h] bits 15-13	Active LCD Port
000b	All Off
001b	LCD1
010b	LCD2
011b to 111b	Reserved

bits 12-10 LCD Output Port Select bits [2:0]
These bits specify the valid output port. Changes to these bits take effect after the end of the current frame. The auto transfer bits (REG[003Ch] bit 0) must be cleared before changing these bits.

Table 10-44: LCD Output Port Selection

REG[0202h] bits 12-10	LCD Output Port
000b	All Off
001b	LCD1
010b	LCD2
011b - 111b	Reserved

bit 9 Software Video Invert
This bit determines whether the RGB type panel data output (FPDAT[17:0], GPIO[9:4]) is inverted or left unchanged (normal). This bit has an effect when the display is active and when the display is blanked (see REG[0202h] bit 8).
When this bit = 0, the panel data output is left unchanged (normal).
When this bit = 1, the panel data output is inverted.

Note
If the Software Video Invert bit is set to 1 when configured for an 8-bit parallel panel, the FPDAT[15:8] pins will toggle.

bit 8 Display Blank
This bit blanks the display of RGB Type panels by disabling the display pipe and forcing all data outputs (FPDAT[17:0], GPIO[9:4]) low (or high).
When this bit = 0, the display is active.
When this bit = 1, display is blanked and all data outputs are forced low or high based on the setting of the Software Video Invert bit (REG[0202h] bit 9).

Table 10-45: LCD Interface Data Output Selection

REG[0202h] bit 8	REG[0202h] bit 9	LCD Interface Data Output
0	0	normal
	1	inverted
1	0	forced low
	1	forced high

Note
For further details, see Table 5-5: "LCD Interface Pin Mapping for Mode 1," on page 42 and Table 5-6: "LCD Interface Pin Mapping for Modes 2/3," on page 43.

bit 7 PIP$^+$ Window Mirror Enable
This bit controls the Mirror Display function for the PIP$^+$ window. Mirror display is independently controlled for the PIP$^+$ Window and the Main window (see REG[0202h] bit 3).
When this bit = 0, mirror display for the PIP$^+$ window is disabled.
When this bit = 1, mirror display for the PIP$^+$ window is enabled.

Note
This bit is effective only in RGB format. Please set REG0234h-bit 2 at the format.

bit 6 Reserved
The default value for this bit is 0.

bits 5-4 PIP+ Window SwivelView Mode Select bits [1:0]
These bits select the SwivelView mode of the PIP$^+$ window. The SwivelView mode (orientation) of the PIP$^+$ window is independently controlled for the PIP$^+$ window and the Main window (see bits 1-0). SwivelView is a counter-clockwise hardware rotation of the displayed image. For more information on SwivelView, see Section 13.1, "SwivelView™ Display".

Note
This bit is effective only in RGB format. Please set REG[0234h] bits 7-6 at the YUV format.

Table 10-46: PIP+ Window SwivelView Mode Selection

REG[0202h] bits 5-4	SwivelView Mode
00b	0° (Normal)
01b	90°
10b	180°
11b	270°

bit 3 Main Window Mirror Enable
This bit controls the Mirror Display function for the Main Window. Mirror display is independently controlled for the PIP$^+$ window (bit 7) and the main window.
When this bit = 0, mirror display for the main window is disabled.
When this bit = 1, mirror display for the main window is enabled.

bits 1-0 Main Window SwivelView Mode Select bits [1:0]
These bits select the SwivelView mode of the Main window. The SwivelView mode (orientation) of the Main window is independently controlled for the Main window and the PIP$^+$ window (see bits 5-4). SwivelView is a counter-clockwise hardware rotation of the displayed image. For more information on SwivelView, see Section 13.1, “SwivelView™ Display”.

Table 10-47: Main Window SwivelView Mode Selection

REG[0202h] bits 1-0	SwivelView Mode
00b	0° (Normal)
01b	90°
10b	180°
11b	270°

REG[0204h] Transparent Overlay Key Color Red Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Transparent Overlay Key Color Red Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Transparent Overlay Key Color Red Data bits [7:0]
These bits only have an effect when PIP$^+$ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the red color component of the Transparent Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0206h] Transparent Overlay Key Color Green Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Transparent Overlay Key Color Green Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Transparent Overlay Key Color Green Data bits [7:0]
These bits only have an effect when PIP$^+$ with Overlay is enabled (REG[0200h] bits 9-8 = 1b1). These bits set the green color component of the Transparent Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0208h] Transparent Overlay Key Color Blue Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Transparent Overlay Key Color Blue Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Transparent Overlay Key Color Blue Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the blue color component of the Transparent Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0210h] Main Window Display Start Address Register 0 Default = 0000h							Read/Write
Main Window Display Start Address bits 15-8							
15	14	13	12	11	10	9	8
Main Window Display Start Address bits 7-0							
7	6	5	4	3	2	1	0

REG[0212h] Main Window Display Start Address Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a					Main Window Display Start Address bits 18-16		
7	6	5	4	3	2	1	0

REG[0212h] bits 2-0
REG[0210h] bits 15-0 Main Window Display Start Address bits [18:0]
These bits specify the Main window starting address for the LCD image in the display buffer. At a color depth of 8 bpp, this register is incremented in 8-bit steps. At 16 bpp, this register should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and this register should be set to an even number. At 32 bpp , this register should be incremented by 32-bit steps.

REG[0214h] Main Window Start Address Status Register Default = 0001h							Read Only
n/a							
15	14	13	12	11	10	9	8
n/a						Main Window Start Address Status	
7	6	5	4	3	2	1	0

bits 1-0
Main Window Start Address Status (Read Only)
When **Double Buffer Mode is disabled** (REG[0200h] bit 12 = 0), these bits indicate the current main window frame status. These bits are updated only after the Main Window Display Start Address has been changed.
When these bits = 01b, the current frame is using the latest Main Window Display Start Address values (REG[0210h] - REG[0212h].
When these bits = 00b, the next frame will use the latest Main Window Display Start Address values (REG[0210h] - REG[0212h]).

When **Double Buffer Mode is enabled** (REG[0200h] bit 12 = 1) and the Main Window is used for the front buffer (REG[0200h] bit 13 = 1), these bits indicate which buffer is currently displayed.
When these bits = 01b, the front buffer which corresponds to the Main window area (REG[0210h] - REG[0212h]) is being displayed.
When this bit = 00b, the back buffer1 as defined by the Back Buffer Display Start Address registers (REG[022Ah] - REG[022Ch]) is being displayed.
When **Triple Buffer Mode is disabled** (REG[0200h] bit 11 = 0), this bit indicates the current main window frame status. These bits are updated only after the Main Window Display Start Address has been changed.
When these bits = 01b, the current frame is using the latest Main Window Display Start Address values (REG[0210h] - REG[0212h].
When these bits = 00b, the next frame will use the latest Main Window Display Start Address values (REG[0210h] - REG[0212h]).

When **Triple Buffer Mode is enabled** (REG[0200h] bit 11 = 1) and the Main Window is used for the front buffer (REG[0200h] bit 13 = 1), these bits indicate which buffer is currently displayed.
When these bits = 01b, the front buffer which corresponds to the Main window area (REG[0210h] - REG[0212h]) is being displayed.
When these bits = 00b, the back1 buffer as defined by the Back Buffer Display Start Address registers (REG[022Ah] - REG[022Ch]) is being displayed.
When these bits = 10b, the back2 buffer as defined by the Back Buffer Display Start Address registers (REG[022Eh] - REG[0230h]) is being displayed.

REG[0216h] Main Window Line Address Offset Register Default = 0000h							Read/Write
n/a		Main Window Vertical Pixel Doubling Enable	Main Window Horizontal Pixel Doubling Enable	Main Window Line Address Offset bits 11-8			
15	14	13	12	11	10	9	8
Main Window Line Address Offset bits 7-0							
7	6	5	4	3	2	1	0

bit 13 Main Window Pixel Doubling Vertical Enable
This bit controls the pixel doubling feature for the vertical dimension or height of the panel (i.e. 160 pixel high data doubled for a 320 pixel high panel).
When this bit = 0, there is no hardware effect.
When this bit = 1, pixel doubling in the vertical dimension (height) is enabled.

When vertical pixel doubling of the main window is enabled, the main window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 1-0) using the following formulas.
For SwivelView 0°
  Address = 0
For SwivelView 90°
  Address = (main window height - (bpp/8))
For SwivelView 180°
  Address = ((main window height - 1) x (main window width)) - (bpp/8)
For SwivelView 270°
  Address = main window line offset x ((main window width ÷ 2) - 1

bit 12 Main Window Pixel Doubling Horizontal Enable
This bit controls the pixel doubling feature for the horizontal dimension or width of the panel (i.e. 160 pixel wide data doubled for a 320 pixel wide panel)
When this bit = 0, there is no hardware effect.
When this bit = 1, pixel doubling in the horizontal dimension (width) is enabled.

When horizontal pixel doubling of the main window is enabled, the main window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 1-0) using the following formulas.
For SwivelView 0°
  Address = 0
For SwivelView 90°
  Address = (main window height - (bpp/8))
For SwivelView 180°
  Address = ((main window height - 1) x (main window width)) - (bpp/8)
For SwivelView 270°
  Address = main window line offset x ((main window width ÷ 2) - 1

bits 11-0 Main Window Line Address Offset bits [11:0]

These bits specify the offset from the beginning of one display line to the beginning of the next display line in the memory used for the main window. At a color depth of 8 bpp, these bits should be incremented by 8-bit steps. At 16 bpp, these bits should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and these bits should be set to an even number. At 32 bpp, these bits should be incremented by 32-bit steps.

Calculate the Line Address Offset as follows (valid for both pixel doubling enabled and disabled).

REG[0216h] bits 11-0 = Line width in pixels x bpp ÷ 8

REG[0218h] PIP+ Display Start Address Register 0
Default = 0000h Read/Write

PIP+ Display Start Address bits 15-8							
15	14	13	12	11	10	9	8
PIP+ Display Start Address bits 7-0							
7	6	5	4	3	2	1	0

REG[021Ah] PIP+ Display Start Address Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a					PIP+ Display Start Address bits 18-16		
7	6	5	4	3	2	1	0

REG[021Ah] bits 2-0
REG[0218h] bits 15-0 PIP+ Display Start Address bits [18:0]

These bits specify the PIP+ window starting address for the LCD image in the display buffer. When the PIP+ function is disabled (REG[0200h] bits 9-8 = 00b), this register is ignored. At a color depth of 8 bpp, this register is incremented in 8-bit steps. At 16 bpp, this register should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and this register should be set to an even number. At 32 bpp, this register should be incremented by 32-bit steps.

REG[021Ch] PIP+ Window Start Address Status Register Default = 0001h							Read Only
n/a							
15	14	13	12	11	10	9	8
n/a						PIP+ Window Start Address Status	
7	6	5	4	3	2	1	0

bits 1-0

PIP+ Window Start Address Status (Read Only)
When **Double Buffer Mode is disabled** (REG[0200h] bit 12 = 0), these bits indicate the current PIP+ window frame status. these bits are updated only after the PIP+ Window Display Start Address has been changed.
When these bits = 01b, the current frame is using the latest PIP+ Window Display Start Address values (REG[0218h] - REG[021Ah].
When these bits = 00b, the next frame will use the latest PIP+ Window Display Start Address values (REG[0218h] - REG[021Ah]).

When **Double Buffer Mode is enabled** (REG[0200h] bit 12 = 1) and the PIP+ Window is used for the front buffer (REG[0200h] bit 13 = 0), these bits indicate which buffer is currently displayed.
When these bits = 01b, the front buffer which corresponds to the PIP+ window area (REG[0218h] - REG[021Ah]) is being displayed.
When these bits = 00b, the back buffer as defined by the Back Buffer Display Start Address registers (REG[022Ah] - REG[022Ch]) is being displayed.PIP+ Window Start Address Status (Read Only)

When **Triple Buffer Mode is disabled** (REG[0200h] bit 11 = 0), this bit indicates the current PIP+ window frame status. these bits are updated only after the PIP+ Window Display Start Address has been changed.
When these bits = 01b, the current frame is using the latest PIP+ Window Display Start Address values (REG[0218h] - REG[021Ah].
When these bits = 00b, the next frame will use the latest PIP+ Window Display Start Address values (REG[0218h] - REG[021Ah]).

When **Triple Buffer Mode is enabled** (REG[0200h] bit 11 = 1) and the PIP+ Window is used for the front buffer (REG[0200h] bit 13 = 0), these bits indicate which buffer is currently displayed.
When these bits = 01b, the front buffer which corresponds to the PIP+ window area (REG[0218h] - REG[021Ah]) is being displayed.
When this bit = 00b, the back1 buffer as defined by the Back Buffer Display Start Address registers (REG[022Ah] - REG[022Ch]) is being displayed.
When these bits = 10b, the back2 buffer as defined by the Back Buffer Display Start Address registers (REG[022Eh] - REG[0230h]) is being displayed.

REG[021Eh] PIP$^+$ Window Line Address Offset Register Default = 0000h — Read/Write							
n/a		PIP$^+$ Window Pixel Doubling Vertical Enable	PIP$^+$ Window Pixel Doubling Horizontal Enable	PIP$^+$ Window Line Address Offset bits 11-8			
15	14	13	12	11	10	9	8
PIP$^+$ Window Line Address Offset bits 7-0							
7	6	5	4	3	2	1	0

bit 13 PIP$^+$ Window Pixel Doubling Vertical Enable
This bit controls the pixel doubling feature for the vertical dimension or height of the panel (i.e. 160 pixel high data doubles for a 320 pixel high panel).
When this bit = 0, there is no hardware effect.
When this bit = 1, pixel doubling in the vertical dimension (height) is enabled.

When vertical pixel doubling of the PIP$^+$ window is enabled, the PIP$^+$ window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 5-4) using the following formulas.
For SwivelView 0°
Address = 0
For SwivelView 90°
Address = (PIP$^+$ window height - (bpp/8))
For SwivelView 180°
Address = ((PIP$^+$ window height - 1) x (PIP$^+$ window width)) - (bpp/8)
For SwivelView 270°
Address = PIP$^+$ window line offset x ((PIP$^+$ window width ÷ 2) - 1

Note
This bit is effective only in RGB format.

bit 12 — PIP+ Window Pixel Doubling Horizontal Enable

This bit controls the pixel doubling feature for the horizontal dimension or width of the panel (i.e. 160 pixel wide data doubles for a 320 pixel wide panel)
When this bit = 0, there is no hardware effect.
When this bit = 1, pixel doubling in the horizontal dimension (width) is enabled.

When horizontal pixel doubling of the PIP+ window is enabled, the PIP+ window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 5-4) using the following formulas.

For SwivelView 0°
Address = 0
For SwivelView 90°
Address = (PIP+ window height - (bpp/8))
For SwivelView 180°
Address = ((PIP+ window height - 1) x (PIP+ window width)) - (bpp/8)
For SwivelView 270°
Address = PIP+ window line offset x ((PIP+ window width ÷ 2) - 1

Note
This bit is effective only in RGB format.

bits 11-0 — PIP+ Window Line Address Offset bits [11:0]

This register specifies the offset from the beginning of one display line to the beginning of the next display line in the memory of the PIP+ window. At a color depth of 8 bpp, these bits should be incremented by 8-bit steps. At 16 bpp, these bits should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and these bits should be set to an even number. At 32 bpp, these bits should be incremented by 32-bit steps.

Calculate the Line Address Offset as follows (valid for both pixel doubling enabled and disabled).
REG[021Eh] bits 11-0 = Line width in pixels x bpp ÷ 8

Note
This bit is effective only in RGB format.

REG[0220h] PIP+ X Start Positions Register Default = 0000h							Read/Write
n/a						PIP+ X Start Position bits 9-8	
15	14	13	12	11	10	9	8
PIP+ X Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP+ Window X Start Position bits [9:0]
These bits determine the X start position of the PIP+ window in relation to the origin of the panel (in pixels).

REG[0222h] PIP+ Y Start Positions Register Default = 0000h							Read/Write
n/a						PIP+ Y Start Position bits 9-8	
15	14	13	12	11	10	9	8
PIP+ Y Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP+ Window Y Start Position bits [9:0]
These bits determine the Y start position of the PIP+ window in relation to the origin of the panel (in pixels).

REG[0224h] PIP+ X End Positions Register Default = 0000h							Read/Write
n/a						PIP+ X End Position bits 9-8	
15	14	13	12	11	10	9	8
PIP+ X End Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP+ Window X End Position bits [9:0]
These bits determine the X end position of the PIP+ window in relation to the origin of the panel (in pixels).

Note
These bits must be set such that the following formula is valid.
REG[0224h] bits 9-0 < Horizontal Display Period

REG[0226h] PIP$^+$ Y End Positions Register Default = 0000h							Read/Write
n/a						PIP$^+$ Y End Position bits 9-8	
15	14	13	12	11	10	9	8
PIP$^+$ Y End Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP$^+$ Window Y End Position bits [9:0]
These bits determine the Y end position of the PIP$^+$ window in relation to the origin of the panel (in pixels).

Note
These bits must be set such that the following formula is valid.
REG[0226h] bits 9-0 < Vertical Display Period

REG[0228h] is Reserved

This register is Reserved and should not be written.

REG[022Ah] Back Buffer1 Display Start Address Register 0 Default = 0000h							Read/Write
Buck Buffer1 Display Start Address bits 15-8							
15	14	13	12	11	10	9	8
Back Buffer1 Display Start Address bits 7-0							
7	6	5	4	3	2	1	0

REG[022Ch] Back Buffer1 Display Start Address Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a					Back Buffer1 Display Start Address bits 18-16		
7	6	5	4	3	2	1	0

REG[022Ch] bits 2-0
REG[022Ah] bits 15-0 Back Buffer1 Display Start Address bits [18:0]

These bits specify the Back1 Buffer window starting address for the LCD image in the display buffer. When the Double Buffer function is disabled (REG[0200h] bits 12-11 $\neq$ 01b) and the Triple Buffer function is disabled (REG[0200h] bits 12-11 $\neq$ 10) this register is ignored.

Note

These Registers is used only with RGB format. The Double/Triple Buffer function of the YUV format is achieved only with REG[0218h] and REG[021Ah]. The specification is described to “Display Mode” Section.

REG[022Eh] Back Buffer2 Display Start Address Register 0 Default = 0000h							Read/Write
Buck Buffer2 Display Start Address bits 15-8							
15	14	13	12	11	10	9	8
Back Buffer2 Display Start Address bits 7-0							
7	6	5	4	3	2	1	0

REG[0230h] Back Buffer2 Display Start Address Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a					Back Buffer Display Start Address bits 18-16		
7	6	5	4	3	2	1	0

REG[022Eh] bits 2-0
REG[0230h] bits 15-0 Back Buffer2 Display Start Address bits [18:0]

These bits specify the Back Buffer2 window starting address for the LCD image in the display buffer. When the Triple Buffer function is disabled (REG[0200h] bits 11 = 0), this register is ignored.

Note

These Registers are used only with RGB formats. The Double/Triple Buffer function of the YUV format is achieved only with REG[0218h] and REG[021Ah]. The specification is described to “Display Mode” Section.

REG[0234h] YUV Display Control Register Default = 0000h							Read/Write
YUV Display Enable	Reserved	n/a			Reserved		n/a
15	14	13	12	11	10	9	8
YUV Display SwivelView Mode Select		n/a			YUV Display Mirror Enable	n/a	Reserved
7	6	5	4	3	2	1	8

bit 15 YUV Display Enable
This bit select the data format stored in memory to the display. When the YUV data is transferred to the LCD, it is converted to RGB by the YRC2 (YUV to RGB Converter 2). This function can provide a 24-bit color display, in the same memory footprint size as 16 bpp RGB.
When this bit = 0, the RGB data is displayed (default).
When this bit = 1, YUV 4:2:2 data is displayed.

bit 14 Reserved
The default value for this bit is 0.

bits 10-9 Reserved
The default value for these bits is 0.

bits 7-6 YUV Display SwivelView Mode Select bits [1:0]
These bits select the SwivelView mode of the YUV Display. The SwivelView mode (orientation) of the YUV Display is independently controlled for the PIP^+ window and the Main window (see bits 1-0). SwivelView is a counter-clockwise hardware rotation of the displayed image. For more information on SwivelView, see Section 13.1, “SwivelView™ Display”.

Table 10-48: YUV Display SwivelView Mode Selection

REG[0234h] bits 4-3	SwivelView Mode
00b	0° (Normal)
01b	90°
10b	180°
11b	270°

bit 2 YUV Display Mirror Enable
This bit controls the mirror function for YUV 4:2:2 display.
When this bit = 0, the mirror function is disabled (default).
When this bit = 1, the mirror function is enabled.

bit 0 Reserved
The default value for this bit is 0.

REG[0236h] YUV Display Size Register Default = 0000h							Read/Write
YUV Display Vertical Size bits 7-0							
15	14	13	12	11	10	9	8
YUV Display Horizontal Size bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 YUV Display Vertical Size bits [7:0]
When YUV 4:2:2 is displayed, these bits determine the vertical size of the YUV 4:2:2 display area, in 2 line resolution.
REG0236h] bits 15-8 = YUV 4:2:2 vertical display in lines ÷ 2

bits 7-0 YUV Display Horizontal Size bits [7:0]
When YUV 4:2:2 is displayed, these bits determine the horizontal size of the YUV 4:2:2 display area, in 2 pixel resolution.
REG[0236h] bits 7-0 = YUV 4:2:2 horizontal display in pixels ÷ 2

REG[0238h] YUV Display Start Offset Register Default = 0000h							Read/Write
YUV Display Start Vertical Offset bits 7-0							
15	14	13	12	11	10	9	8
YUV Display Start Horizontal Offset bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 YUV Display Start Vertical Offset bits [7:0]
These bits determine the vertical offset of the YUV 4:2:2 display area, in 2 line resolution.
REG[0238h] bits 15-8 = YUV 4:2:2 vertical display offset in lines ÷ 2

bits 7-0 YUV Display Start Horizontal Offset bits [7:0]
These bits determine the horizontal offset of the YUV 4:2:2 display area, in 2 pixel resolution.
REG[0238h] bits 7-0 = YUV 4:2:2 horizontal display offset in pixels ÷ 2

REG[023Ah] Fractional Zoom Register Default = 0000							Read/Write
Fractional Zoom Enable	Fractional Zoom Parameter bits 6-0						
15	14	13	12	11	10	9	8
Fractional Zoom Direction	Fractional Zoom Scale bits 6-0						
7	6	5	4	3	2	1	0

bit 15 — Fractional Zoom Enable
This bit controls the fractional zoom function.
When this bit = 0, the fractional zoom function is disabled (default).
When this bit = 1, the fractional zoom function is enabled.

bits 14-8 — Fractional Zoom Parameter bits [6:0]
These bits specify the fractional zoom parameter which is used to “fine-tune” the display image during expansion. The recommended value for these bits is as follows.

REG[023Ah] bits 14-8 = 128 - (REG[023Ah] bits 6-0)

Note
For reduction (REG[023Ah] bit 7 = 1), these bits must be set to 0.

bit 7 — Fractional Zoom Direction
This bit selects the direction of the fractional zoom.
When this bit = 0, fractional zoom expands the image (default).
When this bit = 1, fractional zoom reduces the image.

bits 6-0 Fractional Zoom Scale bits [6:0]
These bits determine the expansion/reduction scaling rate for fractional zoom as follows.

Expansion rate: 256 ÷ (REG[023Ah] bits 6-0 + 128)
Reduction rate: 256 ÷ (REG[023Ah] bits 6-0 + 128) x 2)

Table 10-49: Example Settings for Fractional Zoom

Magnification	REG[023Ah] bit 7	REG[023Ah] bits 14-8	REG[023Ah] bits 6-0
0.625	1	00	77
0.750	1	00	43
1.250	0	51	77
1.375	0	70	58
1.500	0	85	43

When the above equations are used with expansion (REG[023Ah] bit 7 = 0), the display data for the final pixel (or line) is not correct. The following equations must be used to adjust the X-size and Y-size of the PIP$^+$ window (REG[0220h] and REG[0226h].

Where:
Scale = REG[023Ah] bits 6-0
Init = REG[023Ah] bits 14-8

A = Scale + 128
X = Original horizontal size in pixels ∗ 256
Nx = Expanded horizontal size in pixels
Rx = Remainder
Y = Original vertical size in lines ∗ 256
Ny = Expanded horizontal size in pixels
Ry = Remainder

X-(A*(Nx-1)+lint) = Rx
If (Rx + A ≤ 256)
when REG[0220h] = α, REG[0224h]= α +Nx-2
If (256 < Rx + A)
when REG[0220h] = α, REG[0224h]= α +Nx-1

Y-(A*(Ny-1)+lint) = Ry
If (Ry + A ≤ 256)
when REG[0222h] = β, REG[0226h]= β +Ny-2
If (256 < Ry + A)
when REG[0222h] = β, REG[0226h]= β +Ny-1

REG[023Ch] YRC2 Translate Mode Register Default = 0005h							Read/Write
Reserved		YRC2 UV Fix Select bits 1-0		n/a			
15	14	13	12	11	10	9	8
n/a			YRC2 YUV Data Type Select	n/a	YRC2 Transfer Mode bits 2-0		
7	6	5	4	15	2	1	0

bits 15-14 Reserved
The default value for these bits is 0.

bits 13-12 YRC2 UV Fix Select bits [1:0]
These bits control the UV input to the YRC2 (YUV to RGB Converter 2).

Table 10-50: YRC2 UV Input Data Setting

REG[023Ch] bits 13-12	U Data	V Data
00b (default)	Input data	Input data
01b	REG[023Eh] bits 15-8	Input data
10b	Input data	REG[023Eh] bits 7-0
11b	REG[023Eh] bits 15-8	REG[023Eh] bits 7-0

bit 4 YRC2 YUV Data Type Select
This bit selects the YUV data type input to the YRC2 (YUV to RGB Converter 2

Table 10-51: YRC2 YUV Data Type Select

REG[023Ch] bit 4	YUV Data Type	Data Range
0 (default)	YUV	$0 \le Y \le 255$ $0 \le U \le 255$ $0 \le V \le 255$
1	YCbCr	$16 \le Y \le 235$ $16 \le U \le 240$ $16 \le V \le 240$

bits 2-0 YRC2 Transfer Mode bits [2:0]
These bits specify the YRC2 (YUV to RGB Converter 2) transfer mode. Recommended settings are provided for various specifications.

Table 10-52: YRC2 YUV/RGB Conversion Mode

REG[023Ch] bits 2-0	YUV/RGB Conversion
000b	Reserved
001b	Recommendation ITU-R BT.709
010b	Reserved
011b	Reserved
100b	Recommendation ITU-R BT.470-6 System M
101b (default)	Recommendation ITU-R BT.470-6 System B, G (Recommendation ITU-R BT.601-5)
110b	SMPTE 170M
111b	SMPTE 240M(1987)

REG[023Eh] YRC2 UV Data Fix Register Default = 0000h							Read/Write
YRC2 U Data Fix bits 7-0							
15	14	13	12	11	10	9	8
YRC2 V Data Fix bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 YRC2 U Data Fix bits [7:0]
These bits only have an effect when the YRC2 UV Fix Select bits are set to 01b or 11b (REG[023Ch] bits 13-12 = 01b or 11b). The U Data Input of the YRC2 (YUV to RGB Converter 2) data is fixed to the value of these bits.

bits 7-0 YRC1 V Data Fix bits [7:0]
These bits only have an effect when the YRC2 UV Fix Select bits are set to 10b or 11b (REG[023Ch] bits 13-12 = 10b or 11b). The V Data Input of YRC2 (YUV to RGB Converter 2) data is fixed to the value of these bits.

REG[0240h] YRC1 Translate Mode Register Default = 0605h							Read/Write
YUV/RGB Converter Bypass Enable	YUV/RGB Rectangular Write Mode Enable	YUV/RGB Converter Writing Mode Select		YUV/RGB Converter Output Bpp Select bits 1-0		YUV/RGB Converter YUV Output Data Format Select	Reserved
15	14	13	12	11	10	9	8
YUV/RGB Converter Reset	UV Fix bits 1-0 t		YUV Data Type Select	n/a	YUV/RGB Converter Transfer Mode bits 2-0		
7	6	5	4	3	2	1	0

bit 15 YUV/RGB Converter Bypass Enable
When YUV/RGB Converter (YRC) bypass mode is enabled, YUV data from the camera interface or JPEG decoder, or Host goes directly into the internal memory. When the YRC is enabled (bypass mode is disabled), incoming YUV data is converted to RGB format and stored in the display buffer to be displayed by the LCD panel.
When this bit = 0, YUV/RGB Converter bypass mode is disabled (default).
When this bit = 1, YUV/RGB Converter bypass mode is enabled.

Note
The YUV/RGB converter swaps the incoming byte data when it is disabled. To change the YUV data back to normal, set the YRC Output Data Format Select bit (REG[0240h] bit 8) to 1. Disabling the YRC is useful for cameras that can output RGB data.

bit 14
YUV/RGB Rectangular Write Mode Enable
When this bit = 0, continuous write mode is selected. In continuous write mode, data is written to the frame buffer continuously based on the YUV/RGB Converter Frame Buffer Write Start Address registers (REG[0242h]-[0244h]).
When this bit = 1, rectangular write mode is selected. In rectangular write mode, data is written based on the X Pixel Size register (REG[024Ch]) and the Frame Buffer Line Address Offset register (REG[024Eh]).

Note
YUV/RGB Rectangular Write Mode may only be enabled when Single Buffer Writing Mode is selected (REG[0240h] bit 5 = 0).

bits 13-12
YUV/RGB Converter Writing Mode Select
This bit controls switching among single/double/triple buffer writing mode. REG[0242h], REG[0244h], REG[0246h], REG[0248h], REG[024Ah], REG[024Ch] are used for double or triple buffer writing mode and only REG[0242h], REG[0244h] are used for single buffer writing mode.
When these bits = 00b, single buffer writing mode is selected.
When these bits = 01b, double buffer writing mode is selected.
When these bits = 10b, triple buffer writing mode is selected.
When these bits = 11b, Reserved.

bits 11-10
YUV/RGB Converter Output Bpp Select bits [1:0]
These bits specify the color depth in bits-per-pixel (bpp) for the YUV/RGB Converter output.

Table 10-53: YUV/RGB Converter Output Bpp Selection

REG[0240h] bits 11-10	YUV/RGB Converter Output Bpp
00b	16 bpp
01b (default)	
10b	Reserved
11b	32 bpp

bit 9 YUV/RGB Converter Output Data Format Select
This bit selects the output data format of the YUV/RGB Converter (YRC) when it is disabled (REG[0240h] bit 15 = 1). This bit has no effect when the YRC is enabled (REG[0240h] bit 15 = 0).
When this bit = 0, VYUY format is selected. See Table 10-54: “VYUY Output Data Format (REG[0240h] bit 7= 0),” on page 213.
When this bit = 1, YUYV format is selected. See Table 10-55: “YUYV Output Data Format Select (REG[0240h] bit 7= 1),” on page 213.

Table 10-54: VYUY Output Data Format (REG[0240h] bit 7= 0)

Cycle Count	1	2	3	4	...	2n+1	2n+2
D15	V_0^7	U_0^7	V_2^7	U_2^7	...	V_{2n}^7	U_{2n}^7
D14	V_0^6	U_0^6	V_2^6	U_2^6	...	V_{2n}^6	U_{2n}^6
D13	V_0^5	U_0^5	V_2^5	U_2^5	...	V_{2n}^5	U_{2n}^5
D12	V_0^4	U_0^4	V_2^4	U_2^4	...	V_{2n}^4	U_{2n}^4
D11	V_0^3	U_0^3	V_2^3	U_2^3	...	V_{2n}^3	U_{2n}^3
D10	V_0^2	U_0^2	V_2^2	U_2^2	...	V_{2n}^2	U_{2n}^2
D9	V_0^1	U_0^1	V_2^1	U_2^1	...	V_{2n}^1	U_{2n}^1
D8	V_0^0	U_0^0	V_2^0	U_2^0	...	V_{2n}^0	U_{2n}^0
D7	Y_1^7	Y_0^7	Y_3^7	Y_2^7	...	Y_{2n+1}^7	Y_{2n}^7
D6	Y_1^6	Y_0^6	Y_3^6	Y_2^6	...	Y_{2n+1}^6	Y_{2n}^6
D5	Y_1^5	Y_0^5	Y_3^5	Y_2^5	...	Y_{2n+1}^5	Y_{2n}^5
D4	Y_1^4	Y_0^4	Y_3^4	Y_2^4	...	Y_{2n+1}^4	Y_{2n}^4
D3	Y_1^3	Y_0^3	Y_3^3	Y_2^3	...	Y_{2n+1}^3	Y_{2n}^3
D2	Y_1^2	Y_0^2	Y_3^2	Y_2^2	...	Y_{2n+1}^2	Y_{2n}^2
D1	Y_1^1	Y_0^1	Y_3^1	Y_2^1	...	Y_{2n+1}^1	Y_{2n}^1
D0	Y_1^0	Y_0^0	Y_3^0	Y_2^0	...	Y_{2n+1}^0	Y_{2n}^0

Table 10-55: YUYV Output Data Format Select (REG[0240h] bit 7= 1)

Cycle Count	1	2	3	4	...	2n+1	2n+2
D15	Y_0^7	Y_1^7	Y_2^7	Y_3^7	...	Y_{2n}^7	Y_{2n+1}^7
D14	Y_0^6	Y_1^6	Y_2^6	Y_3^6	...	Y_{2n}^6	Y_{2n+1}^6
D13	Y_0^5	Y_1^5	Y_2^5	Y_3^5	...	Y_{2n}^5	Y_{2n+1}^5
D12	Y_0^4	Y_1^4	Y_2^4	Y_3^4	...	Y_{2n}^4	Y_{2n+1}^4
D11	Y_0^3	Y_1^3	Y_2^3	Y_3^3	...	Y_{2n}^3	Y_{2n+1}^3
D10	Y_0^2	Y_1^2	Y_2^2	Y_3^2	...	Y_{2n}^2	Y_{2n+1}^2
D9	Y_0^1	Y_1^1	Y_2^1	Y_3^1	...	Y_{2n}^1	Y_{2n+1}^1
D8	Y_0^0	Y_1^0	Y_2^0	Y_3^0	...	Y_{2n}^0	Y_{2n+1}^0
D7	U_0^7	V_0^7	U_2^7	V_2^7	...	U_{2n}^7	V_{2n+1}^7
D6	U_0^6	V_0^6	U_2^6	V_2^6	...	U_{2n}^6	V_{2n+1}^6
D5	U_0^5	V_0^5	U_2^5	V_2^5	...	U_{2n}^5	V_{2n+1}^5
D4	U_0^4	V_0^4	U_2^4	V_2^4	...	U_{2n}^4	V_{2n+1}^4
D3	U_0^3	V_0^3	U_2^3	V_2^3	...	U_{2n}^3	V_{2n+1}^3
D2	U_0^2	V_0^2	U_2^2	V_2^2	...	U_{2n}^2	V_{2n+1}^2
D1	U_0^1	V_0^1	U_2^1	V_2^1	...	U_{2n}^1	V_{2n+1}^1
D0	U_0^0	V_0^0	U_2^0	V_2^0	...	U_{2n}^0	V_{2n+1}^0

bit 8 Reserved
The default value for this bit is 0.

bit 7 YUV/RGB Converter Reset
This bit resets the YUV/RGB Converter (YRC). It has no effect on the YRC registers. The YRC should be reset after any changes are made to the Resizer Operation registers (REG[0930h]-[096Eh] and before performing a Memory Image JPEG Encode operation.
When this bit is set to 1, the YUV/RGB Converter is reset. This bit must be set back to 0 before the YUV/RGB Converter can be used again.
When this bit is set to 0, there is no hardware effect.

bits 6-5 UV Fix Select bits [1:0]
These bits control the UV input to the YUV/RGB Converter (YRC). The setting of these bits has an effect on the UV data even when the YRC is disabled (REG[0240h] bit 15 = 1)..

Table 10-56: UV Fix Selection

REG[0240h] bits 6-5	UV Input to the YUV/RGB Converter
00b	Original U data, original V data
01b	U data = REG[024Eh] bits 15-8, original V data
10b	Original U data, V data = REG[024Eh] bits 7-0
11b	U data = REG[024Eh] bits 15-8, V data = REG[024Eh] bits 7-0

bit 4 YUV Data Type Select
This bit specifies the data type of the YUV input to the YUV/RGB Converter (YRC)..

Table 10-57: YUV Data Type Selection

REG[0240h] bit 4	YUV Data Type	Data Range
0	YUV	0 =< Y =< 255 0 =< U =< 255 0 =< V =< 255
1	YCbCr	16 =< Y =< 235 16 =< U =< 240 16 =< V =< 240

bits 2-0 YUV/RGB Converter Transfer Mode bits [2:0]
These bits specify the YUV/RGB Transfer mode. Recommended settings are provided for various specifications..

Table 10-58: YUV/RGB Transfer Mode Selection

REG[0240h] bits 2-0	YUV/RGB Specification
000b	Reserved
001b	Recommended for ITU-R BT.709
010b	Reserved
011b	Reserved

Table 10-58: YUV/RGB Transfer Mode Selection

100b	Recommended for ITU-R BT.470-6 System M
101b (Default)	Recommended for ITU-R BT.470-6 System B, G (Recommended for ITU-R BT.601-5)
110b	SMPTE 170M
111b	SMPTE 240M(1987)

REG[0242h] YRC1 Write Start Address 0 Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
YUV/RGB Converter Write Start Address 0 bits 15-8							

7	6	5	4	3	2	1	0
YUV/RGB Converter Write Start Address 0 bits 7-0							

REG[0244h] YRC1 Write Start Address 0 Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a					YUV/RGB Converter Write Start Address bits 18-16		

REG[0244h] bits 2-0
REG[0242h] bits 15-0 YUV/RGB Converter Write Start Address 0 bits [18:0]

These bits determine the start address where the YUV/RGB Converter writes data. The YUV/RGB Converter writes data to the display buffer in 32-bit blocks, therefore bits 1-0 of this register must be set to 00b.

REG[0246h] YRC1 Write Start Address 1 Register 0 Default = 0000h							Read/Write
YUV/RGB Converter Write Start Address 1 bits 15-8							
15	14	13	12	11	10	9	8
YUV/RGB Converter Write Start Address 1 bits 7-0							
7	6	5	4	3	2	1	0

REG[0248h] YRC1 Write Start Address 1 Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a					YUV/RGB Converter Write Start Address 1 bits 19-16		
7	6	5	4	3	2	1	0

REG[0248h] bits 2-0
REG[0246h] bits 15-0 YUV/RGB Converter Write Start Address 1 bits [18:0]
These bits determine the start address for data input from the camera interface and for JPEG decoded images. This register value is valid when Frame Buffer Writing Mode Select bit (REG[0240h] bit 13-12) is set for double buffer writing mode.

REG[024Ah] YRC1 Write Start Address 2 Register 0 Default = 0000h							Read/Write
YUV/RGB Converter Write Start Address 2 bits 15-8							
15	14	13	12	11	10	9	8
YUV/RGB Converter Write Start Address 1 bits 7-0							
7	6	5	4	3	2	1	0

REG[024Ch] YRC1 Write Start Address 2 Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a					YUV/RGB Converter Write Start Address 2 bits 19-16		
7	6	5	4	3	2	1	0

REG[024Ch] bits 2-0
REG[024Ah] bits 15-0 YUV/RGB Converter Write Start Address 2 bits [18:0]
These bits determine the start address for data input from the camera interface and for JPEG decoded images. This register value is valid when Frame Buffer Writing Mode Select bit (REG[0240h] bit 13-12) is set for triple buffer writing mode.

REG[024Eh] YRC1 UV Data Fix Register Default = 0000h							Read/Write
YUV/RGB Converter U Data Fix bits 7-0							
15	14	13	12	11	10	9	8
YUV/RGB Converter V Data Fix bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 YUV/RGB Converter U Data Fix bits [7:0]
These bits only have an effect when the UV Fix Select bits are set to 01b or 11b (REG[0240h] bits 6-5 = 01b or 11b). The U Data Input of the YUV/RGB Converter data is fixed to the value of these bits.

bits 7-0 YUV/RGB Converter V Data Fix bits [7:0]
These bits only have an effect when the UV Fix Select bits are set to 10b or 11b (REG[0240h] bits 6-5 = 10b or 11b). The V Data Input of YUV/RGB Converter data is fixed to the value of these bits.

REG[0250h] YRC1 Rectangle Pixel Width Register Default = 0000h							Read/Write
n/a					YUV/RGB Converter Rectangular Pixel Width bits 10-8		
15	14	13	12	11	10	9	8
YUV/RGB Converter Rectangular Pixel Width bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 YUV/RGB Converter Rectangular Pixel Width Bits [10:0]
These bits specify the horizontal pixel width of the data being written when the YUV/RGB Converter (YRC) is configured for rectangular write mode (REG[0240h] bit 14= 1).
For a color depth of 16 bpp, it specifies an even number of pixels (only bits 9-1 are used).
For a color depth of 32 bpp, it specifies every pixel (all bits 9-0 are used).

REG[0252h] YRC1 Rectangular Line Address Offset Register Default = 0000h							Read/Write
n/a				YUV/RGB Converter Rectangular Line Address Offset bits 11-8			
15	14	13	12	11	10	9	8
YUV/RGB Converter Rectangular Line Address Offset bits 7-0							
7	6	5	4	3	2	1	0

bits 11-0 YUV/RGB Converter Rectangular Line Address Offset Bits [11:0]
These bits specify the number of pixels from the beginning of the current display line to the beginning of the next line when the YUV/RGB Converter (YRC) is configured for rectangular write mode (REG[0240h] bit 6 = 1).
For a color depth of 16 bpp, it specifies an even number of pixels (only bits 11-1 are used).
For a color depth of 32 bpp, it specifies every pixel (all bits 11-0 are used).
When the YUV/RGB Converter is disabled, it specifies every pixel (all bits 11-0 are used).

REG[0254h] YRC1 Memory Configuration Register Default = 0000h							Read Only
Reserved	n/a			Reserved	n/a		
15	14	13	12	11	10	9	8
n/a			Reserved	n/a	YUV/RGB Converter 1 SRAM I/F Write Mode Status bits 1-0 (RO)		YUV/RGB Converter 1 SRAM I/F Data Write Status (RO)
7	6	5	4	3	2	1	0

bit 15 Reserved
This bit is Reserved and should not be written.

bit 11 Reserved
This bit is Reserved and should not be written.

bit 4 Reserved
This bit is Reserved and should not be written.

bits 2-1 YUV/RGB Converter 1 SRAM I/F Data Writing Mode Status Bits [1:0] (Read Only)
These bits indicate the status of the data write mode between YRC1 and SRAM.

Table 10-59: YUV/RGB Converter 1 SRAM Interface Data Write Mode Status

REG[0254h] bits 2-1	Data Write Mode
00b	Single Buffer
01b	Double Buffer
10b	Triple Buffer
11b	Reserved

bit 0 YUV/RGB Converter 1 SRAM I/F Data Write Status (Read Only)
This bit indicates the status of YRC1 data writes to SRAM.
When this bit = 0, the YRC1 is currently writing data to SRAM.
When this bit = 1, the YRC1 is not currently written data to SRAM.

REG[0260h] RGB/YUV Converter Configuration Register
Default = 0005h — Read/Write

RYC Disable	n/a	Reserved		n/a			
15	14	13	12	11	10	9	8
n/a			YUV Data Type Select	n/a	RGB/YUV Transfer Mode bits 2-0		
7	6	5	4	3	2	1	0

bit 15 — RGB/YUV Converter (RYC) Disable
This bit controls the RGB/YUV Converter. The RGB/YUV Converter is used for Memory Image JPEG Encode mode to convert RGB data in the display buffer into YUV data that can be encoded by the JPEG codec.
When this bit = 0, the RGB/YUV Converter is enabled.
When this bit = 1, the RGB/YUV Converter is disabled (bypass mode).

bits 13-12 — Reserved
The default value for these bits is 0.

bit 4 — YUV Data Type Select
This bit selects the output data video type.
When this bit = 0, the data type is YUV.
When this bit = 1, the data type is YCbCr.

bits 2-0 — RGB/YUV Transfer Mode bits [2:0]
These bits specify the RGB/YUV transfer mode. Recommended settings are provided for various specifications..

Table 10-60: RGB/YUV Transfer Mode Selection

REG[0260h] bits 2-0	RGB/YUV Specification
000b	Reserved
001b	Recommended for ITU-R BT.709
010b	Reserved
011b	Reserved
100b	Recommended for ITU-R BT.470-6 System M
101b (Default)	Recommended for ITU-R BT.470-6 System B, G (Recommended for ITU-R BT.601-5)
110b	SMPTE 170M
111b	SMPTE 240M(1987)

REG[0262h] is Reserved

This register is Reserved and should not be written.

REG[0264h] Memory Image JPEG Encode Horizontal Display Period Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							Memory Image JPEG Encode Horizontal Display Period bit 8

7	6	5	4	3	2	1	0
Memory Image JPEG Encode Horizontal Display Period bits 7-0							

bits 8-0 Memory Image JPEG Encode Horizontal Display Period bits [8:0]
These bits specify the Horizontal Display Period for the Memory Image JPEG Encode (MIJE) function, in 2 pixel resolution.

REG[0264h] bits 8-0 = (MIJE HDP in pixels ÷ 2) - 1

REG[0266h] Memory Image JPEG Encode Vertical Display Period Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						Memory Image JPEG Encode Vertical Display Period bits 9-8	

7	6	5	4	3	2	1	0
Memory Image JPEG Encode Vertical Display Period bits 7-0							

bits 9-0 Memory Image JPEG Encode Vertical Display Period bits [9:0]
These bits specify the Vertical Display Period for the Memory Image JPEG Encode (MIJE) function, in 1 line resolution.

REG[0266h] bits 9-0 = MIJE VDP in number of lines - 1

REG[0268h] is Reserved

This register is Reserved and should not be written.

REG[0270h] Host Image JPEG Encode Control Register Default = 0000h							Read/Write
n/a	Host RGB Encode Write Data Format bits 2-0			Host RGB Encode Data End (RO)	Host RGB Encode Status (RO)	n/a	
15	14	13	12	11	10	9	8
n/a	Host RGB Encode Mode Enable	n/a					Host Image JPEG Encode Mode Select
7	6	5	4	3	2	1	0

bits 14-12 Host RGB Encode Write Data Format bits [2:0]
These bits select the host image JPEG encode write data format.

- When REG[0270h] bits [14:12] = 000b through 000b or 011b, the data is written to REG[0278h] only.
- When REG[0270h] bits [14:12] = 100b, 101b, 110b or 111b, the data is first written to REG[0278h], then REG[0276h], alternately..

Table 10-61: Host RGB Encode Write Data Format Selection

REG[0270h] bits 14-12	Host RGB Encode Write Data Format
000b	RGB 5:6:5
001b	Reserved
010b	RGB 4:4:4
011b	RGB 3:3:2
100b	RGB 8:8:8 (32 bit un-packed 1 pixel / 2 cycle)
101b	RGB 8:8:8 (24 bit packed 2 pixel / 3 cycle)
110b	RGB 6:6:6 (32 bit un-packed 1 pixel / 2 cycle)
111b	RGB 6:6:6 (24 bit packed 2 pixel / 3 cycle)

bit 11 Host RGB Encode Data End (Read Only)
This bit indicates when the host image JPEG encode mode for host memory write is not finished.
When this bit = 0, host image JPEG encode mode for host memory write is finished.
When this bit = 1, host image JPEG encode mode for host memory write is not finished.

bit 10 Host RGB Encode Status (RO)
This bit indicates when the host image JPEG encode mode for host memory is active.
When this bit = 0, host image JPEG encode mode for host memory is inactive.
When this bit = 1, host image JPEG encode mode for host memory is active.

bit 6 Host RGB Encode Enable
This bit controls the host image JPEG encode mode for host memory.
When this bit = 0, host image JPEG encode mode for host memory is disabled.
When this bit = 1, host image JPEG encode mode for host memory is enabled.

bit 0 Host Image JPEG Encode Mode Select
This bit selects the Host Image JPEG Encode source between encoding a host image from the S1D13719 memory or encoding a memory image from the host interface.
When this bit = 0, encode a host image from the S1D13719 memory.
When this bit = 1, encode from the host interface.

REG[0272h] Host Image JPEG Encode Horizontal Pixel Count Register Default = 0000h							Read/Write
n/a					Host Image JPEG Encode Horizontal Pixel Count bits 10-8		
15	14	13	12	11	10	9	8
Host Image JPEG Encode Horizontal Pixel Count bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 Host Image JPEG Encode Horizontal Pixel Count bits [10:0]
These bits represent the number of horizontal pixels for the host image JPEG encode.

Horizontal Size = (Value of this Register) + 1

The maximum horizontal size that can be encoded is 2048 pixels.

REG[0274h] Host Image JPEG Encode Vertical Line Count Register Default = 0000h							Read/Write
n/a					Host Image JPEG Encode Vertical Line Count bits 10-8		
15	14	13	12	11	10	9	8
Host Image JPEG Encode Vertical Line Count bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 Host Image JPEG Encode Vertical Line Count bits [10:0]
These bits represent the number of vertical pixels for the host image JPEG encode.

Vertical Size = (Value of this Register) + 1

The maximum vertical size that can be encoded is 2048 lines.

REG[0276h] Host Image JPEG Encode RGB Data Register 0 Default = 0000h							Read/Write
Host Image JPEG Encode RGB Data bits 15-8							
15	14	13	12	11	10	9	8
Host Image JPEG Encode RGB Data bits 7-0							
7	6	5	4	3	2	1	0

REG[0278h] Host Image JPEG Encode RGB Data Register 1 Default = 0000h							Read/Write
Host Image JPEG Encode RGB Data bits 31-24							
15	14	13	12	11	10	9	8
Host Image JPEG Encode RGB Data bits 23-16							
7	6	5	4	3	2	1	0

REG[0278h] bits 15-0
REG[0276h] bits 15-0 Host Image JPEG Encode RGB Data bits [31:0]
These bits are the RGB write data for the host image JPEG encode.

Table 10-62: Host Image JPEG Encode Write Data Format

Host Image JPEG Encode Write Data Format	Data Register	Data Register Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RGB 5:6:5	REG[0276h] Data 1	Not Used															
	REG[0278h] Data 2	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
RGB 4:4:4	REG[0276h] Data 1	Not Used															
	REG[0278h] Data 2	n/a	n/a	n/a	n/a	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
RGB 3:3:2	REG[0276h] Data 1	Not Used															
	REG[0278h] Data 2	R12	R11	R10	G12	G11	G10	B11	B10	R2	R1	R0	G2	G1	G0	B1	B0
RGB 8:8:8 (32 bit un-packed 1 pixel / 2 cycle)	REG[0276h] Data 2	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
	REG[0278h] Data 1	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	R7	R6	R5	R4	R3	R2	R1	R0
RGB 8:8:8 (24 bit packed 2 pixel / 3 cycle)	REG[0276h] Data 1	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
	REG[0278h] Data 2	B15	B14	B13	B12	B11	B10	B9	B8	R7	R6	R5	R4	R3	R2	R1	R0
	REG[0276h] Data 3	R15	R14	R13	R12	R11	R10	R9	R8	G15	G14	G13	G12	G11	G10	G9	G8
RGB 6:6:6 (32 bit un-packed 1 pixel / 2 cycle)	REG[0276h] Data 1	n/a	n/a	G5	G4	G3	G2	G1	G0	n/a	n/a	B5	B4	B3	B2	B1	B0
	REG[0278h] Data 2	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	R5	R4	R3	R2	R1	R0
RGB 6:6:6 (24 bit packed 2 pixel / 3 cycle)	REG[0276h] Data 1	n/a	n/a	G5	G4	G3	G2	G1	G0	n/a	n/a	B5	B4	B3	B2	B1	B0
	REG[0278h] Data 2	n/a	n/a	B13	B12	B11	B10	B9	B8	n/a	n/a	R5	R4	R3	R2	R1	R0
	REG[0276h] Data 3	n/a	n/a	R13	R12	R11	R10	R9	R8	n/a	n/a	G13	G12	G11	G10	G9	G8

REG[0280h] is Reserved

This register is Reserved and should not be written.

10.4.10 GPIO Registers

REG[0300h] GPIO Configuration Register 0
Default = 0000h — Read/Write

GPIO15 Config	GPIO14 Config	GPIO13 Config	GPIO12 Config	GPIO11 Config	GPIO10 Config	GPIO9 Config	GPIO8 Config
15	14	13	12	11	10	9	8
GPIO7 Config	GPIO6 Config	GPIO5 Config	GPIO4 Config	GPIO3 Config	GPIO2 Config	GPIO1 Config	GPIO0 Config
7	6	5	4	3	2	1	0

REG[0302h] GPIO Configuration Register 1
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a		GPIO21 Config	GPIO20 Config	GPIO19 Config	GPIO18 Config	GPIO17 Config	GPIO16 Config
7	6	5	4	3	2	1	0

REG[0302h] bits 5-0
REG[0300h] bits 15-0 GPIO[21:0] Pin IO Configuration

When the GPIO pins (GPIO[19:0]) are configured as inputs at RESET# (CNF1 = 1), these bits can be used to change individual GPIO pins between inputs/outputs. When the GPIO pins are configured as outputs at RESET# (CNF1 = 0), these bits are ignored and the GPIO pins are always outputs.
When this bit = 0 (default), the corresponding GPIO pin is configured as an input pin.
When this bit = 1, the corresponding GPIO pin is configured as an output pin.

REG[0304h] GPIO Input Enable Register 0
Default = 0000h — Read/Write

GPIO15 Input Enable	GPIO14 Input Enable	GPIO13 Input Enable	GPIO12 Input Enable	GPIO11 Input Enable	GPIO10 Input Enable	GPIO9 Input Enable	GPIO8 Input Enable
15	14	13	12	11	10	9	8
GPIO7 Input Enable	GPIO6 Input Enable	GPIO5 Input Enable	GPIO4 Input Enable	GPIO3 Input Enable	GPIO2 Input Enable	GPIO1 Input Enable	GPIO0 Input Enable
7	6	5	4	3	2	1	0

REG[0306h] GPIO Input Enable Register 1
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a		GPIO21 Input Enable	GPIO20 Input Enable	GPIO19 Input Enable	GPIO18 Input Enable	GPIO17 Input Enable	GPIO16 Input Enable
7	6	5	4	3	2	1	0

REG[0306h] bits 5-0
REG[0304h] bits 15-0 GPIO[21:0] Pin Input Enable

These bits are used to enable the input function of each GPIO pin. They must be changed to a 1 after power-on reset to enable the input function of the corresponding GPIO pin.
When this bit = 0 (default), the input function for the corresponding GPIO pin is disabled.
When this bit = 1, the input function for the corresponding GPIO pin is enabled.

Note

When the GPIO pins are configured as outputs at RESET# (CNF1 = 0), the GPIO pins are always outputs and these bits have no effect.

REG[0308h] GPIO Pull Down Control Register 0 Default = FFFFh							Read/Write
GPIO15 Pull-down Control	GPIO14 Pull-down Control	GPIO13 Pull-down Control	GPIO12 Pull-down Control	GPIO11 Pull-down Control	GPIO10 Pull-down Control	GPIO9 Pull-down Control	GPIO8 Pull-down Control
15	14	13	12	11	10	9	8
GPIO7 Pull-down Control	GPIO6 Pull-down Control	GPIO5 Pull-down Control	GPIO4 Pull-down Control	GPIO3 Pull-down Control	GPIO2 Pull-down Control	GPIO1 Pull-down Control	GPIO0 Pull-down Control
7	6	5	4	3	2	1	0

REG[030Ah] GPIO Pull Down Control Register 1 Default = 003Fh							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a		GPIO21 Pull-down Control	GPIO21 Pull-down Control	GPIO19 Pull-down Control	GPIO18 Pull-down Control	GPIO17 Pull-down Control	GPIO16 Pull-down Control
7	6	5	4	3	2	1	0

REG[030Ah] bits 5-0
REG[0308h] bits 15-0 GPIO[21:0] Pull-down Control

All GPIO pins have internal pull-down resistors. These bits individually control the state of the pull-down resistors.
When the bit = 0, the pull-down resistor for the associated GPIO pin is inactive.
When the bit = 1, the pull-down resistor for the associated GPIO pin is active.

REG[030Ch] GPIO Status Register 0 Default = 0000h							Read/Write
GPIO15 Status	GPIO14 Status	GPIO13 Status	GPIO12 Status	GPIO11 Status	GPIO10 Status	GPIO9 Status	GPIO8 Status
15	14	13	12	11	10	9	8
GPIO7 Status	GPIO6 Status	GPIO5 Status	GPIO4 Status	GPIO3 Status	GPIO2 Status	GPIO1 Status	GPIO0 Status
7	6	5	4	3	2	1	0

REG[030Eh] GPIO Status Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a		GPIO21 Status	GPIO20 Status	GPIO19 Status	GPIO18 Status	GPIO17 Status	GPIO16 Status
7	6	5	4	3	2	1	0

REG[030Eh] bits 5-0
REG[030Ch] bits 15-0 GPIO[21:0] Pin IO Status

When GPIOx is configured as an output (see REG[0300h]-REG[0302h]), writing a 1 to this bit drives GPIOx high and writing a 0 to this bit drives GPIOx low.
When GPIOx is configured as an input (see REG[0300h]-REG[0302h]), a read from this bit returns the status of GPIOx.

Note

To read the status of a GPIO pin configured as an input, the GPIO pin must first have it’s input function enabled using REG[0304h]-REG[0306h].

10.4.11 Overlay Registers

REG[0310h] Average Overlay Key Color Red Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Average Overlay Key Color Red Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Average Overlay Key Color Red Data bits [7:0]
These bits only have an effect when PIP^+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the red color component of the Average Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0312h] Average Overlay Key Color Green Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Average Overlay Key Color Green Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Average Overlay Key Color Green Data bits [7:0]
These bits only have an effect when PIP$^+$ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the green color component of the Average Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0314h] Average Overlay Key Color Blue Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Average Overlay Key Color Blue Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Average Overlay Key Color Blue Data bits [7:0]
These bits only have an effect when PIP$^+$ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the blue color component of the Average Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0316h] AND Overlay Key Color Red Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
AND Overlay Key Color Red Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 AND Overlay Key Color Red Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the red color component of the AND Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0318h] AND Overlay Key Color Green Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
AND Overlay Key Color Green Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 AND Overlay Key Color Green Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the green color component of the AND Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[031Ah] AND Overlay Key Color Blue Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
AND Overlay Key Color Blue Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 AND Overlay Key Color Blue Data bits [7:0]
These bits only have an effect when PIP$^+$ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the blue color component of the AND Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[031Ch] OR Overlay Key Color Red Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
OR Overlay Key Color Red Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 OR Overlay Key Color Red Data bits [7:0]
These bits only have an effect when PIP$^+$ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the red color component of the OR Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[031Eh] OR Overlay Key Color Green Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
OR Overlay Key Color Green Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 OR Overlay Key Color Green Data bits [7:0]
These bits only have an effect when PIP$^+$ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the green color component of the OR Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0320h] OR Overlay Key Color Blue Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
OR Overlay Key Color Blue Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 OR Overlay Key Color Blue Data bits [7:0]
These bits only have an effect when PIP$^+$ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the blue color component of the OR Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0322h] INV Overlay Key Color Red Data Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INV Overlay Key Color Red Data bits 7-0							

bits 7-0 INV Overlay Key Color Red Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the red color component of the INV Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0324h] INV Overlay Key Color Green Data Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INV Overlay Key Color Green Data bits 7-0							

bits 7-0 INV Overlay Key Color Green Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the green color component of the INV Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0326h] INV Overlay Key Color Blue Data Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
INV Overlay Key Color Blue Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 — INV Overlay Key Color Blue Data bits [7:0]
These bits only have an effect when PIP^+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the blue color component of the INV Overlay Key Color. For more information on Overlays, see Section 13.4, “Overlay Display”.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 12.3.5, “Bit Cover When LUT Bypassed”.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0328h] Overlay Miscellaneous Register Default = 0000h							Read/Write
Overlay PIP+ Window Bit Shift	n/a	Overlay Main Window Bit Shift	n/a				
15	14	13	12	11	10	9	8
n/a			INV Overlay Key Color Enable	OR Overlay Key Color Enable	AND Overlay Key Color Enable	Average Overlay Key Color Enable	Transparent Overlay Key Color Enable
7	6	5	4	3	2	1	0

bit 15 — Overlay PIP^+ Window Bit Shift
This bit only has an effect if the Display Mode Select bits are set for PIP^+ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 13.4, “Overlay Display”.
When this bit = 0, the PIP^+ window pixel data is normal.
When this bit = 1, the PIP^+ window is pixel data is bit shifted to the right by 1 bit.

bits 13 — Overlay Main Window Bit Shift
This bit only has an effect if the Display Mode Select bits are set for PIP+ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 13.4, “Overlay Display”.
When this bit = 0, the main window pixel data is normal.
When this bit = 1, the main window pixel data is bit shifted to the right by 1 bit.

bit 4 INV Overlay Key Color Enable
This bit only has an effect if the Display Mode Select bits are set for PIP+ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 13.4, “Overlay Display”.
When this bit = 0, the INV overlay key color function is disabled.
When this bit = 1, the INV overlay key color function is enabled.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

bit 3 OR Overlay Key Color Enable
This bit only has an effect if the Display Mode Select bits are set for PIP+ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 13.4, “Overlay Display”.
When this bit = 0, the OR overlay key color function is disabled.
When this bit = 1, the OR overlay key color function is enabled.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

bit 2 AND Overlay Key Color Enable
This bit only has an effect if the Display Mode Select bits are set for PIP+ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 13.4, “Overlay Display”.
When this bit = 0, the AND overlay key color function is disabled.
When this bit = 1, the AND overlay key color function is enabled.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

bit 1 Average Overlay Key Color Enable
This bit only has an effect if the Display Mode Select bits are set for PIP^+ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 13.4, “Overlay Display”.
When this bit = 0, the average overlay key color function is disabled.
When this bit = 1, the average overlay key color function is enabled.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

bit 0 Transparent Overlay Key Color Enable
This bit only has an effect if the Display Mode Select bits are set for PIP^+ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 13.4, “Overlay Display”.
When this bit = 0, the transparent overlay key color function is disabled.
When this bit = 1, the transparent overlay key color function is enabled.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

10.4.12 LUT1 (Main Window)

	High Byte	Low Byte
0400h	Green 0	Red 0
0402h	n/a	Blue 0
0404h	Green 1	Red 1
	⋮	⋮
07FEh	n/a	Blue 255

Figure 10-2: LUT1 Mapping

REG[0400 - 07FCh] LUT1 Data Register 0 Default = not applicable							Write Only
LUT1 Green Data bits 7-0							
15	14	13	12	11	10	9	8
LUT1 Red Data bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 LUT1 (Main Window) Green Data bits [7:0]
These bits are used to set the LUT1 Green Data. There are 256 entries in LUT1 from REG[0400h] to REG[07FCh]. LUT1 is used for the Main Window.

bits 7-0 LUT1 (Main Window) Red Data bits [7:0]
These bits are used to set the LUT1 Red Data. There are 256 entries in LUT1 from REG[0400h] to REG[07FCh]. LUT1 is used for the Main Window.

Note
Wait (7Ts) is necessary to read this register. Please apply a Soft Wait when Host is in Indirect Interface Mode.

REG[0402 - 07FEh] LUT1 Data Register 1 Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
LUT1 Blue Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 LUT1 (Main Window) Blue Data bits [7:0]
These bits are used to set the LUT1 Blue Data. There are 256 entries in LUT1 from REG[0402h] to REG[07FEh]. LUT1 is used for the Main Window.

Note
Wait (7Ts) is necessary to read this register. Please apply a Soft Wait when Host is in Indirect Interface Mode.

10.4.13 LUT2 (PIP$^+$ Window)

	High Byte	Low Byte
0800h	Green 0	Red 0
0802h	n/a	Blue 0
0804h	Green 1	Red 1
	⋮	⋮
08FEh	n/a	Blue 63

Figure 10-3: LUT2 mapping

REG[0800 - 08FCh] LUT2 Data Register 0 Default = not applicable							Write Only
LUT2 Green Data bits 7-0							
15	14	13	12	11	10	9	8
LUT2 Red Data bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 LUT2 (PIP$^+$ Window) Green Data bits [7:0]
These bits are used to set the LUT2 Green Data. There are 64 entries in LUT2 from REG[0800h] to REG[08FCh]. LUT2 is used for the PIP$^+$ Window.

bits 7-0 LUT2 (PIP$^+$ Window) Red Data bits [7:0]
These bits are used to set the LUT2 Red Data. There are 64 entries in LUT2 from REG[0800h] to REG[08FCh]. LUT2 is used for the PIP$^+$ Window.

Note
Wait (7Ts) is necessary to read this register. Please apply a Soft Wait when Host is in Indirect Interface Mode.

REG[0802 - 08FEh] LUT2 Data Register 1 Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
LUT2 Blue Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 LUT2 (PIP$^+$ Window) Blue Data bits [7:0]
These bits are used to set the LUT2 Blue Data. There are 64 entries in LUT2 from REG[0802h] to REG[08FEh]. LUT2 is used for the PIP$^+$ Window.

Note
Wait (7Ts) is necessary to read this register. Please apply a Soft Wait when Host is in Indirect Interface Mode.

10.4.14 Resizer Operation Registers

Note

The resizer registers must not be changed while receiving data from the camera interface, JPEG decoder, or host interface.

<table>
<tr><td colspan="8">REG[0930h] Global Resizer Control Register
Default = 0000h — Read/Write</td></tr>
<tr><td colspan="5">n/a</td><td>Resizer Frame Reduction</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">n/a</td><td>Camera Jpeg Data Input En</td><td>Captured Data Input Select (WO)</td><td>Output Source Select</td><td>n/a</td><td colspan="2">Camera Display Control bits 1-0</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
</table>

bit 10 Resizer Frame Reduction
This bit controls frame reduction in the resizer block.
When this bit = 0, the resizer performs no reduction.
When this bit = 1, the resizer performs frame reduction by using only every second frame.

bit 9 Reserved
The default value for this bit is 0.

bit 8 Reserved
The default value for this bit is 0.

bit 5 Camera Jpeg Encode Data Input Enable
When the JPEG encoded data is input from CMOS camera (ET8E90-AS), this bit =1.
When this bit = 0, input except Jpeg encoded data.
When this bit = 1, the following operation.
a) The YRC Block is stopped.
b) The dummy V/HSync signal is output from the Resizer block to the JPEG block.

bit 4 Captured Data Input Select (Write Only)
This bit selects the data input for the capture resizer.
When this bit = 0, input from the camera interface is selected.
When this bit = 1, input from the RGB/YUV Converter (RYC) is selected.

bit 3 Output Source Select
This bit selects which resizer outputs data to the YUV/RGB Converter (YRC). Typically, the view resizer is selected when data comes from the camera interface since JPEG encode dimensions may differ from display dimensions. For JPEG decode and host to S1D13719 YUV mode, the view resizer must be selected.
When this bit = 0, the view resizer outputs data to the YRC.
When this bit = 1, the capture resizer outputs data to the YRC and the view resizer logic is powered down.

Table 10-63: Output Source Select

Output Source Select REG[0930h] bit 3	View Resizer Enable REG[0940h] bit 0	Capture Resizer Enable REG[0960h] bit 0	to YUV/RGB Converter	to JPEG Line Buffer
0	0	0	—	—
0	0	1	—	—
0	1	0	Available	—
0	1	1	Available	Available
1	0	0	—	—
1	0	1	Available	Available
1	1	0	—	—
1	1	1	Available	Available

bits 1-0 Camera Display Control bits [1:0]
These bits control how camera data is displayed when a JPEG encode operation is performed (REG[0980h] bits 3-1 = 000b) and when YUV to Host mode (JPEG Bypass) is enabled (REG[0980h] bits 3-1 = 011b or 111b).

Table 10-64: Camera Display Control Selection

REG[0930h] bits 1-0	Function
00b	**JPEG Encode:** YUV data from the camera interface is continuously written to the display buffer until a JPEG encode operation is performed. When a JPEG encode operation is started (REG[098Ah] bit 0 = 1), camera data is no longer written to the display buffer once the next frame is written. After REG[098Ah] bit 0 is set to 0, camera data is again written to the display buffer from the next frame. **JPEG Bypass:** YUV data from the camera interface is continuously written to the JPEG FIFO and converted YUV data (YUV/RGB Converter) is continuously written to the display buffer.
01b	**JPEG Encode:** When a JPEG encode operation is started, REG[098A] bit 0 = 1b, only the next frame of camera data is written to the display buffer. When a JPEG encode operation is not enabled, REG[098A] bit 0 = 0b, camera data is not written to the display buffer. **JPEG Bypass:** YUV data from the camera interface is continuously written to the JPEG FIFO. When the shutter is enabled, REG[098A] bit 0 = 1b, camera data is written to the display buffer. When the shutter is disabled, REG[098A] bit 0 = 0b, camera data is not written to the display buffer.
10b	**JPEG Encode:** Data from the camera interface is always written to the display buffer. **JPEG Bypass:** YUV data from the camera interface is continuously written to the JPEG FIFO and converted YUV data (YUV/RGB Converter) is continuously written to the display buffer.
11b	Reserved.

REG[0932h] through REG[093Eh] are Reserved

These registers are Reserved and should not be written.

View (Display) Resizer Registers

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REG[0940h] View Resizer Control Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
View Resizer Software Reset (WO)	n/a				View Resizer Independent Horizontal/Vertical Scaling Enable	View Resizer Register Update VSYNC Enable	View Resizer Enable
7	6	5	4	3	2	1	0

bit 7 View Resizer Software Reset (Write Only)
When the resizers are activated by writing a 1 to REG[0940h] bit 0 or REG[0960h] bit 0 and a 1 is written to this bit, the view resizer logic is reset.
When a 0 is written to this bit, there is no hardware effect.

bit 2 View Resizer Independent Horizontal/Vertical Scaling Enable
When this bit = 0, the horizontal and vertical scaling rates are the same. Both horizontal and vertical scaling rates are controlled by REG[094Ch] bits 5-0.
When this bit = 1, the horizontal and vertical scaling rates can be selected independently. Horizontal scaling rate is controlled by REG[094Ch] bits 5-0 and vertical scaling rate is controlled by REG[094Eh] bits 13-8.

bit 1 View Resizer Register Update VSYNC Enable
When this bit = 0, the View Resizer use the new register value immediately.
When this bit = 1, the View Resizer uses the previous register value until the next VSYNC occurs.

bit 0 View Resizer Enable
This bit controls the view resizer logic.
When this bit = 0, the view resizer logic is disabled.
When this bit = 1, the view resizer logic is enabled.

Note
When this bit and the Capture Resizer Enable bit (REG[0960h] bit 0) are both set to 0, the clock to the resizer block is automatically stopped.

REG[0944h] View Resizer Start X Position Register Default = 0000h							Read/Write
n/a					View Resizer Start X Position bits 10-8		
15	14	13	12	11	10	9	8
View Resizer Start X Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 View Resizer Start X Position bits [10:0]
These bits determine the X start position for the View Resizer. These bits must be programmed according to the restrictions in Section 15, “Resizers”.

REG[0946h] View Resizer Start Y Position Register Default = 0000h							Read/Write
n/a					View Resizer Start Y Position bits 10-8		
15	14	13	12	11	10	9	8
View Resizer Start Y Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 View Resizer Start Y Position bits [10:0]
These bits determine the Y start position for the View Resizer. These bits must be programmed according to the restrictions in Section 15, “Resizers”.

REG[0948h] View Resizer End X Position Register Default = 027Fh							Read/Write
n/a					View Resizer End X Position bits 10-8		
15	14	13	12	11	10	9	8
View Resizer End X Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 View Resizer End X Position bits [10:0]
These bits determine the X End position for the View Resizer. These bits must be programmed according to the restrictions in Section 15, “Resizers”.

REG[094Ah] View Resizer End Y Position Register Default = 01DFh							Read/Write
n/a					View Resizer End Y Position bits 10-8		
15	14	13	12	11	10	9	8
View Resizer End Y Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 View Resizer End Y Position bits [10:0]
These bits determine the Y end position for the View Resizer. These bits must be programmed according to the restrictions in Section 15, “Resizers”.

REG[094Ch] View Resizer Operation Setting Register 0							
Default = 8080h							Read/Write
View Resizer Vertical Scaling Rate bits 7-0							
15	14	13	12	11	10	9	8
View Resizer Horizontal Scaling Rate bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 View Resizer Vertical Scaling Rate bits [7:0]
These bits determine the view resizer vertical scaling rate when REG[0940h] bit 2 = 1. Not all scaling rates are available for all scaling modes (see REG[094Eh]).

Table 10-65: View Resizer Vertical Scaling Rate Selection

REG[094Ch] bits 15-8	**View Resizer Vertical Scaling Rate**			
	REG[094Eh] bits 1-0 = 00b	**REG[094Eh] bits 1-0 = 01b**	**REG[094Eh] bits 1-0 = 10b**	**REG[094Eh] bits 1-0 = 11b**
0000 0000b	Reserved	Reserved	Reserved	Reserved
0000 0001b	n/a	1/128	1/128	Reserved
0000 0010b	n/a	2/128	2/128	Reserved
0000 0011b	n/a	3/128	3/128	Reserved
0000 0100b	n/a	4/128	4/128	Reserved
0000 0101b	n/a	5/128	5/128	Reserved
0000 0110b	n/a	6/128	6/128	Reserved
0000 0111b	n/a	7/128	7/128	Reserved
0000 1000b	n/a	8/128	8/128	Reserved
0000 1001b	n/a	9/128	9/128	Reserved
0000 1010b	n/a	10/128	10/128	Reserved
0000 1011b	n/a	11/128	11/128	Reserved
0000 1100b	n/a	12/128	12/128	Reserved
0000 1101b	n/a	13/128	13/128	Reserved
0000 1110b	n/a	14/128	14/128	Reserved
0000 1111b	n/a	15/128	15/128	Reserved
0001 0000b	n/a	16/128	16/128	Reserved
0001 0001b	n/a	17/128	17/128	Reserved
0001 0010b	n/a	18/128	18/128	Reserved
0001 0011b	n/a	19/128	19/128	Reserved
0001 0100b	n/a	20/128	20/128	Reserved
0001 0101b	n/a	21/128	21/128	Reserved
0001 0110b	n/a	22/128	22/128	Reserved
0001 0111b	n/a	23/128	23/128	Reserved
0001 1000b	n/a	24/128	24/128	Reserved
0001 1001b	n/a	25/128	25/128	Reserved
0001 1010b	n/a	26/128	26/128	Reserved
0001 1011b	n/a	27/128	27/128	Reserved
0001 1100b	n/a	28/128	28/128	Reserved
0001 1101b	n/a	29/128	29/128	Reserved
0001 1110b	n/a	30/128	30/128	Reserved
0001 1111b	n/a	31/128	31/128	Reserved
0010 0000b	n/a	32/128	32/128	Reserved
0010 0001b ～ 0011 1111b	n/a	33/128 ～ 63/128	33/128 ～ 63/128	Reserved
0100 0000b	n/a	64/128	64/128	Reserved
0100 0001b ～ 0111 1111b	n/a	65/128 ～ 127/128	65/128 ～ 127/128	Reserved
1000 0000b	n/a	128/128	128/128	Reserved

bits 7-0 View Resizer Horizontal Scaling Rate bits [7:0]
These bits determine the view resizer horizontal scaling rate when REG[0940h] bit 2 = 1. When REG[0940h] bit 2 = 0, these bits specify both the horizontal and the vertical scaling rate. Not all scaling rates are available for all scaling modes (see REG[094Eh]).

Table 10-66: View Resizer Horizontal Scaling Rate Selection

REG[094Ch] bits 15-8	View Resizer Vertical Scaling Rate			
	REG[094Eh] bits 1-0 = 00b	REG[094Eh] bits 1-0 = 01b	REG[094Eh] bits 1-0 = 10b	REG[094Eh] bits 1-0 = 11b
0000 0000b	Reserved	Reserved	Reserved	Reserved
0000 0001b	n/a	1/128	1/128	Reserved
0000 0010b	n/a	2/128	2/128	Reserved
0000 0011b	n/a	3/128	Reserved	Reserved
0000 0100b	n/a	4/128	4/128	Reserved
0000 0101b	n/a	5/128	Reserved	Reserved
0000 0110b	n/a	6/128	Reserved	Reserved
0000 0111b	n/a	7/128	Reserved	Reserved
0000 1000b	n/a	8/128	8/128	Reserved
0000 1001b	n/a	9/128	Reserved	Reserved
0000 1010b	n/a	10/128	Reserved	Reserved
0000 1011b	n/a	11/128	Reserved	Reserved
0000 1100b	n/a	12/128	Reserved	Reserved
0000 1101b	n/a	13/128	Reserved	Reserved
0000 1110b	n/a	14/128	Reserved	Reserved
0000 1111b	n/a	15/128	Reserved	Reserved
0001 0000b	n/a	16/128	16/128	Reserved
0001 0001b	n/a	17/128	Reserved	Reserved
0001 0010b	n/a	18/128	Reserved	Reserved
0001 0011b	n/a	19/128	Reserved	Reserved
0001 0100b	n/a	20/128	Reserved	Reserved
0001 0101b	n/a	21/128	Reserved	Reserved
0001 0110b	n/a	22/128	Reserved	Reserved
0001 0111b	n/a	23/128	Reserved	Reserved
0001 1000b	n/a	24/128	Reserved	Reserved
0001 1001b	n/a	25/128	Reserved	Reserved
0001 1010b	n/a	26/128	Reserved	Reserved
0001 1011b	n/a	27/128	Reserved	Reserved
0001 1100b	n/a	28/128	Reserved	Reserved
0001 1101b	n/a	29/128	Reserved	Reserved
0001 1110b	n/a	30/128	Reserved	Reserved
0001 1111b	n/a	31/128	Reserved	Reserved
0010 0000b	n/a	32/128	32/128	Reserved
0010 0001b ～ 0011 1111b	n/a	33/128 ～ 63/128	Reserved	Reserved
0100 0000b	n/a	64/128	64/128	Reserved
0100 0001b ～ 0111 1111b	n/a	65/128 ～ 127/128	Reserved	Reserved
1000 0000b	n/a	128/128	128/128	Reserved

REG[094Eh] View Resizer Operation Setting Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a				Reserved		View Resizer Scaling Mode bits 1-0	
7	6	5	4	3	2	1	0

bits 3-2 Reserved
The default value for these bits is 0.

bits 1-0 View Resizer Scaling Mode bits [1:0]
These bits determine the view resizer scaling mode. Not all scaling modes are available for all scaling rates. Before selecting a scaling mode, set the View Resizer Vertical Scaling Rate bits (REG[094Eh] bits 13-8) and/or the View Resizer Horizontal Scaling Rate bits (REG[094Ch] bits 5-0) to a valid scaling rate. Enabling a scaling mode with an unsupported scaling rate (reserved or n/a) may turn off the view resizer.

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Table 10-67: View Resizer Scaling Mode Selection

REG[094Eh] bits 1-0	View Resizer Scaling Mode
00b	no resizer scaling
01b	V/H Reduction
10b	V: Reduction, H: Average
11b	Reserved

Capture (Encode) Resizer Registers

REG[0960h] Capture Resizer Control Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Capture Resizer Software Reset (WO)	n/a				Capture Resizer Independent Horizontal/Vertical Scaling Enable	Capture Resizer Register Update VSYNC Enable	Capture Resizer Enable
7	6	5	4	3	2	1	0

bit 7 Capture Resizer Software Reset (Write Only)
When a 0 is written to this bit, there is no hardware effect.
When the resizers are activated by writing a 1 to REG[940h] bit 0 or REG[0960h] bit 0 and a 1 is written to this bit, the capture resizer logic is reset.

bit 2 Capture Resizer Independent Horizontal/Vertical Scaling Enable
When this bit = 0, the horizontal and vertical scaling rates are the same. Both horizontal and vertical scaling rates are controlled by REG[096Ch] bits 4-0.
When this bit = 1, the horizontal and vertical scaling rates can be selected independently. Horizontal scaling rate is controlled by REG[096Ch] bits 4-0 and vertical scaling rate is controlled by REG[096Ch] bits 12-8.

bit 1 Capture Resizer Register Update VSYNC Enable
When this bit = 0, the Capture Resizer use the new register value immediately.
When this bit = 1, the Capture Resizer uses the previous register value until the next VSYNC occurs.

bit 0 Capture Resizer Enable
This bit controls the capture resizer logic.
When this bit = 0, the capture resizer logic is disabled.
When this bit = 1, the capture resizer logic is enabled.

Note
When this bit and the View Resizer Enable bit (REG[0940h] bit 0) are both set to 0, the clock to the resizer block is automatically stopped.

REG[0964h] Capture Resizer Start X Position Register Default = 0000h							Read/Write
n/a					Capture Resizer Start X Position bits 10-0		
15	14	13	12	11	10	9	8
Capture Resizer Start X Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 Capture Resizer Start X Position bits [10:0]
These bits determine the X start position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 15, “Resizers”.

The following image size limitations must be observed when the JPEG functions (or JPEG Bypass) are used.

Table 10-68: Capture Resizer Limitations

YUV Format	Minimum Horizontal Resolution	Minimum Vertical Resolution	Minimum Size
YUV 4:4:4	multiples of 1 pixel	multiples of 1 line	8 pixels/8 lines
YUV 4:2:2	multiples of 2 pixels	multiples of 1 line	16 pixels/8 lines
YUV 4:2:0	multiples of 2 pixels	multiples of 2 lines	16 pixels/16 lines
YUV 4:1:1	multiples of 4 pixels	multiples of 1 line	32 pixels/8 lines

REG[0966h] Capture Resizer Start Y Position Register Default = 0000h							Read/Write
n/a					Capture Resizer Start Y Position bits 10-8		
15	14	13	12	11	10	9	8
Capture Resizer Start Y Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 Capture Resizer Start Y Position bits [10:0]
These bits determine the Y start position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 15, “Resizers”.

REG[0968h] Capture Resizer End X Position Register Default = 027Fh							Read/Write
n/a					Capture Resizer End X Position bits 10-8		
15	14	13	12	11	10	9	8
Capture Resizer End X Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 Capture Resizer End X Position bits [10:0]
These bits determine the X End position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 15, “Resizers”.

REG[096Ah] Capture Resizer End Y Position Register Default = 01DFh							Read/Write
n/a					Capture Resizer End Y Position bits 10-8		
15	14	13	12	11	10	9	8
Capture Resizer End Y Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 Capture Resizer End Y Position bits [10:0]
These bits determine the Y end position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 15, “Resizers”.

REG[096Ch] Capture Resizer Operation Setting Register 0 Default = 8080h							Read/Write
Capture Resizer Vertical Scaling Rate bits 5-0							
15	14	13	12	11	10	9	8
Capture Resizer Horizontal Scaling Rate bits 5-0							
7	6	5	4	3	2	1	0

bits 13-8 Capture Resizer Vertical Scaling Rate bits [5:0]
These bits determine the capture resizer vertical scaling rate when REG[0960h] bit 2 = 1. Not all scaling rates are available for all scaling modes (see REG[096Eh]).

Table 10-69: Capture Resizer Vertical Scaling Rate Selection

REG[096Ch] bits 15-8	Capture Resizer Vertical Scaling Rate			
	REG[096Eh] bits 1-0 = 00b	**REG[096Eh] bits 1-0 = 01b**	**REG[096Eh] bits 1-0 = 10b**	**REG[096Eh] bits 1-0 = 11b**
0000 0000b	Reserved	Reserved	Reserved	Reserved
0000 0001b	n/a	1/128	1/128	Reserved
0000 0010b	n/a	2/128	2/128	Reserved
0000 0011b	n/a	3/128	3/128	Reserved
0000 0100b	n/a	4/128	4/128	Reserved
0000 0101b	n/a	5/128	5/128	Reserved
0000 0110b	n/a	6/128	6/128	Reserved
0000 0111b	n/a	7/128	7/128	Reserved
0000 1000b	n/a	8/128	8/128	Reserved
0000 1001b	n/a	9/128	9/128	Reserved
0000 1010b	n/a	10/128	10/128	Reserved
0000 1011b	n/a	11/128	11/128	Reserved
0000 1100b	n/a	12/128	12/128	Reserved
0000 1101b	n/a	13/128	13/128	Reserved
0000 1110b	n/a	14/128	14/128	Reserved
0000 1111b	n/a	15/128	15/128	Reserved
0001 0000b	n/a	16/128	16/128	Reserved
0001 0001b	n/a	17/128	17/128	Reserved
0001 0010b	n/a	18/128	18/128	Reserved
0001 0011b	n/a	19/128	19/128	Reserved
0001 0100b	n/a	20/128	20/128	Reserved
0001 0101b	n/a	21/128	21/128	Reserved
0001 0110b	n/a	22/128	22/128	Reserved
0001 0111b	n/a	23/128	23/128	Reserved
0001 1000b	n/a	24/128	24/128	Reserved
0001 1001b	n/a	25/128	25/128	Reserved
0001 1010b	n/a	26/128	26/128	Reserved
0001 1011b	n/a	27/128	27/128	Reserved
0001 1100b	n/a	28/128	28/128	Reserved
0001 1101b	n/a	29/128	29/128	Reserved
0001 1110b	n/a	30/128	30/128	Reserved
0001 1111b	n/a	31/128	31/128	Reserved
0010 0000b	n/a	32/128	32/128	Reserved
0010 0001b ～ 0011 1111b	n/a	33/128 ～ 63/128	33/128 ～ 63/128	Reserved
0100 0000b	n/a	64/128	64/128	Reserved
0100 0001b ～ 0111 1111b	n/a	65/128 ～ 127/128	65/128 ～ 127/128	Reserved
1000 0000b	n/a	128/128	128/128	Reserved

bits 5-0 Capture Resizer Horizontal Scaling Rate bits [5:0]
These bits determine the capture resizer horizontal scaling rate when REG[0960h] bit 2 = 1. When REG[0960h] bit 2 = 0, these bits specify both the horizontal and the vertical scaling rate. Not all scaling rates are available for all scaling modes (see REG[096Eh]).

Table 10-70: Capture Resizer Horizontal Scaling Rate Selection

REG[096Ch] bits 15-8	**Capture Resizer Vertical Scaling Rate**			
	REG[096Eh] bits 1-0 = 00b	**REG[096Eh] bits 1-0 = 01b**	**REG[096Eh] bits 1-0 = 10b**	**REG[096Eh] bits 1-0 = 11b**
0000 0000b	Reserved	Reserved	Reserved	Reserved
0000 0001b	n/a	1/128	1/128	Reserved
0000 0010b	n/a	2/128	2/128	Reserved
0000 0011b	n/a	3/128	Reserved	Reserved
0000 0100b	n/a	4/128	4/128	Reserved
0000 0101b	n/a	5/128	Reserved	Reserved
0000 0110b	n/a	6/128	Reserved	Reserved
0000 0111b	n/a	7/128	Reserved	Reserved
0000 1000b	n/a	8/128	8/128	Reserved
0000 1001b	n/a	9/128	Reserved	Reserved
0000 1010b	n/a	10/128	Reserved	Reserved
0000 1011b	n/a	11/128	Reserved	Reserved
0000 1100b	n/a	12/128	Reserved	Reserved
0000 1101b	n/a	13/128	Reserved	Reserved
0000 1110b	n/a	14/128	Reserved	Reserved
0000 1111b	n/a	15/128	Reserved	Reserved
0001 0000b	n/a	16/128	16/128	Reserved
0001 0001b	n/a	17/128	Reserved	Reserved
0001 0010b	n/a	18/128	Reserved	Reserved
0001 0011b	n/a	19/128	Reserved	Reserved
0001 0100b	n/a	20/128	Reserved	Reserved
0001 0101b	n/a	21/128	Reserved	Reserved
0001 0110b	n/a	22/128	Reserved	Reserved
0001 0111b	n/a	23/128	Reserved	Reserved
0001 1000b	n/a	24/128	Reserved	Reserved
0001 1001b	n/a	25/128	Reserved	Reserved
0001 1010b	n/a	26/128	Reserved	Reserved
0001 1011b	n/a	27/128	Reserved	Reserved
0001 1100b	n/a	28/128	Reserved	Reserved
0001 1101b	n/a	29/128	Reserved	Reserved
0001 1110b	n/a	30/128	Reserved	Reserved
0001 1111b	n/a	31/128	Reserved	Reserved
0010 0000b	n/a	32/128	32/128	Reserved
0010 0001b ～0011 1111b	n/a	33/128 ～ 63/128	Reserved	Reserved
0100 0000b	n/a	64/128	64/128	Reserved
0100 0001b ～0111 1111b	n/a	65/128 ～ 127/128	Reserved	Reserved
1000 0000b	n/a	128/128	128/128	Reserved

REG[096Eh] Capture Resizer Operation Setting Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a				Reserved		Capture Resizer Scaling Mode bits 1-0	
7	6	5	4	3	2	1	0

bits 3-2 Reserved
The default value for these bits is 0.

bits 1-0 Capture Resizer Scaling Mode bits [1:0]
These bits determine the capture resizer scaling mode. Not all scaling rates are available for all scaling modes. Before selecting a scaling mode, set the Capture Resizer Vertical Scaling Rate bits (REG[096Eh] bits 13-8) and/or the Capture Resizer Horizontal Scaling Rate bits (REG[096Ch] bits 5-0) to a valid scaling rate. Enabling a scaling mode with an unsupported scaling rate (reserved or n/a) may turn off the capture resizer.

Table 10-71: Capture Resizer Scaling Mode Selection

REG[096Eh] bits 1-0	Capture Resizer Scaling Mode
00b	no resizer scaling
01b	V/H Reduction
10b	V: Reduction, H: Average
11b	Reserved

10.4.15 JPEG Module Registers

REG[0980h] JPEG Control Register Default = 0000h							Read/Write
Reserved							JPEG 180° Rotation Enable
15	14	13	12	11	10	9	8
JPEG Module SW Reset (WO)	Reserved		YUV Output Data Range Select	JPEG Data Control bits 2-0			JPEG Module Enable
7	6	5	4	3	2	1	0

bits 15-12 — Reserved
The default value for these bits is 0.

bit 8 — JPEG 180° Rotation Enable
This bit is only for camera data encode. This bit selects the rotation mode for JPEG encoded data.
When this bit = 0, the JPEG encoded data is normal.
When this bit = 1, the JPEG encoded data is rotated 180°.

Note
The dimensions of the image must be in MCU size multiples.

bit 7 — JPEG Module Software Reset (Write Only)
This bit initiates a software reset of the internal JPEG module circuit. The JPEG module should be reset using this bit before each JPEG encode operation.

This bit resets only the internal JPEG module circuit and has no effect on the JPEG codec registers (REG[1000h]-[17A2h], the JPEG codec or the JPEG module registers (REG[0980h]-[09E0h]), except as follows.
REG[0984] is reset except for bits 14, 5, and 1.
REG[09B4] is reset
REG[09B6] is reset
REG[09AC] is reset
REG[09AA] is reset
REG[09A8] is reset
REG[09A2] is reset

To reset the JPEG codec, set the JPEG Codec Software Reset bit (REG[1002h] bit 7) to 1.
When a 1 is written to this bit, the JPEG module is reset.
When a 0 is written to this bit, there is no hardware effect.

bit 6 — Reserved
The default value for this bit is 0.

bit 5 — Reserved
The default value for this bit is 0.

bit 4 — YUV Data No Offset Select
This bit specifies whether an offset is applied to the U and V data when in YUV Capture, YUV Display, Host Encode, and Host Decode modes, REG[0980] bits [3:1] = 001b, 011b, 100b, 101b, or 111b. This bit is used in conjunction with REG[0110] bit 8 to select the desired YUV output capture range for YUV Capture mode.

When this bit = 0, an offset is applied to the U and V data (MSB is inverted).
When this bit = 1, no offset is applied to the U and V data is not modified.

Table 10-72: YUV Output Range Selection (REG[0980h] = 011b or 111b)

Camera Interface Input YUV Data	REG[0110h] bit 8	REG[0980h] bit 4	YUV Output Data Range
Straight Binary	0	0	0 =< Y =< 255 -128 =< U =< 127 -128 =< V =< 127 or 16 =< Y =< 235 -112 =< Cb=< 112 -112 =< Cr=< 112
		1	0 =< Y =< 255 0 =< U =< 255 0 =< V =< 255 or 16 =< Y =< 235 16 =< Cb=< 240 16 =< Cr =< 240
	1	0	0 =< Y =< 255 0 =< U =< 255 0 =< V =< 255 or 16 =< Y =< 235 16 =< Cb =< 240 16 =< Cr =< 240
		1	0 =< Y =< 255 -128 =< U =< 127 -128 =< V =< 127 or 16 =< Y =< 235 -112 =< Cb =< 112 -112 =< Cr =< 112

Table 10-72: YUV Output Range Selection (REG[0980h] = 011b or 111b) (Continued)

Camera Interface Input YUV Data	REG[0110h] bit 8	REG[0980h] bit 4	YUV Output Data Range
Offset Binary	0	0	0 =< Y =< 255 0 =< U =< 255 0 =< V =< 255 or 16 =< Y =< 235 16 =< Cb =< 240 16 =< Cr =< 240
		1	0 =< Y =< 255 -128 =< U =< 127 -128 =< V =< 127 or 16 =< Y =< 235 -112 =< Cb =< 112 -112 =< Cr =< 112
	1	0	0 =< Y =< 255 -128 =< U =< 127 -128 =< V =< 127 or 16 =< Y =< 235 -112 =< Cb=< 112 -112 =< Cr=< 112
		1	0 =< Y =< 255 0 =< U =< 255 0 =< V =< 255 or 16 =< Y =< 235 16 =< Cb=< 240 16 =< Cr =< 240

Table 10-73: YUV Input Range Selection (REG[0980h] = 001b or 101b)

Host Interface Input YUV Data	REG[0980h] bit 4	YUV Input Data Range
Straight Binary	0	0 ≤ Y ≤ 255 -128 ≤ U ≤ 127 -128 ≤ V ≤ 127 or 16 ≤ Y ≤ 235 -112 ≤ Cb ≤ 112 -112 ≤ Cr ≤ 112
	1	0 ≤ Y ≤ 255 0 ≤ U ≤ 255 0 ≤ V ≤ 255 or 16 ≤ Y ≤ 235 16 ≤ Cb ≤ 240 16 ≤ Cr ≤ 240
Offset Binary	0	0 ≤ Y ≤ 255 0 ≤ U ≤ 255 0 ≤ V ≤ 255 or 16 ≤ Y ≤ 235 16 ≤ Cb ≤ 240 16 ≤ Cr ≤ 240
	1	0 ≤ Y ≤ 255 -128 ≤ U ≤ 127 -128 ≤ V ≤ 127 or 16 ≤ Y ≤ 235 -112 ≤ Cb ≤ 112 -112 ≤ Cr ≤ 112

bits 3-1 JPEG Data Control bits [2:0]

Table 10-74: JPEG Data Mode Selection

REG[0980h] bits 3-1	JPEG Data Mode	Description
000b	JPEG Encode/Decode	In this mode the encode data paths are: • **Camera Interface** => Capture Resizer => JPEG Line Buffer => Codec Core => JPEG FIFO => Host Interface • **Display Buffer** => RGB/YUV Converter => Capture Resizer => JPEG Line Buffer => Codec Core => JPEG FIFO => Host Interface • **Host Interface** => RGB/YUV Converter => Capture Resizer => JPEG Line Buffer => Codec Core => JPEG FIFO => Host Interface In this mode the decode data path is: • **Host Interface** => JPEG FIFO => Codec Core => JPEG Line Buffer => View Resizer => RGB/YUV Converter => Display Buffer
001b	YUV Data Input from Host (YUV 4:2:2)	The data by-passes the JPEG Module.
010b	Reserved	
011b	YUV Data Output to Host (YUV 4:2:2)	The data by-passes the JPEG Module.
100b	Host Input/Output JPEG Encode/Decode (YUV 4:2:0 or YUV 4:2:2)	In this mode the encode data path is: • **Host Interface** => JPEG Line Buffer => Codec Core => JPEG FIFO => Host Interface In this mode the decode data path is: • **Host Interface** => JPEG FIFO => Codec Core => JPEG Line Buffer => Host Interface
101b	YUV Data Input from Host (YUV 4:2:0)	The data by-passes the JPEG Module.
110b	Reserved	
111b	YUV Data Output to Host (YUV 4:2:0)	The data by-passes the JPEG Module.

bit 0 JPEG Module Enable
This bit enables/disables the JPEG module and its associated registers. **If the JPEG module is disabled, REG[1000h] - REG[17A2h] must not be accessed.**
When this bit = 1, the JPEG module is enabled and a clock source is supplied.
When this bit = 0, the JPEG module is disabled and the clock source is disabled.

Note

The JPEG module must be disabled before the View Resizer Enable bit (REG[0940h] bit 0) or the Capture Resizer Enable bit (REG[0960h] bit 0) are disabled.

REG[0982h] JPEG Status Flag Register
Default = 8080h — Read/Write

Reserved	JPEG Codec File Out Status (RO)	JPEG FIFO Threshold Status bits 1-0 (RO)		Encode Size Limit Violation Flag	JPEG FIFO Threshold Trigger Flag	JPEG FIFO Full Flag	JPEG FIFO Empty Flag
15	14	13	12	11	10	9	8
Reserved		JPEG Decode Complete Flag	Decode Marker Read Flag	Reserved	JPEG Line Buffer Overflow Flag (RO)	JPEG Codec Interrupt Flag (RO)	JPEG Line Buffer Interrupt Flag (RO)
7	6	5	4	3	2	1	0

bit 15 — Reserved
The default value for this bit is 1.

bit 14 — JPEG Codec File Out Status (Read Only)
This bit indicates the status of the JPEG Codec output.
When this bit = 0, the JPEG Codec is not outputing encoded data.
When this bit = 1, the JPEG Codec is encoding or outputing encoded data.

bits 13-12 — JPEG FIFO Threshold Status bits [1:0] (Read Only)
These bits indicate how much data is currently in the JPEG FIFO. See the JPEG FIFO Size register (REG[09A4h]) for information on setting the JPEG FIFO size.

Table 10-75: JPEG FIFO Threshold Status

REG[0982h] bits 13-12	JPEG FIFO Threshold Status
00b	no data (same as empty
01b	more than 4 bytes of data exist
10b	more than 1/4 of specified FIFO size data exists
11b	more than 1/2 of specified FIFO size data exists

bit 11 — Encode Size Limit Violation Flag
This flag is asserted when the JPEG compressed data size is over the encode size limit as specified in the Encode Size Limit registers (REG[09B0h], REG[09B2h]). This flag is masked by the JPEG Encode Size Limit Violation Interrupt Enable bit and is only available when REG[0986h] bit 11 = 1.

For Reads:
When this bit = 0, no violation has occurred.
When this bit = 1, an encode size limit violation has occurred.

For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the Encode Size Limit Violation Flag is cleared.

Note
For further information on the use of this bit, see Section 14.1.2, “JPEG Codec Interrupts”.

bit 10 JPEG FIFO Threshold Trigger Flag
This flag is asserted when the amount of data in the JPEG FIFO meets the condition specified by the JPEG FIFO Trigger Threshold bits (REG[09A0h] bits 5-4). This flag is masked by the JPEG FIFO Threshold Trigger Interrupt Enable bit and is only available when REG[0986h] bit 10 = 1.

For Reads:
When this bit = 0, the amount of data in the JPEG FIFO is less than the JPEG FIFO Trigger Threshold.
When this bit = 1, the amount of data in the JPEG FIFO has reached the JPEG FIFO Trigger Threshold.

For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the FIFO Threshold Trigger Flag is cleared.

Note
For further information on the use of this bit, see Section 14.1.2, “JPEG Codec Interrupts”.

bit 9 JPEG FIFO Full Flag
This flag is asserted when the JPEG FIFO is full. This flag is masked by the JPEG FIFO Full Interrupt Enable bit and is only available when REG[0986h] bit 9 = 1.

For Reads:
When this bit = 0, the JPEG FIFO is not full.
When this bit = 1, the JPEG FIFO is full.

For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the JPEG FIFO Full Flag is cleared.

Note
For further information on the use of this bit, see Section 14.1.2, “JPEG Codec Interrupts”.

bit 8 JPEG FIFO Empty Flag
This flag is asserted when the JPEG FIFO is empty. This flag is masked by the JPEG FIFO Empty Interrupt Enable bit and is only available when REG[0986h] bit 8 = 1.

For Reads:
When this bit = 0, the JPEG FIFO is not empty.
When this bit = 1, the JPEG FIFO is empty.

For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the JPEG FIFO Empty Flag is cleared.

Note
For further information on the use of this bit, see Section 14.1.2, “JPEG Codec Interrupts”.

bit 7 Reserved
The default value for this bit is 1.

bit 6 Reserved
The default value for this bit is 0.

bit 5 JPEG Decode Complete Flag
This flag is asserted when the JPEG decode operation is finished. This flag is masked by the JPEG Decode Complete Interrupt Enable bit and is only available when REG[0986h] bit 5 = 1.

For Reads:
When this bit = 0, the JPEG decode operation is not finished yet.
When this bit = 1, the JPEG decode operation is finished.

For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, this bit is cleared.

Note
When error detection is enabled (REG[101Ch] bits 1-0 = 01b) and an error is detected while decoding a JPEG image, this status bit is not set at the end of the decode process.

Note
For further information on the use of this bit, see Section 14.1.2, “JPEG Codec Interrupts”.

bit 4 Decode Marker Read Flag
This flag is asserted during the JPEG decoding process when decoded marker information is read from the JPEG file. This flag is masked by the JPEG Decode Marker Read Interrupt Enable bit and is only available when REG[0986h] bit 4 = 1.
When this bit = 0, a JPEG decode marker has not been read.
When this bit = 1, a JPEG decode marker has been read.

To clear this flag, disable the Decode Marker Read Interrupt Enable bit (REG[0986h] bit 4 = 0).

Note
For further information on the use of this bit, see Section 14.1.2, “JPEG Codec Interrupts”.

bit 3 Reserved
The default value for this bit is 0.

bit 2 JPEG Line Buffer Overflow Flag (Read Only)
This flag is asserted when a JPEG Line Buffer overflow occurs. This flag is masked by the JPEG Line Buffer Overflow Interrupt Enable bit and is only available when REG[0986h] bit 2 = 1.
When this bit = 0, a JPEG Line Buffer overflow has not occurred.
When this bit = 1, a JPEG Line Buffer overflow has occurred.

To clear this flag, perform a JPEG Software Reset (REG[0980h] bit 7 = 1).

Note
For further information on the use of this bit, see Section 14.1.2, “JPEG Codec Interrupts”.

bit 1 JPEG Codec Interrupt Flag (Read Only)
This flag is asserted when the JPEG codec generates an interrupt. This flag is masked by the JPEG Codec Interrupt Enable bit and is only available when REG[0986h] bit 1 = 1).
When this bit = 0, the JPEG codec has not generated an interrupt.
When this bit = 1, the JPEG codec has generated an interrupt.

To clear this flag, read the JPEG Operation Status bit (REG[1004h] bit 0).

Note
For further information on the use of this bit, see Section 14.1.2, “JPEG Codec Interrupts”.

bit 0 JPEG Line Buffer Interrupt Flag (Read Only)
This bit is valid only when YUV Capture/Display mode is selected (REG[0980h] bits 3-1 ≠ 000b). This bit is set when a JPEG Line Buffer Interrupt occurs in REG[09C0h] and is used for YUV data transfers with interrupt handling. This flag is masked by the JPEG Line Buffer Interrupt Enable bit and is only available when REG[0986h] bit 0 = 1). This bit is cleared when all JPEG Line Buffer Interrupt requests are cleared in REG[09C0h].

When this bit = 0, the JPEG Line Buffer has not generated an interrupt.
When this bit = 1, the JPEG Line Buffer has generated an interrupt.

REG[0984h] JPEG Raw Status Flag Register
Default = 8180h — Read Only

15	14	13	12	11	10	9	8
Reserved	JPEG Codec File Out Status	JPEG FIFO Threshold Status bits 1-0		Raw Encode Size Limit Violation Flag	Raw JPEG FIFO Threshold Trigger Flag	Raw JPEG FIFO Full Flag	Raw JPEG FIFO Empty Flag

7	6	5	4	3	2	1	0
Reserved		Raw JPEG Decode Complete Flag	Raw Decode Marker Read Flag	Reserved	Raw JPEG Line Buffer Overflow Flag	Raw JPEG Codec Interrupt Flag	Raw JPEG Line Buffer Interrupt Flag

bit 15 Reserved
The default value for this bit is 1.

bit 14 JPEG Codec File Out Status (Read Only)
This bit provides the status of the JPEG Codec output.
When this bit = 0, the JPEG Codec is not outputing encoded data.
When this bit = 1, the JPEG Codec is encoding or outputing encoded data.

bits 13-12 JPEG FIFO Threshold Status bits [1:0] (Read Only)
These bits indicate how much data is currently in the JPEG FIFO. See the JPEG FIFO Size Register (REG[09A4h) for information on setting the JPEG FIFO Size.

Table 10-76: JPEG FIFO Threshold Status

REG[0984h] bits 13-12	JPEG FIFO Threshold Status
00b	no data (same as empty
01b	more than 4 bytes of data exist
10b	more than 1/4 of specified FIFO size data exists
11b	more than 1/2 of specified FIFO size data exists

bit 11 Raw Encode Size Limit Violation Flag (Read Only)
This flag is asserted when the JPEG encoded data size is over the size limit as specified in the Encode Size Limit registers (REG[09B02h] - REG[09B2h]). This flag is not affected by the JPEG Encode Size Limit Violation Interrupt Enable bit (REG[0986h] bit 11).
When this bit = 0, no violation has occurred.
When this bit = 1, an encode size limit violation has occurred.

To clear this flag, write a 1 to the Encode Size Limit Violation Flag, REG[0982h] bit 11, when an Encode Size Limit Violation condition no longer exists. (i.e. Set the Encode Size Limit, REG[09B0h] and REG[09B2h] > Encode Size Result, REG[09B4h] and REG[09B6h], or reset the JPEG Module, REG[0980h] bit 7 = 1.)

bit 10 Raw JPEG FIFO Threshold Trigger Flag (Read Only)
This flag is asserted when the amount of data in the JPEG FIFO meets the condition specified by the JPEG FIFO Trigger Threshold bits (REG[09A0] bits 5-4). This flag is not affected by the JPEG FIFO Threshold Trigger Interrupt Enable bit (REG[0986h] bit 10).
When this bit = 0, the amount of data in the JPEG FIFO is less than the JPEG FIFO Trigger Threshold.
When this bit = 1, the amount of data in the JPEG FIFO has reached the JPEG FIFO Trigger Threshold.

To clear this flag, write a 1 to the JPEG FIFO Threshold Trigger Flag, REG[0982] bit 10, when a JPEG FIFO Threshold Trigger condition no longer exists. (i.e. Set the JPEG FIFO Threshold in REG[09A0] bits [5:4] greater, empty the JPEG FIFO until it's level is below the specified threshold, or reset the JPEG Module, REG[0980] bit 7 = 1.)

bit 9 Raw JPEG FIFO Full Flag (Read Only)
This flag is asserted when the JPEG FIFO is full. This flag is not affected by the JPEG FIFO Full Interrupt Enable bit (REG[0986h] bit 9).
When this bit = 0, the JPEG FIFO is not full.
When this bit = 1, the JPEG FIFO is full.

To clear this flag, write a 1 to the JPEG FIFO Full Flag, REG[0982h] bit 9, when the JPEG FIFO is no longer full or after a JPEG Module reset, REG[0980h] bit 7 = 1.

bit 8 Raw JPEG FIFO Empty Flag (Read Only)
This flag is asserted when the JPEG FIFO is empty. This flag is not affected by the JPEG FIFO Empty Interrupt Enable bit (REG[0986h] bit 8).
When this bit = 0, the JPEG FIFO is not empty.
When this bit = 1, the JPEG FIFO is empty.

To clear this flag, write a 1 to the JPEG FIFO Empty Flag, REG[0982h] bit 8, when the JPEG FIFO is no longer empty or after a JPEG Module reset, REG[0980h] bit 7 = 1.

Note
This bit is not affected by the JPEG FIFO Clear bit (REG[09A0h] bit 2).

bit 7 Reserved
The default value for this bit is 1.

bit 6 Reserved
The default value for this bit is 0.

bit 5	Raw JPEG Decode Complete Flag (Read Only) This flag is asserted when the JPEG decode operation is finished. This flag is not affected by the JPEG Decode Complete Interrupt Enable bit (REG[0986h] bit 5). When this bit = 0, the JPEG decode operation is not finished yet. When this bit = 1, the JPEG decode operation is finished. To clear this flag, write a 1 to the JPEG Decode Complete Flag (REG[0982h] bit 5 = 1). **Note** When error detection is enabled (REG[101Ch] bits 1-0 = 01b) and an error is detected while decoding a JPEG image, this status bit is not set at the end of the decode process.
bit 4	Raw JPEG Decode Marker Read Flag (Read Only) This flag is asserted during the JPEG decoding process when decoded marker information is read from the JPEG file and when REG[0986h] bit 4 = 1. When this bit = 0, a JPEG decode marker has not been read. When this bit = 1, a JPEG decode marker has been read. To clear this flag, disable the JPEG Decode Marker Read Interrupt Enable bit (REG[0986h] bit 4 = 0).
bit 3	Reserved The default value for this bit is 0.
bit 2	Raw JPEG Line Buffer Overflow Flag (Read Only) This flag is asserted when a JPEG Line Buffer overflow occurs. This flag is not affected by the JPEG Line Buffer Overflow Interrupt Enable (REG[0986h] bit 2). When this bit = 0, a JPEG Line Buffer overflow has not occurred. When this bit = 1, a JPEG Line Buffer overflow has occurred. To clear this flag, perform a JPEG module software reset (REG[0980h] bit 7 = 1).
bit 1	Raw JPEG Codec Interrupt Flag (Read Only) This flag is asserted when an interrupt is generated by the JPEG codec. This flag is not affected by the JPEG Codec Interrupt Enable bit (REG[0986h] bit 1). When this bit = 0, no interrupt has been generated. When this bit = 1, the JPEG codec has generated an interrupt. To clear this flag, read the JPEG Operation Status bit (REG[1004h] bit 0).
bit 0	Raw JPEG Line Buffer Interrupt Flag This bit is valid only when YUV Capture/Display mode is selected (REG[0980h] bits 3-1 ≠ 000b). This flag is not affected by the JPEG Line Buffer Interrupt Enable bit (REG[0986h] bit 0). This bit is set when a JPEG Line Buffer Interrupt occurs in REG[09C0h] and is cleared when all JPEG Line Buffer Interrupt requests are cleared in REG[09C0h]. When this bit = 0, the JPEG Line Buffer has not generated an interrupt. When this bit = 1, the JPEG Line Buffer has generated an interrupt.

REG[0986h] JPEG Interrupt Control Register Default = 0000h							Read/Write
Reserved				Encode Size Limit Violation Interrupt Enable	JPEG FIFO Threshold Trigger Interrupt Enable	JPEG FIFO Full Interrupt Enable	JPEG FIFO Empty Interrupt Enable
15	14	13	12	11	10	9	8
Reserved		JPEG Decode Complete Interrupt Enable	Decode Marker Read Interrupt Enable	Reserved	JPEG Line Buffer Overflow Interrupt Enable	JPEG Codec Interrupt Enable	JPEG Line Buffer Interrupt Enable
7	6	5	4	3	2	1	0

bits 15-12 Reserved
The default value for these bits is 0.

bit 11 Encode Size Limit Violation Interrupt Enable
This bit controls the encode size limit violation interrupt. The status of this interrupt can be determined using the Encode Size Limit Violation Flag bit (REG[0982h] bit 11).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 10 JPEG FIFO Threshold Trigger Interrupt Enable
This bit controls the JPEG FIFO threshold trigger interrupt. The status of this interrupt can be determined using the JPEG FIFO Threshold Trigger Flag bit (REG[0982h] bit 10).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 9 JPEG FIFO Full Interrupt Enable
This bit controls the JPEG FIFO full interrupt. The status of this interrupt can be determined using the JPEG FIFO Full Flag bit (REG[0982h] bit 9).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 8 JPEG FIFO Empty Interrupt Enable
This bit controls the JPEG FIFO empty interrupt. The status of this interrupt can be determined using the JPEG FIFO Empty Flag bit (REG[0982h] bit 8).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 7 Reserved
The default value for this bit is 0.

bit 6 Reserved
The default value for this bit is 0.

bit 5 JPEG Decode Complete Interrupt Enable
This bit controls the JPEG decode complete interrupt. The status of this interrupt can be determined using the JPEG Decode Complete Flag bit (REG[0982h] bit 5).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 4 JPEG Decode Marker Read Interrupt Enable
This bit controls the JPEG decode marker read interrupt. The status of this interrupt can be determined using the JPEG Decode Complete Flag (REG[0982h] bit 4).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 3 Reserved
The default value for this bit is 0.

bit 2 JPEG Line Buffer Overflow Interrupt Enable
This bit controls the JPEG line buffer overflow interrupt. The status of this interrupt can be determined using the Line Buffer Overflow Flag (REG[0982h] bit 2).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 1 JPEG Codec Interrupt Enable
This bit controls the JPEG codec interrupt. The status of this interrupt can be determined using the JPEG Codec Interrupt Flag (REG[0982h] bit 1).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 0 JPEG Line Buffer Interrupt Enable
This bit controls the JPEG Line Buffer Interrupt. The status of this interrupt can be determined using the JPEG Line Buffer Interrupt Flag (REG[0982h] bit 0).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

This bit should be disabled if YUV Data in not being input from host and then displayed (REG[0980h] bits 3-1 = 001b or 101b).

REG[0988h] is Reserved

This register is Reserved and should not be written.

REG[098Ah] JPEG Code Start/Stop Control Register Default = 0000h							Write Only
n/a							
15	14	13	12	11	10	9	8
n/a							JPEG Start/Stop Control
7	6	5	4	3	2	1	0

bit 0 JPEG Start/Stop Control (Write Only)
This bit controls the JPEG codec for both JPEG encode mode and YUV data capture (JPEG bypass) mode. This bit is not used for JPEG decoding.

For JPEG Encode:
When this bit is set to 0, the JPEG codec will be ready to capture from the next frame.
When this bit is set to 1, the JPEG codec starts capturing the next frame and then stops.

For YUV Data Capture (JPEG Bypass):
When this bit is set to 0, YUV data capturing stops at the end of the current frame.
When this bit is set to 1, YUV data capturing starts from the next frame.

Note
The encode of continuous Frame is one time in 2 Frame.

REG[098Ch] through REG[098Eh] are Reserved

These registers are Reserved and should not be written.

10.4.16 JPEG FIFO Setting Register

REG[09A0h] JPEG FIFO Control Register Default = 0000h							Read/Write
Reserved							
15	14	13	12	11	10	9	8
Reserved		JPEG FIFO Trigger Threshold bits 1-0		Reserved	JPEG FIFO Clear (WO)	JPEG FIFO Direction (RO)	n/a
7	6	5	4	3	2	1	0

bits 15-6 Reserved
The default value for these bits is 0.

bits 5-4 JPEG FIFO Trigger Threshold bits [1:0]
These bits set the JPEG FIFO Threshold Trigger Flag (REG[0982h] bit 10) when the specified conditions are met.

Table 10-77: JPEG FIFO Trigger Threshold Selection

REG[09A0h] bits 5-4	JPEG FIFO Trigger Threshold
00b	Never trigger
01b	Trigger when the JPEG FIFO contains 4 bytes of data or more
10b	Trigger when the JPEG FIFO contains more than 1/4 of the specified JPEG FIFO size (REG[09A4h] bits 3-0)
11b	Trigger when the JPEG FIFO contains more than 1/2 of the specified JPEG FIFO size (REG[09A4h] bits 3-0)

bit 3 Reserved
The default value for this bit is 0.

bit 2 JPEG FIFO Clear (Write Only)
This bit clears the JPEG FIFO. It is recommended that the JPEG module should also be reset (REG[0980h] bit 7 = 1) when the JPEG FIFO is cleared.
When this bit = 0, there is no hardware effect.
When this bit = 1, the JPEG FIFO, the JPEG FIFO Read/Write Pointer registers (REG[09AAh]-[09ACh]), and the JPEG FIFO Valid Data Size registers (REG[09A8h] are cleared.

The following sequence is used clear the JPEG FIFO.

1. Clear the JPEG FIFO, REG[09A0h] bit 2 = 1.
2. Perform 2 dummy reads from REG[09A6h] to ensure that the JPEG FIFO is empty.
3. Reset the JPEG module, REG[0980h] bit 7 = 1.

Note
Clearing the JPEG FIFO using this bit has no effect on the Raw JPEG FIFO Empty Flag (REG[0984h] bit 8).

Note
This bit only clears the JPEG FIFO and does not clear the JPEG Line Buffer. For details on using the JPEG FIFO, see Section 14.1.1, “JPEG FIFO”.

bit 1 JPEG FIFO Direction Bit (Read Only)
This bit indicates the configuration of the JPEG FIFO.
When this bit = 0, the JPEG FIFO is configured to receive (encode process).
When this bit = 1, the JPEG FIFO is configured to transmit (decode process).

REG[09A2h] JPEG FIFO Status Register Default = 8001h							Read Only
Reserved							
15	14	13	12	11	10	9	8
Reserved				JPEG FIFO Threshold Status bits 1-0		JPEG FIFO Full Status	JPEG FIFO Empty Status
7	6	5	4	3	2	1	0

bits 15-4 Reserved
The default value for these bits is 0.

bits 3-2 JPEG FIFO Threshold Status bits [1:0] (Read Only)
These bits indicate the amount of data in the JPEG FIFO.

Table 10-78: JPEG FIFO Threshold Status

REG[09A2h] bits 3-2	JPEG FIFO Threshold Status
00b	No data (Same as Empty)
01b	4 bytes of data or more exists
10b	More than 1/4 of the specified JPEG FIFO size data exists (see REG[09A4h] bits 3-0)
11b	More than 1/2 of the specified JPEG FIFO size data exists (see REG[09A4h] bits 3-0)

bit 1 JPEG FIFO Full Status (Read Only)
This bit indicates whether the JPEG FIFO is full.
When this bit = 0, the JPEG FIFO is not full.
When this bit = 1, the JPEG FIFO is full.

bit 0 JPEG FIFO Empty Status (Read Only)
This bit indicates that the JPEG FIFO is empty.
When this bit = 0, the JPEG FIFO is not empty.
When this bit = 1, the JPEG FIFO is empty.

REG[09A4h] JPEG FIFO Size Register Default = 0000h							Read/Write
Reserved							
15	14	13	12	11	10	9	8
Reserved	JPEG FIFO Size bits 6-0						
7	6	5	4	3	2	1	0

bits 15-5 Reserved
The default value for these bits is 0.

bits 4-0 JPEG FIFO Size bits [6:0]
These bits determine the JPEG FIFO size in 4K byte units. The maximum size of the JPEG FIFO is 512K bytes. These bits also specify the amount of memory reserved for the JPEG FIFO.

JPEG FIFO size = (REG[09A4h] bits 4-0 + 1) x 4K bytes

Note
For further information on S1D13719 memory mapping, see Section 8, “Memory Map”.

REG[09A6h] JPEG FIFO Read/Write Port Register							
Default = Not Applicable							Read/Write
JPEG FIFO Read/Write Port bits 15-8							
15	14	13	12	11	10	9	8
JPEG FIFO Read/Write Port bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 JPEG FIFO Read/Write Port bits [15:0]
These bits are the access port for the JPEG FIFO. The current address pointed to by the port can be determined using the JPEG FIFO Read Pointer register (REG[09AAh) and the JPEG FIFO Write Pointer register (REG[09ACh]).

When JPEG encoding is selected, these bits are used as the JPEG FIFO read data port. When JPEG decoding is selected, these bits are used as the JPEG FIFO write data port. When YUV data is output to the Host interface (REG[0980] bits 3-1 = 011b or 111b), these bits are used as the JPEG FIFO read data port.

Note
Since the JPEG FIFO is 32 bits wide and the Host CPU interface is 16 bits wide, this register must be accessed an even number of times.

REG[09A8h] JPEG FIFO Valid Data Size Register							
Default = 0000h							Read Only
JPEG FIFO Valid Data Size bits 15-8							
15	14	13	12	11	10	9	8
JPEG FIFO Valid Data Size bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 JPEG FIFO Valid Data Size bits [15:0] (Read Only)
These bits indicate the valid data size in 32-bit units which can be read from the JPEG FIFO. If the JPEG file size is not aligned on 32-bit boundaries, the JPEG FIFO may contain more data (1 to 3 bytes) than the indicated size. See the Encode Size Result registers (REG[09B4h]-[09B6h]) to determine the correct data size.

Note
If the JPEG FIFO is set to larger than 256K Bytes, this register does not report the correct amount of data in the JPEG FIFO.

REG[09AAh] JPEG FIFO Read Pointer Register Default = 0000h							Read Only
JPEG FIFO Read Pointer bits 15-8							
15	14	13	12	11	10	9	8
JPEG FIFO Read Pointer bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 JPEG FIFO Read Pointer bits [15:0] (Read Only)
These bits are used during evaluation and are for reference only. These bits indicate the 32-bit read pointer into the JPEG FIFO. The read pointer is automatically incremented when either a read or write to/from the JPEG FIFO Read/Write Port register (REG[09A6h]) takes place. For details on the JPEG FIFO, see Section 14.1.1, “JPEG FIFO”.

REG[09ACh] JPEG FIFO Write Pointer Register Default = 0000h							Read Only
JPEG FIFO Write Pointer bits 15-8							
15	14	13	12	11	10	9	8
JPEG FIFO Write Pointer bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 JPEG FIFO Write Pointer bits [15:0] (Read Only)
These bits are used during evaluation and are for reference only. These bits indicate the 32-bit write pointer into the JPEG FIFO. The write pointer is automatically incremented when a write to the JPEG FIFO Read/Write Port register (REG[09A6h]) takes place. For details on the JPEG FIFO, see Section 14.1.1, “JPEG FIFO”.

REG[09AEh] JPEG FIFO Extend Register Default = 0000h							Read Only
n/a						JPEG FIFO Valid Data Size bits 17-16	
15	14	13	12	11	10	9	8
n/a		Reserved		n/a		Reserved	
15	14	5	4	15	14	1	0

bits 9-8 JPEG FIFO Valid Data Size bits [17:16] (Read Only)
These bits extend the JPEG FIFO Valid Data Size (REG[09A8h]) to 18-bits.

bits 5-4 Reserved
The default value for these bits is 0.

bits 1-0 Reserved
The default value for these bits is 0.

REG[09B0h] Encode Size Limit Register 0 Default = 0000h							Read/Write
Encode Size Limit bits 15-8							
15	14	13	12	11	10	9	8
Encode Size Limit bits 7-0							
7	6	5	4	3	2	1	0

REG[09B2h] Encode Size Limit Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Encode Size Limit bits 23-16							
7	6	5	4	3	2	1	0

REG[09B2h] bits 7-0
REG[09B0h] bits 15-0 Encode Size Limit bits [23:0]

These bits are required for the JPEG encode process only. These bits specify the data size limit, in bytes, for the encoded JPEG file.

Note

Setting these registers to 0 will disable the Encode Size Limit Violation function and REG[0984h] bit 11 will not be set.

REG[09B4h] Encode Size Result Register 0 Default = 0000h							Read Only
Encode Size Result bits 15-8							
15	14	13	12	11	10	9	8
Encode Size Result bits 7-0							
7	6	5	4	3	2	1	0

REG[09B6h] Encode Size Result Register 1 Default = 0000h							Read Only
n/a							
15	14	13	12	11	10	9	8
Encode Size Result bits 23-16							
7	6	5	4	3	2	1	0

REG[09B6h] bits 7-0
REG[09B4h] bits 15-0 Encode Size Result bits [23:0] (Read Only)

These bits are required for the JPEG encode process only. These bits indicate the data size result, in bytes, for the encoded JPEG file.

REG[09B8h] JPEG File Size Register 0 Default = 0000h							Read/Write
JPEG File Size bits 15-8							
15	14	13	12	11	10	9	8
JPEG File Size bits 7-0							
7	6	5	4	3	2	1	0

REG[09BAh] JPEG File Size Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
JPEG File Size bits 23-16							
7	6	5	4	3	2	1	0

REG[09BAh] bits 7-0
REG[09B8h] bits 15-0 JPEG File Size bits [23:0]
These bits are required for the JPEG decode process only. These bits specify the JPEG file size in bytes and must be set before the Host begins writing decoded data to the JPEG FIFO.

REG[09BCh] JPEG FIFO Address Offset Register Default = 0040h							Read/Write
n/a							JPEG FIFO Address Offset bit 8
15	14	13	12	11	10	9	8
JPEG FIFO Address Offset bits 7-0							
7	6	5	4	3	2	1	0

bits 8-0 JPEG FIFO Address Offset bits [8:0]
These bits specify the MSB [18:10] of the 19-bit JPEG FIFO address (bits 9-0 are 0’s).

Note
Default is 10000h.

Note
The JPEG FIFO start address should be set so that the JPEG FIFO will fit in the remaining amount of memory, otherwise it will wrap to the beginning of memory.

10.4.17 JPEG Line Buffer Setting Register

REG[09C0h] JPEG Line Buffer Status Flag Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a					JPEG Line Buffer Full Flag	JPEG Line Buffer Half Flag	JPEG Line Buffer Empty Flag
7	6	5	4	3	2	1	0

bit 2 JPEG Line Buffer Full Flag
This flag is asserted when the JPEG Line Buffer becomes full. This flag is masked by the JPEG Line Buffer Full Interrupt Enable bit and is only available when REG[09C6h] bit 2 = 1.
When this bit = 0, the JPEG Line Buffer is not full.
When this bit = 1, the JPEG Line Buffer is full.

To clear this flag, when the JPEG Line Buffer is not full, write a 1 to this bit.

bit 1 JPEG Line Buffer Half Full Flag
This flag is asserted when the JPEG Line Buffer has become half full. This flag is masked by the JPEG Line Buffer Half Full Interrupt Enable bit and is only available when REG[09C6h] bit 1 = 1.
When this bit = 0, the JPEG Line Buffer is not half full.
When this bit = 1, the JPEG Line Buffer is half full.

To clear this flag, when the JPEG Line Buffer is not half full, write a 1 to this bit.

bit 0 JPEG Line Buffer Empty Flag
This flag is asserted when the JPEG Line Buffer becomes empty. This flag is masked by the JPEG Line Buffer Empty Interrupt Enable bit and is only available when REG[09C6h] bit 0 = 1.
When this bit = 0, the JPEG Line Buffer is not empty.
When this bit = 1, the JPEG Line Buffer is empty.

To clear this flag, when the JPEG Line Buffer is not empty, write a 1 to this bit.

REG[09C2h] JPEG Line Buffer Raw Status Flag Register Default = 0000h							Read Only
n/a							
15	14	13	12	11	10	9	8
n/a					Raw JPEG Line Buffer Full Flag	Raw JPEG Line Buffer Half Flag	Raw JPEG Line Buffer Empty Flag
7	6	5	4	3	2	1	0

bit 2 — Raw JPEG Line Buffer Full Flag (Read Only)
This flag is asserted when the JPEG Line Buffer becomes full. This flag is not affected by the JPEG Line Buffer Full Interrupt Enable bit (REG[09C6h] bit 2).
When this bit = 0, the JPEG Line Buffer is not full.
When this bit = 1, the JPEG Line Buffer is full.

To clear this flag, when the JPEG Line Buffer is not full, write a 1 to REG[09C0h] bit 2.

bit 1 — Raw JPEG Line Buffer Half Full Flag (Read Only)
This flag is asserted when the JPEG Line Buffer becomes half full. This flag is not affected by the JPEG Line Buffer Half Full Interrupt Enable bit (REG[09C6h] bit 1).
When this bit = 0, the JPEG Line Buffer is not half full.
When this bit = 1, the JPEG Line Buffer is half full.

To clear this flag, when the JPEG Line Buffer is not half full, write a 1 to REG[09C0h] bit 1.

bit 0 — Raw JPEG Line Buffer Empty Flag (Read Only)
This flag is asserted when the JPEG Line Buffer becomes empty. This flag is not affected by the JPEG Line Buffer Empty Interrupt Enable bit (REG[09C6h] bit 0).
When this bit = 0, the JPEG Line Buffer is not empty.
When this bit = 1, the JPEG Line Buffer is empty.

To clear this flag, when the JPEG Line Buffer is not empty, write a 1 to REG[09C0h] bit 0.

REG[09C4h] JPEG Line Buffer Raw Current Status Register Default = F001h							Read Only
Reserved				Reserved			
15	14	13	12	11	10	9	8
Reserved	n/a				Raw JPEG Line Buffer Full Current Status	Raw JPEG Line Buffer Half Full Current Status	Raw JPEG Line Buffer Empty Current Status
7	6	5	4	3	2	1	0

bits 15-12 — Reserved
The default value for these bits is 1111b.

bits 11-8 — Reserved
The default value for these bits is 0.

bit 2 Raw JPEG Line Buffer Full Current Status (Read Only)
This flag indicates the current status of the JPEG Line Buffer. This flag is not affected by the JPEG Line Buffer Full Interrupt Enable bit (REG[09C6h] bit 2).
When this bit = 0, the JPEG Line Buffer is not full.
When this bit = 1, the JPEG Line Buffer is full.

bit 1 Raw JPEG Line Buffer Half Full Current Status (Read Only)
This flag indicates the current status of the JPEG Line Buffer. This flag is not affected by the JPEG Line Buffer Half Full Interrupt Enable bit (REG[09C6h] bit 1).
When this bit = 0, the JPEG Line Buffer is not half full.
When this bit = 1, the JPEG Line Buffer is half full.

bit 0 Raw Line Buffer Empty Current Status (Read Only)
This flag indicates the current status of the JPEG Line Buffer. This flag is not affected by the JPEG Line Buffer Empty Interrupt Enable bit (REG[09C6h] bit 0).
When this bit = 0, the JPEG Line Buffer is not empty.
When this bit = 1, the JPEG Line Buffer is empty.

REG[09C6h] JPEG Line Buffer Interrupt Control Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a					JPEG Line Buffer Full Interrupt Enable	JPEG Line Buffer Half Full Interrupt Enable	JPEG Line Buffer Empty Interrupt Enable
7	6	5	4	3	2	1	0

bit 2 JPEG Line Buffer Full Interrupt Enable
This bit controls the JPEG Line Buffer Full Interrupt. The status of the interrupt can be determined using the JPEG Line Buffer Full Flag (REG[09C0h] bit 2).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 1 JPEG Line Buffer Half Full Interrupt Enable
This bit controls the JPEG Line Buffer Half Full Interrupt. The status of the interrupt can be determined using the JPEG Line Buffer Half Full Flag (REG[09C0h] bit 1).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 0 JPEG Line Buffer Empty Interrupt Enable
This bit controls the JPEG Line Buffer Empty Interrupt. The status of the interrupt can be determined using the JPEG Line Buffer Empty Flag (REG[09C0h] bit 0).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

REG[09C8h] through REG[09CEh] are Reserved

These registers are Reserved and should not be written.

REG[09D0h] JPEG Line Buffer Configuration Register Default = 2800h							Read/Write
Reserved	JPEG Line Buffer Raw Horizontal Pixel Size bits 10-4 (RO)						
15	14	13	12	11	10	9	8
JPEG Line Buffer Raw Horizontal Pixel Size bits 3-0 (RO)				Reserved	JPEG Line Buffer Horizontal Pixel Size bits 2-0		
7	6	5	4	3	2	1	0

bit 15 Reserved
The default value for this bit is 0.

bits 14-4 JPEG Line Buffer Raw Horizontal Pixel Size bits [10:0] (Read Only
These bits provide actual (real number) of the horizontal pixel size supported by the JPEG Line Buffer as set in bits 2-0.

bit 3 Reserved
The default value for this bit is 0.

bits 2-0 JPEG Line Buffer Horizontal Pixel Size bits [2:0]
These bits indicate the horizontal pixel size supported by the JPEG Line Buffer.

Note
When these bits = 101b, “2047” is read in bits 14-4. There is no problem in operation though original WUXGA is 1920.

Table 10-79: Supported Horizontal Pixel Size

REG[09D0h] bits 2-0	Supported Horizontal Pixel Size	Line Buffer Size
000b	VGA (640)	30k Bytes
001b	SVGA (800)	38k Bytes
010b	XGA (1024)	48k Bytes
011b	SXGA (1280)	60k Bytes
100b	XUGA (1600)	75k Bytes
101b	WUXGA (2047)	96k Bytes
101b - 111b	Reserved	

.

REG[09D2h] JPEG Line Buffer Address Offset Register Default = 0000h							Read/Write
Reserved							
15	14	13	12	11	10	9	8
Reserved		JPEG Line Buffer Address Offset bits 5-0					
7	6	5	4	3	2	1	0

bit 15-6 Reserved
The default value for these bits is 0.

bits 5-0 JPEG Line Buffer Address Offset bits
This bit is effect of REG[0F02h]. Please refer to the explanation of REG[0F02h].

REG[09D4h] through REG[09DEh] are Reserved

These registers are Reserved and should not be written

REG[09E0h] JPEG Line Buffer Read/Write Port Register Default = 0000h							Read/Write
JPEG Line Buffer Read/Write Port bits 15-8							
15	14	13	12	11	10	9	8
JPEG Line Buffer Read/Write Port bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 JPEG Line Buffer Read/Write Port bits [15:0]
If YUV data is being input from the Host, these bits are used as the JPEG Line Buffer read/write port. For all other modes, these bits have no hardware effect.

When YUV data is input from Host I/F (REG[0980] bits 3-1 = 001b or 101b), this port becomes the JPEG Line Buffer write port.
When encoded YUV data is input from Host I/F (REG[0980] bits 3-1 = 100b), this port becomes the JPEG Line Buffer write port.
When decoded YUV data is output to Host I/F (REG[0980] bits 3-1 = 100b), this port becomes the JPEG Line Buffer read port.

10.4.18 Interrupt Control Registers

REG[0A00h] Interrupt Status Register Default = 0000h							Read Only
n/a					Reserved		
15	14	13	12	11	10	9	8
SD Card Interrupt Status	n/a		Host Interrupt Status	Camera Interrupt Status	JPEG Interrupt Status	2D BitBLT Interrupt Status	Debug Interrupt Status
7	6	5	4	3	2	1	0

bit 10-8 Reserved
The default value for these bits is 0.

bit 7 SD Card Interrupt Status (Read Only)
This bit indicates the status of the SD Card interrupt.
When this bit = 0, no SD Card interrupt has occurred.
When this bit = 1, a SD Card interrupt has occurred. Status bits must be read in REG[6008] to determine the exact nature of the interrupt.

bit 4 Host Interrupt Status (Read Only)
This bit indicates the status of the Host interrupt.
When this bit = 0, no Host interrupt has occurred.
When this bit = 1, a Host interrupt has occurred. Status bits must be read in REG[0A0Ah] to determine the exact nature of the interrupt.

bit 3 Camera Interrupt Status (Read Only)
This bit indicates the status of the Camera Interrupt.
When this bit = 0, no Camera interrupt has occurred.
When this bit = 1, a Camera interrupt has occurred. Status bits must be read in REG[0116h] to determine the exact nature of the interrupt.

bit 2 JPEG Interrupt Status (Read Only)
This bit indicates the status of the JPEG Interrupt.
When this bit = 0, no JPEG interrupt has occurred.
When this bit = 1, a JPEG interrupt has occurred. Status bits must be read in REG[0982h] to determine the exact nature of the interrupt.

bit 1 2D BitBLT Interrupt Status (Read Only)
This bit indicates the status of the BitBLT Interrupt.
When this bit = 0, no BitBLT interrupt has occurred.
When this bit = 1, a BitBLT interrupt has occurred. Status bits must be read in REG[8030h] to determine the exact nature of the interrupt.

bit 0 Debug Interrupt Status (Read Only)
This bit indicates the status of the Debug Interrupt.
When this bit = 0, no Debug interrupt has occurred.
When this bit = 1, a Debug interrupt has occurred. Status bits must be read in REG[0A06h] to determine the exact nature of the interrupt.

REG[0A02h] Interrupt Control Register 0 Default = 0000h							Read/Write
n/a					Reserved		
15	14	13	12	11	10	9	8
SD Card Interrupt Enable	n/a		Host Interrupt Enable	Camera Interrupt Enable	JPEG Interrupt Enable	2D BitBLT Interrupt Enable	Debug Interrupt Enable
7	6	5	4	3	2	1	0

bits 10-8 Reserved
The default value for these bits is 0.

bit 7 SD Card Interrupt Enable
This bit controls the SD Card interface interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 4 Host Interrupt Enable
This bit controls the Host interface interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 3 Camera Interrupt Enable
This bit controls the Camera interface interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 2 JPEG Interrupt Enable
This bit controls the JPEG codec interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 1 2D BitBLT Interrupt Enable
This bit controls the BitBLT interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 0 Debug Interrupt Enable
This bit controls the debug interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

REG[0A04h] Interrupt Control Register 1
Default = 0000h Read/Write

n/a					Reserved		
15	14	13	12	11	10	9	8
SD Card Manual Interrupt	n/a		Host Manual Interrupt	Camera Manual Interrupt	JPEG Manual Interrupt	2D BitBLT Manual Interrupt	Debug Manual Interrupt
7	6	5	4	3	2	1	0

bits 10-8 Reserved
The default value for these bits is 0.

bit 7 SD Card Manual Interrupt
This bit manually sets a SD Card interface interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

bit 4 Host Manual Interrupt
This bit manually sets a Host interface interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

bit 3 Camera Manual Interrupt
This bit manually sets a Camera interface interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

bit 2 JPEG Manual Interrupt
This bit manually sets a JPEG codec interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

bit 1 2D BitBLT Manual Interrupt
This bit manually sets a BitBLT interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

bit 0 Debug Manual Interrupt
This bit manually sets a debug interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

REG[0A06h] Debug Status Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a		Reserved		YRC Memory Write Complete Flag	LCD Interface Status Flag	Display FIFO Empty Flag	YUV/RGB Write Buffer Overflow Flag
7	6	5	4	3	2	1	0

bits 5-4 Reserved
The default value for these bits is 0.

bit 3 YRC Memory Write Complete Flag
For Reads:
When this bit = 0, the interrupt is not occurred.
When this bit = 1, the interrupt is occurred.

For Writes:
When this bit is written as 0, there is no hardware effect.
When this bit is written as 1, the flag is cleared.

bit 2 LCD Interface Complete Flag
For Reads:
When this bit = 0, the interrupt is not occurred.
When this bit = 1, the interrupt is occurred.

For Writes:
When this bit is written as 0, there is no hardware effect.
When this bit is written as 1, the flag is cleared.

bit 1 Display FIFO Empty Flag
This flag indicates whether the panel interface has attempted to read data from the display FIFO while it is empty. This flag can be used to generate an interrupt (INT signal) to the Host by setting both the Display FIFO Empty Interrupt Enable (REG[0A08h] bit 1 = 1) and the Debug Interrupt Enable (REG[0A02h] bit 0 = 1). This bit is masked by REG[0A08h] bit 1
For Reads:
When this bit = 0, the panel interface has not attempted to read data from the display FIFO while it is empty.
When this bit = 1, the panel interface has attempted to read data from the display FIFO while it is empty.

For Writes:
When this bit is written as 0, there is no hardware effect.
When this bit is written as 1, the Display FIFO Empty Flag is cleared.

bit 0 YUV/RGB Write Buffer Overflow Flag
For Reads:
When this bit = 0, no write buffer overflow has occurred.
When this bit = 1, a write buffer overflow has occurred in the path from the YUV/RGB converter to the display buffer.

For Writes:
When this bit is written as 0, there is no hardware effect.
When this bit is written as 1, the YUV/RGB write buffer overflow flag is cleared.

REG[0A08h] Interrupt Control for Debug Register Default = 0000h							Read/Write
LCD VDNP Interrupt Select	LCD VNDP Interrupt Polarity	n/a					
15	14	13	12	11	10	9	8
n/a		Reserved		YRC Memory Write Complete Interrupt Enable	LCD Interface Interrupt Enable	Display FIFO Empty Interrupt Enable	YUV/RGB Write Buffer Overflow Interrupt Enable
7	6	5	4	3	2	1	0

bit 15 LCD VNDP Interrupt Select
When this bit = 0, the LCD VNDP Interrupt is derived from VNDP
When this bit = 1, the LCD VNDP Interrupt is derived from FPFRAME

bit 14 LCD VNDP Interrupt Polarity
When this bit = 0, the LCD VNDP Interrupt polarity is VNDP rising edge / FPFRAME falling edge.
When this bit = 1, the LCD VNDP Interrupt polarity is VNDP falling edge / FPFRAME rising edge

bits 5-4 Reserved
The default value for these bits is 0.

bit 3 YRC Memory Write Complete Interrupt Enable
This bit controls the YRC Memory Write Complete interrupt.
When this bit = 0, the YRC Memory Write Complete interrupt is disabled.
When this bit = 1, the YRC Memory Write Complete interrupt is enabled.

bit 2 LCD Interface Interrupt Enable
This bit controls the LCD Interface interrupt.
When this bit = 0, the LCD Interface interrupt is disabled.
When this bit = 1, the LCD Interface interrupt is enabled

bit 1 Display FIFO Empty Interrupt Enable
This bit controls the display FIFO empty interrupt.
When this bit = 0, the display FIFO empty interrupt is disabled.
When this bit = 1, the display FIFO empty interrupt is enabled.

bit 0 YUV/RGB Write Buffer Overflow Interrupt Enable
This bit controls the YUV/RGB write buffer overflow flag interrupt output.
When this bit = 1, the YUV/RGB write buffer overflow interrupt is enabled.
When this bit = 0, the YUV/RGB write buffer overflow interrupt is disabled.

REG[0A0Ah] Host Cycle Interrupt Status Register Default = 0000h							Read/Write
Cycle Time Out Interrupt Raw Status	n/a						
15	14	13	12	11	10	9	8
n/a		Reserved					
7	6	5	4	3	2	1	0

bit 15 Cycle Time Out Interrupt Raw Status
This bit indicates the raw status of the Cycle Time Out Interrupt which happens when an access cycle to/from the JPEG Line Buffer lasts longer than the specified Time Out Value (REG[0A0Eh] bits 4-0). If a Cycle Time Out Interrupt occurs and the Cycle Time Out Interrupt is enabled (REG[0A0Ch] bit 15 = 1) and the Host Interrupt Enable bit (REG[0A02h] bit 4) is set to 1, the INT pin is asserted.
When this bit = 0, a interrupt has not occurred.
When this bit = 1, a Cycle Time Out Interrupt has occurred.

To clear this bit, write a 1 to this bit.

bits 5-0 Reserved
The default value for these bits is 0.

REG[0A0Ch] Host Cycle Interrupt Control Register Default = 0000h							Read/Write
Cycle Time Out Interrupt Enable	n/a						
15	14	13	12	11	10	9	8
n/a		Reserved					
7	6	5	4	3	2	1	0

bit 15 Cycle Time Out Interrupt Enable
When this bit is 0, the Host Interrupt Request bit is not set.
When this bit is 1, the Host Interrupt Request bit is set.

bits 5-0 Reserved
The default value for these bits is 0.

REG[0A0Eh] Cycle Time Out Control Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Reserved	n/a		Time Out Value bits 4-0				
7	6	5	4	3	2	1	0

bit 7 Reserved
The default value for this bit is 0.

bits 4-0 Time Out Value bits [4:0]
These bits control the length of time (time out value) allowed for an access cycle to the JPEG FIFO, JPEG Line Buffer, or BitBLT FIFO to take place before a terminate cycle is generated. The time out value is specified as follows and should be configured to a default value of 1Fh at initialization.

REG[0A0Eh] bits 4-0 = Time Out Value in CLKs
Time Out Value = Internal System Clock ÷ 2

REG[0A10h] is Reserved

This register is Reserved and should not be written.

REG[0A20h] Indirect Interface Interrupt Flag Register Default = 0000h							Read/Write
n/a		Reserved		JPEG LB Read Error Interrupt Flag	JPEG LB Write Error Interrupt Flag	JPEG FIFO Read Error Interrupt Flag	JPEG FIFO Write Error Interrupt Flag
15	14	13	12	11	10	9	8
n/a						Memory Read Error Interrupt Flag	Memory Write Error Interrupt Flag
7	6	5	4	3	2	1	0

Note
These bits are only valid when the Indirect Host Interface is selected (see CNF[4:2]. This register must not be accessed when using Direct Host Interface modes.

Note
After each interrupt assertion the corresponding error flags are set, and then the interrupt is released.

bits 13-12 Reserved
The default value for these bits is 0.

bit 11 JPEG Line Buffer Read Error Interrupt Flag
This bit indicates the status of the JPEG Line Buffer Read Error Interrupt.
When this bit = 0, a JPEG Line Buffer Read Error Interrupt has not occurred.
When this bit = 1, a JPEG Line Buffer Read Error Interrupt has occurred.

To clear this bit, write this bit as 1.

bit 10 JPEG Line Buffer Write Error Interrupt Flag
This bit indicates the status of the JPEG Line Buffer Write Error Interrupt.
When this bit = 0, a JPEG Line Buffer Write Error Interrupt has not occurred.
When this bit = 1, a JPEG Line Buffer Write Error Interrupt has occurred.

To clear this bit, write this bit as 1.

bit 9 JPEG FIFO Read Error Interrupt Flag
This bit indicates the status of the JPEG FIFO Read Error Interrupt.
When this bit = 0, a JPEG FIFO Read Error Interrupt has not occurred.
When this bit = 1, a JPEG FIFO Read Error Interrupt has occurred.

To clear this bit, write this bit as 1.

bit 8 JPEG FIFO Write Error Interrupt Flag
This bit indicates the status of the JPEG FIFO Write Error Interrupt.
When this bit = 0, a JPEG FIFO Write Error Interrupt has not occurred.
When this bit = 1, a JPEG FIFO Write Error Interrupt has occurred.

To clear this bit, write this bit as 1.

bit 1 Memory Read Error Interrupt Flag
This bit indicates the status of the Memory Read Error Interrupt.
When this bit = 0, a Memory Read Error Interrupt has not occurred.
When this bit = 1, a Memory Read Error Interrupt has occurred.

To clear this bit, write this bit as 1.

bit 0 Memory Write Error Interrupt Flag
This bit indicates the status of the Memory Write Error Interrupt.
When this bit = 0, a Memory Write Error Interrupt has not occurred.
When this bit = 1, a Memory Write Error Interrupt has occurred.

To clear this bit, write this bit as 1.

REG[0A22h] Indirect Interface Interrupt Control Register							
Default = 0000h							Read/Write
n/a		Reserved		JPEG LB Read Error Interrupt Enable	JPEG LB Write Error Interrupt Enable	JPEG FIFO Read Error Interrupt Enable	JPEG FIFO Write Error Interrupt Enable
15	14	13	12	11	10	9	8
n/a						Memory Read Error Interrupt Enable	Memory Write Error Interrupt Enable
7	6	5	4	3	2	1	0

These bits are only valid when the Indirect Host Interface is selected (see CNF[4:2]).
This register must not be accessed when using Direct Host Interface modes.

bits 13-12 Reserved
The default value for these bits is 0.

bit 11 JPEG Line Buffer Read Error Interrupt Enable
This bit controls the JPEG Line Buffer Read Error Interrupt.
When this bit = 0, the JPEG Line Buffer Read Error Interrupt is disabled.
When this bit = 1, the JPEG Line Buffer Read Error Interrupt is enabled.

bit 10 JPEG Line Buffer Write Error Interrupt Enable
This bit controls the JPEG Line Buffer Write Error Interrupt.
When this bit = 0, the JPEG Line Buffer Write Error Interrupt is disabled.
When this bit = 1, the JPEG Line Buffer Write Error Interrupt is enabled.

bit 9 JPEG FIFO Read Error Interrupt Enable
This bit controls the JPEG FIFO Read Error Interrupt.
When this bit = 0, the JPEG FIFO Read Error Interrupt is disabled.
When this bit = 1, the JPEG FIFO Read Error Interrupt is enabled.

bit 8 JPEG FIFO Write Error Interrupt Enable
This bit controls the JPEG FIFO Write Error Interrupt.
When this bit = 0, the JPEG FIFO Write Error Interrupt is disabled.
When this bit = 1, the JPEG FIFO Write Error Interrupt is enabled.

bit 1 Memory Read Error Interrupt Enable
This bit controls the Memory Read Error Interrupt.
When this bit = 0, the Memory Read Error Interrupt is disabled.
When this bit = 1, the Memory Read Error Interrupt is enabled.

bit 0 Memory Write Error Interrupt Enable
This bit controls the Memory Write Error Interrupt.
When this bit = 0, the Memory Write Error Interrupt is disabled.
When this bit = 1, the Memory Write Error Interrupt is enabled.

REG[0A40h] Interrupt Request Status Register
Default = 0000h Read Only

n/a					Reserved	Reserved	Reserved
15	14	13	12	11	10	9	8
SD Card Interrupt Request Status	n/a		Host Interface Interrupt Request Status	Camera Interrupt Request Status	JPEG Interrupt Request Status	2D BitBLT Interrupt Request Status	Debug Interrupt Request Status
7	6	5	4	3	2	1	0

bits 10-8 Reserved
The default value for these bits is 0.

bit 7 SD Card Interface Interrupt Request Status (Read Only)
When this bit = 0, a SD Card interface interrupt has not occurred.
When this bit = 1, a SD Card interface interrupt request has occurred.

bit 4 Host Interface Interrupt Request Status (Read Only)
When this bit = 0, a host interface interrupt has not occurred.
When this bit = 1, a host interface interrupt request has occurred.

bit 3 Camera Interrupt Request Status (Read Only)
When this bit = 0, a camera interrupt request has not occurred.
When this bit = 1, a camera interrupt request has occurred.

bit 2 JPEG Interrupt Request Status (Read Only)
When this bit = 0, a JPEG interrupt request has not occurred.
When this bit = 1, a JPEG interrupt request has occurred.

bit 1 2D BitBLT Interrupt Request Status (Read Only)
When this bit = 0, a BitBLT interrupt request has not occurred.
When this bit = 1, a BitBLT interrupt request has occurred.

bit 0 Debug Interrupt Request Status (Read Only)
When this bit = 0, a debug interrupt request has not occurred.
When this bit = 1, a debug interrupt request has occurred.

10.4.19 JPEG Encode Performance Register

REG[0F00h] JPEG Encode Performance Register
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a							JPEG Encode Fixed Table Mode
7	6	5	4	3	2	1	0

bit 0 — JPEG Encode Fixed Table Mode
When this bit = 0, the JPEG Encoding process runs in “Fixed Table Mode” (High Performance).
When this bit = 1, the JPEG Encoding process runs in “Standard Mode”.
When Fixed table Mode is enabled, the Huffman Tables must be programmed according to the tables specified in the ISO/IEC IS 10918-1 ANNEX K in the ITU-T recommendation T.81 book K. For recommended values see the bit descriptions for the Huffman Tables (REG[1400h] - [17A2h]).

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REG[0F02h] JPEG Extended Address Register
Default = 0000h — Read/Write

n/a					Reserved		
15	14	13	12	11	10	9	8
n/a					JPEG Line Buffer Start Address bits 2-0		
7	6	5	4	3	2	1	0

bits 10-8 — Reserved
The default value for these bits is 0.

bits 2-0 — JPEG Line Buffer Start Address bits [2:0]
These bits in conjunction with the JPEG Line Buffer Address Offset bit (REG[09D2h] bits 5-0) determine the final start address of the JPEG Line Buffer. These bits must not be changed while the JPEG codec is busy (REG[1004h] bit 0 = 1).

Table 10-80: JPEG Line Buffer Start Address

REG[0F02h] bits 2-0	REG[09D2h] bits 5-0	JPEG Line Buffer Start Address
000b	000000b	00000h
000b	000001b	00400h
000b	000010b	00800h
000b	000011b	00C00h
000b	000100b	01000h
000b	000101b	01400h
000b	000110b	01800h
000b	000111b	01C00h
000b	001000b	02000h
000b	001001b	02400h
000b	001010b	02800h
000b	001011b	02C00h
000b	001100b	03000h
000b	001101b	03400h

Table 10-80: JPEG Line Buffer Start Address (Continued)

REG[0F02h] bits 2-0	REG[09D2h] bits 5-0	JPEG Line Buffer Start Address
000b	001110b	03800h
000b	001111b	03C00h
000b	010000b	04000h
000b	010001b	04400h
000b	:	:
000b	011111b	07C00h
000b	100000b	08000h
000b	100001b	08400h
000b	:	:
000b	111111b	0FC00h
001b	000000b	10000h
001b	000001b	10400h
001b	:	:
001b	111111b	1FC00h
010b	000000b	20000h
010b	:	:
011b	000000b	30000h
011b	:	:
011b	100000b	38000h
011b	:	:
100b	000000b	40000h
100b	:	:
100b	100000b	48000h
100b	:	:
101b	000000b	50000h
101b	:	:
101b	100000b	58000h
101b	:	:
110b	000000b	60000h
110b	:	:
110b	100000b	68000h
110b	:	:
111b	000000b	70000h
111b	:	:
111b	100000b	78000h
111b	:	:
111b	111111b	7FC00h

Note

JPEG Line Buffer Start Address is able to assign it in the range of 7FC00h from 0000h.

10.4.20 JPEG Codec Registers

REG[1000h] Operation Mode Setting Register
Default = 0000h   Read/Write

15	14	13	12	11	10	9	8
n/a							
Reserved	n/a		Reserved	Marker Insert Enable	JPEG Operation Select	YUV Format Select bits 1-0	
7	6	5	4	3	2	1	0

bit 7 Reserved
The default value for this bit is 0.

bit 4 Reserved
The default value for this bit is 0.

bit 3 Marker Insert Enable
This bit determines if the marker (see REG[1020h] - [1066h]) is inserted during JPEG encoding. During JPEG decoding this bit is ignored.
When this bit = 0, the marker is not inserted.
When this bit = 1, the entire marker is inserted into the JPEG file.

Note
When the marker is inserted, the entire 36 byte marker (REG[1020h] - [1066h]) is inserted into the JPEG file regardless of what value the marker length bits (REG[1024h] - [1026h]) specify.

bit 2 JPEG Operation Select
This bit selects the JPEG operation and the input source for the resizer block. This bit should be set to 0 when resizing data from the camera. This bit must be cleared before the JPEG module is disabled (REG[0980h] bit 0 = 0).

Table 10-81: JPEG Operation Selection

REG[1000h] bit 2	JPEG Operation
0	Encode
1	Decode

bits 1-0 YUV Format Select bits [1:0]
These bits select the YUV format of the JPEG codec. For the JPEG encode process, these bits must be set to the desired YUV format. For the JPEG decode process, these bits are read only and indicate the YUV format of the data being decoded.

Table 10-82: YUV Format Selection

REG[1000h] bits 1-0	YUV Format
00b	4:4:4 (decode only)
01b	4:2:2 (encode/decode)
10b	4:2:0 (encode/decode)
11b	4:1:1 (encode/decode)

Note
Only YUV 4:2:0 and YUV 4:2:2 are supported for Host input JPEG decode/encode.

REG[1002h] Command Setting Register Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
JPEG Codec SW Reset	n/a						JPEG Operation Start
7	6	5	4	3	2	1	0

Note
This register is write only. Reading this register may cause the JPEG Codec to behave unexpectedly.

Note
When the JPEG codec is working, this register must not be written to, except to perform a JPEG codec software reset.

bit 7 JPEG Codec Software Reset (Write Only)
This bit initiates a software reset of the JPEG Codec. The JPEG Codec registers (REG[1000h] - [17A2h]) are not affected.
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the JPEG Codec is reset.

bit 0 JPEG Operation Start (Write Only)
This bit is used to begin a JPEG operation.
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the JPEG operation is started.

REG[1004h] JPEG Operation Status Register Default = 0000h							Read Only
n/a							
15	14	13	12	11	10	9	8
n/a							JPEG Operation Status (RO)
7	6	5	4	3	2	1	0

Note

This register is read only. Writing this register may cause the JPEG Codec to behave unexpectedly.

bit 0 JPEG Operation Status (Read Only)
This bit indicates the state of the JPEG codec and clears the JPEG codec interrupt (REG[0982h] bit 1) when read.
When this bit = 0, the JPEG codec is idle.
When this bit = 1, the JPEG codec is busy (a decode or encode operation is in progress).

REG[1006h] Quantization Table Number Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a		Reserved			Color 3 Table Select	Color 2 Table Select	Color 1 Table Select
7	6	5	4	3	2	1	0

bits 5-3 Reserved
The default value for these bits is 0.

bit 2 Color 3 Table Select
When this bit = 0, the Color 3 Table uses Quantization Table No. 0 (REG[1200 - 127Eh].
When this bit = 1, the Color 3 Table uses Quantization Table No. 1 (REG[1280 - 12FEh].

bit 1 Color 2 Table Select
When this bit = 0, the Color 2 Table uses Quantization Table No. 0 (REG[1200 - 127Eh].
When this bit = 1, the Color 2 Table uses Quantization Table No. 1 (REG[1280 - 12FEh].

bit 0 Color 1 Table Select
When this bit = 0, the Color 1 Table uses Quantization Table No. 0 (REG[1200 - 127Eh].
When this bit = 1, the Color 1 Table uses Quantization Table No. 1 (REG[1280 - 12FEh].

REG[1008h] Huffman Table Number Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a		AC Color 3 Table Select	DC Color 3 Table Select	AC Color 2 Table Select	DC Color 2 Table Select	AC Color 1 Table Select	DC Color 1 Table Select
7	6	5	4	3	2	1	0

bit 5 AC Color 3 Table Select
When this bit = 0, the AC Color 3 Table uses the AC Huffman Table No. 0 (REG[1440-145Eh] and REG[1460-15A2h]).
When this bit = 1, the AC Color 3 Table uses the AC Huffman Table No. 1 (REG[1640-165Eh] and REG[1660-17A2h]).

bit 4 DC Color 3 Table Select
When this bit = 0, the DC Color 3 Table uses the DC Huffman Table No. 0 (REG[1400-141Eh] and REG[1420-1436h]).
When this bit = 1, the DC Color 3 Table uses the DC Huffman Table No. 1 (REG[1600-161Eh] and REG[1620-1636h]).

bit 3 AC Color 2 Table Select
When this bit = 0, the AC Color 2 Table uses the AC Huffman Table No. 0 (REG[1440-145Eh] and REG[1460-15A2h]).
When this bit = 1, the AC Color 2 Table uses the AC Huffman Table No. 1 (REG[1640-165Eh] and REG[1660-17A2h]).

bit 2 DC Color 2 Table Select
When this bit = 0, the DC Color 2 Table uses the DC Huffman Table No. 0 (REG[1400-141Eh] and REG[1420-1436h]).
When this bit = 1, the DC Color 2 Table uses the DC Huffman Table No. 1 (REG[1600-161Eh] and REG[1620-1636h]).

bit 1 AC Color 1 Table Select
When this bit = 0, the AC Color 1 Table uses the AC Huffman Table No. 0 (REG[1440-145Eh] and REG[1460-15A2h]).
When this bit = 1, the AC Color 1 Table uses the AC Huffman Table No. 1 (REG[1640-165Eh] and REG[1660-17A2h]).

bit 0 DC Color 1 Table Select
When this bit = 0, the DC Color 1 Table uses the DC Huffman Table No. 0 (REG[1400-141Eh] and REG[1420-1436h]).
When this bit = 1, the DC Color 1 Table uses the DC Huffman Table No. 1 (REG[1600-161Eh] and REG[1620-1636h]).

REG[100Ah] DRI Setting Register 0							
Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
DRI Value bits 15-8							
7	6	5	4	3	2	1	0

REG[100Ch] DRI Setting Register 1							
Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
DRI Value bits 7-0							
7	6	5	4	3	2	1	0

REG[100Ah] bits 7-0
REG[100Ch] bits 7-0 DRI Value bits [15:0]

These bits determine the MCU number for RST marker insertion during encoding. During decoding, these bits are ignored. The DRI value bits must be set when JPEG 180° Rotation Encode is enabled (REG[0980h] bit 8 = 1). The DRI (Designated Restart Interval) value must be set as follows.

DRI = Image Width / Horizontal MCU Size

Where:

MCU Size depends on the YUV format (REG[1000h] bits 1-0) as follows

Table 10-83: MCU Size

REG[1000h] bits 1-0	YUV Format	MCU Size (Horizontal x Vertical)
00b	Reserved	Reserved
01b	4:2:2	16 x 8
10b	4:2:0	16 x 16
11b	4:1:1	32 x 8

REG[100Eh] Vertical Pixel Size Register 0
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
Y Pixel Size bits 15-8							
7	6	5	4	3	2	1	0

REG[1010h] Vertical Pixel Size Register 1
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
Y Pixel Size bits 7-0							
7	6	5	4	3	2	1	0

REG[100Eh] bits 7-0
REG[1010h] bits 7-0 Y Pixel Size bits [15:0]

For the JPEG encode process, these bits specify the vertical image size before encoding takes place.
For the JPEG decode process, these bits are read-only and indicate the vertical image size.

The following restrictions must be observed when setting the Vertical Pixel Size. The minimum resolution must be set based on the YUV format as follows.

Table 10-84: Vertical Pixel Size Minimum Resolution Restrictions

YUV Format	Minimum Resolution
4:4:4 (decode only)	1x1
4:2:2 (encode/decode)	2x1
4:2:0 (encode/decode)	2x2
4:1:1 (encode/decode)	4x1

Note

For all processes (JPEG encode/decode and YUV capture/display) the following formula must be valid.

Vertical Pixel Size > 1

REG[1012h] Horizontal Pixel Size Register 0 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
X Pixel Size bits 15-8							
7	6	5	4	3	2	1	0

REG[1014h] Horizontal Pixel Size Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
X Pixel Size bits 7-0							
7	6	5	4	3	2	1	0

REG[1012h] bits 7-0
REG[1014h] bits 7-0 X Pixel Size bits [15:0]

For the JPEG encode process, these bits specify the horizontal image size before encoding takes place.
For the JPEG decode process, these bits are read-only and indicate the horizontal image size.

The following restrictions must be observed when setting the Vertical Pixel Size. The minimum resolution must be set based on the YUV format as follows.

Table 10-85: Horizontal Pixel Size Minimum Resolution Restrictions

YUV Format	Minimum Resolution	Minimum Horizontal Pixel Size
4:2:2	2x1	2
4:2:0	2x2	16
4:1:1	4x1	4

Note
1:1 camera clock JPEG encode should be limited to a maximum resolution of 800x600.

REG[1016h] Through REG[101Ah] are Reserved

These registers are Reserved and should not be written.

REG[101Ch] RST Marker Operation Setting Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a						RST Marker Operation Select bits 1-0	
7	6	5	4	3	2	1	0

bits 1-0 RST Marker Operation Select bits [1:0]
For the JPEG decode process, these bits select the RST Marker Operation.
For the JPEG encode process, these bits are not used.

Table 10-86: RST Marker Selection

REG[101Ch] bits 1-0	RST Marker Operation
00b	**Error detection and data revise function is turned off** This option should only be used when it is certain that the JPEG file to be decoded is correct and has no errors. If there is an error in the file, no error detection will take place and the decode process will not finish correctly.
01b	**Error detection on** When an error is detected during the decode process, the decode process finishes and the JPEG interrupt is asserted (REG[0A00h] bit 2 = 1). To determine the exact nature of the operational error see REG[0982h]. To determine the JPEG decode error (file error), check the JPEG Error Status bits (REG[101Eh] bits 6-3). Because the decode process finished before normal completion, all data can not be displayed. If the JPEG file is to be decoded again with the Data Revise function on, a software reset is required (see REG[1002h] bit 7).
10b	**Data revise function on** When an error is detected during the decode process, data is skipped/added automatically and the decode process continues normally to the end of file. After the decode process finishes, a data revise interrupt is asserted. Because the decode process is finished completely, the next JPEG file can be decoded immediately.
11b	Reserved

REG[101Eh] RST Marker Operation Status Register Default = 0000h							Read Only
n/a							
15	14	13	12	11	10	9	8
Revise Code	JPEG Error Status bits 3-0				n/a		
7	6	5	4	3	2	1	0

Note
This register resets to 0000h after reading.

bit 7 Revise Code (Read Only)
This bit is valid only when the data revise function is enabled using the RST Marker Selection bits (REG[101Ch bits 1-0 = 10b).
For the JPEG decode process, this bit indicates whether a revise operation has been done.
For the JPEG encode process, this bit is not used.
When this bit = 0, a revise operation was not done.
When this bit = 1, a revise operation was done.

bits 6-3 JPEG Error Status [3:0] (Read Only)
These bits are valid only when error detection is enabled using the RST Marker Selection bits (REG[101Ch bits 1-0 = 01b).
For the JPEG decode process, these bits indicate the type of JPEG error. If these bits return 0000b, no error has occurred.
For the JPEG encode process, these bits are not used.

Table 10-87: JPEG Error Status

REG[101Eh] bits 6-3	JPEG Error Status
0000b	No error
0001b - 1010b	Reserved
1011b	Restart interval error
1100b	Image size error
1101b - 1111b	Reserved

REG[1020 - 1066h] Insertion Marker Data Register Default = 00FFh							Read/Write
n/a							
15	14	13	12	11	10	9	8
Insert marker Data bits 7-0							
7	6	5	4	3	2	1	0

REG[1020h-1066h] These registers (36 bytes) store the Insertion Marker Data which gets inserted into the JPEG file. Only the even bytes are used. All unused registers (up to REG[1200h]) should be filled with FFh. The registers are defined as follows.

Table 10-88: Insertion Marker Data Register Usage

Register	Description
REG[1020h]-[1022h]	These registers set the insertion marker code type.
REG[1024h]-[1026h]	These registers set the marker length (0002h - 0022h).
REG[1028h]-[1066h]	These registers set the marker data (up to a maximum of 32 bytes). Note that all unused registers must be filled with FFh.

REG[1200 - 127Eh] Quantization Table No. 0 Register Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
Quantization Table No. 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1200-127Eh] Quantization Table No. 0
These registers are used for the JPEG encode process only.

REG[1280 - 12FEh] Quantization Table No. 1 Register							
Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
Quantization Table No. 1 bits 7-0							
7	6	5	4	3	2	1	0

REG[1280-12FEh] Quantization Table No. 1
These registers are used for the JPEG encode process only.

REG[1400 - 141Eh] DC Huffman Table No. 0 Register 0							
Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
DC Huffman Table No. 0 Register 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1400-141Eh] DC Huffman Table No. 0 (Write Only)
These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 0 must be programmed as follows.

Table 10-89: DC Huffman Table No. 0 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1400h]	00h	REG[1408h]	01h	REG[1410h]	01h	REG[1418h]	00h
REG[1402h]	01h	REG[140Ah]	01h	REG[1412h]	00h	REG[141Ah]	00h
REG[1404h]	05h	REG[140Ch]	01h	REG[1414h]	00h	REG[141Ch]	00h
REG[1406h]	01h	REG[140Eh]	01h	REG[1416h]	00h	REG[141Eh]	00h

REG[1420 - 1436h] DC Huffman Table No. 0 Register 1							
Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
Reserved (must be all 0)				DC Huffman Table No. 0 Register 1 bits 3-0			
7	6	5	4	3	2	1	0

REG[1420-1436h] DC Huffman Table No. 0 (Write Only)
These registers are used for the JPEG encode process only and set a group number based on the order of probability of occurrence. Only bits 3-0 are used (bits 7-4 must be set to 0). When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 0 must be programmed as follows.

Table 10-90: DC Huffman Table No. 1 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1420h]	00h	REG[1426h]	03h	REG[142Ch]	06h	REG[1432h]	09h
REG[1422h]	01h	REG[1428h]	04h	REG[142Eh]	07h	REG[1434h]	0Ah
REG[1424h]	02h	REG[142Ah]	05h	REG[1430h]	08h	REG[1436h]	0Bh

REG[1440 - 145Eh] AC Huffman Table No. 0 Register 0 Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
AC Huffman Table No. 0 Register 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1440-145Eh] AC Huffman Table No. 0 (Write Only)
These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 0 must be programmed as follows.

Table 10-91: AC Huffman Table No. 0 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1440h]	00h	REG[1448h]	03h	REG[1450h]	05h	REG[1458h]	00h
REG[1442h]	02h	REG[144Ah]	02h	REG[1452h]	05h	REG[145Ah]	00h
REG[1444h]	01h	REG[144Ch]	04h	REG[1454h]	04h	REG[145Ch]	01h
REG[1446h]	03h	REG[144Eh]	03h	REG[1456h]	04h	REG[145Eh]	7Dh

REG[1460 - 15A2h] AC Huffman Table No. 0 Register 1 Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
AC Huffman Table No. 0 Register 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1460-15A2h] AC Huffman Table No. 0 (Write Only)
These registers are used for the JPEG encode process only and set a zero run length / group number based on the order of probability of occurrence. When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 0 must be programmed as follows.

Table 10-92: AC Huffman Table No. 0 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1460h]	01h	REG[14B0h]	17h	REG[1500h]	6Ah	REG[1550h]	B7h
REG[1462h]	02h	REG[14B2h]	18h	REG[1502h]	73h	REG[1552h]	B8h
REG[1464h]	03h	REG[14B4h]	19h	REG[1504h]	74h	REG[1554h]	B9h
REG[1466h]	00h	REG[14B6h]	1Ah	REG[1506h]	75h	REG[1556h]	BAh
REG[1468h]	04h	REG[14B8h]	25h	REG[1508h]	76h	REG[1558h]	C2h
REG[146Ah]	11h	REG[14BAh]	26h	REG[150Ah]	77h	REG[155Ah]	C3h
REG[146Ch]	05h	REG[14BCh]	27h	REG[150Ch]	78h	REG[155Ch]	C4h
REG[146Eh]	12h	REG[14BEh]	28h	REG[150Eh]	79h	REG[155Eh]	C5h
REG[1470h]	21h	REG[14C0h]	29h	REG[1510h]	7Ah	REG[1560h]	C6h
REG[1472h]	31h	REG[14C2h]	2Ah	REG[1512h]	83h	REG[1562h]	C7h
REG[1474h]	41h	REG[14C4h]	34h	REG[1514h]	84h	REG[1564h]	C8h
REG[1476h]	06h	REG[14C6h]	35h	REG[1516h]	85h	REG[1566h]	C9h
REG[1478h]	13h	REG[14C8h]	36h	REG[1518h]	86h	REG[1568h]	CAh
REG[147Ah]	51h	REG[14CAh]	37h	REG[151Ah]	87h	REG[156Ah]	D2h
REG[147Ch]	61h	REG[14CCh]	38h	REG[151Ch]	88h	REG[156Ch]	D3h
REG[147Eh]	07h	REG[14CEh]	39h	REG[151Eh]	89h	REG[156Eh]	D4h
REG[1480h]	22h	REG[14D0h]	3Ah	REG[1520h]	8Ah	REG[1570h]	D5h
REG[1482h]	71h	REG[14D2h]	43h	REG[1522h]	92h	REG[1572h]	D6h
REG[1484h]	14h	REG[14D4h]	44h	REG[1524h]	93h	REG[1574h]	D7h
REG[1486h]	32h	REG[14D6h]	45h	REG[1526h]	94h	REG[1576h]	D8h
REG[1488h]	81h	REG[14D8h]	46h	REG[1528h]	95h	REG[1578h]	D9h
REG[148Ah]	91h	REG[14DAh]	47h	REG[152Ah]	96h	REG[157Ah]	DAh
REG[148Ch]	A1h	REG[14DCh]	48h	REG[152Ch]	97h	REG[157Ch]	E1h
REG[148Eh]	08h	REG[14DEh]	49h	REG[152Eh]	98h	REG[157Eh]	E2h
REG[1490h]	23h	REG[14E0h]	4Ah	REG[1530h]	99h	REG[1580h]	E3h
REG[1492h]	42h	REG[14E2h]	53h	REG[1532h]	9Ah	REG[1582h]	E4h
REG[1494h]	B1h	REG[14E4h]	54h	REG[1534h]	A2h	REG[1584h]	E5h
REG[1496h]	C1h	REG[14E6h]	55h	REG[1536h]	A3h	REG[1586h]	E6h
REG[1498h]	15h	REG[14E8h]	56h	REG[1538h]	A4h	REG[1588h]	E7h
REG[149Ah]	52h	REG[14EAh]	57h	REG[153Ah]	A5h	REG[158Sh]	E8h
REG[149Ch]	D1h	REG[14ECh]	58h	REG[153Ch]	A6h	REG[158Ch]	E9h
REG[149Eh]	F0h	REG[14EEh]	59h	REG[153Eh]	A7h	REG[158Eh]	EAh
REG[14A0h]	24h	REG[14F0h]	5Ah	REG[1540h]	A8h	REG[1590h]	F1h
REG[14A2h]	33h	REG[14F2h]	63h	REG[1542h]	A9h	REG[1592h]	F2h
REG[14A4h]	62h	REG[14F4h]	64h	REG[1544h]	AAh	REG[1594h]	F3h
REG[14A6h]	72h	REG[14F6h]	65h	REG[1546h]	B2h	REG[1596h]	F4h
REG[14A8h]	82h	REG[14F8h]	66h	REG[1548h]	B3h	REG[1598h]	F5h
REG[14AAh]	09h	REG[14FAh]	67h	REG[154Ah]	B4h	REG[159Ah]	F6h
REG[14ACh]	0Ah	REG[14FCh]	68h	REG[154Ch]	B5h	REG[159Ch]	F7h
REG[14AEh]	16h	REG[14FEh]	69h	REG[154Eh]	B6h	REG[159Eh]	F8h
						REG[15A0h]	F9h
						REG[15A2h]	FAh

REG[1600 - 161Eh] DC Huffman Table No. 1 Register 0 Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
DC Huffman Table 1 Register No. 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1600-161Eh] DC Huffman Table No. 1 (Write Only)
These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 1 must be programmed as follows.

Table 10-93: DC Huffman Table No. 1 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1600h]	00h	REG[1608h]	01h	REG[1610h]	01h	REG[1618h]	00h
REG[1602h]	03h	REG[160Ah]	01h	REG[1612h]	01h	REG[161Ah]	00h
REG[1604h]	01h	REG[160Ch]	01h	REG[1614h]	01h	REG[161Ch]	00h
REG[1606h]	01h	REG[160Eh]	01h	REG[1616h]	00h	REG[161Eh]	00h

REG[1620 - 1636h] DC Huffman Table No. 1 Register 1 Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
Reserved (must be all 0)				DC Huffman Table No. 1 Register 1 bits 3-0			
7	6	5	4	3	2	1	0

REG[1620-1636h] DC Huffman Table No. 1 (Write Only)
These registers are used for the JPEG encode process only and set a group number based on the order of probability of occurrence. Only bits 3-0 are used (bits 7-4 must be set to 0). When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 1 must be programmed as follows.

Table 10-94: DC Huffman Table No. 1 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1620h]	00h	REG[1626h]	03h	REG[162Ch]	06h	REG[1632h]	09h
REG[1622h]	01h	REG[1628h]	04h	REG[162Eh]	07h	REG[1634h]	0Ah
REG[1624h]	02h	REG[162Ah]	05h	REG[1630h]	08h	REG[1636h]	0Bh

REG[1640 - 165Eh] AC Huffman Table No. 1 Register 0							
Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
AC Huffman Table No. 1 Register 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1640-165Eh] AC Huffman Table No. 1 (Write Only)
These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 1 must be programmed as follows.

Table 10-95: AC Huffman Table No. 1 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1640h]	00h	REG[1648h]	04h	REG[1650h]	07h	REG[1658h]	00h
REG[1642h]	02h	REG[164Ah]	04h	REG[1652h]	05h	REG[165Ah]	01h
REG[1644h]	01h	REG[164Ch]	03h	REG[1654h]	04h	REG[165Ch]	02h
REG[1646h]	02h	REG[164Eh]	04h	REG[1656h]	04h	REG[165Eh]	77h

REG[1660 - 17A2h] AC Huffman Table No. 1 Register 1							
Default = not applicable							Write Only
n/a							
15	14	13	12	11	10	9	8
AC Huffman Table No. 1 Register 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1660-17A2h] AC Huffman Table No. 1 (Write Only)
These registers are used for the JPEG encode process only and set a zero run length / group number based on the order of probability of occurrence. When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 1 must be programmed as follows.

Table 10-96: AC Huffman Table No. 1 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1660h]	00h	REG[16B0h]	E1h	REG[1700h]	69h	REG[1750h]	B5h
REG[1662h]	01h	REG[16B2h]	25h	REG[1702h]	6Ah	REG[1752h]	B6h
REG[1664h]	02h	REG[16B4h]	F1h	REG[1704h]	73h	REG[1754h]	B7h
REG[1666h]	03h	REG[16B6h]	17h	REG[1706h]	74h	REG[1756h]	B8h
REG[1668h]	11h	REG[16B8h]	18h	REG[1708h]	75h	REG[1758h]	B9h
REG[166Ah]	04h	REG[16BAh]	19h	REG[170Ah]	76h	REG[175Ah]	BAh
REG[166Ch]	05h	REG[16BCh]	1Ah	REG[170Ch]	77h	REG[175Ch]	C2h
REG[166Eh]	21h	REG[16BEh]	26h	REG[170Eh]	78h	REG[175Eh]	C3h
REG[1670h]	31h	REG[16C0h]	27h	REG[1710h]	79h	REG[1760h]	C4h
REG[1672h]	06h	REG[16C2h]	28h	REG[1712h]	7Ah	REG[1762h]	C5h
REG[1674h]	12h	REG[16C4h]	29h	REG[1714h]	82h	REG[1764h]	C6h
REG[1676h]	41h	REG[16C6h]	2Ah	REG[1716h]	83h	REG[1766h]	C7h
REG[1678h]	51h	REG[16C8h]	35h	REG[1718h]	84h	REG[1768h]	C8h
REG[167Ah]	07h	REG[16CAh]	36h	REG[171Ah]	85h	REG[176Ah]	C9h
REG[167Ch]	61h	REG[16CCh]	37h	REG[171Ch]	86h	REG[176Ch]	CAh
REG[167Eh]	71h	REG[16CEh]	38h	REG[171Eh]	87h	REG[176Eh]	D2h
REG[1680h]	13h	REG[16D0h]	39h	REG[1720h]	88h	REG[1770h]	D3h
REG[1682h]	22h	REG[16D2h]	3Ah	REG[1722h]	89h	REG[1772h]	D4h
REG[1684h]	32h	REG[16D4h]	43h	REG[1724h]	8Ah	REG[1774h]	D5h
REG[1686h]	81h	REG[16D6h]	44h	REG[1726h]	92h	REG[1776h]	D6h
REG[1688h]	08h	REG[16D8h]	45h	REG[1728h]	93h	REG[1778h]	D7h
REG[168Ah]	14h	REG[16DAh]	46h	REG[172Ah]	94h	REG[177Ah]	D8h
REG[168Ch]	42h	REG[16DCh]	47h	REG[172Ch]	95h	REG[177Ch]	D9h
REG[168Eh]	91h	REG[16DEh]	48h	REG[172Eh]	96h	REG[177Eh]	DAh
REG[1690h]	A1h	REG[16E0h]	49h	REG[1730h]	97h	REG[1780h]	E2h
REG[1692h]	B1h	REG[16E2h]	4Ah	REG[1732h]	98h	REG[1782h]	E3h
REG[1694h]	C1h	REG[16E4h]	53h	REG[1734h]	99h	REG[1784h]	E4h
REG[1696h]	09h	REG[16E6h]	54h	REG[1736h]	9Ah	REG[1786h]	E5h
REG[1698h]	23h	REG[16E8h]	55h	REG[1738h]	A2h	REG[1788h]	E6h
REG[169Ah]	33h	REG[16EAh]	56h	REG[173Ah]	A3h	REG[178Ah]	E7h
REG[169Ch]	52h	REG[16ECh]	57h	REG[173Ch]	A4h	REG[178Ch]	E8h
REG[169Eh]	F0h	REG[16EEh]	58h	REG[173Eh]	A5h	REG[178Eh]	E9h
REG[16A0h]	15h	REG[16F0h]	59h	REG[1740h]	A6h	REG[1790h]	EAh
REG[16A2h]	62h	REG[16F2h]	5Ah	REG[1742h]	A7h	REG[1792h]	F2h
REG[16A4h]	72h	REG[16F4h]	63h	REG[1744h]	A8h	REG[1794h]	F3h
REG[16A6h]	D1h	REG[16F6h]	64h	REG[1746h]	A9h	REG[1796h]	F4h
REG[16A8h]	0Ah	REG[16F8h]	65h	REG[1748h]	AAh	REG[1798h]	F5h
REG[16AAh]	16h	REG[16FAh]	66h	REG[174Ah]	B2h	REG[179Ah]	F6h
REG[16ACh]	24h	REG[16FCh]	67h	REG[174Ch]	B3h	REG[179Ch]	F7h
REG[16AEh]	34h	REG[16FEh]	68h	REG[174Eh]	B4h	REG[179Eh]	F8h
						REG[17A0h]	F9h
						REG[17A2h]	FAh

10.4.21 SD Memory Card Interface Registers

REG[6000h] SD Memory Card Configuration Register 0 Default = 0000h							Read/Write
n/a							Reserved
15	14	13	12	11	10	9	8
n/a				SD Memory Card Software Reset (WO)	Reserved		SD Memory Card Interface Enable
7	6	5	4	3	2	1	0

bit 8 Reserved
The default value for this bit is 0.

bit 3 SD Memory Card Software Reset (Write Only)
This bit performs a software reset of the SD Memory Card interface and resets REG[6100h] - REG[613Eh].
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, a software reset is performed.

bits 2-1 Reserved
The default value for these bits is 0.

bit 0 SD Memory Card Interface Enable
This bit enables the SD Memory Card interface. When the interface is disabled, REG[6100h] - REG[613Eh] are inaccessible and the SD Card pins (SDDAT[3:0], SDCMD, SDCLK) are forced to inputs.
When this bit = 0, the SD Memory Card interface is disabled (default).
When this bit = 1, the SD Memory Card interface is enabled.

Note
When the SD Memory Card Interface is disabled (REG[6000h] bit 0 = 0), the pull-down control bits (REG[0308h] bits 15-11 and REG[030Ah] bits 3-0) must be set when the GPIO's are outputs to avoid unnecessary current draw.

REG[6004h] SD Memory Card Configuration Register 2 Default = xxxxh							Read/Write
n/a							
15	14	13	12	11	10	9	8
SDDAT3 Status	SDDAT2 Status	SDDAT1 Status	SDDAT0 Status	SDCMD Status	SDCLK Status	SDWP Status (RO)	SDCD# Status (RO)
7	6	5	4	3	2	1	0

bit 7 SDDAT3 Status
When SDDAT3 is an input, this bit indicates the status of SDDAT3.
For Reads:
When this bit returns a 0, SDDAT3 input is low.
When this bit returns a 1, SDDAT3 input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 6 SDDAT2 Status
When SDDAT2 is an input, this bit indicates the status of SDDAT2.
For Reads:
When this bit returns a 0, SDDAT2 input is low.
When this bit returns a 1, SDDAT2 input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 5 SDDAT1 Status
When SDDAT1 is an input, this bit indicates the status of SDDAT1.
For Reads:
When this bit returns a 0, SDDAT1 input is low.
When this bit returns a 1, SDDAT1 input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 4 SDDAT0 Status
When SDDAT0 is an input, this bit indicates the status of SDDAT0.
For Reads:
When this bit returns a 0, SDDAT0 input is low.
When this bit returns a 1, SDDAT0 input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 3 SDCMD Status
When SDCMD is an input, this bit indicates the status of SDCMD.
For Reads:
When this bit returns a 0, SDCMD input is low.
When this bit returns a 1, SDCMD input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 2 SDCLK Status
When the SDCLK is an input, this bit indicates the status of SDCLK.
For Reads:
When this bit returns a 0, SDCLK input is low.
When this bit returns a 1, SDCLK input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 1 SDWP Status (Read Only)
This bit indicates the status of SDWP.
When this bit returns a 0, SDWP input is low.
When this bit returns a 1, SDWP input is high.

bit 0 SDCD# Status (Read Only)
This bit indicates the status of SDCD#.
When this bit returns a 0, SDCD# input is low.
When this bit returns a 1, SDCD# input is high.

REG[6008h] SD Memory Card Interrupt Flag Register Default = 0000h							Read Only
n/a						SDCD# Raw Status (RO)	SD Card Detect Interrupt Flag (RO)
15	14	13	12	11	10	9	8
SDCLK Change Interrupt Flag (RO)	Send Command Interrupt Flag (RO)	Receive Response Interrupt Flag (RO)	Wait Busy Interrupt Flag (RO)	Receive Data Interrupt Flag (RO)	Send Data Interrupt Flag (RO)	Send 8 Clock Interrupt Flag (RO)	Synchronous Reset Interrupt Flag (RO)
7	6	5	4	3	2	1	0

bit 9 SDCD# Raw Status (Read Only)
This bit indicates the status of the SDCD# pin.
When this bit returns a 0, SDCD# is low input.
When this bit returns a 1, SDCD# is high input.

bit 8 SD Card Detect Interrupt Flag (Read Only)
This bit indicates the status of the SD Card Detect Interrupt.
When this bit returns a 0, a SD Card Detect Interrupt has not occurred.
When this bit returns a 1, a SD Card Detect Interrupt has occurred.

bit 7 SDCLK Change Interrupt Flag (Read Only)
This bit indicates the status of the SDCLK Change Interrupt.
When this bit returns a 0, a SDCLK Change Interrupt has not occurred.
When this bit returns a 1, a SDCLK Change Interrupt has occurred.

bit 6 Send Command Interrupt Flag (Read Only)
This bit indicates the status of the Send Command Interrupt.
When this bit returns a 0, a Send Command Interrupt has not occurred.
When this bit returns a 1, a Send Command Interrupt has occurred.

bit 5 Receive Response Interrupt Flag (Read Only)
This bit indicates the status of the Receive Response Interrupt.
When this bit returns a 0, a Receive Response Interrupt has not occurred.
When this bit returns a 1, a Receive Response Interrupt has occurred.

bit 4 Wait Busy Interrupt Flag (Read Only)
This bit indicates the status of the Wait Busy Interrupt.
When this bit returns a 0, a Wait Busy Interrupt has not occurred.
When this bit returns a 1, a Wait Busy Interrupt has occurred.

bit 3 Receive Data Interrupt Flag (Read Only)
This bit indicates the status of the Receive Data Interrupt.
When this bit returns a 0, a Receive Data Interrupt has not occurred.
When this bit returns a 1, a Receive Data Interrupt has occurred.

bit 2 Send Data Interrupt Flag (Read Only)
This bit indicates the status of the Send Data Interrupt.
When this bit returns a 0, a Send Data Interrupt has not occurred.
When this bit returns a 1, a Send Data Interrupt has occurred.

bit 1 — Send 8 Clock Interrupt Flag (Read Only)
This bit indicates the status of the Send 8 Clock Interrupt.
When this bit returns a 0, a Send 8 Clock Interrupt has not occurred.
When this bit returns a 1, a Send 8 Clock Interrupt has occurred.

bit 0 — Synchronous Reset Interrupt Flag (Read Only)
This bit indicates the status of the Synchronous Reset Interrupt.
When this bit returns a 0, a Synchronous Reset Interrupt has not occurred.
When this bit returns a 1, a Synchronous Reset Interrupt has occurred.

REG[600Ah] SD Memory Card Interrupt Enable Register
Default = 0000h — Read/Write

n/a							SD Card Detect Interrupt Enable
15	14	13	12	11	10	9	8
SDCLK Change Interrupt Enable	Send Command Interrupt Enable	Receive Response Interrupt Enable	Wait Busy Interrupt Enable	Receive Data Interrupt Enable	Send Data Interrupt Enable	Send 8 Clock Interrupt Enable	Synchronous Reset Interrupt Enable
7	6	5	4	3	2	1	0

bit 8 — SD Card Detect Interrupt Enable
This bit enables the SD Card Detect Interrupt.
When this bit = 0, the SD Card Detect Interrupt is not enabled.
When this bit = 1, the SD Card Detect Interrupt is enabled.

bit 7 — SDCLK Change Interrupt Enable
This bit enables the SDCLK Change Interrupt.
When this bit = 0, the SDCLK Change Interrupt is not enabled.
When this bit = 1, the SDCLK Change Interrupt is enabled.

bit 6 — Send Command Interrupt Enable
This bit enables the Send Command Interrupt.
When this bit = 0, the Send Command Interrupt is not enabled.
When this bit = 1, the Send Command Interrupt is enabled.

bit 5 — Receive Response Interrupt Enable
This bit enables the Receive Response Interrupt.
When this bit = 0, the Receive Response Interrupt is not enabled.
When this bit = 1, the Receive Response Interrupt is enabled.

bit 4 — Wait Busy Interrupt Enable
This bit enables the Wait Busy Interrupt.
When this bit = 0, the Wait Busy Interrupt is not enabled.
When this bit = 1, the Wait Busy Interrupt is enabled.

bit 3 — Receive Data Interrupt Enable
This bit enables the Receive Data Interrupt.
When this bit = 0, the Receive Data Interrupt is not enabled.
When this bit = 1, the Receive Data Interrupt is enabled.

bit 2 — Send Data Interrupt Enable
This bit enables the Send Data Interrupt.
When this bit = 0, the Send Data Interrupt is not enabled.
When this bit = 1, the Send Data Interrupt is enabled.

bit 1 Send 8 Clock Interrupt Enable
This bit enables the Send 8 Clock Interrupt.
When this bit = 0, the Send 8 Clock Interrupt is not enabled.
When this bit = 1, the Send 8 Clock Interrupt is enabled.

bit 0 Synchronous Reset Interrupt Enable
This bit enables the Synchronous Reset Interrupt.
When this bit = 0, the Synchronous Reset Interrupt is not enabled.
When this bit = 1, the Synchronous Reset Interrupt is enabled.

REG[600Ch] SD Memory Card Interrupt Clear Register Default = xxxxh							Write Only
n/a							SD Card Detect Interrupt Clear (WO)
15	14	13	12	11	10	9	8
SDCLK Change Interrupt Clear (WO)	Send Command Interrupt Clear (WO)	Receive Response Interrupt Clear (WO)	Wait Busy Interrupt Clear (WO)	Receive Data Interrupt Clear (WO)	Send Data Interrupt Clear (WO)	Send 8 Clock Interrupt Clear (WO)	Synchronous Reset Interrupt Clear (WO)
7	6	5	4	3	2	1	0

bit 8 SD Card Detect Interrupt Clear (Write Only)
This bit enables the SD Card Detect Interrupt.
When this bit = 0, there is no hardware effect.
When this bit = 1, the SD Card Detect Interrupt is cleared.

bit 7 SDCLK Change Interrupt Clear (Write Only)
This bit enables the SDCLK Change Interrupt.
When this bit = 0, there is no hardware effect.
When this bit = 1, the SDCLK Change Interrupt is cleared.

bit 6 Send Command Interrupt Clear (Write Only)
This bit enables the Send Command Interrupt.
When this bit = 0, there is no hardware effect.
When this bit = 1, the Send Command Interrupt is cleared.

bit 5 Receive Response Interrupt Clear (Write Only)
This bit enables the Receive Response Interrupt.
When this bit = 0, there is no hardware effect.
When this bit = 1, the Receive Response Interrupt is cleared.

bit 4 Wait Busy Interrupt Clear (Write Only)
This bit enables the Wait Busy Interrupt.
When this bit = 0, there is no hardware effect.
When this bit = 1, the Wait Busy Interrupt is cleared.

bit 3 Receive Data Interrupt Clear (Write Only)
This bit enables the Receive Data Interrupt.
When this bit = 0, there is no hardware effect.
When this bit = 1, the Receive Data Interrupt is cleared.

bit 2 Send Data Interrupt Clear (Write Only)
This bit enables the Send Data Interrupt.
When this bit = 0, there is no hardware effect.
When this bit = 1, the Send Data Interrupt is cleared.

bit 1 Send 8 Clock Interrupt Clear (Write Only)
This bit enables the Send 8 Clock Interrupt.
When this bit = 0, there is no hardware effect.
When this bit = 1, the Send 8 Clock Interrupt is cleared.

bit 0 Synchronous Reset Interrupt Clear (Write Only)
This bit enables the Synchronous Reset Interrupt.
When this bit = 0, there is no hardware effect.
When this bit = 1, the Synchronous Reset Interrupt is cleared.

REG[6100h] SD Memory Card Control Register 0 Default = 0031h							Read/Write
n/a							
15	14	13	12	11	10	9	8
SDCLK Divide Select bits 3-0				Reserved		SD Card Interrupt Enable	SD Card Interrupt Flag
7	6	5	4	3	2	1	0

bits 7-4 SDCLK Divide Select bits [3:0]
These bits select the divide ratio for the SD Memory Card clock (SDCLK signal). The clock source for the SD Memory Card clock is the system clock. When the divide ratio is changed, write a 1 to the SDCLK Change Start bit (REG[6104h] bit 7 = 1) and wait for the change to take effect (REG[6104h] bit 7 = 0) before using the SD Memory Clock interface.

Table 10-97: SD Memory Card Clock Divide Ratio Selection

REG[6100h] bits 7-4	SD Memory Card Clock Divide Ratio
0000b	Reserved
0001b	2:1 (see Note)
0010b	3:1 (see Note)
0011b (default)	4:1
0101b	62:1
1001b	130:1
1010b	131:1
1110b	255:1
1111b	256:1
others	Reserved

Note
SD Memory Card Clock Divide Ratio must be configured such that the resulting SDCLK frequency does not exceed 13.75MHz (see Section 7.6.2, “SD Memory Card Clock Output”).

The following table provides some examples of typical SD Memory Card clock configurations.

Table 10-98: System Clock Frequency and SD Card Clock

System Clock Frequency	REG[6100h] bits 7-4	
	Identification Mode	Data Transfer Mode
~52MHz	1010 (~396KHz)	0011 (~13MHz)
~55MHz	1110 (~215KHz)	0011 (~13.75MHz Max)

bits 3-2 Reserved
The default value for these bits is 0.

bit 1 SD Card Interrupt Enable
This bit controls the SD Memory Card Interrupt (SDCD#) and masks the SD Card Interrupt Status bit (REG[0A00h] bit 7).
When this bit = 0, the interrupt is disabled (default).
When this bit = 1, the interrupt is enabled.

bit 0 SD Card Interrupt Flag
This bit indicates that a SD Card Interrupt has occurred (change in card detect, SDCD#).
This bit is not masked by the SD Card Interrupt Enable bit (REG[6100h] bit 1).
For Reads:
When this bit returns a 0, the interrupt has not occurred.
When this bit returns a 1, the interrupt has occurred (SDCD# signal has changed).
For Writes:
When a 0 is written to this bit, the flag is cleared.
When a 1 is written to this bit, there is no hardware effect.

Note
This bit is cleared on a SD card software reset (REG[6104h] bit 0 = 1).

REG[6102h] SD Memory Card Control Register 1 Default = 00x1h							Read/Write
n/a							
15	14	13	12	11	10	9	8
SDWP Status (RO)	SDGPO Inverted Data	Reserved			Response Data Length	Multi Block Enable	Data Bus Width
7	6	5	4	3	2	1	0

bit 7 SDWP Status (Read Only)
This bit indicates the status of SDWP (write protect) which is sampled by the clock.
When this bit returns a 0, SDWP is low input (card is write protected or no card is present).
When this bit returns a 1, SDWP is high input.

bit 6 SDGPO Inverted Data
This bit determines the polarity of SDGPO.
When this bit = 0, SDGPO is forced high.
When this bit = 1, SDGPO is forced low (default).

bits 5-3 Reserved
The default value for these bits is 0.

bit 2 Response Data Length
This bit determines the length of the response from the memory card, in bits. This bit must be set for the appropriate length before initiating a Receive Response Start (REG[6104h] bit 5).
When this bit = 0, the response length is 48 bits (default) and SD Memory Card Response Registers A - F (REG[6134h] - REG[613Eh] are used.
When this bit = 1, the response length is 136 bits and SD Memory Card Response Registers 0 - F (REG[6120h] - REG[613Eh] are used.

bit 1 Multi Block Enable
This bit controls the multi block read/write function. This bit must be set for the appropriate multi block setting before initiating a Receive Data Start (REG[6104h] bit 3) or a Send Data Start (REG[6104h] bit 2).
When this bit = 0, multi block reads/writes are disabled (default).
When this bit = 1, multi block reads/writes are enabled.

bit 0 Data Bus Width
This bit specifies the SD Memory Card data bus width, in bits, and should be set according to the SD Card. This bit must be set appropriately before initiating a Receive Data Start (REG[6104h] bit 3) or a Send Data Start (REG[6104h] bit 2).
When this bit = 0, the data bus width is four bits and SDDAT[3:0] are used to transfer data.
When this bit = 1, the data bus width is one bit and SDDAT0 is used to transfer data (default).

REG[6104h] SD Memory Card Function Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
SDCLK Change Start	Send Command Start	Receive Response Start	Wait Busy Start	Receive Data Start	Send Data Start	Send 8 Clock Start	Synchronous Reset Start
7	6	5	4	3	2	1	0

bit 7 SDCLK Change Start
This bit controls changes to the SD Memory Card clock (SDCLK) frequency.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the change to the SD Memory Card clock frequency begins
For Reads:
When this bit returns a 0, the change to the SD Memory Card clock frequency has completed.
When this bit returns a 1, the change to the SD Memory Card clock frequency has not completed yet.

The typical sequence for changing the SD Memory Card clock is as follows.

1. Select the SDCLK Divide Ratio using REG[6100h] bits 7-4.
2. Write a 1 to the SDCLK Change Start bit.
3. Wait for the SDCLK Change Start bit to return a 0. Once this bit returns a 0, the change is effective and the interface can be enabled.

bit 6 Send Command Start
This bit controls the transmission of commands and parameters to the SD Memory Card.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the command/parameter stored in REG[610Ch], REG[6110h] - REG[6116h] is transmitted on SDCMD.
For Reads:
When this bit returns a 0, the command/parameter transmission has completed.
When this bit returns a 1, the command/parameter is still being transmitted.

bit 5 Receive Response Start
This bit controls the reception of responses from the SD Memory Card. The Response Data Length bit (REG[6102h] bit 2) must be set according to the expected response length before starting to receive the response using this bit.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the response reception begins on SDCMD and can be read from REG[6120h] - REG[613Eh].
For Reads:
When this bit returns a 0, the response reception has completed.
When this bit returns a 1, the response reception is still being received.

bit 4 Wait Busy Start
This bit controls the reception of wait busy signals from the SD Memory Card.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the wait busy reception begins.
For Reads:
When this bit returns a 0, the wait busy reception has completed.
When this bit returns a 1, the wait busy reception is still being received.

bit 3 Receive Data Start
This bit controls the reception of data from the SD Memory Card. The Response Data Length bit (REG[6102h] bit 2) and the Multi Block Enable bit (REG[6102h] bit 1) must be set according to the expected response type before starting to receive the response.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the data reception begins on the SDDAT lines and is read from REG[6118h] - REG[611Eh].
For Reads:
When this bit returns a 0, the data reception has completed.
When this bit returns a 1, the data reception is still being received.

bit 2 Send Data Start
This bit controls the transmission of data to the SD Memory card. The Multi Block Enable bit (REG[6102h] bit 1) must be set according to the type of data to be sent before starting to transmit the data.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the data written to REG[6118h] - REG[611E] is transmitted on the SDDAT lines.
For Reads:
When this bit returns a 0, the data transmission has completed.
When this bit returns a 1, the data transmission is still being sent.

bit 1 Send 8 Clock Start
This bit controls the transmission of eight clocks to the SD Memory Card.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the transmission begins.
For Reads:
When this bit returns a 0, the transmission has completed.
When this bit returns a 1, the eight clocks are still being transmitted.

bit 0 Synchronous Reset Start
This bit performs a synchronous reset of the SD Memory Card interface registers REG[6104h] and REG[6106h]. This reset has no effect on the following SD Memory Card registers - REG[6100h] - REG[6102h] and REG[6108h] - REG[613Eh].
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, a synchronous reset begins.
For Reads:
When this bit returns a 0, the synchronous reset has completed.
When this bit returns a 1, the synchronous reset is still taking place.

REG[6106h] SD Memory Card Status Register Default = 00x0h							Read Only
n/a							
15	14	13	12	11	10	9	8
Reserved	SDCD# Status	Data Writable	Data Readable	Data CRC Error	Response Over Error	Response CRC Error	Time Over Error
7	6	5	4	3	2	1	0

Note
This register is read only and must not be written to at any time.

bit 7 Reserved
The default value for this bit is 0.

bit 6 SDCD# Status (Read Only)
This bit indicates the status of the SDCD# pin as taken with the sampling clock.
When this bit returns a 0, SDCD# is low input.
When this bit returns a 1, SDCD# is high input.

bit 5 Data Writable (Read Only)
This bit indicates whether data can be written to the SD Memory Card.
When this bit returns a 0, writing data is not possible.
When this bit returns a 1, writing data is possible.

bit 4 Data Readable (Read Only)
This bit indicates whether data can be read from the SD Memory Card.
When this bit returns a 0, reading data is not possible.
When this bit returns a 1, reading data is possible.

bit 3 Data CRC Error (Read Only)
This bit indicates when a data CRC error has occurred.
When this bit returns a 0, a CRC error has not occurred.
When this bit returns a 1, a CRC error has occurred.

bit 2 Response Over Error (Read Only)
This bit indicates that the response from the SD Memory Card has exceeded more than 64 clocks.
When this bit returns a 0, the response is not more than 64 clocks.
When this bit returns a 1, the response is more than 64 clocks.

bit 1 Response CRC Error (Read Only)
This bit indicates that a CRC error has occurred in the response from the SD Memory Card.
When this bit returns a 0, a CRC error has not occurred.
When this bit returns a 1, a CRC error has occurred.

bit 0 Time Over Error (Read Only)
This bit indicates that a Time Over Error has occurred during data transmission.
When this bit returns a 0, a time over error has not occurred.
When this bit returns a 1, a time over error has occurred.

REG[6108h] SD Memory Card Data Length Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
Reserved						Data Length bits 9-8	
7	6	5	4	3	2	1	0

REG[610Ah] SD Memory Card Data Length Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
Data Length bits 7-0							
7	6	5	4	3	2	1	0

REG[6108h] bits 7-2 Reserved
The default value for these bits is 0.

REG[6108h] bits 1-0
REG[610Ah] bits 7-0 Data Length bits [9:0]
These bits specify the SD Memory Card data length.

The data length must be programmed such that the following formula is valid.

$$1 \le \text{Data Length} \le 512$$

REG[610Ch] SD Memory Card Command Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
Reserved		Command bits 5-0					
7	6	5	4	3	2	1	0

bits 7-6 Reserved
The default value of these bits is 0.

bits 5-0 Command bits [5:0]
These bits specify the command to be transmitted to the SDCMD signal when data is transmitted.

REG[610Eh] SD Memory Card Timer Register							
Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Timer Value bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Timer Value bits [7:0]
These bits specify the timer value used to limit the length of data and command accesses to/from the SD Memory Card. An error occurs when the timer value is exceeded by any SD Memory Card access. To determine the nature of the error, check the status bits in the SD Memory Card Status register (REG[6106h].

Timer limit = REG[610Eh] bits 7-0 x SD Memory Card clock cycle (time)

REG[6110h] SD Memory Card Parameter Register 0							
Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Parameter 0 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Parameter 0 bits [7:0]
These bits specify Parameter 0 which is used when data is transmitted to the SDCMD signal. Data is transmitted as follows: Command, Parameter 0, Parameter 1, Parameter 2, and Parameter 3.

REG[6112h] SD Memory Card Parameter Register 1							
Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Parameter 1 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Parameter 1 bits [7:0]
These bits specify Parameter 1 which is used when data is transmitted to the SDCMD signal. Data is transmitted as follows: Command, Parameter 0, Parameter 1, Parameter 2, and Parameter 3.

REG[6114h] SD Memory Card Parameter Register 2							
Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Parameter 2 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Parameter 2 bits [7:0]
These bits specify Parameter 2 which is used when data is transmitted to the SDCMD signal. Data is transmitted as follows: Command, Parameter 0, Parameter 1, Parameter 2, and Parameter 3.

REG[6116h] SD Memory Card Parameter Register 3 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Parameter 3 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Parameter 3 bits [7:0]
These bits specify Parameter 3 which is used when data is transmitted to the SDCMD signal. Data is transmitted as follows: Command, Parameter 0, Parameter 1, Parameter 2, and Parameter 3.

REG[6118h - 611Eh] SD Memory Card Data Registers Default = 00xxh							Read/Write
n/a							
15	14	13	12	11	10	9	8
Write Data / Read Data							
7	6	5	4	3	2	1	0

REG[6118h] bits 7-0
REG[611Ah] bits 7-0
REG[611Ch] bits 7-0
REG[611Eh] bits 7-0

Write Data / Read Data
These bits specify the read/write data to be received from/transmitted to the SD Memory Card. When the Data Writable bit returns a 0 (REG[6106h] bit 5 = 0), writing data to the SD Memory Card is not possible. When the Data Readable bit returns a 0 (REG[6106h] bit 4 = 0), reading data from the SD Memory Card is not possible.

REG[6120h] SD Memory Card Response Register 0 Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response 0 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 0 bits [7:0]
These bits contain the Response 0 data received from the SD Memory Card at the SDCMD signal.

REG[6122h] SD Memory Card Response Register 1 Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response 1 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 1 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 1 data received from the SD Memory Card at the SDCMD signal.

REG[6124h] SD Memory Card Response Register 2 Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response 2 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 2 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 2 data received from the SD Memory Card at the SDCMD signal.

REG[6126h] SD Memory Card Response Register 3 Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response 3 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 3 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 3 data received from the SD Memory Card at the SDCMD signal.

REG[6128h] SD Memory Card Response Register 4 Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response 4 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 4 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 4 data received from the SD Memory Card at the SDCMD signal.

REG[612Ah] SD Memory Card Response Register 5 Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response 5 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 5 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 5 data received from the SD Memory Card at the SDCMD signal.

REG[612Ch] SD Memory Card Response Register 6 Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response 6 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 6 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 6 data received from the SD Memory Card at the SDCMD signal.

REG[612Eh] SD Memory Card Response Register 7 Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response 7 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 7 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 7 data received from the SD Memory Card at the SDCMD signal.

REG[6130h] SD Memory Card Response Register 8 Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response 8 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 8 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 8 data received from the SD Memory Card at the SDCMD signal.

REG[6132h] SD Memory Card Response Register 9 Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response 9 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 9 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 9 data received from the SD Memory Card at the SDCMD signal.

REG[6134h] SD Memory Card Response Register A Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response A bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response A bits [7:0]
These bits contain the Response A data received from the SD Memory Card at the SDCMD signal.

REG[6136h] SD Memory Card Response Register B Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response B bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response B bits [7:0]
These bits contain the Response B data received from the SD Memory Card at the SDCMD signal.

REG[6138h] SD Memory Card Response Register C Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response C bits 7-0							
7	6	5	4	3	2	1	0

its 7-0 Response C bits [7:0]
These bits contain the Response C data received from the SD Memory Card at the SDCMD signal.

REG[613Ah] SD Memory Card Response Register D Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response D bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response D bits [7:0]
These bits contain the Response D data received from the SD Memory Card at the SDCMD signal.

REG[613Ch] SD Memory Card Response Register E Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response E bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response E bits [7:0]
These bits contain the Response E data received from the SD Memory Card at the SDCMD signal.

REG[613Eh] SD Memory Card Response Register F Default = 00FFh							Read Only
n/a							
15	14	13	12	11	10	9	8
Response F bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response F bits [7:0]
These bits contain the Response F data received from the SD Memory Card at the SDCMD signal.

10.4.22 2D BitBLT Registers

Note
The S1D13719 BitBLT engine does not support 32 bpp .

REG[8000h] BitBLT Control Register 0
Default = 0000h — Write Only

n/a							
15	14	13	12	11	10	9	8
BitBLT Reset	n/a						BitBLT Enable
7	6	5	4	3	2	1	0

bit 7 — BitBLT Reset (Write Only)
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the 2D BitBLT engine is reset.

bit 0 — BitBLT Enable (Write Only)
When a 0 is written to this bit, the 2D BitBLT operation is terminated.
When a 1 is written to this bit, the 2D BitBLT operation is started.

REG[8002h] BitBLT Control Register 1
Default = 0000h — Read/Write

Reserved							
15	14	13	12	11	10	9	8
n/a					Color Format Select	Destination Linear Select	Source Linear Select
7	6	5	4	3	2	1	0

bits 15-8 — Reserved
The default value for these bits is 0.

bit 2 — BitBLT Color Format Select
This bit selects the color format that the 2D operation is applied to.
When this bit = 0, 8 bpp (256 color) format is selected.
When this bit = 1, 16 bpp (64K color) format is selected.

Note
The BitBLT engine does not support color depths of 32 bpp.

bit 1 — BitBLT Destination Linear Select
When this bit = 0, the Destination BitBLT is stored as a rectangular region of memory.
When this bit = 1, the Destination BitBLT is stored as a contiguous linear block of memory.

The BitBLT Memory Address Offset register (REG[8014h]) determines the address offset from the start of one line to the next line.

bit 0 — BitBLT Source Linear Select
When this bit = 0, the Source BitBLT is stored as a rectangular region of memory.
When this bit = 1, the Source BitBLT is stored as a contiguous linear block of memory.

The BitBLT Memory Address Offset register (REG[8014h]) determines the address offset from the start of one line to the next line.

REG[8004h] BitBLT Status Register 0
Default = 0000h — Read Only

n/a			Reserved				
15	14	13	12	11	10	9	8
Reserved	FIFO Not Empty	FIFO Half Full	FIFO Full Status	n/a			BitBLT Busy Status
7	6	5	4	3	2	1	0

bits 12-8 — Reserved
The default value for these bits is 0.

bit 7 — Reserved
The default value for these bits is 0.

bit 6 — BitBLT FIFO Not-Empty Status (Read Only)
This bit indicates if the BitBLT FIFO is empty or not.
When this bit = 0, the BitBLT FIFO is empty.
When this bit = 1, the BitBLT FIFO has at least one entry.
To reduce system memory read latency, software can monitor this bit prior to a BitBLT read burst operation.

The following table shows the number of words available in the BitBLT FIFO under different status conditions.

Table 10-99: Possible BitBLT FIFO Writes

BitBLT Status Register (REG[8004h])			Word Writes Available
FIFO Not Empty Status	FIFO Half Full Status	FIFO Full Status	
0	0	0	16
1	0	0	8
1	1	0	up to 8
1	1	1	0 (do not write)

bit 5 — BitBLT FIFO Half Full Status (Read Only)
This bit indicates whether the BitBLT FIFO is more or less than half full.
When this bit = 0, the BitBLT FIFO is less than half full.
When this bit = 1, the BitBLT FIFO is half full or greater than half full.

bit 4 BitBLT FIFO Full Status (Read Only)
This bit indicates whether the BitBLT FIFO is full or not. **This bit must be confirmed as not full (0) before writing to the BitBLT FIFO.**
When this bit = 0, the BitBLT FIFO is not full.
When this bit = 1, the BitBLT FIFO is full.

bit 0 BitBLT Busy Status (Read Only)
This bit indicates the state of the current BitBLT operation.
When this bit = 0, the BitBLT operation is complete.
When this bit = 1, the BitBLT operation is in progress.

REG[8006h] is Reserved

This register is Reserved and should not be written.

REG[8008h] BitBLT Command Register 0							
Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a				BitBLT Operation bits 3-0			
7	6	5	4	3	2	1	0

bits 3-0 BitBLT Operation bits [3:0]
These bits specify the 2D Operation to be performed

Note
.When the Indirect Interface Mode, BitBLT Operation is limited (Read BitBLT).

Table 10-100: BitBLT Operation Selection

BitBLT Operation bits 3-0	BitBLT Operation	Direct I/F	Indirect I/F
0000b	Reserved	—	—
0001b	Read BitBLT	support	not support
0010b	Move BitBLT in positive direction with ROP	support	support
0011b	Move BitBLT in negative direction with ROP	support	support
0100b	Reserved	—	—
0101b	Transparent Move BitBLT in positive direction	support	support
0110b	Pattern Fill with ROP	support	support
0111b	Pattern Fill with transparency	support	support
1000b	Reserved	—	—
1001b	Reserved	—	—
1010b	Move BitBLT with Color Expansion	support	support
1011b	Move BitBLT with Color Expansion and transparency	support	support
1100b	Solid Fill	support	support
Other combinations	Reserved	—	—

REG[800Ah] BitBLT Command Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a				BitBLT ROP Code bits 3-0			
7	6	5	4	3	2	1	0

bits 3-0 BitBLT Raster Operation Code/Color Expansion bits [3:0]
These bits determine the ROP Code for Write BitBLT and Move BitBLT. Bits 2-0 also specify the start bit position for Color Expansion.

Table 10-101: BitBLT ROP Code/Color Expansion Function Selection

BitBLT ROP Code bits 3-0	Boolean Function for Write BitBLT and Move BitBLT	Boolean Function for Pattern Fill	Start Bit Position for Color Expansion
0000b	0 (Blackness)	0 (Blackness)	bit 0
0001b	~S . ~D or ~(S + D)	~P . ~D or ~(P + D)	bit 1
0010b	~S . D	~P . D	bit 2
0011b	~S	~P	bit 3
0100b	S . ~D	P . ~D	bit 4
0101b	~D	~D	bit 5
0110b	S ^ D	P ^ D	bit 6
0111b	~S + ~D or ~(S . D)	~P + ~D or ~(P . D)	bit 7
1000b	S . D	P . D	bit 0
1001b	~(S ^ D)	~(P ^ D)	bit 1
1010b	D	D	bit 2
1011b	~S + D	~P + D	bit 3
1100b	S	P	bit 4
1101b	S + ~D	P + ~D	bit 5
1110b	S + D	P + D	bit 6
1111b	1 (Whiteness)	1 (Whiteness)	bit 7

Note
S = Source, D = Destination, P = Pattern.

REG[800Ch] BitBLT Source Start Address Register 0
Default = 0000h Read/Write

BitBLT Source Start Address bits 15-8							
15	14	13	12	11	10	9	8
BitBLT Source Start Address bits 7-0							
7	6	5	4	3	2	1	0

REG[800Eh] BitBLT Source Start Address Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
			BitBLT Source Start Address bits 20-16				
7	6	5	4	3	2	1	0

REG[800Eh] bits 4-0
REG[800Ch] bits 15-0 BitBLT Source Start Address bits [20:0]

These bits specify the source start address for the BitBLT operation.
If data is sourced from the CPU, then bit 0 is used for byte alignment within a 16-bit word and the other address bits are ignored. In pattern fill operation, the BitBLT Source Start Address is defined by the following equation.

Value programmed to the Source Start Address Register =
Pattern Base Address + Pattern Line Offset + Pixel Offset.

The following table shows how Source Start Address Register is defined for 8 and 16 bpp color depths.

Table 10-102: BitBLT Source Start Address Selection

Color Format	Pattern Base Address [20:0]	Pattern Line Offset [2:0]	Pixel Offset [3:0]
8 bpp	BitBLT Source Start Address [20:6]	BitBLT Source Start Address [5:3]	BitBLT Source Start Address [2:0]
16 bpp	BitBLT Source Start Address [20:7]	BitBLT Source Start Address [6:4]	BitBLT Source Start Address [3:0]

REG[8010h] BitBLT Destination Start Address Register 0 Default = 0000h							Read/Write
BitBLT Destination Start Address bits 15-8							
15	14	13	12	11	10	9	8
BitBLT Destination Start Address bits 7-0							
7	6	5	4	3	2	1	0

REG[8012h] BitBLT Destination Start Address Register 1 Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a			BitBLT Destination Start Address bits 20-16				
7	6	5	4	3	2	1	0

REG[8012h] bits 4-0
REG[8010h] bits 15-0 BitBLT Destination Start Address bits [20:0]
These bits specify the destination start address for the BitBLT operation.

REG[8014h] BitBLT Memory Address Offset Register Default = 0000h							Read/Write
n/a					BitBLT Memory Address Offset bits 10-8		
15	14	13	12	11	10	9	8
BitBLT Memory Address Offset bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 BitBLT Memory Address Offset bits [10:0]
These bits are the display's 11-bit address offset from the starting word of line *n* to the starting word of line *n + 1*. They are used only for address calculation when the BitBLT is configured as a rectangular region of memory. They are not used for the displays.

REG[8018h] BitBLT Width Register Default = 0000h							Read/Write
n/a						BitBLT Width bits 9-8	
15	14	13	12	11	10	9	8
BitBLT Width bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 BitBLT Width bits [9:0]
These bits determine the BitBLT width in pixels.
BitBLT width in pixels = (REG[8018h] bits 9-0) + 1

REG[801Ch] BitBLT Height Register Default = 0000h							Read/Write
n/a						BitBLT Height bits 9-8	
15	14	13	12	11	10	9	8
BitBLT Height bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 BitBLT Height bits [9:0]
These bits determine the BitBLT height in lines.
BitBLT height in lines = (REG[801Ch] bits 9-0) + 1

REG[8020h] BitBLT Background Color Register Default = 0000h							Read/Write
BitBLT Background Color bits 15-8							
15	14	13	12	11	10	9	8
BitBLT Background Color bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 BitBLT Background Color bits [15:0]
These bits specify the BitBLT background color for Color Expansion or key color for Transparent BitBLT. For 16 bpp color depths (REG[8002h] bit 4 = 1), bits 15-0 are used. For 8 bpp color depths (REG[8002h] bit 4 = 0), bits 7-0 are used.

REG[8024h] BitBLT Foreground Color Register Default = 0000h							Read/Write
BitBLT Foreground Color bits 15-8							
15	14	13	12	11	10	9	8
BitBLT Foreground Color bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 BitBLT Foreground Color bits [15:0]
These bits specify the BitBLT foreground color for Color Expansion or Solid Fill. For 16 bpp color depths (REG[8002h] bit 4 = 1), bits 15-0 are used. For 8 bpp color depths (REG[8002h] bit 4 = 0), bits 7-0 are used.

REG[8030h] BitBLT Interrupt Status Register Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a							BitBLT Operation Complete Flag
7	6	5	4	3	2	1	0

bit 0 BitBLT Operation Complete Flag
This bit is set when the BitBLT operation is finished. This bit is masked by REG[8032h] bit 0.
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the flag is cleared.

REG[8032h] BitBLT Interrupt Control Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a							BitBLT Operation Complete Interrupt Enable
7	6	5	4	3	2	1	0

bit 0 BitBLT Operation Complete Interrupt Enable
This bit determines whether an interrupt is generated when the current BitBLT operation finishes.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

REG[10000h] 2D BitBLT Data Memory Mapped Region Register
Default = not applicable Read/Write

BitBLT Data bits 15-8							
15	14	13	12	11	10	9	8
BitBLT Data bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 BitBLT Data bits [15:0]
This register specifies the BitBLT data when a Direct Interface is selected (CNF[4:2]).

11 Power Save Modes

11.1 Power-On/Power-Off Sequence

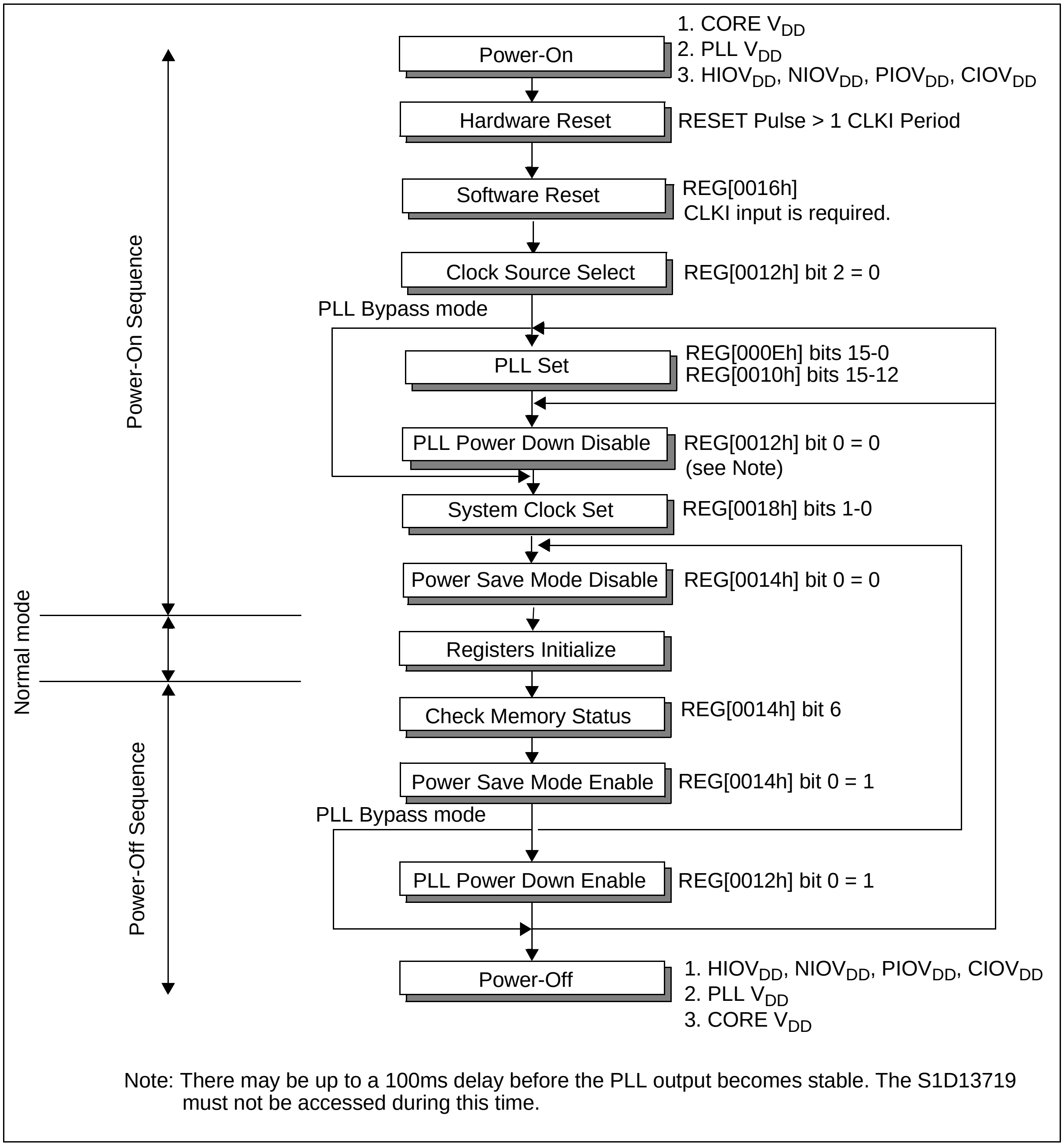


Figure 11-1: Power-On/Power-Off Sequence

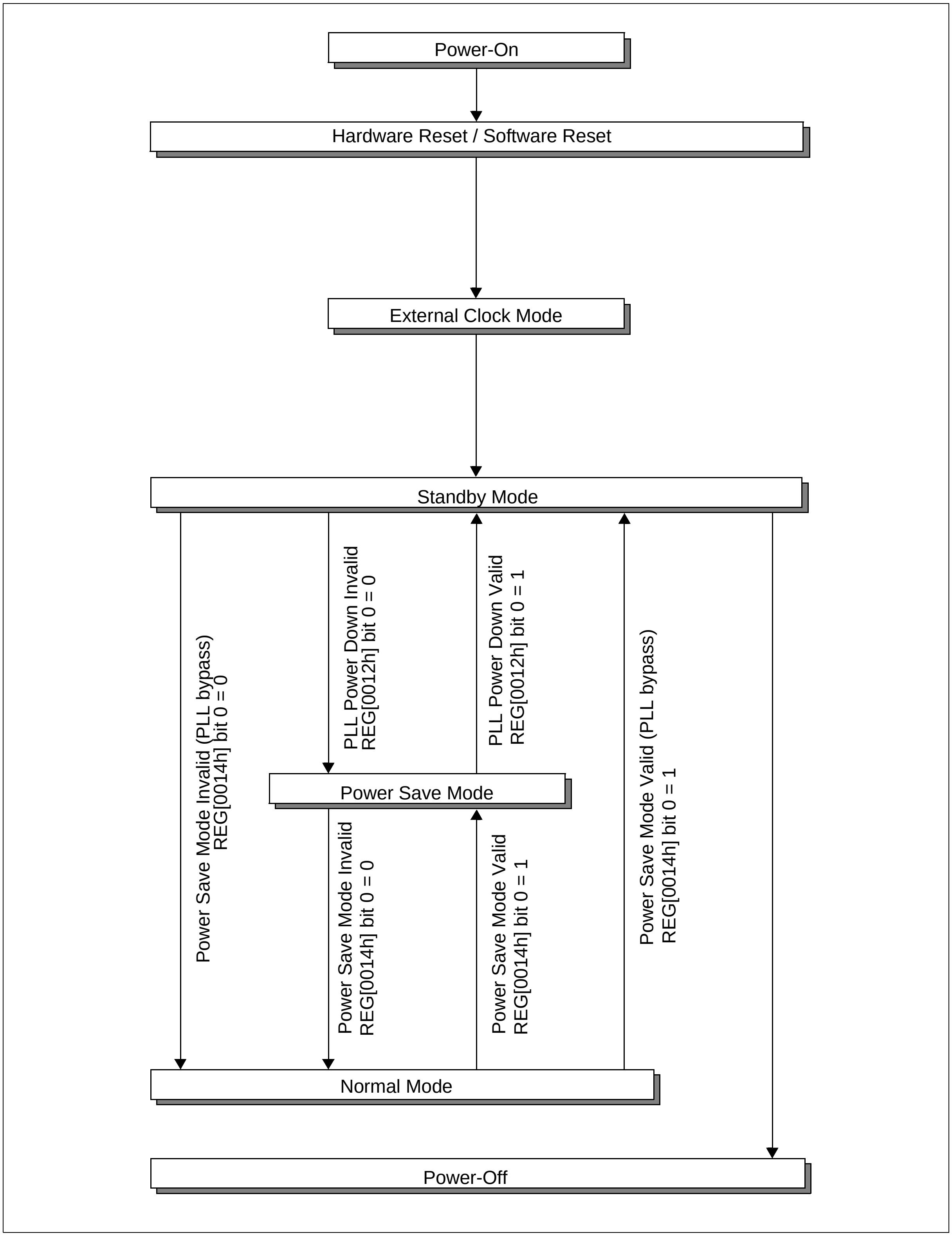


Figure 11-2: Power Modes

11.1.1 Power-On

When powering-on the S1D13719, the following sequence must be used unless all power is active within 10 ms.

1. $COREV_{DD}$ On
2. $PLLV_{DD}$ On
3. $HIOV_{DD}$, $PIOV_{DD}$, CIO1/CIO2 V_{DD} On

11.1.2 Reset

After power-on, an active low hardware reset pulse, which is one external clock cycle (CLKI) in length, must be input to the S1D13719 RESET# pin. All registers, including the Clock Setting registers (REG[000Eh] - REG[0018h]) are reset by a hardware reset. After releasing the RESET# signal, the Clock Setting registers are immediately accessible.

A software reset is enabled by writing to REG[0016h]. All registers beyond REG[0018h] are reset to their default values by a software reset (REG[0000h] - REG[0018h] are not reset). After a software reset, the registers cannot be accessed for 4 external clock cycles (CLKI).

Note

Power save mode must be enabled (REG[0014h] bit 0 = 1) **before** performing a software reset. After performing the software reset, wait a minimum of 100ms before disabling power save mode (REG[0014h] bit 0 = 0).

11.1.3 Standby Mode

Standby Mode offers the lowest power consumption because all internal clock supplies are stopped and the PLL is disabled. Once the PLL is disabled (REG[0012h] bit 0 = 1), wait a minimum delay of 100s **before** stopping CLKI. This mode must be entered before turning off the power supplies or setting the PLL registers.

11.1.4 Power Save Mode

Power Save Mode stops all internal clock supplies. This mode must be entered before setting the System Clock Setting register (REG[0018h]). Also, there may be up to a 100ms delay before the PLL output becomes stable after it is enabled. The S1D1719 should be in Power Save Mode during this time.

11.1.5 Normal Mode

All functions are available in Normal Mode. However, clocks to modules that are not in use are dynamically stopped. Before enabling Power Save Mode (REG[0014] bit 0 = 1) from Normal Mode, confirm that the memory controller is idle (REG[0014h] bit 6 = 1).

11.1.6 Power-Off

When powering-off the S1D13719, the following sequence must be used.

1. HIOV$_{DD}$, PIOV$_{DD}$, CIO1,2V$_{DD}$ Off
2. PLLV$_{DD}$ Off
3. COREV$_{DD}$ Off

11.2 Power Save Mode Function

Table 11-1: Power Save Mode Function Selection

Item		Reset State	Power Save Mode	Normal Mode
IO (Register) Access Possible?	REG[0000h-0018h], REG[0300h-030Eh]	Yes	Yes	Yes
	All other registers	No	No	Yes
Memory Access Possible?		No	No	Yes
Look-Up Table Registers Access Possible?		No	No	Yes
Display Active?		No	No	Yes
LCD1, LCD2 Interface Outputs and GPIO Pins configured for Panel Support	FPCS1#	Inactive	Inactive	Active
	FPCS2#, FPSO, FPSCLK when (REG[0032h] bits 1,0 = 00b or 10b)	FPCS2# inactive, FPSO and FPSCLK forced low	FPCS2# inactive, FPSO forced low and FPSCLK see note 1	Active
	FPCS2#, FPSO, FPSCLK when (REG[0032h] bits 1,0 not equal to 00b or 10b)	FPCS2# inactive, FPSO and FPSCLK forced low	FPCS2# inactive, FPSO forced low and FPSCLK see note 1	Active
	All other pins	Forced Low	Forced Low	Active
GPIO Pins configured as GPIOs	CNF2 = 1	Input	GPIO State	GPIO State
	CNF2 = 0	Forced Low	GPO State	GPO State
Camera Interface Pins		Forced Low	Forced Low	Active
System Clock		Forced Low	Active	Active
Pixel Clock		Forced Low	Forced Low	Active
Serial Clock	For the LCD2 Serial Panel I/F setting (REG[0032h] bits 1,0 = 00b or 10b)	Inactive	Active	Active
	For all other settings	Forced Low	Forced Low	Active
Camera1, Camera2 Clock		Forced Low	Keeps same state as when entering Power Save	Active
JPEG Module	REG[0980] bit 0 = 0	Inactive	Inactive	Inactive
	REG[0980] bit 0 = 1	Inactive	Inactive	Active
BitBLT Module		Inactive	Inactive	Active

1. The state of the FPSCLK pin when entering Power Save mode depends on which panel is active as follows.

Table 11-2: FPSCLK Level During Power Save

Mode	REG[0032h] bits 1-0	Active Panel	FPSCLK Level in Power Save Mode
1	00b	LCD1	as set by REG[0054h] bits 1-0
		LCD2	as set by REG[005Ch] bits 1-0
2	10b	LCD1	Low
		LCD2	as set by REG[005Ch] bits 1-0
3	11b	LCD1	Low
		LCD2	Low
4	01b	LCD1	as set by REG[0054h] bits 1-0
		LCD2	Low

12 Display Modes

12.1 Display Modes

The S1D13719 supports the following combination of LCD panels and display modes. For modes 1 and 4, the LCD1 panel cannot be displayed while the LCD2 panel is refreshed. For modes 2 and 3, the LCD1 and LCD2 panels cannot be refreshed at the same time.

Table 12-1: Display Modes

Display Mode	LCD1 Panel	LCD2 Panel	REG[0032h] bits 1-0
1	RGB	Serial	00b
4	RGB	Parallel	01b
2	Parallel	Serial	10b
3	Parallel	Parallel	11b

12.2 Color Depths

Both RGB format and YUV format image data can be stored in the display buffer, with up to 13609216 colors (24 bpp) being simultaneously displayed for the YUV format image data.

Table 12-2: Color Resolution 1

Format	Color Depth	Main Window Display	PIP$^+$ Window Display	Display Image
RGB 3:3:2	8 bpp	available	available	RGB Input
RGB 5:6:5	16 bpp	available	available	JPEG/Camera/RGB Input
RGB 6:6:6	18 bpp	available	available	JPEG/Camera/RGB Input
YUV 4:2:2	24 bpp	not available	available	JPEG/Camera/YUV Input

Table 12-3: Color Resolution 2

Format	SwivelView	Mirror	Pixel Doubling	Zoom	Registers
RGB 3:3:2	available	available	available	not available	REG[0200h] ～ [0233h]
RGB 5:6:5	available	available	available	not available	REG[0200h] ～ [0233h]
RGB 6:6:6	available	available	available	not available	REG[0200h] ～ [0233h]
YUV 4:2:2	available	available	available	available	REG[0234h] ～ [023Fh]

12.3 Look-up Table (LUT) Architecture

The S1D13719 is designed with two Look-up Tables (LUTs). LUT1 is used for the main window and LUT2 is used for the PIP$^+$ window. LUT1 supports color depths of 8 bpp and 16 bpp. LUT2 supports color depths of 8 bpp and 16 bpp. Common LUT data can be used in 16 bpp.

The number of LUT elements changes depending on the color depth and the LUT used as follows. For further details, see the example diagrams for the specified color depth for each LUT.

Table 12-4: LUT Architecture Summary

LUT Used	Color Depth	RGB Format	LUT Elements Used		
			Red	Green	Blue
LUT1	8 bpp	8-bit direct index	256	256	256
	16 bpp	5:6:5	32	64	32
LUT2	8 bpp	3:3:2[1]	8	8	4
	16 bpp	5:6:5[1]	32	64	32

Note

For 8 bpp and 16 bpp color depths using LUT2, the data stored in the display buffer is expanded to 6:6:6 format after the LUT by adding the appropriate LSB data. For more information see, Section 12.3.2, “LUT2 (PIP+ Window) for 8bpp Architecture” and Section 12.3.4, “LUT2 (PIP+ Window) for 16 bpp Architecture”.

12.3.1 LUT1 (Main Window) for 8bpp Architecture

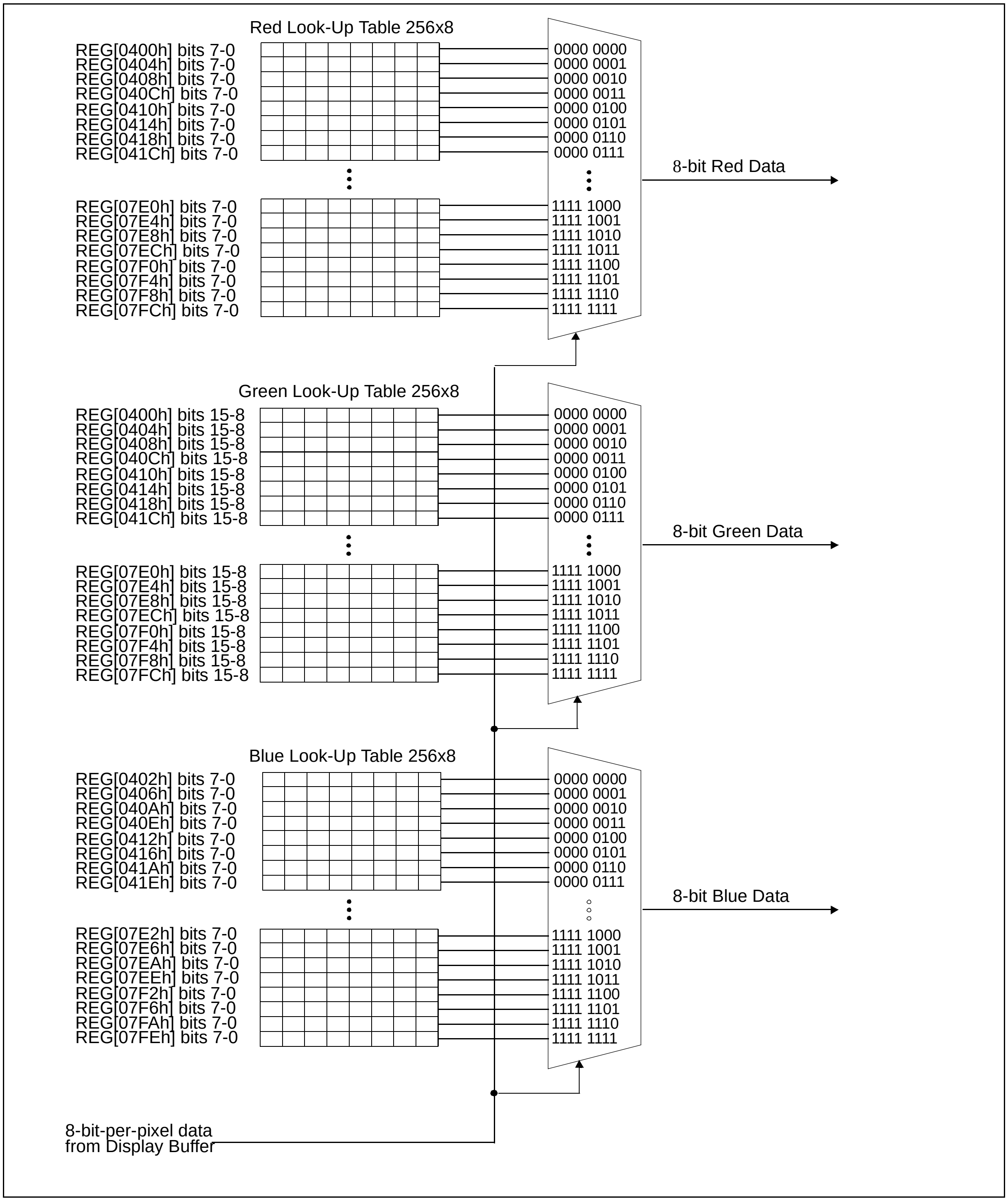


Figure 12-1: LUT1 (8 bpp) Architecture

12.3.2 LUT2 (PIP+ Window) for 8bpp Architecture

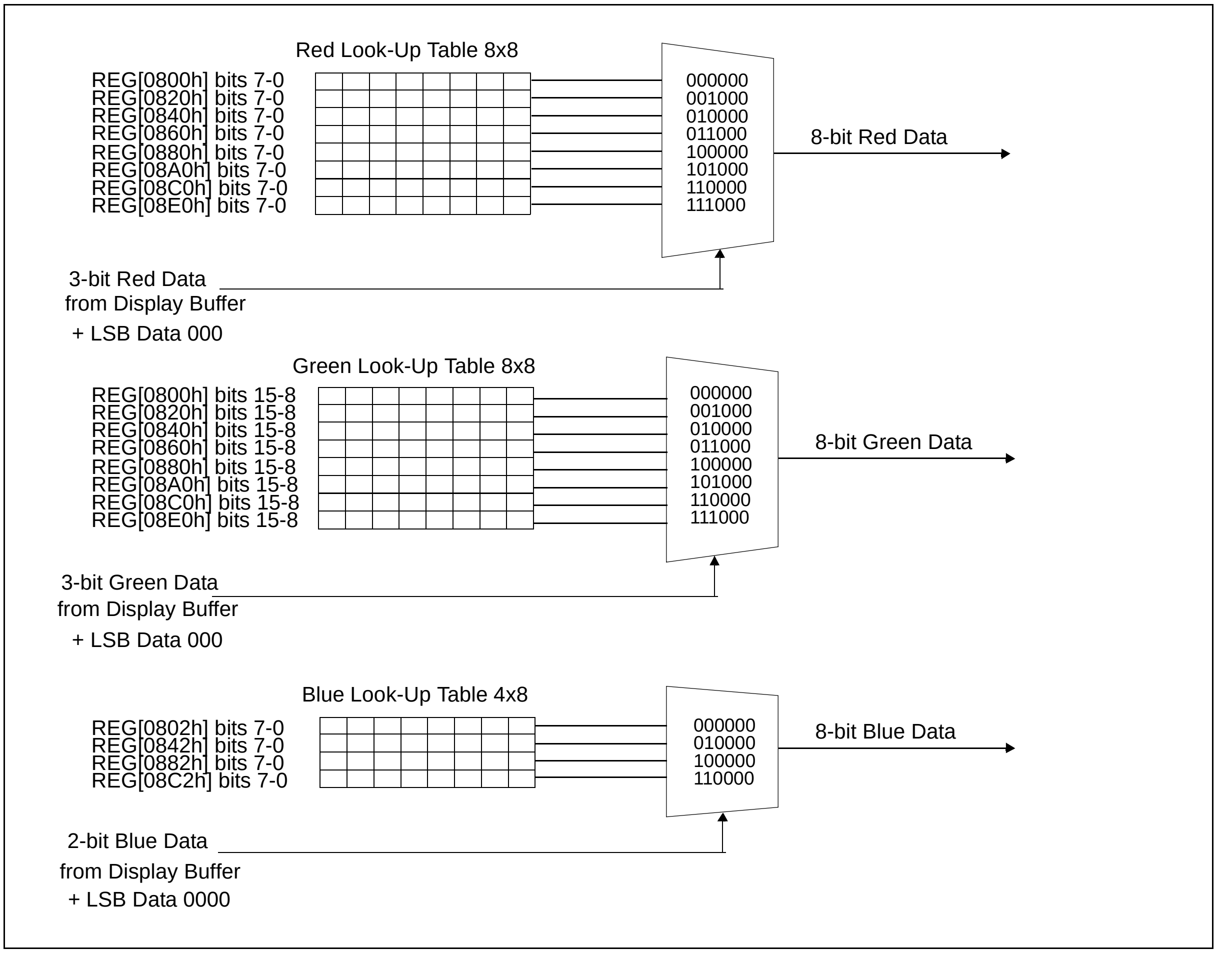


Figure 12-2: LUT2 (8 bpp) Architecture

12.3.3 LUT1 (Main Window) for 16 bpp Architecture

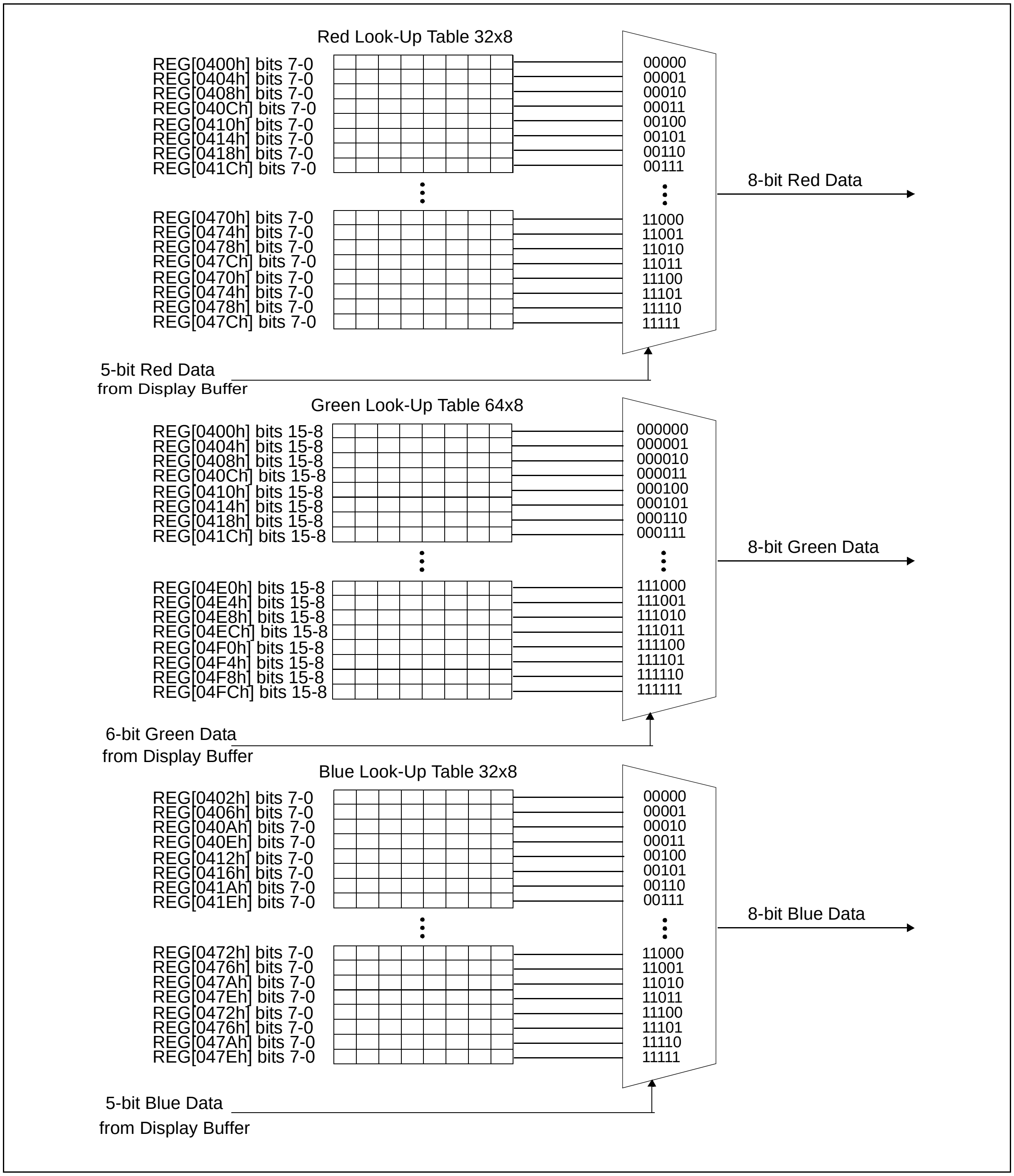


Figure 12-3: LUT1 (16 bpp) Architecture

12.3.4 LUT2 (PIP+ Window) for 16 bpp Architecture

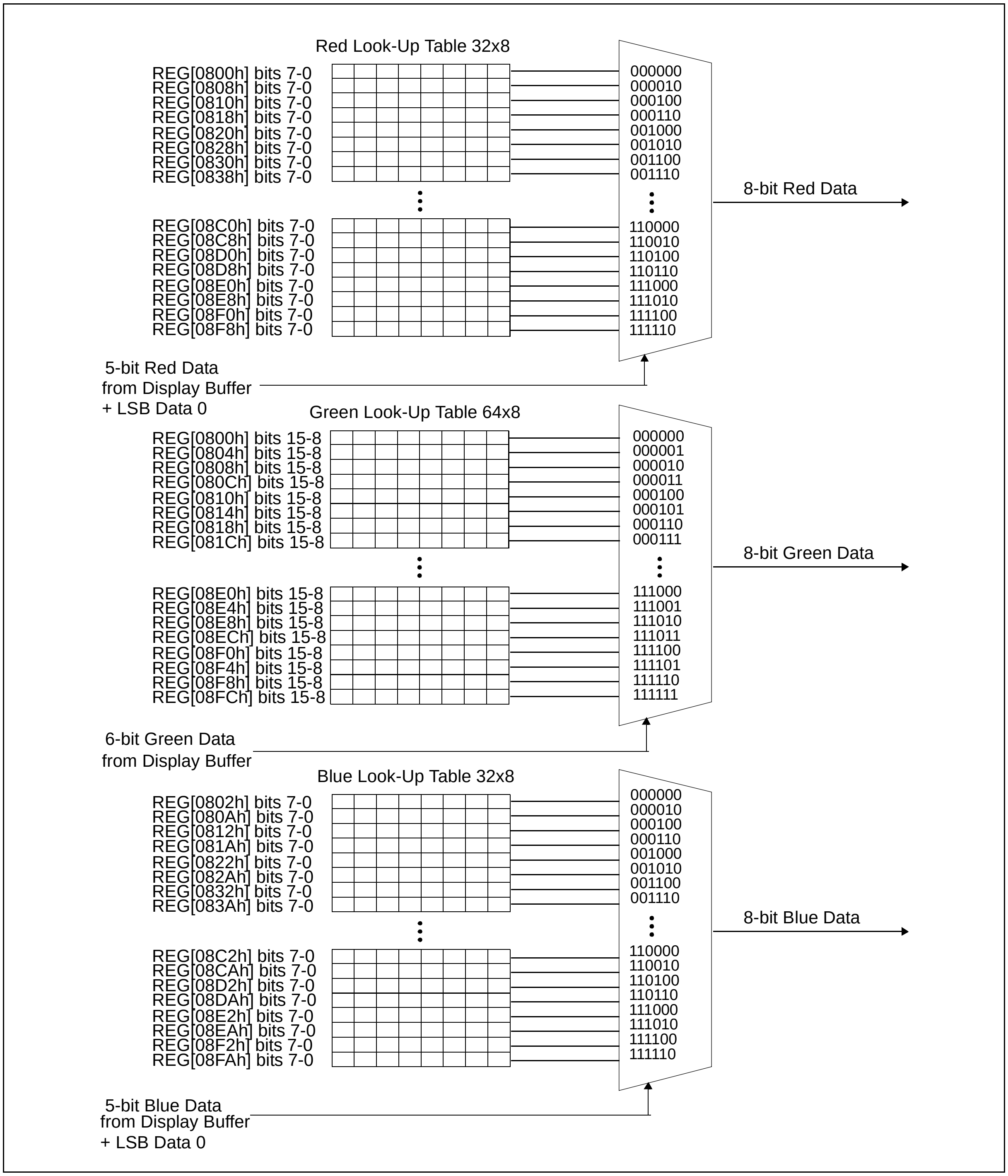


Figure 12-4: LUT2 (16 bpp) Architecture

12.3.5 Bit Cover When LUT Bypassed

When the LUT is bypassed, 8 bpp and 16 bpp data are not indexed using the LUT. The data is expanded to 24 bpp (or bit covered) by copying the MSB to the LSBs as follows.

When the LUT is bypassed, data from the YRC2 (YUV to RGB Converter 2) is output without any changes.

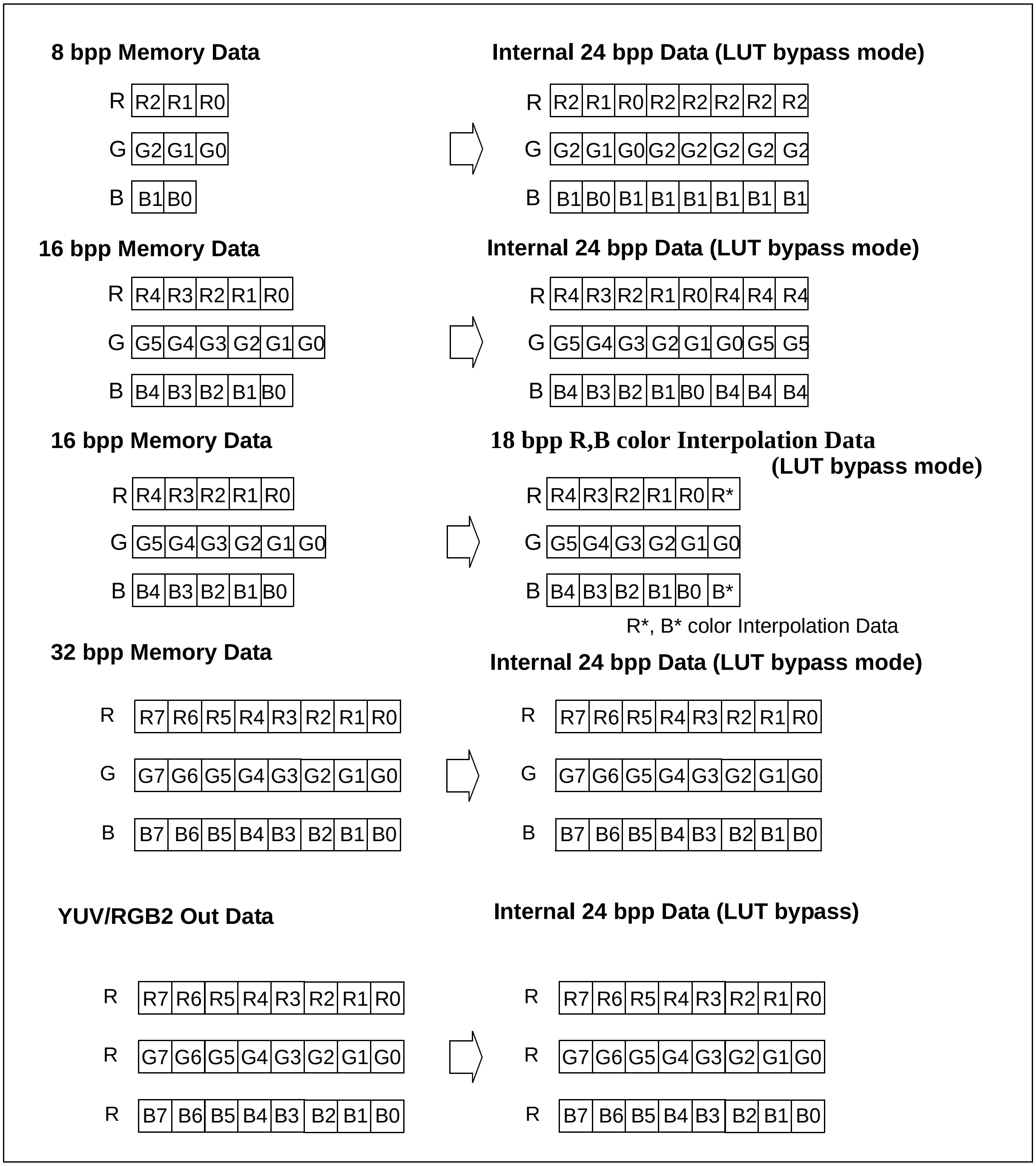


Figure 12-5: Bit Cover when LUT is bypassed

12.3.6 LCD Output Data

The LCD output data format differs depending on the data bus width of the connected LCD panel and the mode used. When data is output to the panel, the least significant bits of the internal 8:8:8 data are truncated.

12.4 Image Data Format

This section shows the image data format for 8 bpp/16 bpp/18 bpp/24 bpp color depths.

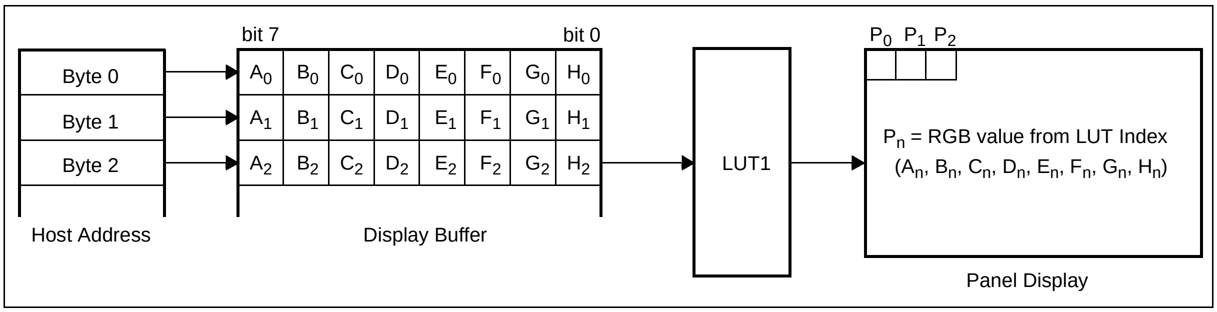


Figure 12-6: LUT1 8 bpp Mode

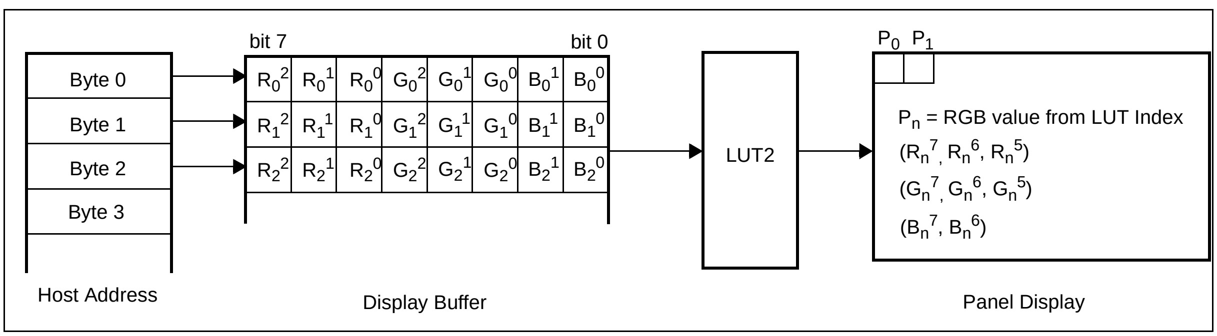


Figure 12-7: LUT2 8 bpp Mode

12.4.1 16 Bpp Mode (LUT is used)

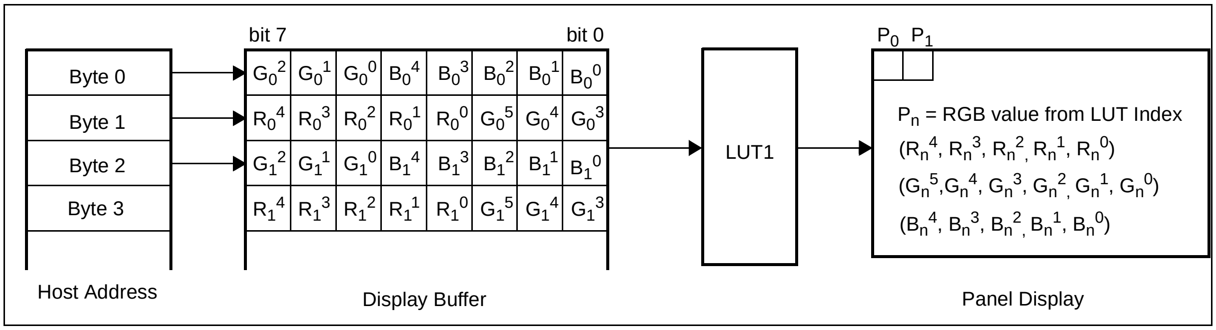


Figure 12-8: LUT1 16 bpp Mode

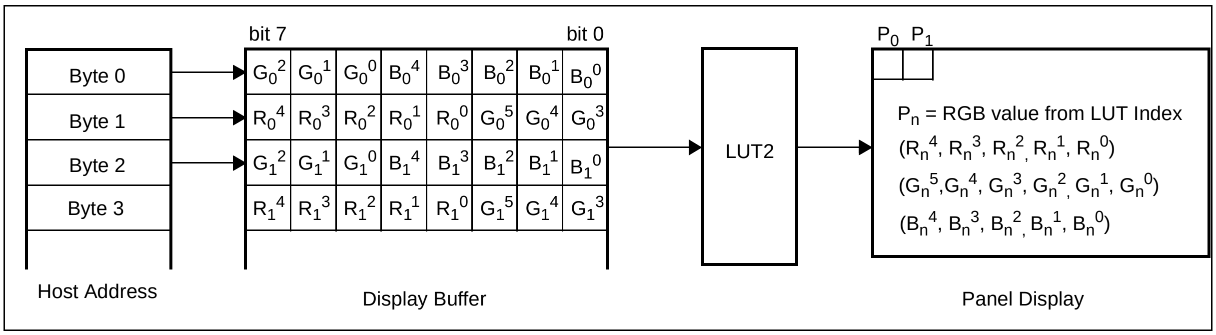


Figure 12-9: LUT2 16 bpp Mode

12.4.2 8 Bpp Mode (LUT is bypassed)

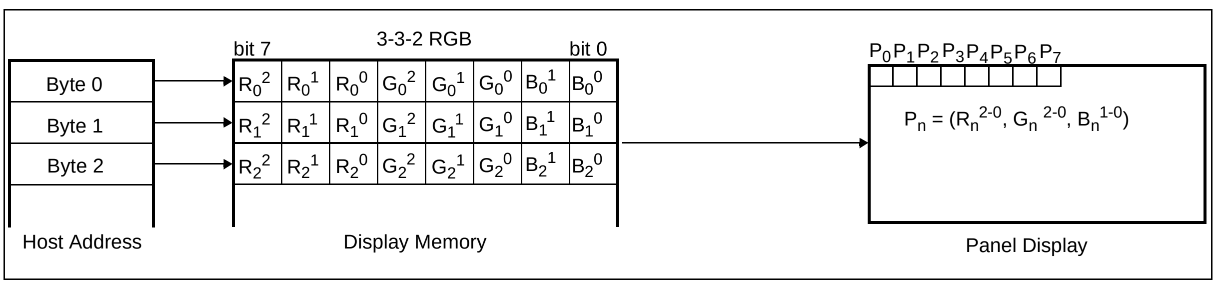


Figure 12-10: LUT 8 bpp Bypass Mode

12.4.3 16 Bpp Mode (LUT is bypassed)

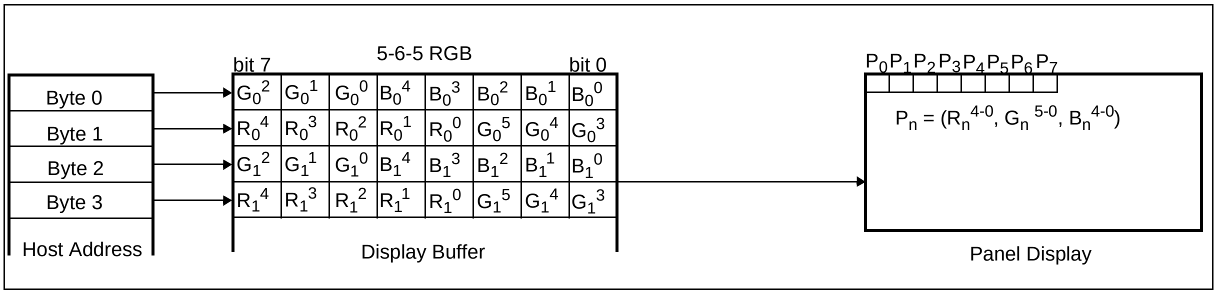


Figure 12-11: LUT 16 bpp Bypass Mode

12.4.4 32 Bpp Mode (LUT is bypassed)

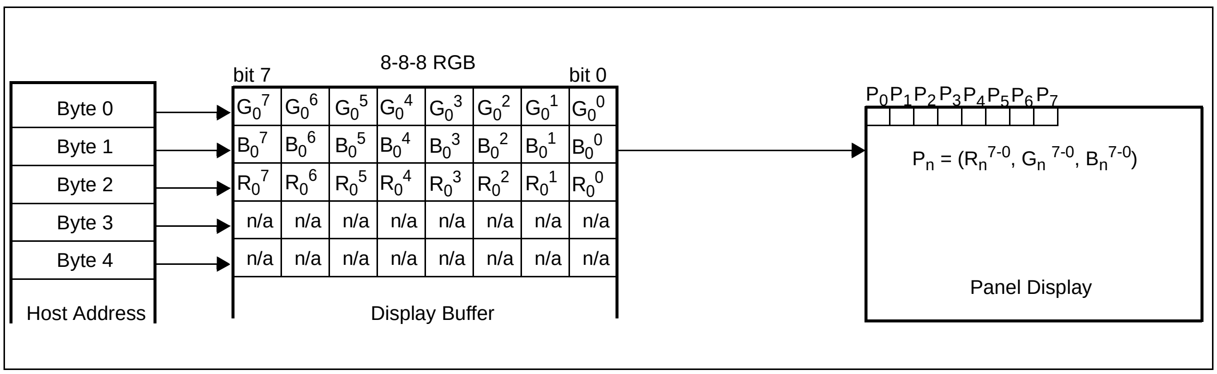


Figure 12-12: LUT for 32 bpp Bypass Mode

12.4.5 24 Bpp (YUV 4:2:2) Mode (LUT is bypassed)

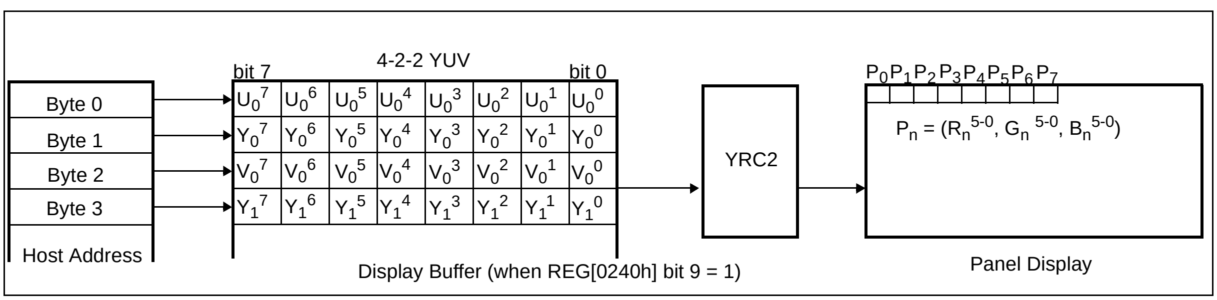


Figure 12-13: LUT 24 bpp Bypass Mode (YUV 4:2:2)

12.5 Memory Data Format

This section shows the format for image data stored in memory.

12.5.1 Format RGB 3:3:2

bit 15															bit 0
R_1^2	R_1^1	R_1^0	G_1^2	G_1^1	G_1^0	B_1^1	B_1^0	R_0^2	R_0^1	R_0^0	G_0^2	G_0^1	G_0^0	B_0^1	B_0^0
R_3^2	R_3^1	R_3^0	G_3^2	G_3^1	G_3^0	B_3^1	B_3^0	R_2^2	R_2^1	R_2^0	G_2^2	G_2^1	G_2^0	B_2^1	B_2^0
R_5^2	R_5^1	R_5^0	G_5^2	G_5^1	G_5^0	B_5^1	B_5^0	R_4^2	R_4^1	R_4^0	G_4^2	G_4^1	G_4^0	B_4^1	B_4^0
R_7^2	R_7^1	R_7^0	G_7^2	G_7^1	G_7^0	B_7^1	B_7^0	R_6^2	R_6^1	R_6^0	G_6^2	G_6^1	G_6^0	B_6^1	B_6^0

Display Buffer

Figure 12-14: Memory Data (RGB 3:2:2)

12.5.2 Format RGB 5:6:5

bit 15															bit 0
R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1
R_1^5	R_1^4	R_1^3	R_1^2	R_1^1	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1
R_2^5	R_2^4	R_2^3	R_2^2	R_2^1	G_2^5	G_2^4	G_2^3	G_2^2	G_2^1	G_2^0	B_2^5	B_2^4	B_2^3	B_2^2	B_2^1
R_3^5	R_3^4	R_3^3	R_3^2	R_3^1	G_3^5	G_3^4	G_3^3	G_3^2	G_3^1	G_3^0	B_3^5	B_3^4	B_3^3	B_3^2	B_3^1

Display Buffer

Figure 12-15: Memory Data (RGB 5:6:5)

12.5.3 Format YUV 4:2:2

bit 15															bit 0
Y_0^7	Y_0^6	Y_0^5	Y_0^4	Y_0^3	Y_0^2	Y_0^1	Y_0^0	U_0^7	U_0^6	U_0^5	U_0^4	U_0^3	U_0^2	U_0^1	U_0^0
Y_1^7	Y_1^6	Y_1^5	Y_1^4	Y_1^3	Y_1^2	Y_1^1	Y_1^0	V_0^7	V_0^6	V_0^5	V_0^4	V_0^3	V_0^2	V_0^1	V_0^0
Y_2^7	Y_2^6	Y_2^5	Y_2^4	Y_2^3	Y_2^2	Y_2^1	Y_2^0	U_1^7	U_1^6	U_1^5	U_1^4	U_1^3	U_1^2	U_1^1	U_1^0
Y_3^7	Y_3^6	Y_3^5	Y_3^4	Y_3^3	Y_3^2	Y_3^1	Y_3^0	V_1^7	V_1^6	V_1^5	V_1^4	V_1^3	V_1^2	V_1^1	V_1^0

Display Buffer (Ref.REG[0240h] bit 9)

Figure 12-16: Memory Data (YUV 4:2:2)

12.6 LCD Refresh

The S1D13719 can control LCD refresh (data transfer to the LCD) when serial/parallel interface LCD panels are selected. The LCD refresh can be synchronized with the FPVIN1/FPVIN2 input.

12.6.1 LCD Frame Transfer

The S1D13719 can transfer one LCD data frame using a software trigger (see REG[003Ah] bit 0). The following procedure should be used to initiate a LCD frame transfer.

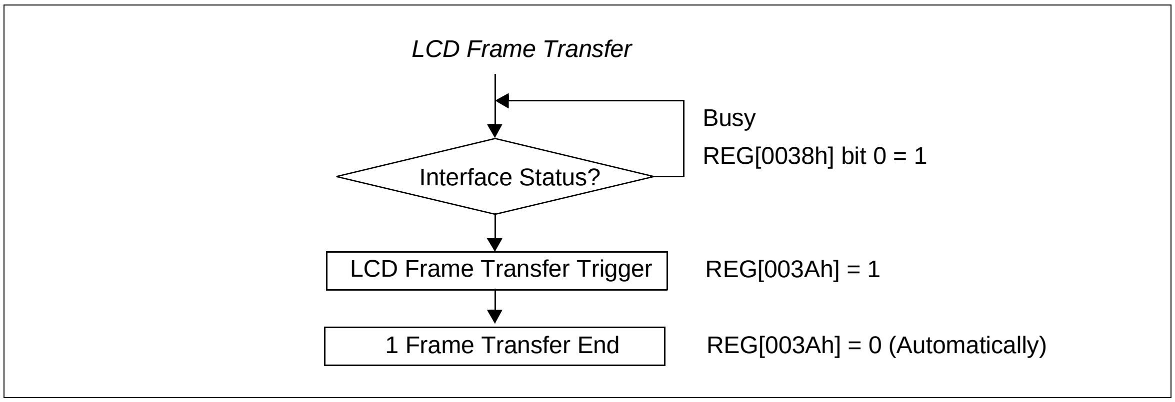


Figure 12-17: LCD Frame Transfer Procedure

12.6.2 LCD Auto Transfer

The S1D13719 can transfer LCD data frames automatically triggered by camera frame input. In this mode (see REG[003Ch] bit 0), each time a frame is received from the camera, the image data is automatically transferred. When this mode is enabled, the camera input frame cycle must be set longer than the LCD frame cycle. The following procedure should be used to enable automatic LCD frame transfers.

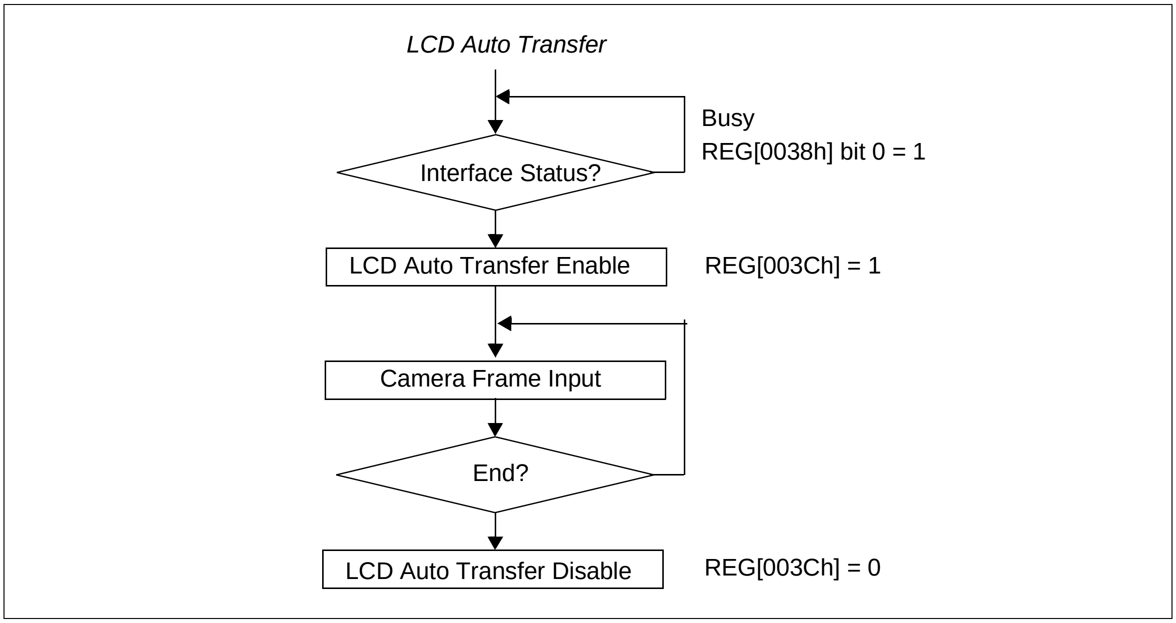


Figure 12-18: LCD Auto Transfer Procedure

12.6.3 LCD Frame Synchronization

Parallel interface LCD panel can begin the data transfer synchronizing with the input signal of the FPVIN1/FPVIN2 pins. Moreover, it is possible to output it to the LCD panel by making the FPVIN1/FPVIN2 pins an output signal.

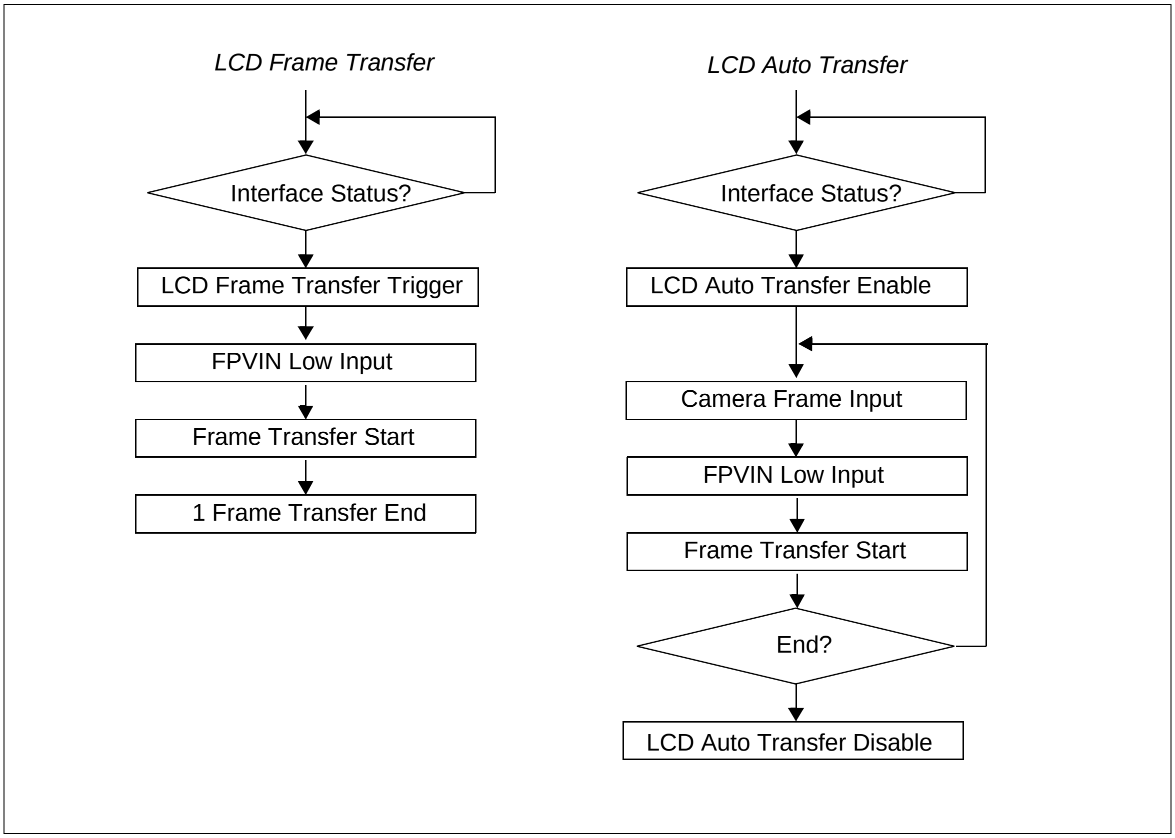
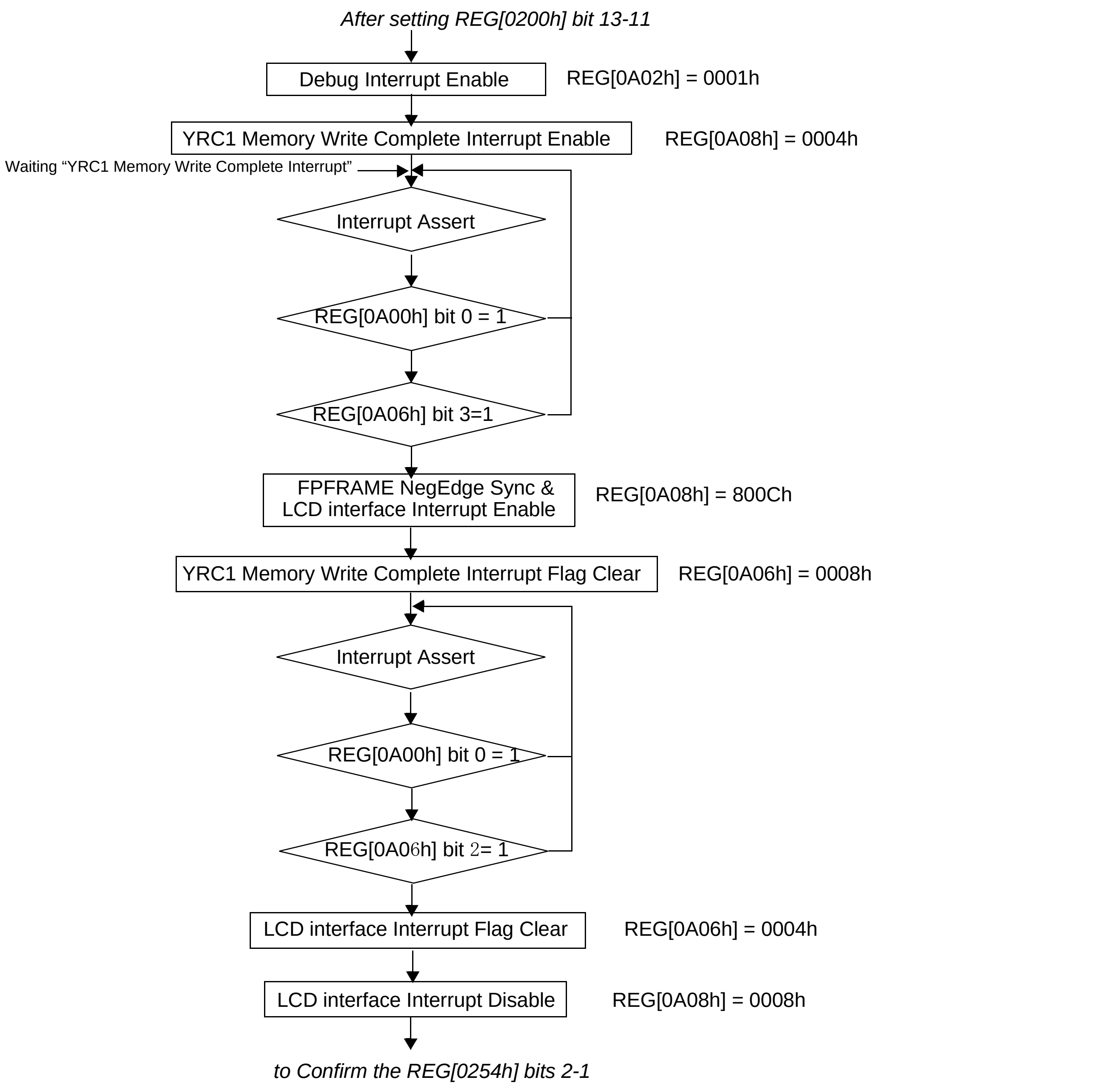
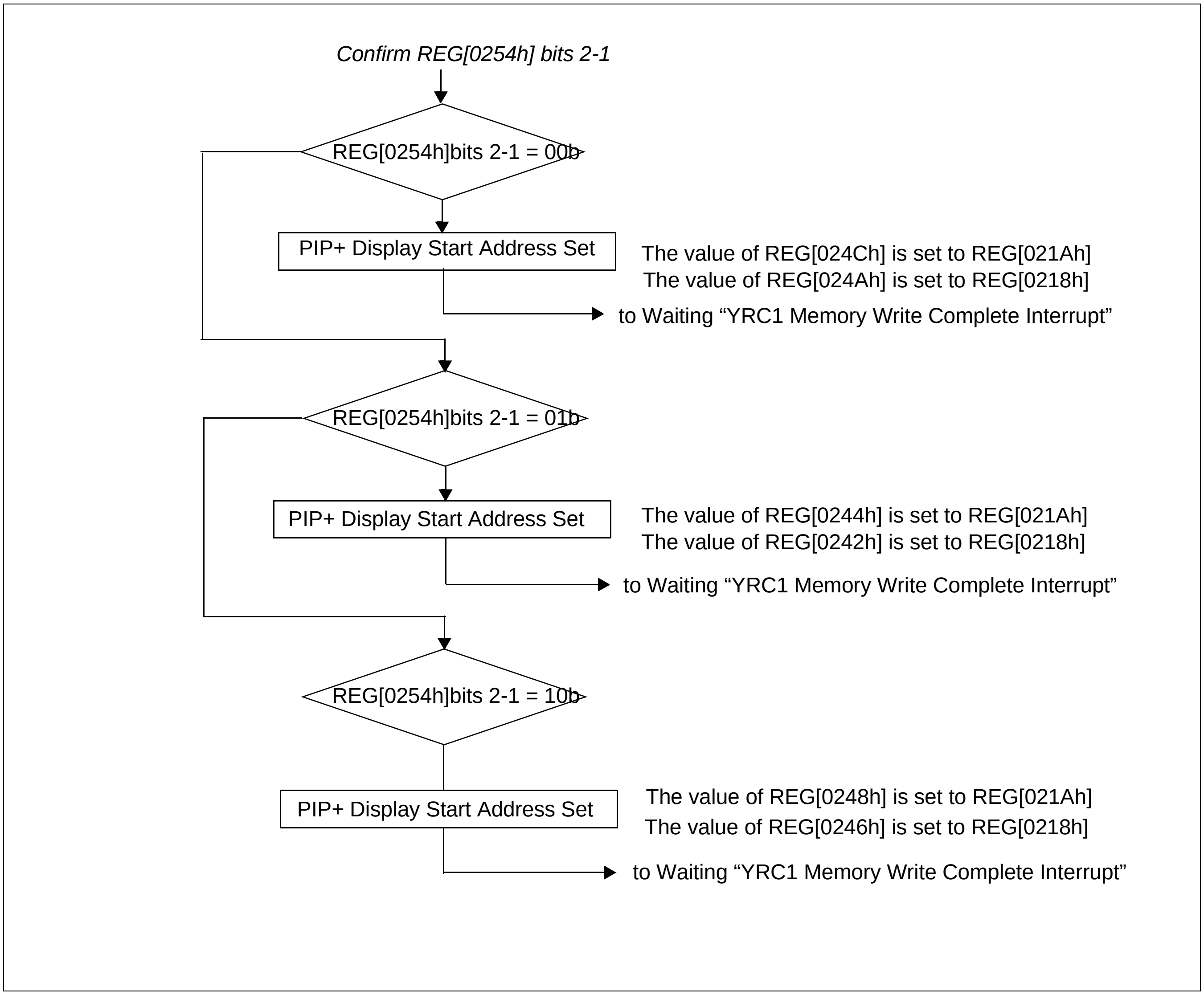


Figure 12-19: LCD Frame Synchronization

12.6.4 PIP+ Window Triple Buffer for YUV format

The Triple Buffer function of the YUV format is achieved only with 0218h and 021Ah. Sequence is shown in the following.




Confirm REG[0254h] bits 2-1
REG[0254h]bits 2-1 = 00b
PIP+ Display Start Address Set
The value of REG[024Ch] is set to REG[021Ah]
The value of REG[024Ah] is set to REG[0218h]
to Waiting “YRC1 Memory Write Complete Interrupt”
REG[0254h]bits 2-1 = 01b
PIP+ Display Start Address Set
The value of REG[0244h] is set to REG[021Ah]
The value of REG[0242h] is set to REG[0218h]
to Waiting “YRC1 Memory Write Complete Interrupt”
REG[0254h]bits 2-1 = 10b
PIP+ Display Start Address Set
The value of REG[0248h] is set to REG[021Ah]
The value of REG[0246h] is set to REG[0218h]
to Waiting “YRC1 Memory Write Complete Interrupt”

13 Display Functions

13.1 SwivelView™ Display

Most computer displays are refreshed in landscape orientation - from left to right and top to bottom. Computer images are stored in the same manner. SwivelView is designed to rotate the displayed image on a LCD by 90°, 180°, or 270° in a counter-clockwise direction. The rotation is done in hardware and is transparent to the user for all display buffer reads and writes. By processing the rotation in hardware, SwivelView offers a performance advantage over software rotation of the displayed image.

The image is not actually rotated in the display buffer since there is no address translation during Host CPU read/write. The image is rotated during display refresh.

The rotation of 90° and 270° doubles by 4 times and 16 bpp/18 bpp in number 8 bpp of accesses of buffers for the display.

13.1.1 90° SwivelView

The following figure shows how the programmer sees a portrait image and how the image is being displayed. The application image is written to the S1D13719 in the following sense: A-B-C-D. The display is refreshed in the following sense: B-D-A-C.

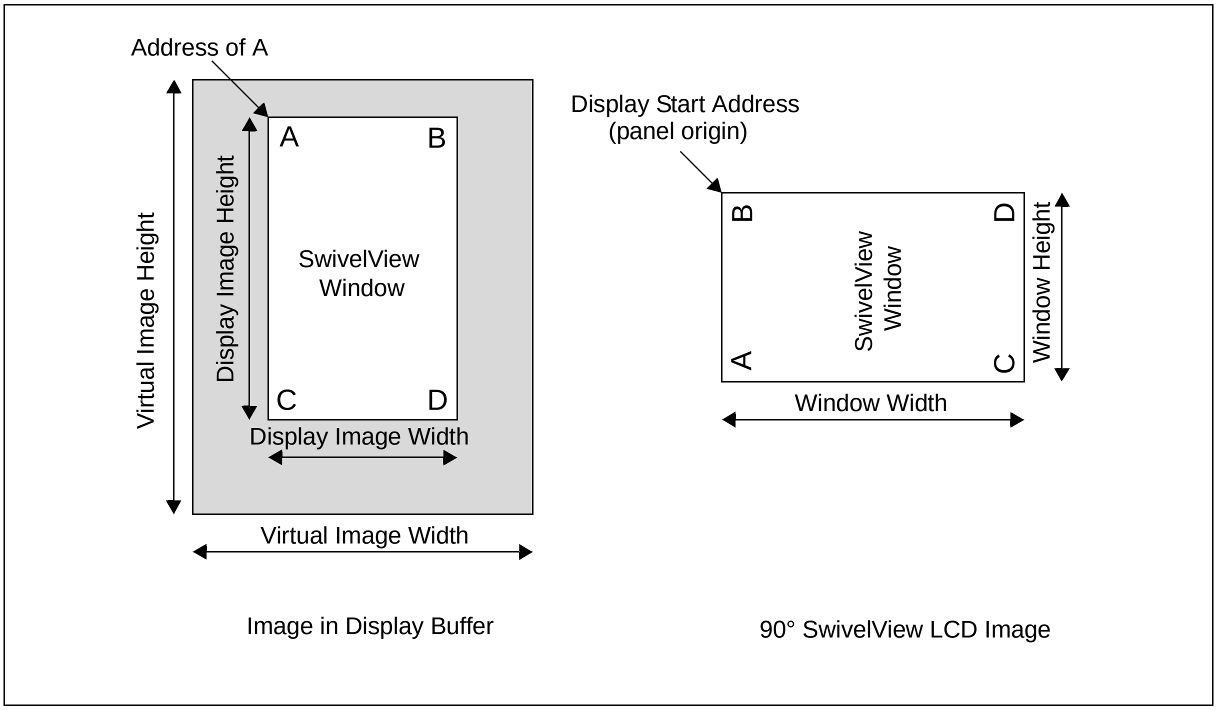


Figure 13-1: Relationship Between The Screen Image and the Image Refreshed in 90° SwivelView

Display Start Address

The display refresh circuitry starts at pixel "B", therefore the Display Start Address register must be programmed with the address of pixel "B".

Display Start Address = Address of A + Line Address Offset - (bpp ÷ 8)

Line Address Offset

Line Address Offset is set as byte counts per 1 line of virtual image.

Line Address Offset = Virtual Image Width x bpp ÷ 8

Memory Address of a Given Pixel

To calculate the address of pixel at any given position for the Main Window or PIP$^+$ window, use the following formula.

Memory Address (X,Y) = [(X - 1) + (Y - 1) x virtual panel width] x bpp ÷ 8

13.1.2 180° SwivelView

The following figure shows how the programmer sees a landscape image and how the image is being displayed. The application image is written to the S1D13719 in the following sense: A–B–C–D. The display is refreshed in the following sense: D-C-B-A.

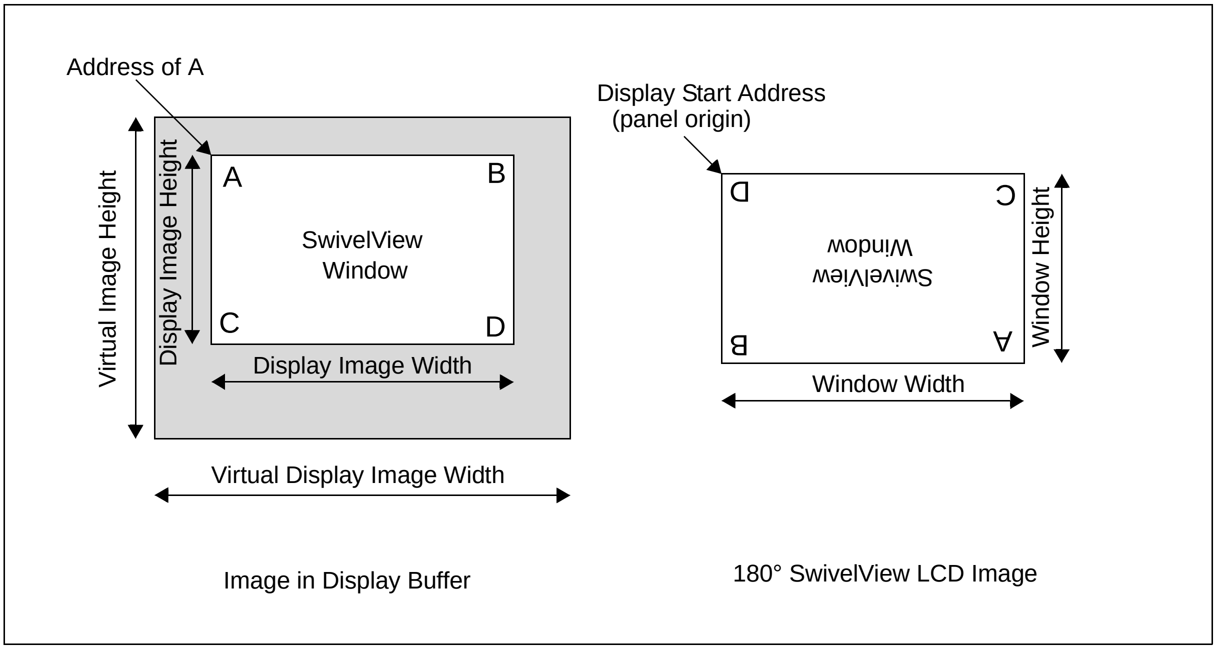


Figure 13-2: Relationship Between The Screen Image and the Image Refreshed in 180° SwivelView

Display Start Address

The display refresh circuitry starts at pixel “D”, therefore the Display Start Address register must be programmed with the address of pixel “D”.

Display Start Address= Address of A + Line Address Offset x Window Height - (bpp ÷ 8)

Line Address Offset

Line Address Offset is set as byte counts per 1 line of virtual image.

Line Address Offset = Virtual Image Width x bpp ÷ 8

Memory Address of a Given Pixel

To calculate the address of pixel at any given position for the Main Window or PIP$^+$ window, use the following formula.

Memory Address (X,Y) = [(X - 1) + (Y - 1) x virtual panel height] x bpp ÷ 8

13.1.3 270° SwivelView

The following figure shows how the programmer sees a portrait image and how the image is being displayed. The application image is written to the S1D13721 in the following sense: A–B–C–D. The display is refreshed in the following sense: C-A-D-B.

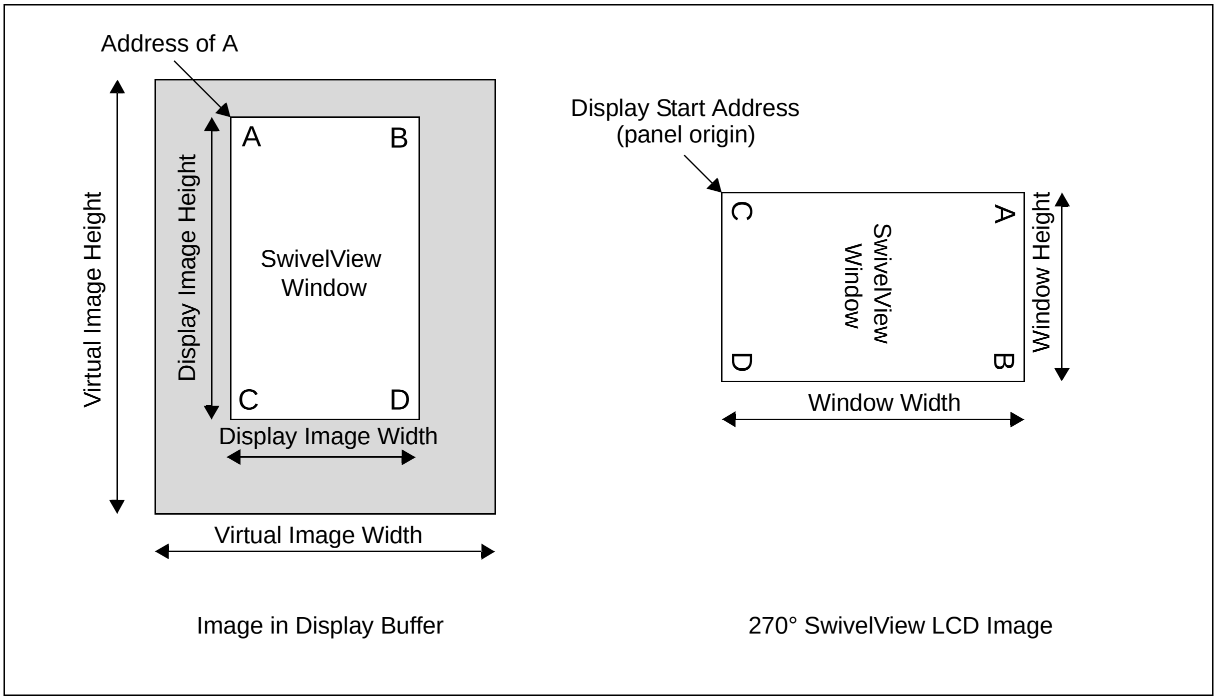


Figure 13-3: Relationship Between The Screen Image and the Image Refreshed in 270° SwivelView

Display Start Address

The display refresh circuitry starts at pixel "C", therefore the Display Start Address register must be programmed with the address of pixel "C".

Display Start Address
= Address of A + Line Address Offset × (Window Width - 1)

Line Address Offset

Line Address Offset is set as byte counts per 1 line of virtual image.

Line Address Offset = Virtual Image Width x bpp ÷ 8

Memory Address of a Given Pixel

To calculate the address of pixel at any given position for the Main Window or PIP+ window, use the following formula.

Memory Address (X,Y) = [(X - 1) + (Y - 1) x virtual panel width] x bpp ÷ 8

13.2 Mirror Display

Most computer displays are refreshed from left to right and top to bottom. The Mirror Display function refreshes the display from right to left - “mirroring” the display. Mirror Display is performed by hardware and no changes in the way display data is stored in the display buffer are required.

Mirror Display can be enabled independently on either the main window (REG[0202h] bit 3), the PIP^+ window (REG[0202h] bit 7), or both.

13.2.1 Mirror Display for SwivelView 0°

The following figure shows how the programmer sees a portrait image and how the image is being displayed. The application image is written to the S1D13719 in the following sense: A–B–C–D. The display is refreshed in the following sense: B-A-D-C.

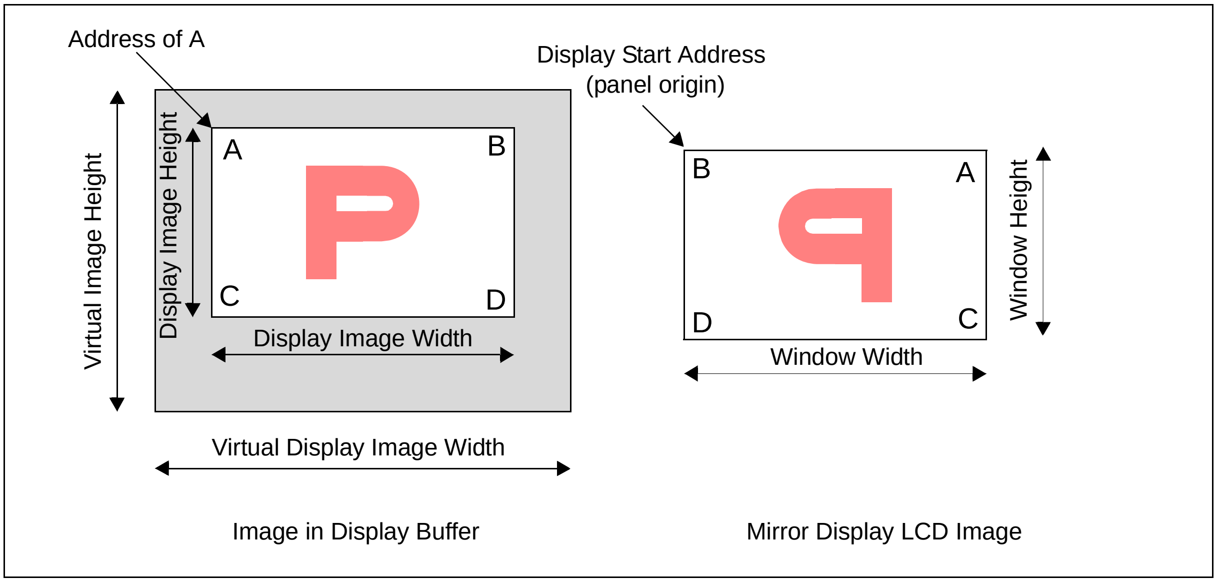


Figure 13-4: Relationship Between The Screen Image and the Image Refreshed in Mirror Display

Display Start Address

The display refresh circuitry starts at pixel “B”, therefore the Display Start Address register must be programmed with the address of pixel “B”.

Display Start Address= Address of A + Line Address Offset - (bpp ÷ 8)

Line Address Offset

Line Address Offset is set to the number of bytes per line of virtual image.

Line Address Offset = Virtual Image Width x bpp ÷ 8

13.2.2 Combination with SwivelView

When both Mirror Display and SwivelView are enabled, the image is rotated (SwivelView effect) after the Mirror Display effect takes place. The Display Start Address should be set to the left upper pixel of display image.

Combination with 90° SwivelView

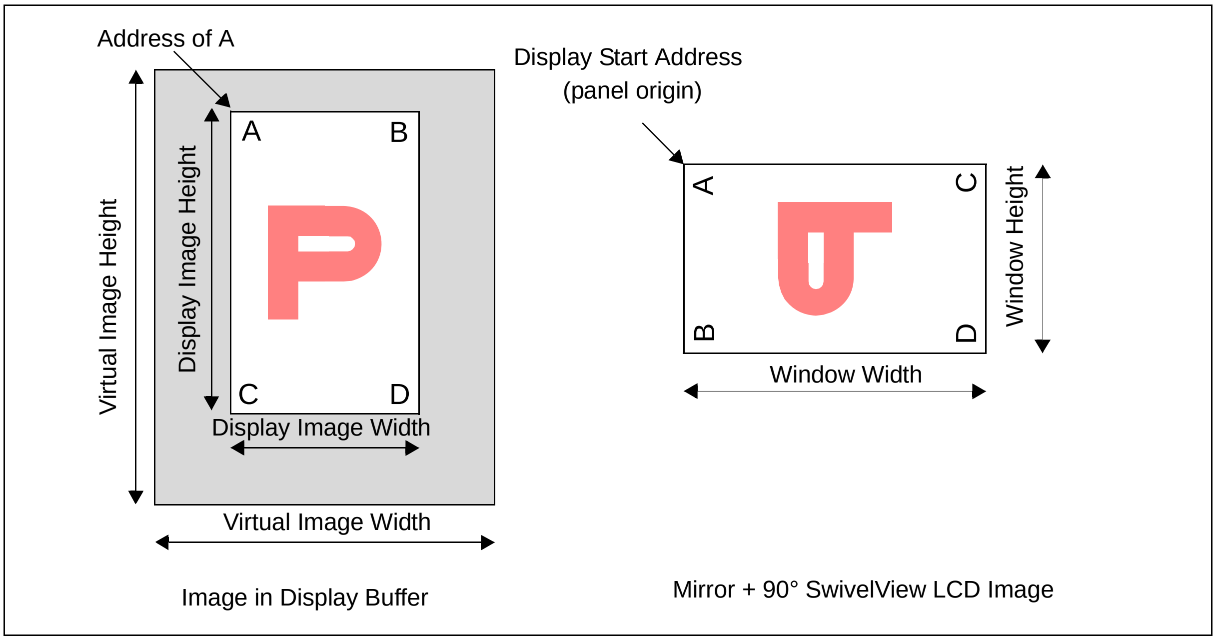


Figure 13-5: Mirror and 90° SwivelView Display

Combination with 180° SwivelView

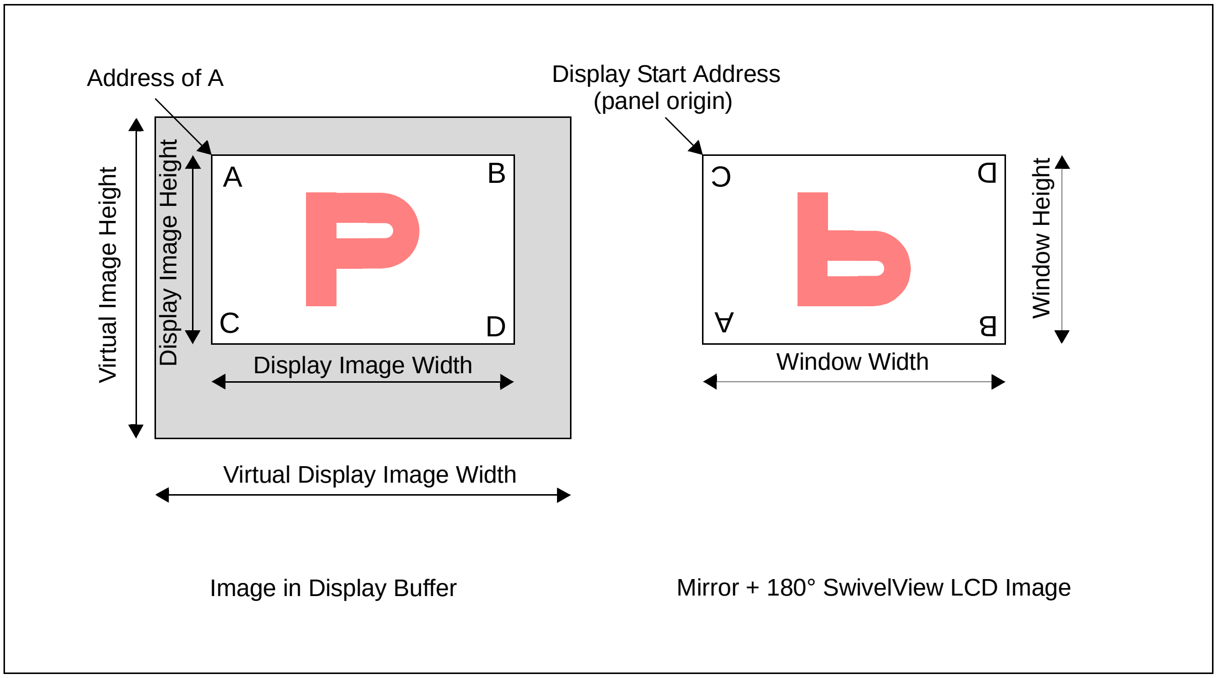


Figure 13-6: Mirror and 180° SwivelView Display

Combination with 270° SwivelView

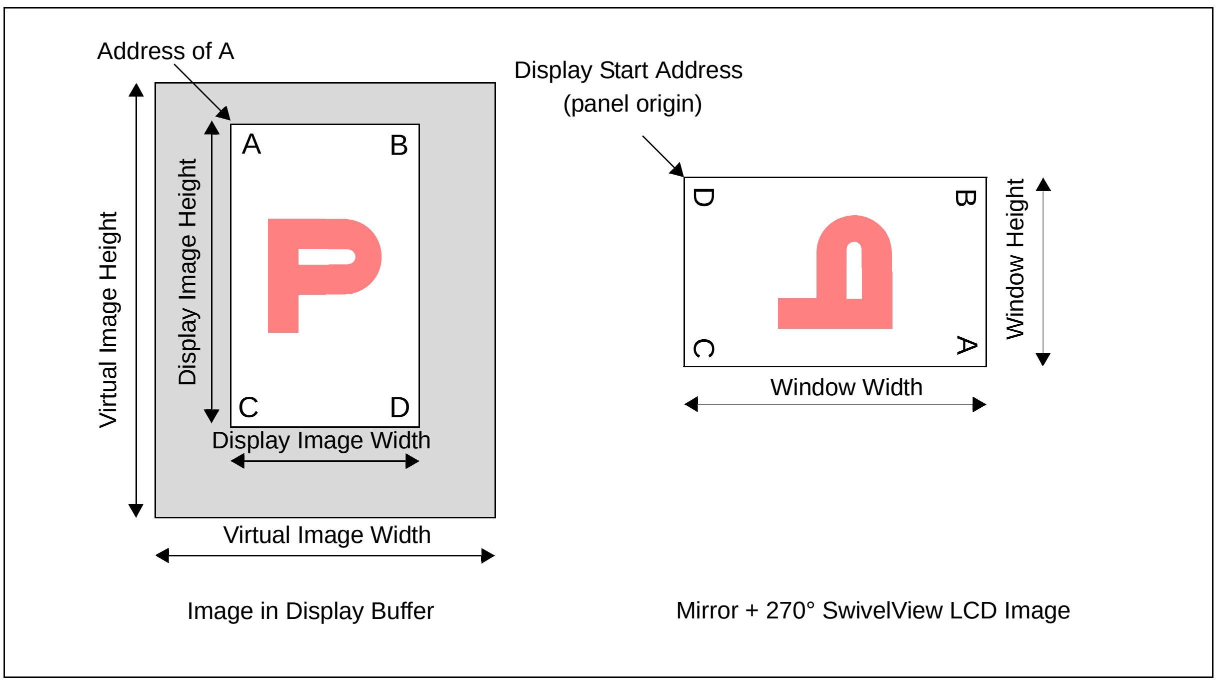


Figure 13-7: Mirror and 270° SwivelView Display

13.3 Picture-in-Picture Plus (PIP$^+$)

Picture-in-Picture Plus (PIP$^+$) enables a secondary window (or PIP$^+$ window) within the main display window. The PIP$^+$ window may be positioned anywhere within the main window display and is controlled using the PIP$^+$ Window control registers (REG[0218h]-[0228h]). The PIP$^+$ window color depth (REG[0200h] bits 3-2) and SwivelView orientation (REG[0202h] bits 5-4) are independent from the Main window.

The following diagrams show examples of a PIP$^+$ window within a main window and the registers used to position it.

13.3.1 PIP$^+$ for SwivelView 0°

The location where the PIP$^+$ window is displayed is set by setting Start/End Horizontal (X)/Vertical (Y) positions. The size of the PIP$^+$ window must be smaller than the size of the main window.

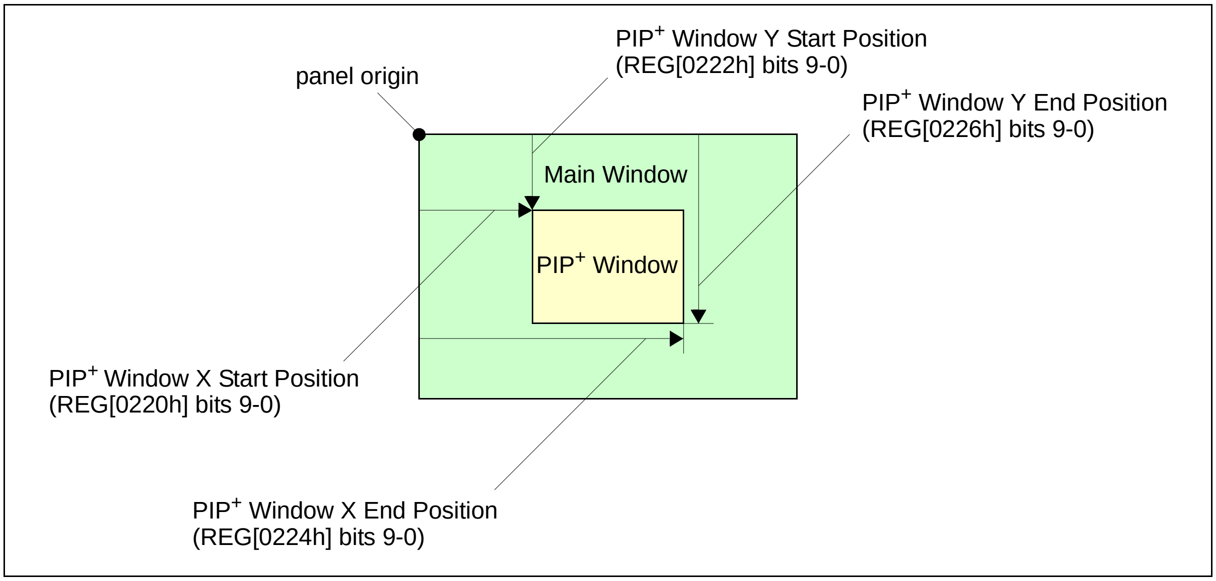


Figure 13-8: PIP$^+$ Display

13.3.2 Combination with SwivelView

The Picture-in-Picture Plus feature can be combined with the SwivelView feature. The PIP+ window start position is determined by the SwivelView rotation of the main window.

PIP+ Window in SwivelView 90° Main Window

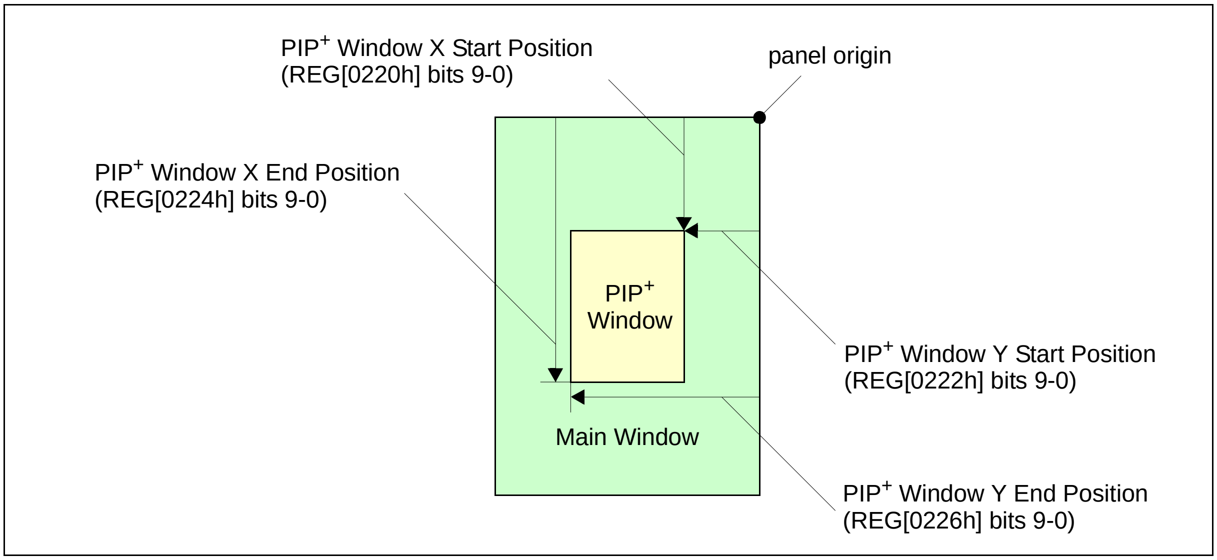


Figure 13-9: PIP+ Window in SwivelView 90° Main Window

PIP+ Window in SwivelView 180° Main Window

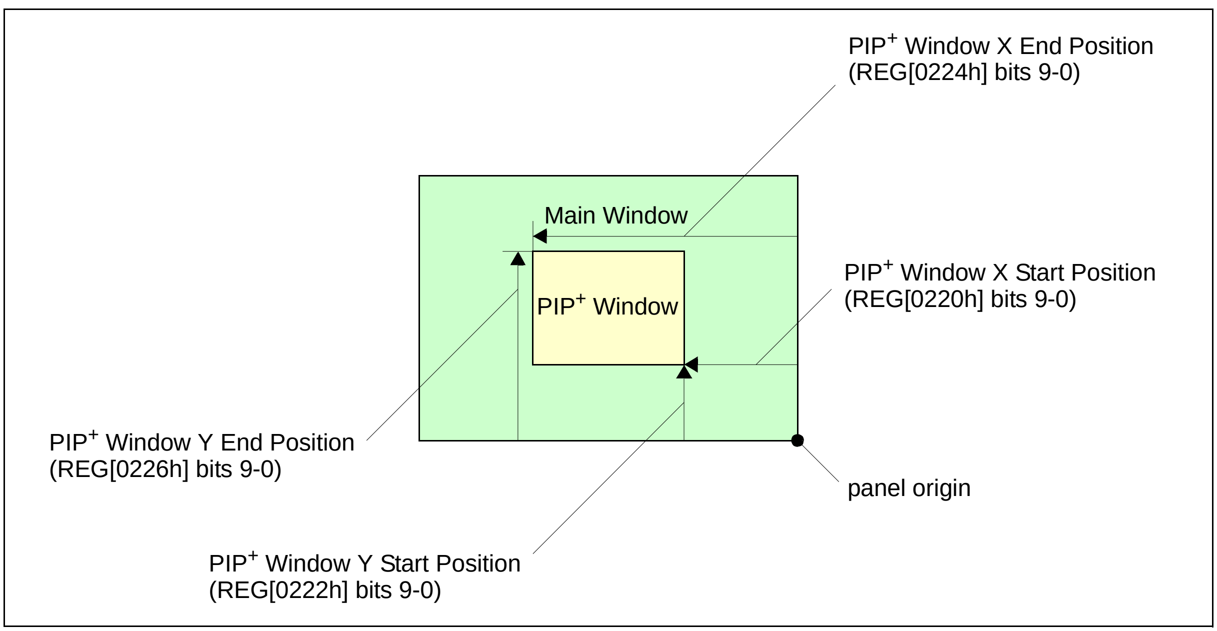


Figure 13-10: PIP+ Window in SwivelView 180° Main Window

PIP+ Window in SwivelView 270° Main Window

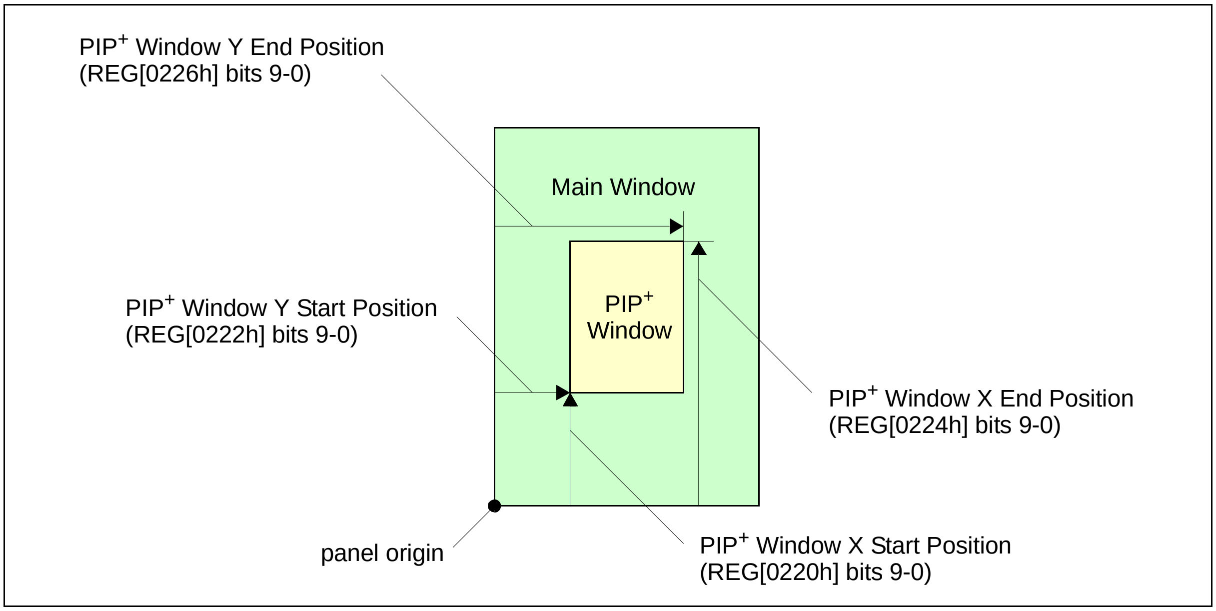


Figure 13-11: PIP+ Window in SwivelView 270° Main Window

13.3.3 PIP$^+$ Display Examples

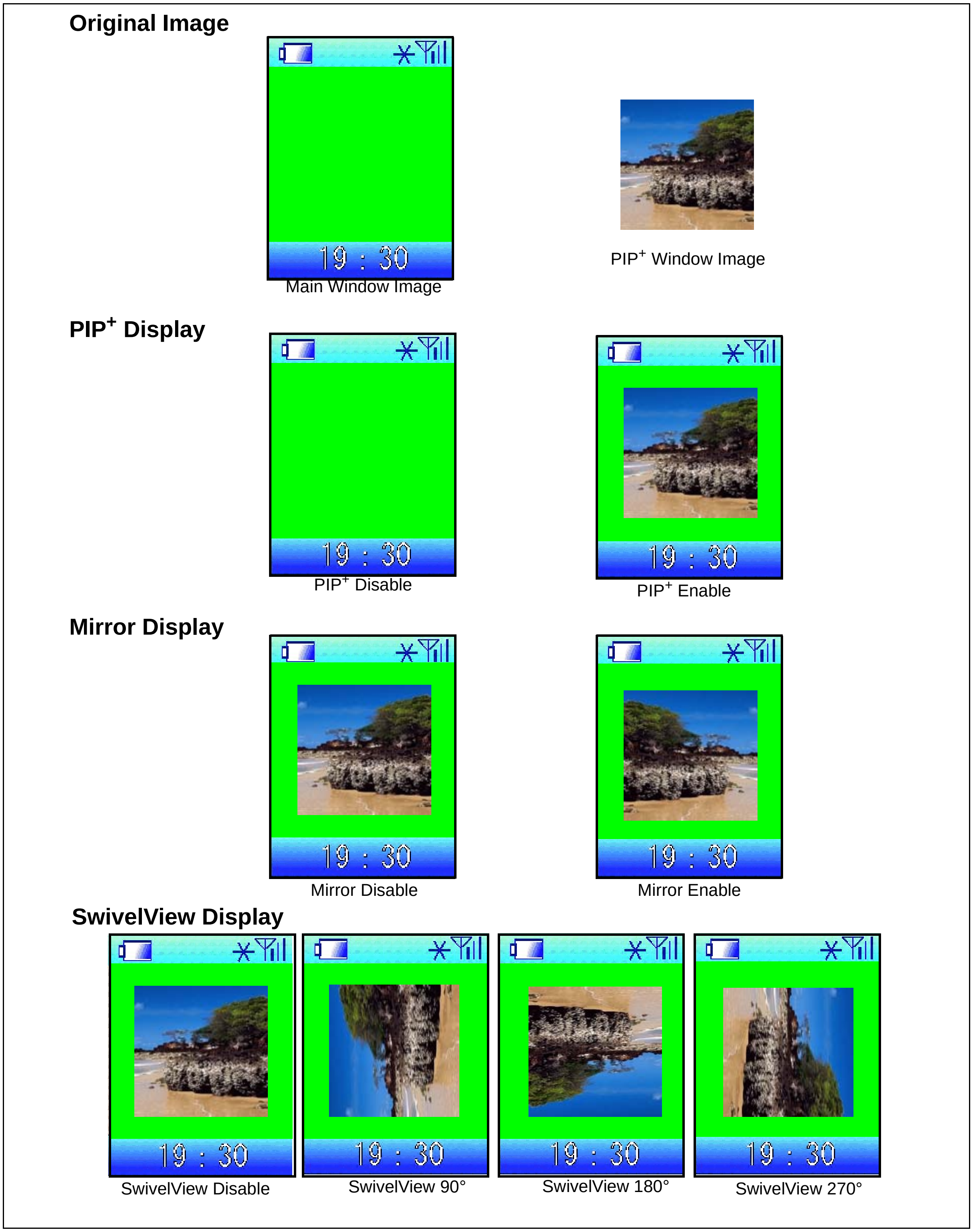


Figure 13-12: PIP$^+$ Display Examples

13.4 Overlay Display

When Picture-in-Picture Plus (PIP^+) is enabled, the S1D13719 supports an overlay with the following functions: Transparent, Average, AND, OR, INV, and bit shift. The overlay settings are specified using the Overlay Key Color registers for each RGB color and individual Overlay Key Color Enable bits (see REG[0328h]) as follows.

Table 13-1: Overlay Mode Selection

Register	Overlay PIP^+ Window Bit Shift (REG[0328h] bit 15)	Overlay Main Window Bit Shift (REG[0328h] bit 13)	Display Image
Transparent Overlay Key Color REG[0204h] REG[0206h] REG[0208h]	0	*	PIP^+ window data
	1		(PIP^+ window data)/2
Average Overlay Key Color REG[0310h] REG[0312h] REG[0314h]	0	0	((PIP^+ window data) + (Key Color data))/2
		1	((PIP^+ window data) + (Key Color data)/2)/2
	1	0	((PIP^+ window data)/2 + (Key Color data))/2
		1	((PIP^+ window data)/2 + (Key Color data)/2)/2
AND Overlay Key Color REG[0316h] REG[0318h] REG[031Ah]	0	0	(PIP^+ window data) AND (Key Color data)
		1	(PIP^+ window data) AND (Key Color data)/2
	1	0	(PIP^+ window data)/2 AND (Key Color data)
		1	(PIP^+ window data)/2 AND (Key Color data)/2
OR Overlay Key Color REG[031Ch] REG[031Eh] REG[0320h]	0	0	(PIP^+ window data) OR (Key Color data)
		1	(PIP^+ window data) OR (Key Color data)/2
	1	0	(PIP^+ window data)/2 OR (Key Color data)
		1	(PIP^+ window data)/2 OR (Key Color data)/2
INV Overlay Key Color REG[0322h] REG[0324h] REG[0326h]	0	*	Negative image of (PIP^+ window data)
	1		Negative image of (PIP^+ window data)/2

The following table shows the resulting PIP$^+$ window color when overlay is combined with the PIP$^+$ Window Bit Shift and the Main Window Bit Shift functions.

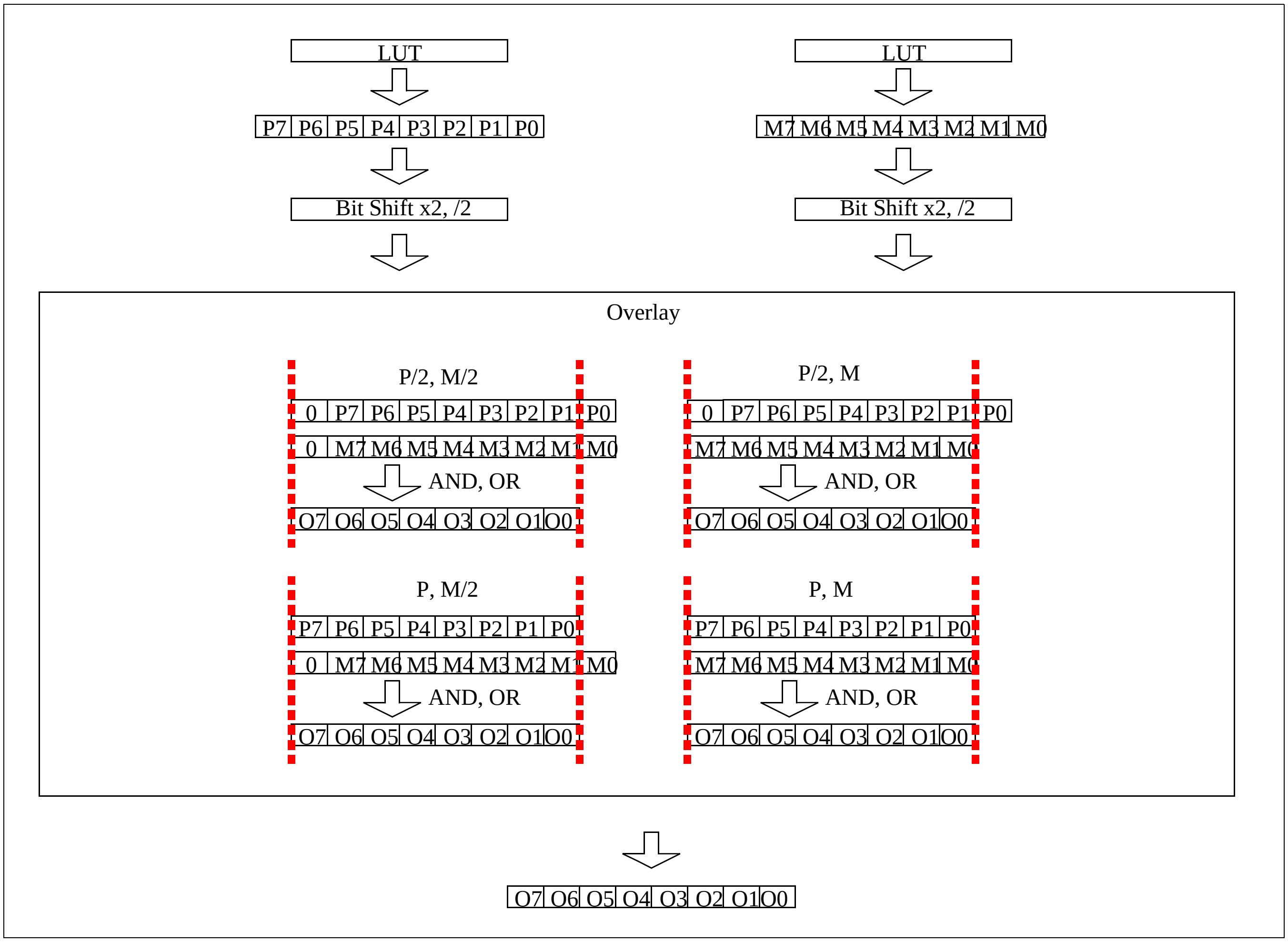


Figure 13-13: Data Flow for Bit Shift Function

13.4.1 Overlay Display Effects

When PIP$^+$ is disabled (REG[0200h] bits 9-8 = 00b)

- Only the Main window is displayed and the PIP$^+$ Window is ignored.

When PIP$^+$ is enabled (REG[0200h] bits 9-8 = 01b)

- The PIP$^+$ window area “overlays” the Main window area. The Overlay Key Color settings are ignored.

When PIP$^+$ with overlay is enabled (REG[0200h] bits 9-8 = 11b)

- The PIP$^+$ window area “overlays” the Main window area only on areas of the Main window where the color matches the overlay key color. For the Main window area, only the Main window is displayed.

- For the PIP$^+$ Window area, if the Main window data is same as the Overlay Key color, then the PIP$^+$ window data is mixed with the Main window data as specified for each overlay function (see Figure 13-14: “Overlay Display Effects 1,” on page 367). If the Main window data differs from the Overlay Key color, then the Main window data is displayed. If two or more Overlays are active, they have the following priority: Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color. A lower priority overlay function is ignored and only the highest priority overlay function is displayed.

Figure 13-14: Overlay Display Effects 1

Figure 13-15: Overlay Display Effects 2

13.4.2 Overlay Function Priority

If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color. In the case where Transparent and INV overlay are enabled, the INV function is ignored.

13.5 Pixel Doubling

The pixel doubling feature provides doubling of the size of the display data (resulting image) in either the horizontal direction, vertical direction, or both. For example, 160x120 image data can be expanded to completely fill a 320x240 physical display. This function can be enabled on both the main window or the PIP$^+$ window (RGB format only). The following diagram shows an example of a pixel doubling the PIP$^+$ window image.

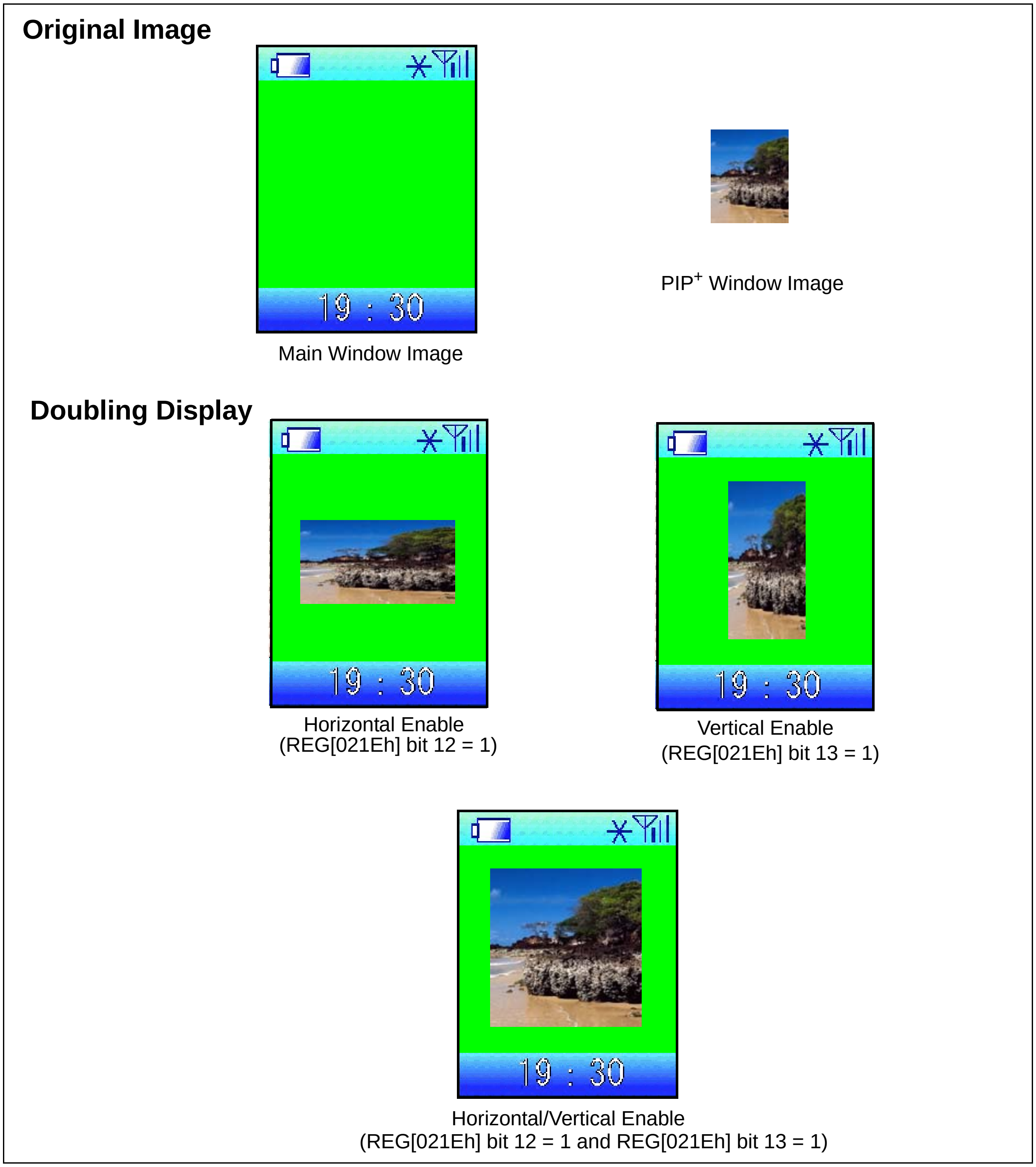


Figure 13-16: Pixel Doubling Example (PIP$^+$ Window)

13.6 Zoom Display

PIP$^+$ window image data can be expanded or reduced using the Zoom function (YUV 4:2:2 format only). Expansion is done by expanding the data using linear interpolation. Reduction is done using a simple reduction algorithm. The Zoom and Overlay functions can also be combined as shown below.

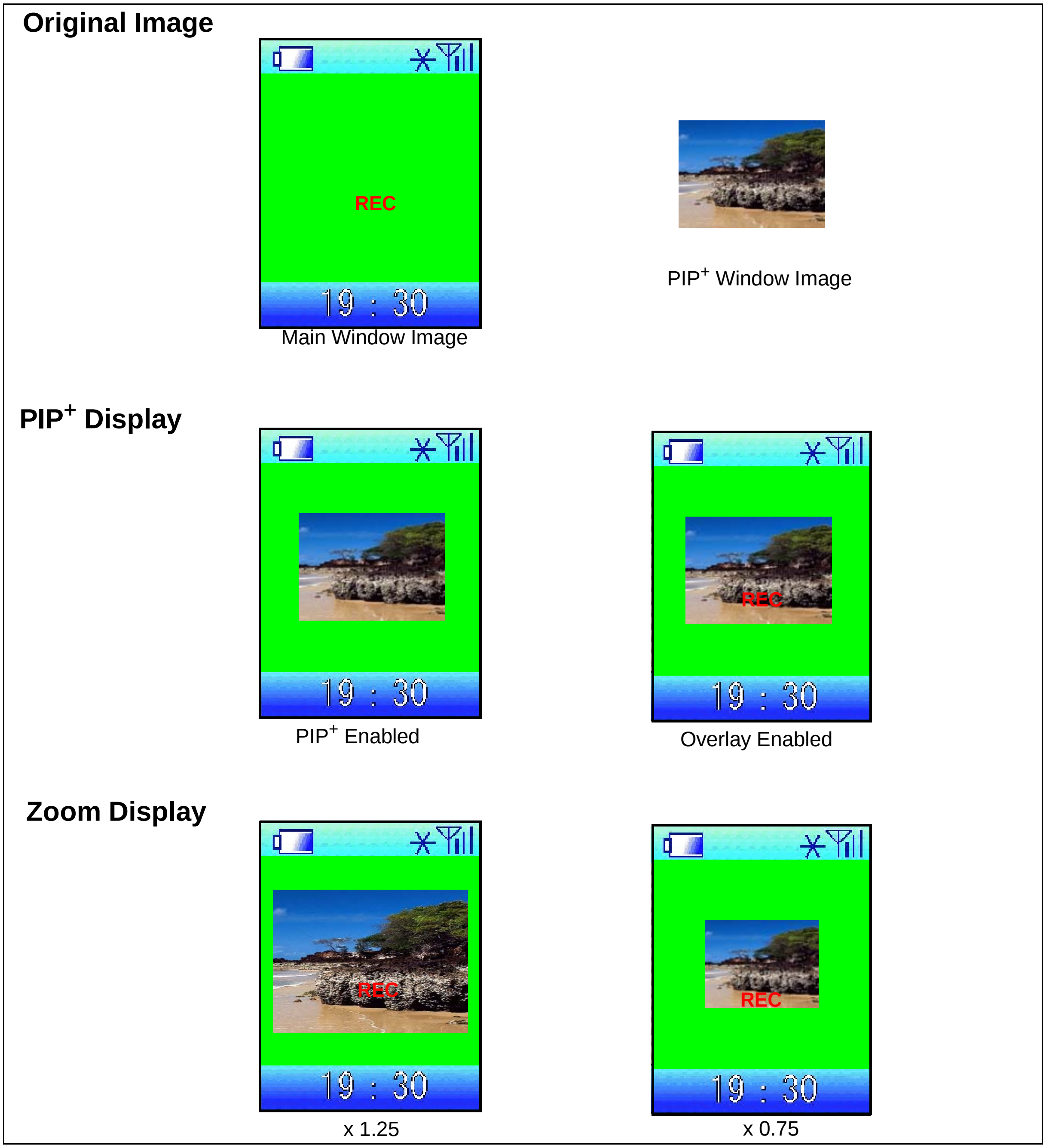


Figure 13-17: Zoom Display Example 1

The zoom display expansion ratio can be set independent of the PIP+ window size.

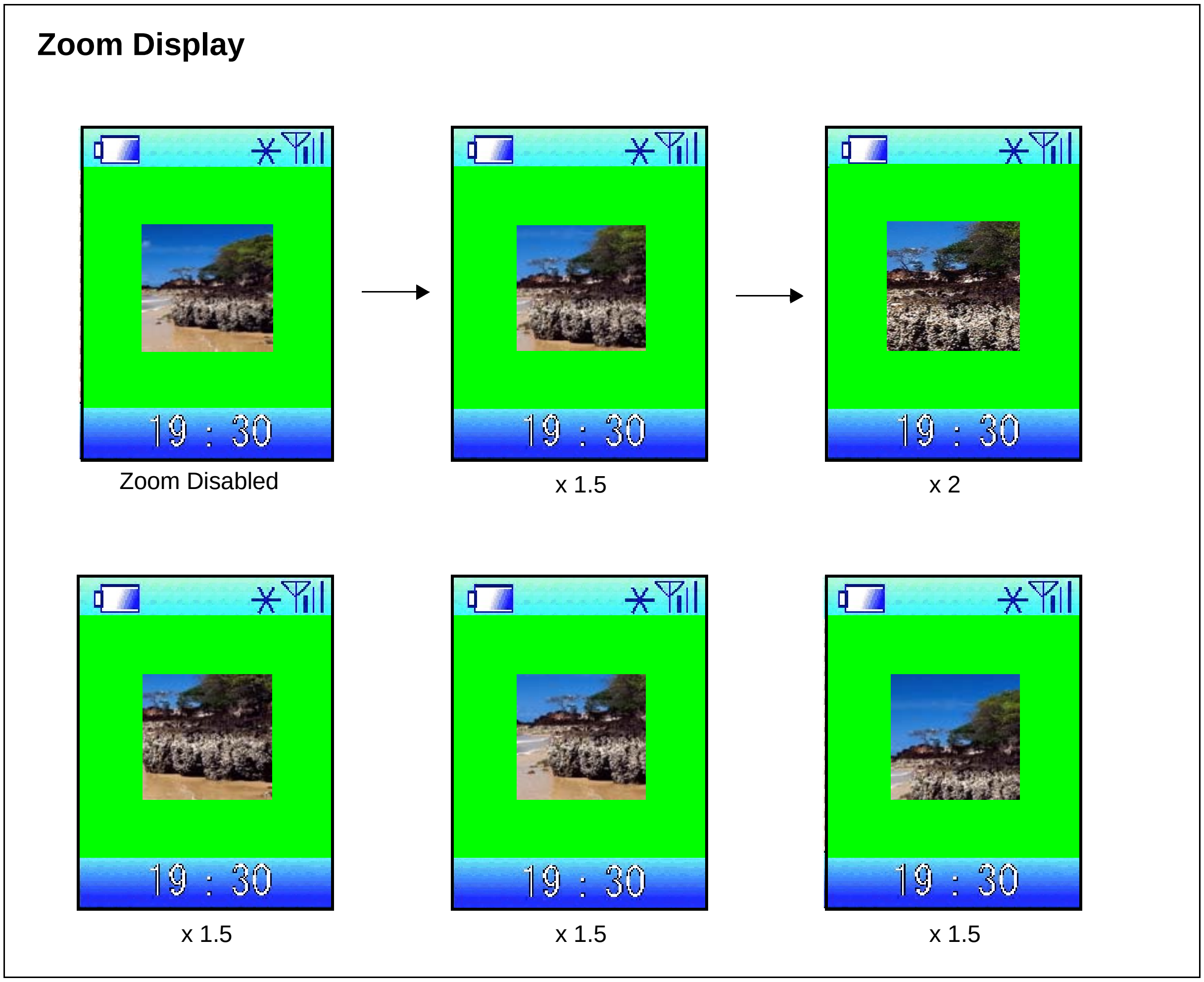


Figure 13-18: Zoom Display Example 2

14 JPEG Encode/Decode Operation

The S1D13719 JPEG Codec is based on the JPEG baseline standard and the arithmetic accuracy satisfies the requirement of the compatibility test of JPEG Part-2 (ISO/IEC10918-2). The maximum image size is 1600 x 1200 and the image to be compressed/decompressed must be YUV format with a minimum resolution as shown in Table 14-1: "Minimum Resolution Restrictions".

The following image restrictions must be observed for JPEG encode/decode, YUV data input from the Host (only YUV 4:2:2), and YUV data to the Host (only YUV 4:2:2). The image must be in YUV format and the minimum image resolution must be set based on the YUV format as follows.

Table 14-1: Minimum Resolution Restrictions

YUV Format	Minimum Resolution
4:4:4 (decode only)	1x1
4:2:2 (encode/decode)	2x1
4:1:1 (encode/decode)	4x1

The quantization table accommodates two compression tables and four decompression tables. The Huffman table accommodates two tables for each AC and DC. It is possible to insert markers (up to a 36 byte maximum size) during the encoding process. Markers which can be processed and automatically translated during the decoding process are SOI, SOF0, SOS, DQT, DHT, DRI, RSTm and EOI. The decoding process supports YUV 4:4:4, YUV 4:2:2, and YUV 4:1:1, and the encoding process supports YUV 4:2:2 and 4:1:1 format. RGB format is not supported. The image data processing ratio is almost less than 1/15 second at 640x480 resolution. However, the image data processing ratio is not guaranteed since it depends on the image data, the Huffman table and the quantization table.

14.1 JPEG Features

14.1.1 JPEG FIFO

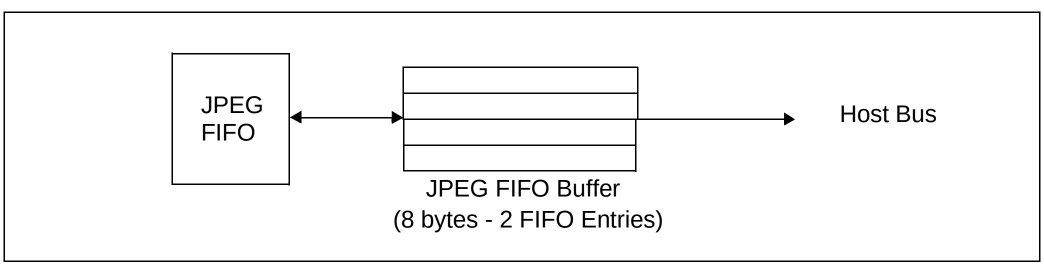


Figure 14-1: JPEG FIFO Overview

The JPEG FIFO is mapped at the beginning of the display buffer and is programmable to a maximum size of 128K bytes using REG[09A4h]. The JPEG file size and Host CPU performance should be considered when determining the JPEG FIFO size.

The status of the JPEG FIFO can be checked using the JPEG FIFO Status register (REG[09A2h]). It is also possible to indicate the JPEG FIFO status using interrupts via the JPEG Interrupt Control register (REG[0986h]).

The JPEG FIFO must be read by the Host CPU during the JPEG encode process.

Before reading the JPEG FIFO, confirm that the FIFO is not empty using the JPEG FIFO Empty Status bit (REG[09A2h] bit 0) and JPEG FIFO Threshold Status bits (REG[09A2h] bits 3-2). After confirmation, read one entry from the FIFO. Note that the FIFO must be read twice for each entry in the FIFO (32-bit FIFO but only 16-bit read/write port).

The JPEG FIFO must be written by the Host CPU during the JPEG decode process. Much like the methods for reading the JPEG FIFO, writing to the JPEG FIFO can be done entry by entry or as a block of data once it has been determined how many entries are available in the JPEG FIFO. If the JPEG FIFO is full and data is written to it by the Host CPU, WAIT# will be asserted until space becomes available in the FIFO.

14.1.2 JPEG Codec Interrupts

The JPEG codec can generate the following interrupts to avoid continuously poling the JPEG status bits. Using interrupts decreases the CPU load for a JPEG process. For information on the JPEG Interrupt register bits, see the register descriptions in Section 10.4.15, “JPEG Module Registers”.

1. **JPEG Codec Interrupt Flag (REG[0982h] bit 1)**
   This flag is asserted when all JPEG processes have finished without errors, or during the decode process when a RST marker process error is detected. This interrupt flag should be enabled when RST marker error detection is enabled.

   However, if the RST marker is not required during the decode process, confirm that the operation has finished using the JPEG Decode Complete Flag (REG[0982h] bit 5). For the encoding process, confirm that the operation has finished using the JPEG FIFO Empty Flag (REG[0982h] bit 8) and the JPEG Operation Status bit (REG[1004h] bit 0).

2. **JPEG Line Buffer Overflow Flag (REG[0982h] bit 2)**
   If the JPEG FIFO is read slower than the JPEG Line Buffer is written to during the encoding process, this flag is asserted when the JPEG Line Buffer overflows. This flag should be enabled for JPEG encoding.

3. **JPEG Decode Marker Read Flag (REG[0982h] bit 4)**
   During JPEG decoding, this flag is asserted when marker information is read from the JPEG file. Marker information may include resize settings or LCD settings. JPEG decoding is stopping while this flag is asserted and does not restart until after this flag is cleared (REG[0986h] bit 4 = 0).

4. **JPEG Decode Complete Flag (REG[0982h] bit 5)**
This flag is asserted after the JPEG decode process is finished and the decompressed image data is stored in memory. This flag is useful as a trigger for enabling the overlay or display of the image.

5. **JPEG FIFO Empty Flag (REG[0982h] bit 8)**
This flag is asserted when the JPEG FIFO is empty. For the decode process, this flag is useful for timing JPEG data writes to the FIFO and to identify when the JPEG decode process is finished completely. For the encode process, this flag indicates that the entire JPEG file has been read by the host.

6. **JPEG FIFO Full Flag (REG[0982h] bit 9)**
This flag is asserted when the JPEG FIFO is full. For the encode process, this flag is used as a trigger for increasing the priority of host reads to the FIFO. For the decode process, this flag indicates if it is possible to write data to the FIFO.

7. **JPEG FIFO Threshold Trigger Flag (REG[0982h] bit 10)**
This flag is asserted when the amount of data in the JPEG FIFO meets the condition programmed into the JPEG FIFO Trigger Threshold bits (REG[09A0h] bits 5-4). This flag is useful for timing when the host will start to read JPEG compressed data in the FIFO.

8. **Encode Size Limit Violation Flag (REG[0982h] bit 11)**
This flag is asserted when the compressed JPEG data size is greater than the programmed size in the JPEG Encode Size Limit registers (see REG[09B0h] - REG[09B2h]).

14.1.3 JPEG Bypass Modes

The S1D13719 can bypass the JPEG Codec in order for the Host CPU to capture raw YUV data from the camera interface (YUV Data Capture Mode). The S1D13719 can also bypass the JPEG Codec in order for the Host CPU to send raw YUV data to be displayed (YUV Data Display Mode). For YUV Data Capture Mode, YUV data is still sent to the Host CPU through the JPEG FIFO which is accessed through REG[09A6h]. For YUV Data Display Mode, the JPEG FIFO is bypassed and the Host CPU writes YUV data directly to the JPEG Line Buffer using the JPEG Line Buffer Write Port (REG[09E0h]).

The raw YUV data can be in either of the two YUV format as follows (YUV 4:2:2 = 2x1).

	YUV 4:2:2
Nth line	UYVYUYVY
N+1th line	UYVYUYVY

14.2 Example Sequences

14.2.1 JPEG Encoding Process

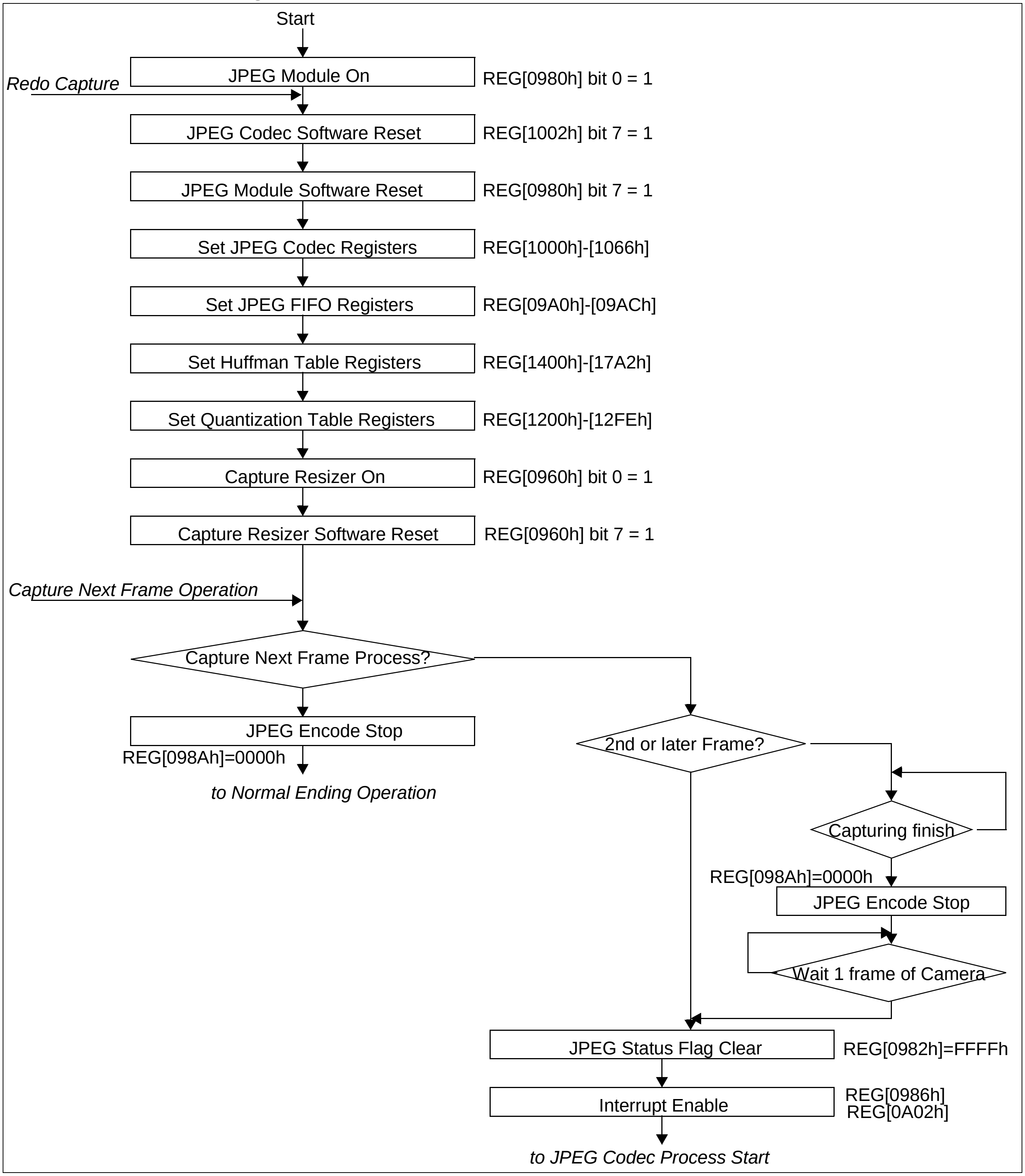


Figure 14-2: JPEG Encoding Process (1 of 4)

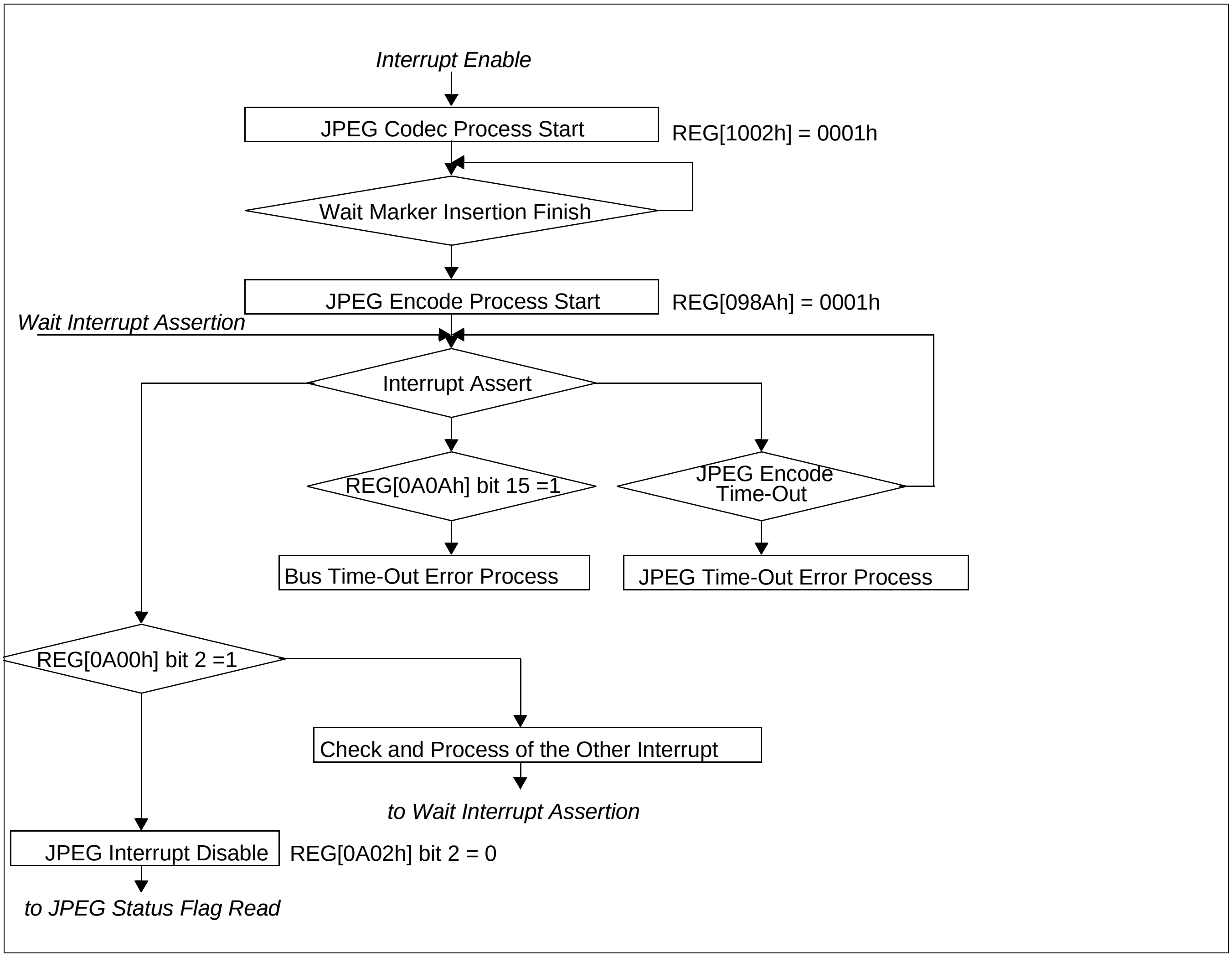


Figure 14-3: JPEG Encoding Process (2 of 4)

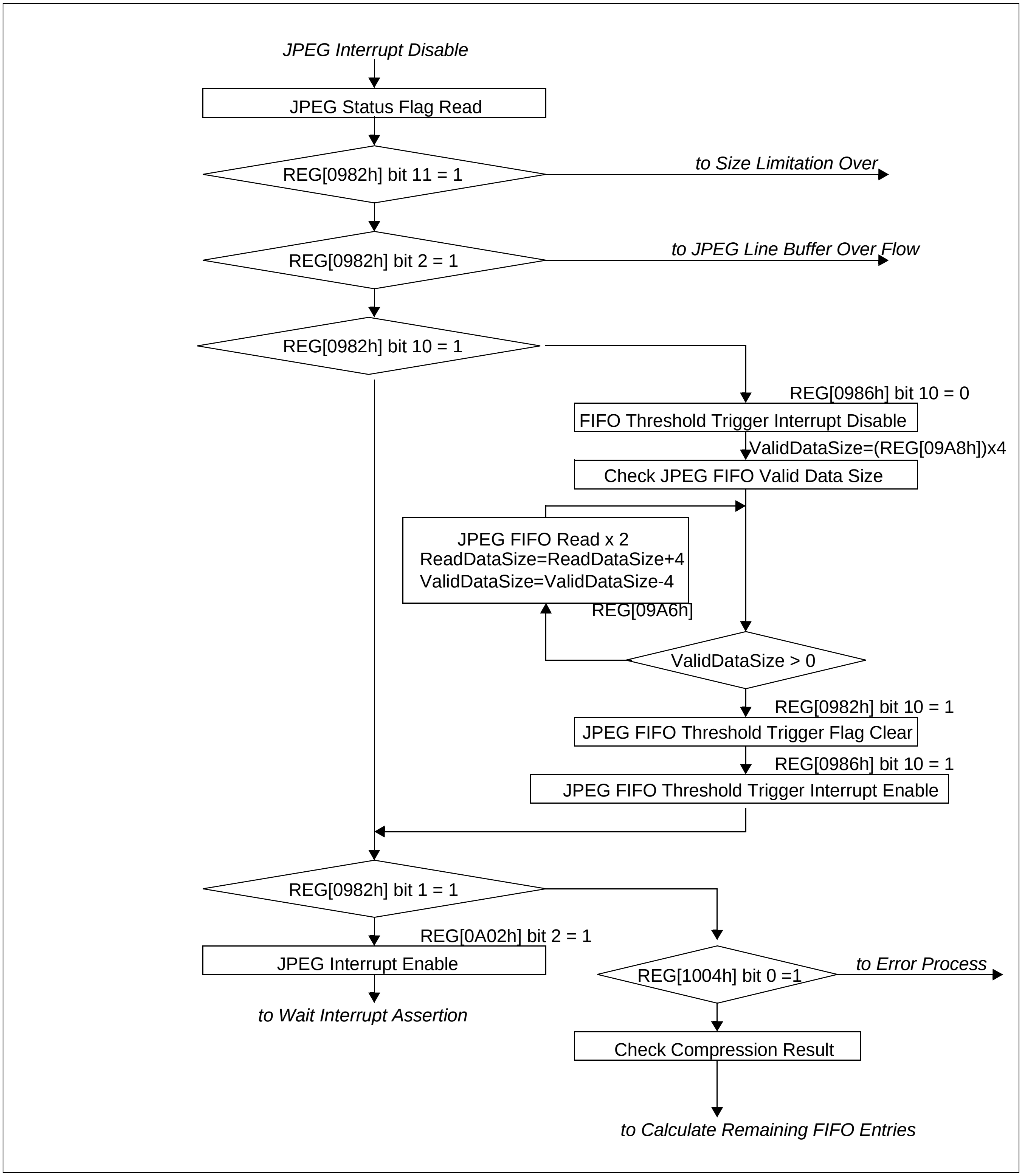


Figure 14-4: JPEG Encoding Process (3 of 4)

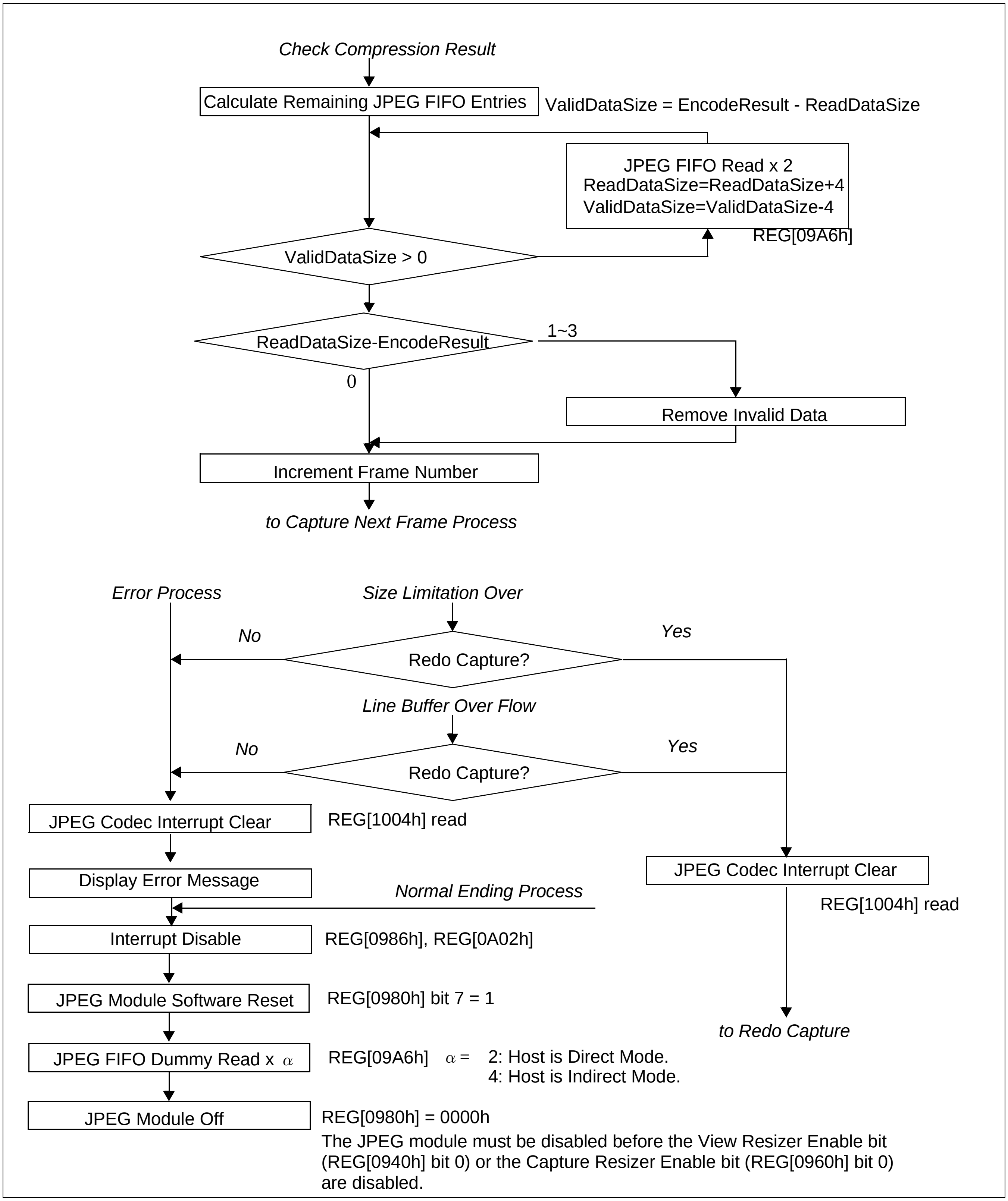


Figure 14-5: JPEG Encoding Process (4 of 4)

1. Initialize the camera interface registers (REG[0100h]-[0124h]).
2. Enable the JPEG module, set REG[0980h] bits 3-0 = 0001.
3. Initialize the JPEG Codec registers.
    a. Software reset the JPEG codec, set REG[1002h] bit 7 = 1.
    b. Select the operation mode for encoding, set REG[1000h] bit 2 = 0.
    c. Set the desired quantization table number (REG[1006h]) and the huffman table number (REG[1008h]).
    d. Select the DRI setting (REG[100Ah]-[100Ch]).
    e. Configure the vertical pixel size (REG[100Eh]-[1010h]) and the horizontal pixel size (REG[1012h]-[1014h]).
    f. Set the Insertion Marker Data in REG[1020h]-[1066h]. When REG[1000h] bit 3 = 1, the data in these registers is written to the JPEG file. Unused bits must be written as FFh.
    g. Initialize Quantization Table No. 0 (REG[1200h]-[127Eh]) and Quantization Table No. 1 (REG[1280h]-[12FEh]) with the following sequence.

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64

h. Set DC Huffman Tables and the AC Huffman Tables according to ISO/IEC 10918 attachment K, each numerical formula is specified as follows:

DC Huffman Table No. 0 Register 0 (REG[1400h-141Eh]) is set as A
DC Huffman Table No. 0 Register 1 (REG[1420h-1436h]) is set as B
AC Huffman Table No. 0 Register 0 (REG[1440h-145Eh]) is set as C
AC Huffman Table No. 0 Register 1 (REG[1460h-15A2h]) is set as D
DC Huffman Table No. 1 Register 0 (REG[1600h-161Eh]) is set as E
DC Huffman Table No. 1 Register 1 (REG[1620h-1636h]) is set as F
AC Huffman Table No. 1 Register 0 (REG[1640h-165Eh]) is set as G
AC Huffman Table No. 1 Register 1 (REG[1660h-17A2h]) is set as H

A:	00h, 01h, 05h, ..., 00h, 00h	16 byte
B:	00h, 01h, 02h, ..., 0Ah, 0Bh	12 byte
C:	00h, 02h, 01h, 03h, ...01h, 7Dh	16 byte
D:	01h, 02h, 03h, ..., F9h, FAh	162 byte
E:	00h, 03h, 01h, ..., 00h, 00h	16 byte
F:	00h, 01h, 02h, ..., 0Ah, 0Bh	12 byte
G:	00h, 02h, 01h, 02h, ..., 02h, 77h	16 byte
H:	00h, 01h, 02h, ..., F9h, FAh	162 byte

4. Set the JPEG module registers.

   a. Enable the JPEG module and perform a JPEG software reset (REG[0980h] = 81h).

   b. Specify the JPEG FIFO size (REG[09A4h]). The FIFO size is determined using the following formula:

      JPEG FIFO size = ((REG[09A4h] bits 3-0) + 1) x 4K bytes.

      Example: for a JPEG FIFO size of 12K bytes, REG[09A4h] = 2
      (2 + 1) x 4KB = 12K bytes

   c. Set the Encode Size Limit (REG[09B0h]-[09B2h]) in bytes. To generate an interrupt when the encode size limit is exceeded use the Encode Size Limit Violation Flag (REG[0982h] bit 11).

   d. Clear the JPEG FIFO (REG[09A0h] bit 2 = 1).

   e. Set the JPEG FIFO Threshold Trigger (REG[09A0h] bits 5-4).

5. Set the capture resizer registers. The vertical and horizontal dimensions must be the same as the JPEG vertical and horizontal sizes as programmed in step 3e.

6. Start the encode process.
    a. Clear all status bits by writing REG[0982h] as FFFFh
    b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0E07h.
    c. Start the JPEG operation (REG[1002h] bit 0 = 1)
    d. Start capturing (REG[098Ah] bit 0 = 1)

    After setting REG[1002h] bit 0 = 1, 2ms (internal system clock = 50Mhz) is required to generate the Markers. If REG[098Ah] bit 0 is set to 1 before 2ms, capturing will start only after generating the Markers (after 2 ms has passed).

Host CPU Process

7. Wait for the JPEG FIFO Threshold condition to be met. This can be done using the JPEG FIFO Threshold Interrupt (see REG[0986h]) or by polling the JPEG FIFO Threshold Status bits (REG[0982h] bits 13-12). If the interrupt method is used, the interrupt should be disabled after it is asserted.
8. Confirm the FIFO Valid Data Size (REG[09A8h]).
9. Read the JPEG FIFO Read/Write register twice (REG[09A6h]). Two reads from the 16-bit FIFO read/write register are required to get the entire 32-bit FIFO entry.
10. If using the interrupt method, the interrupt should be re-enabled again.
11. Loop steps 7 through 9 continuously until the FIFO Valid Data Size reaches 0 (REG[09A8h] = 0) and the JPEG Operation Status is idle (REG[1004h] bit 0 = 0).
12. When the encode process finishes, check the actual file size with the Encode Size Result registers (REG[09B4h]-[09B6h]).
13. Confirm the process is complete with the JPEG Codec Interrupt Flag (REG[0982h] bit 1).
14. Stop the JPEG codec using the JPEG Start/Stop Control bit (REG[098Ah] bit 0 = 0).

14.2.2 Memory Image JPEG Encoding Process

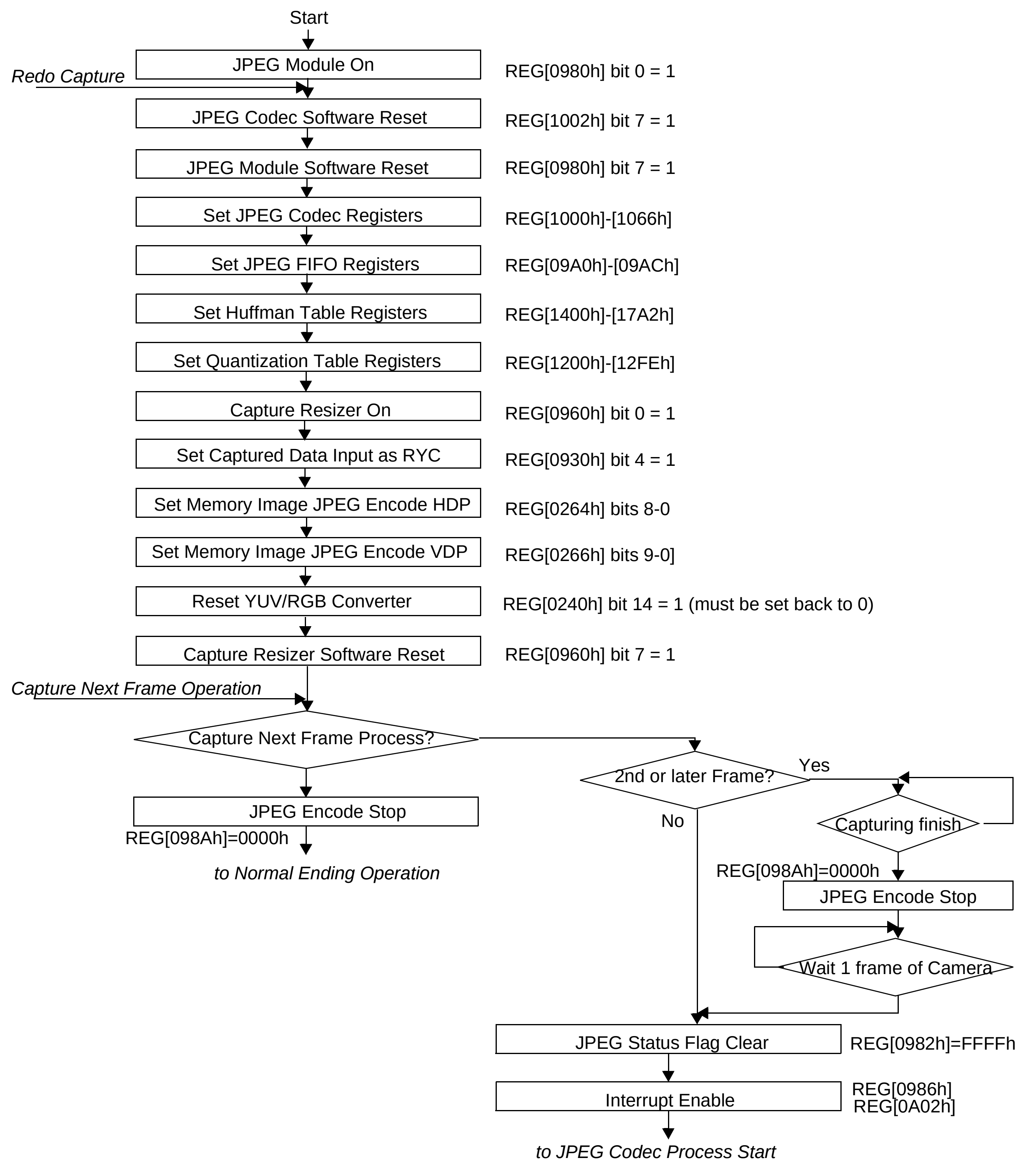


Figure 14-6: Memory Image JPEG Encoding Process (1 of 4)

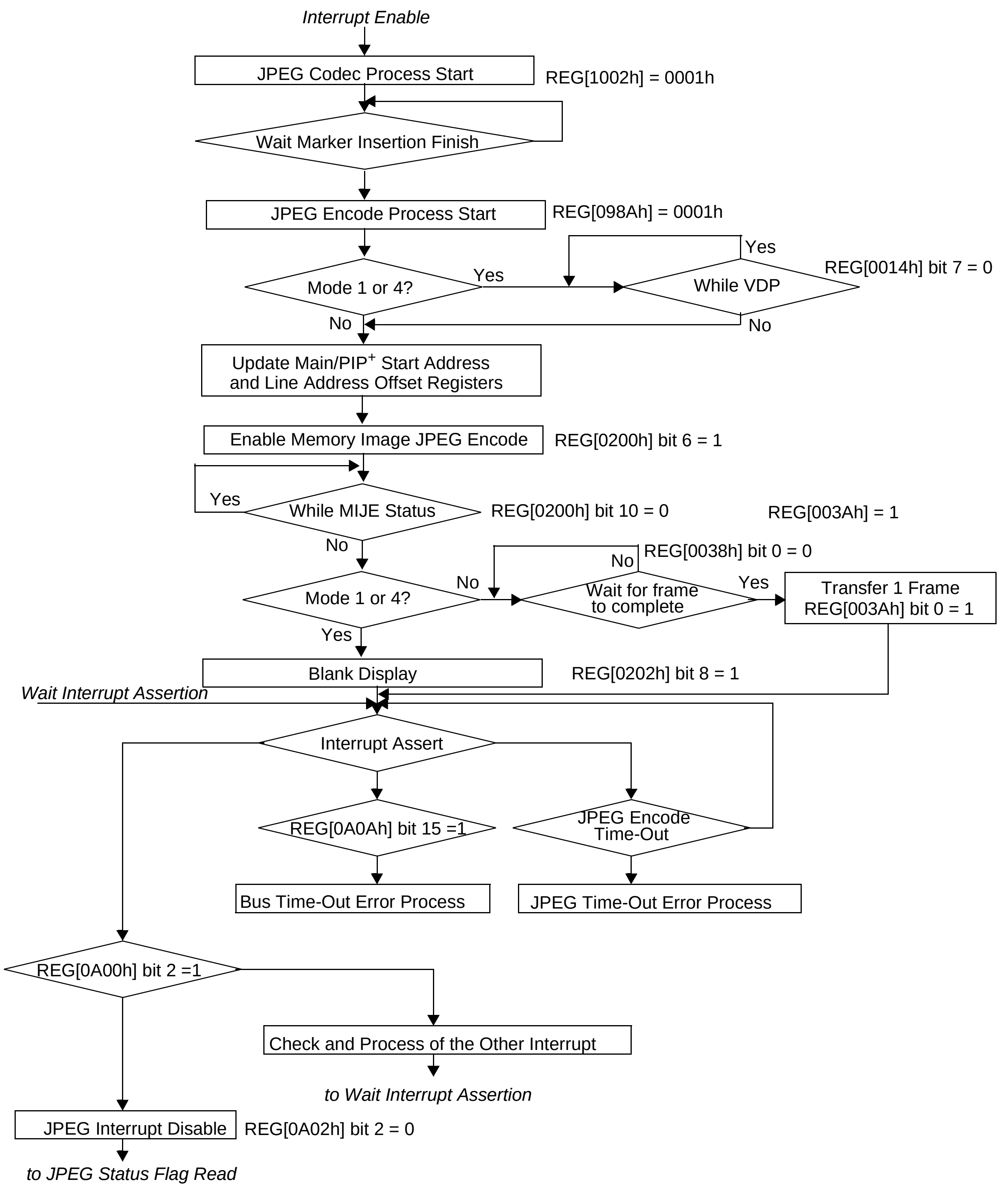


Figure 14-7: Memory Image JPEG Encoding Process (2 of 4)

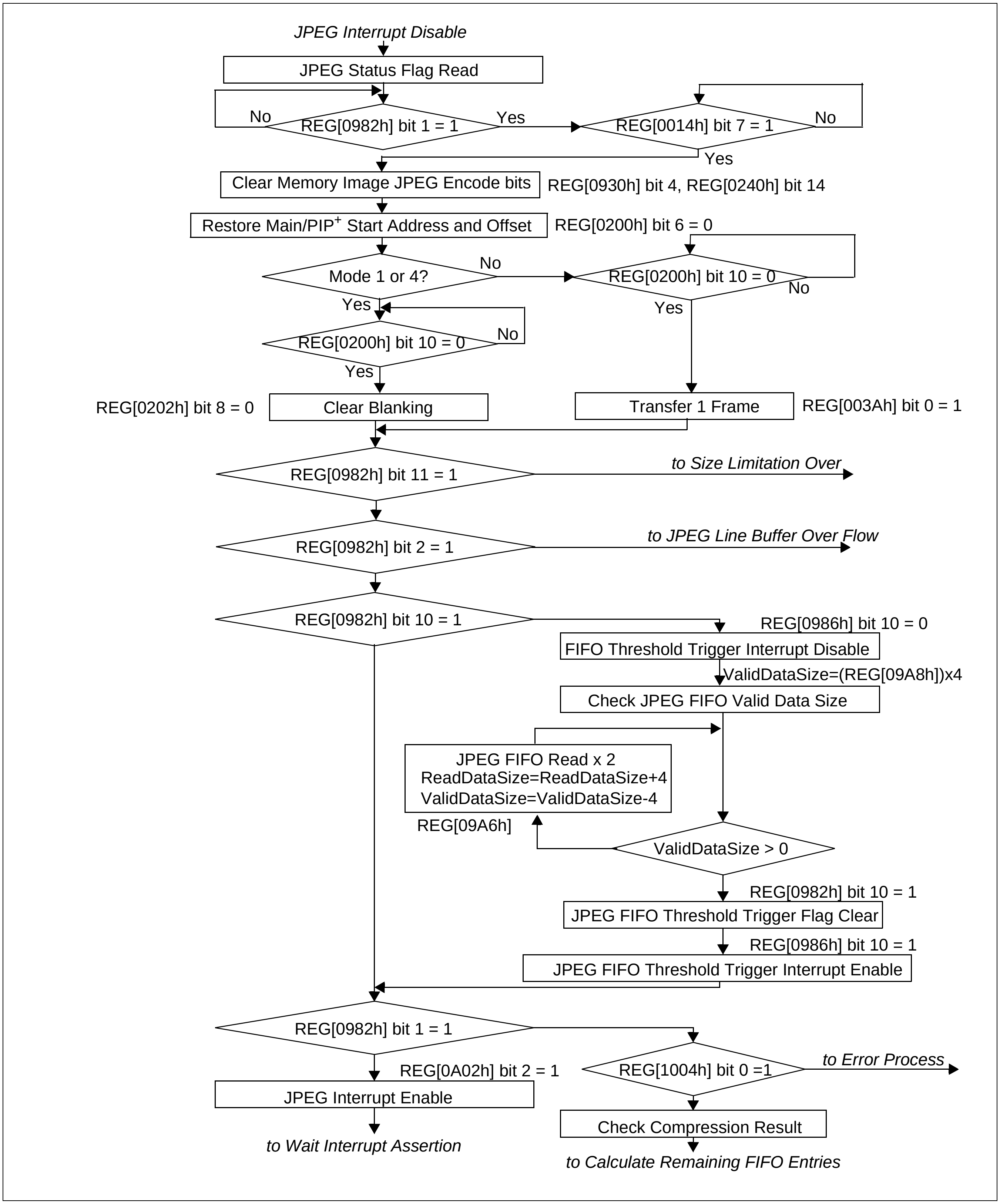


Figure 14-8: Memory Image JPEG Encoding Process (3 of 4)

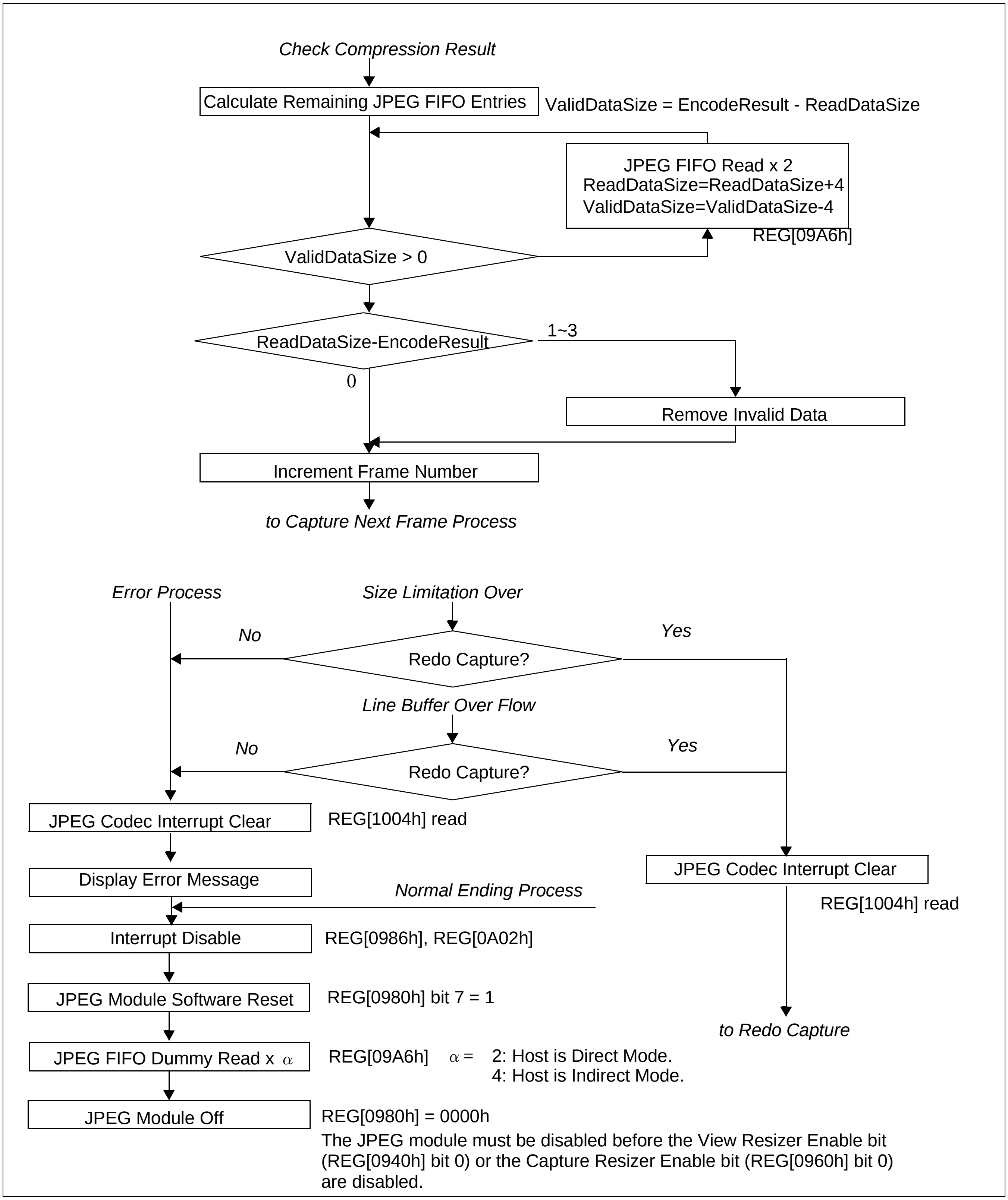


Figure 14-9: Memory Image JPEG Encoding Process (4 of 4)

14.2.3 Memory Image JPEG Encoding Process from Host I/F (RGB format)

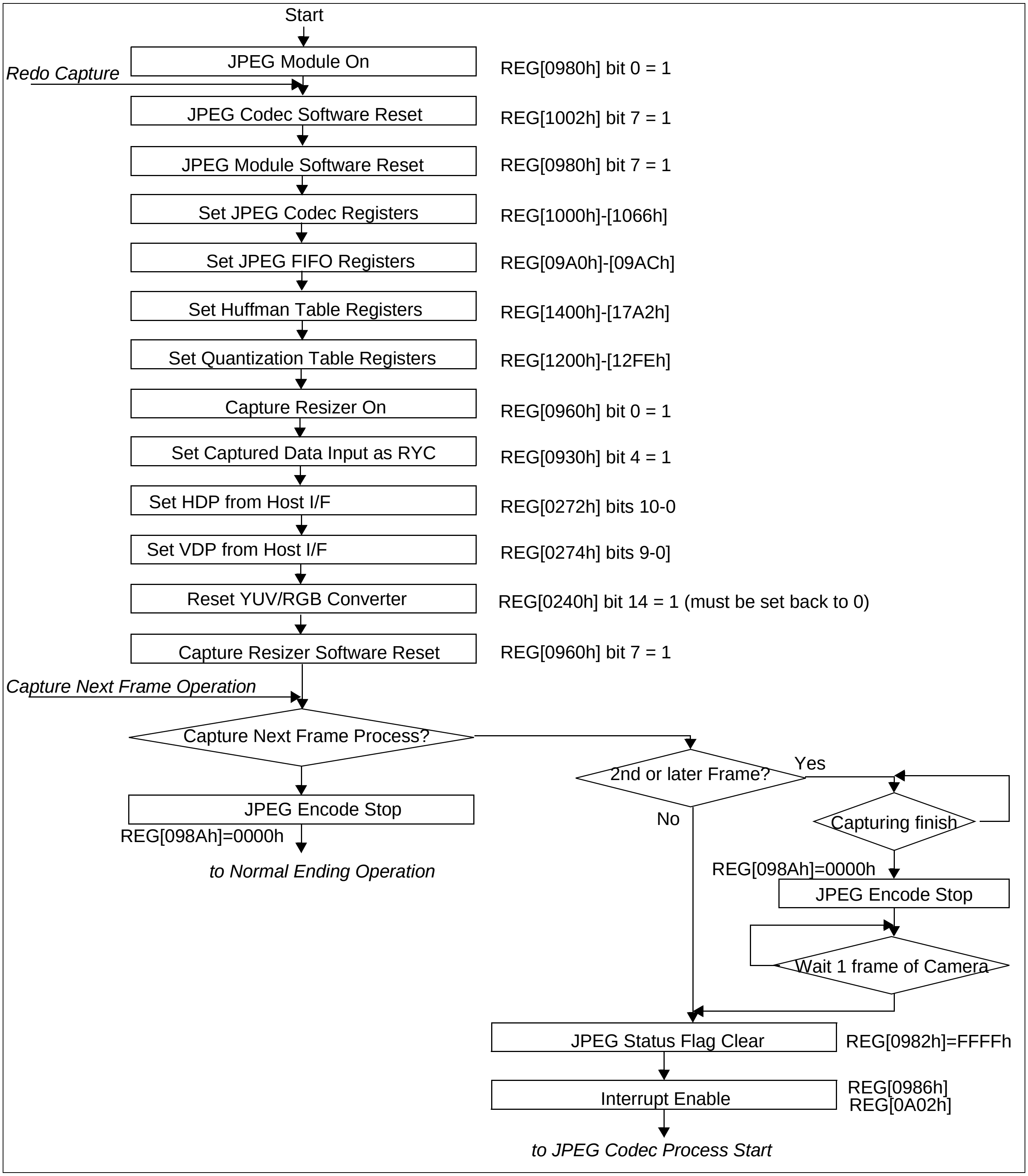


Figure 14-10: Memory Image JPEG Encoding Process from Host I/F (RGB format) (1 of 4)

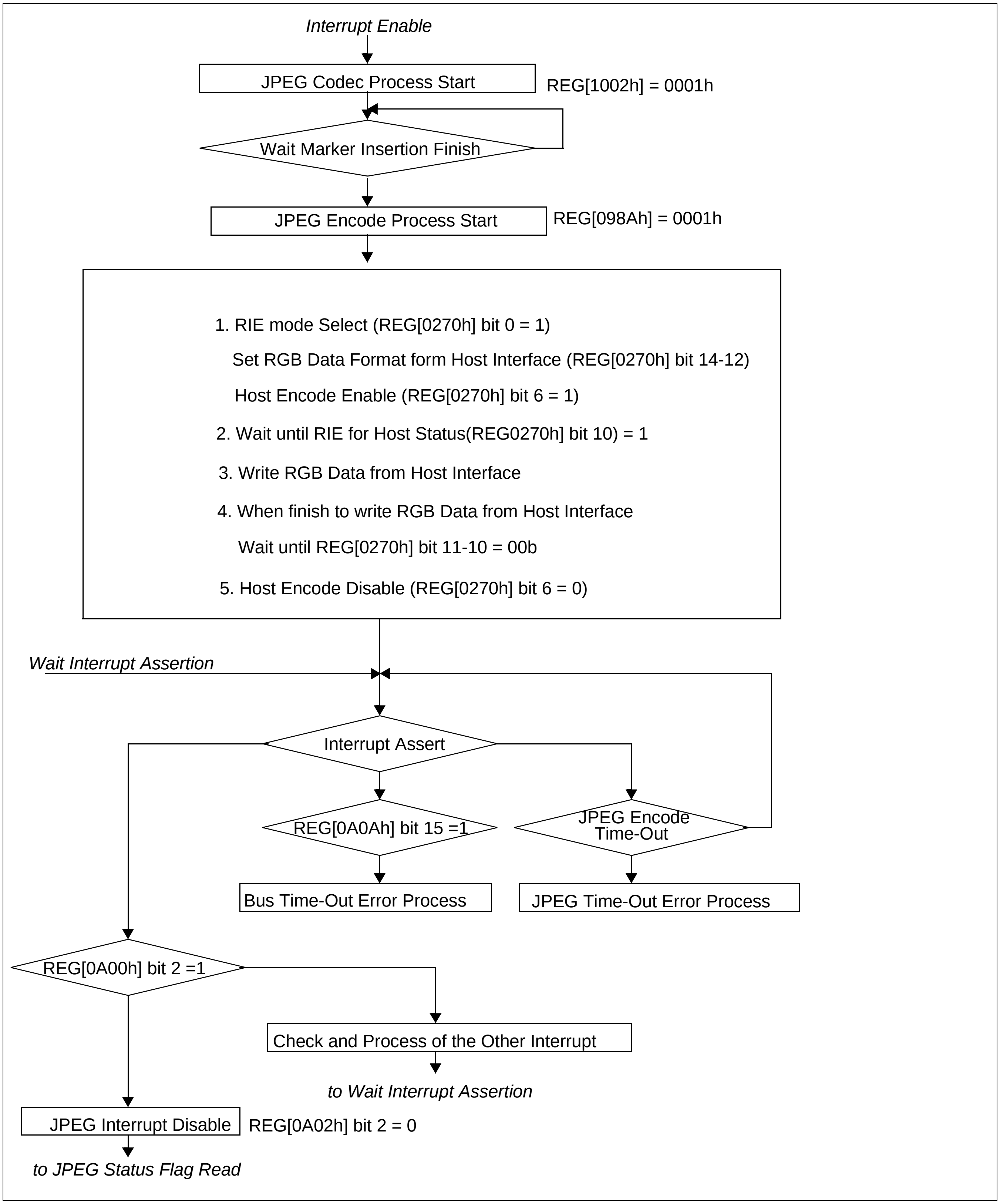


Figure 14-11: Memory Image JPEG Encoding Process from Host I/F (RGB format) (2 of 4)

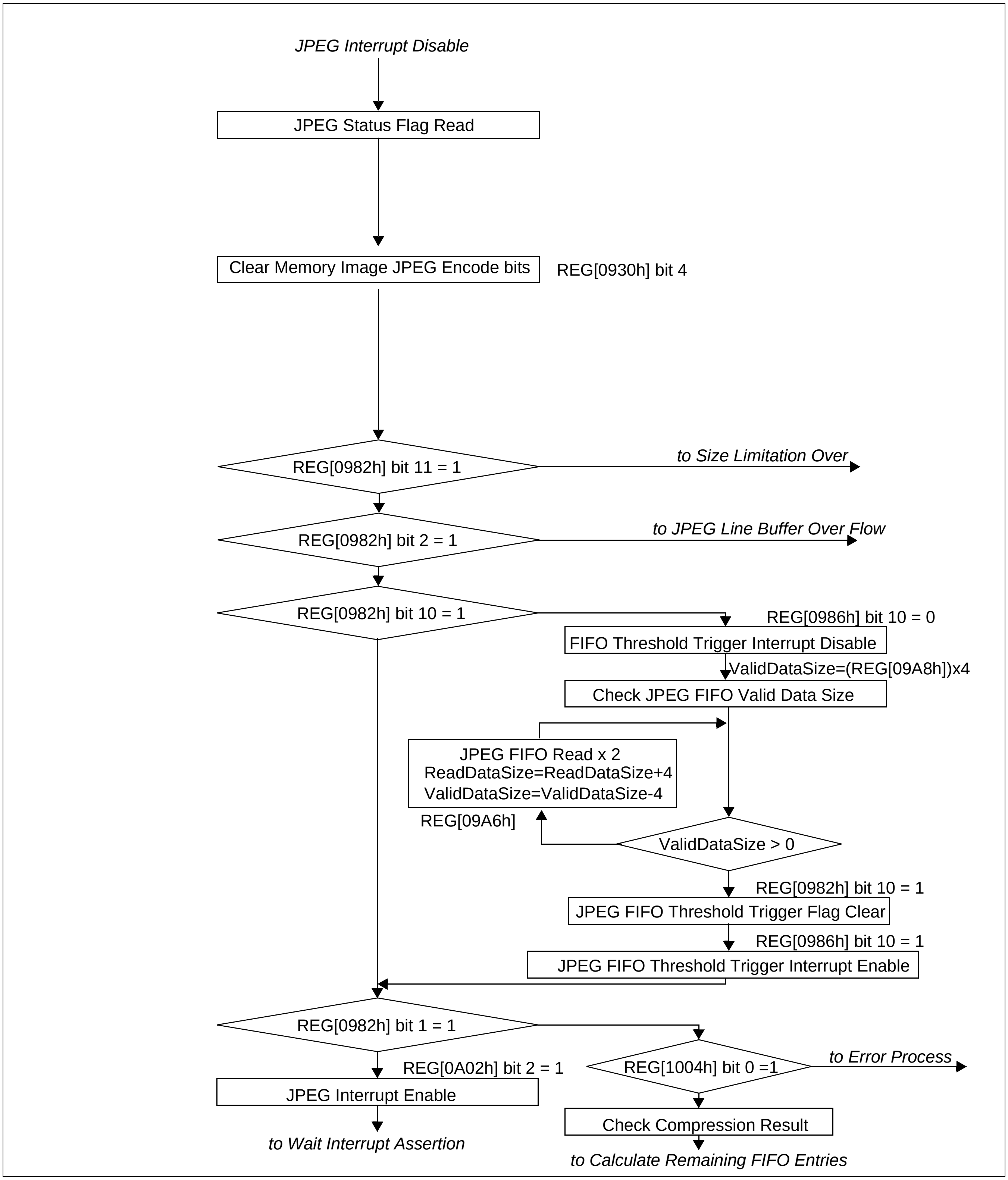


Figure 14-12: Memory Image JPEG Encoding Process from Host I/F (RGB format) (3 of 4)

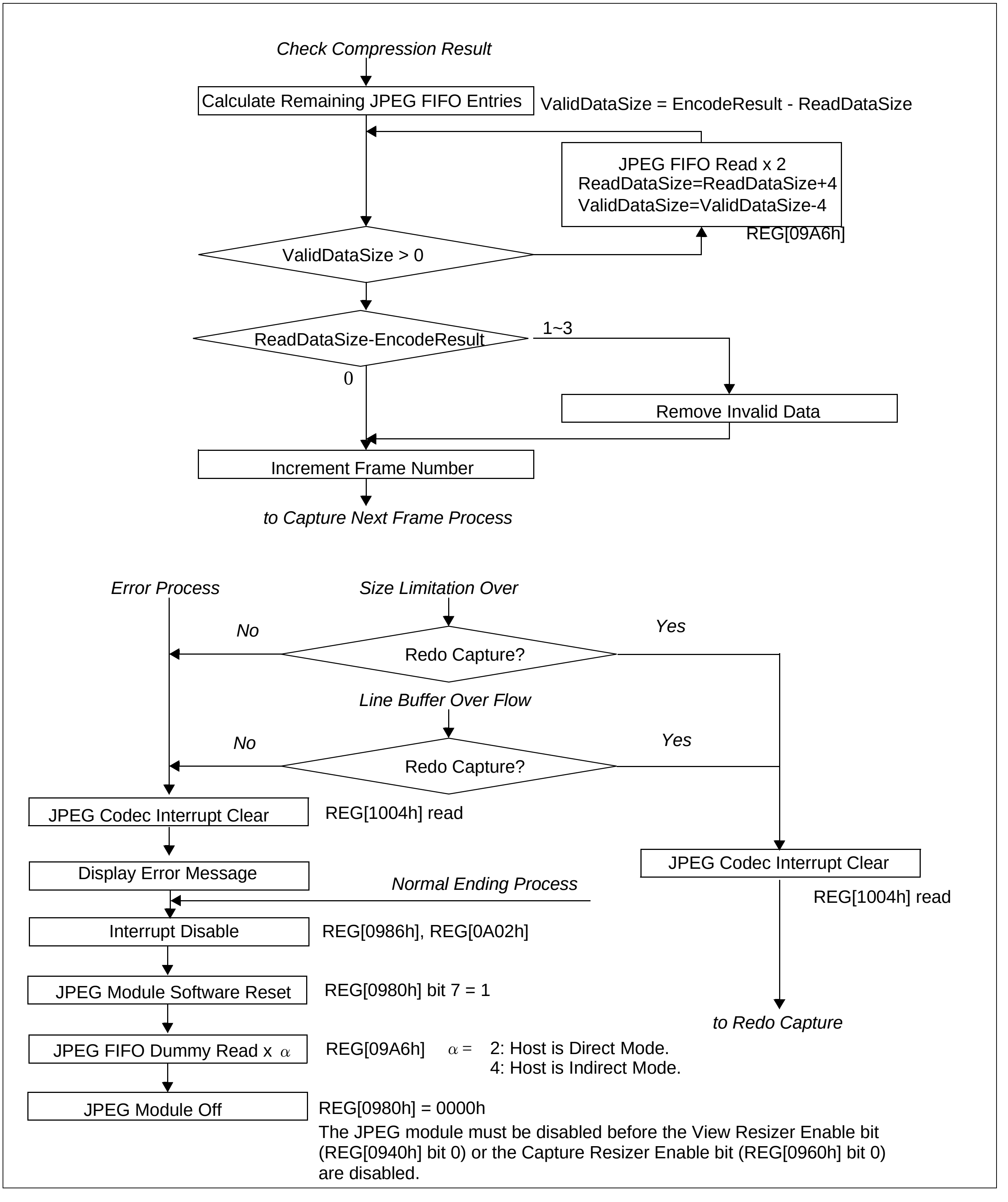


Figure 14-13: Memory Image JPEG Encoding Process from Host I/F (RGB format) (4 of 4)

14.2.4 JPEG Decoding Process

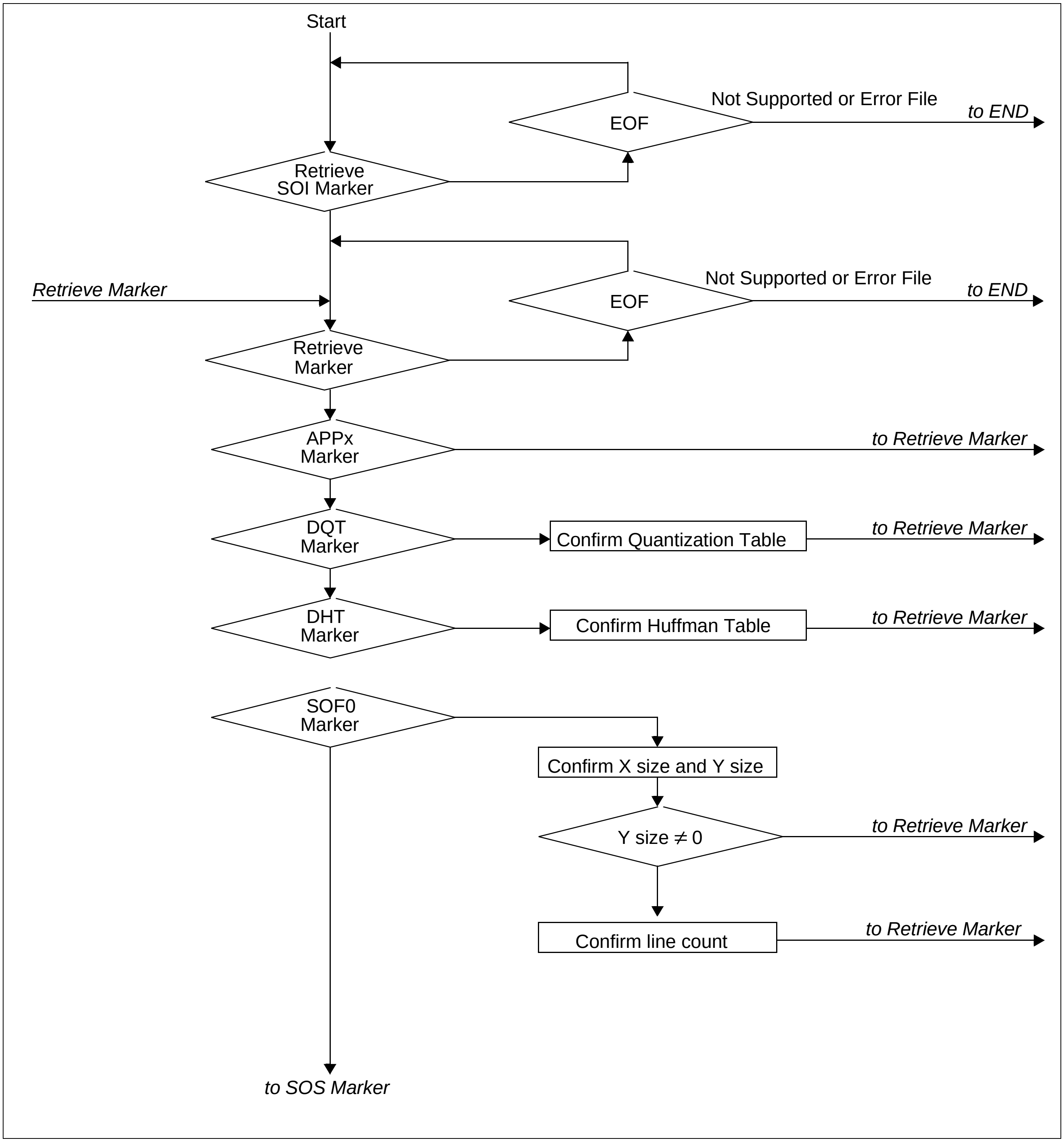


Figure 14-14: JPEG Decoding Process (1 of 6)

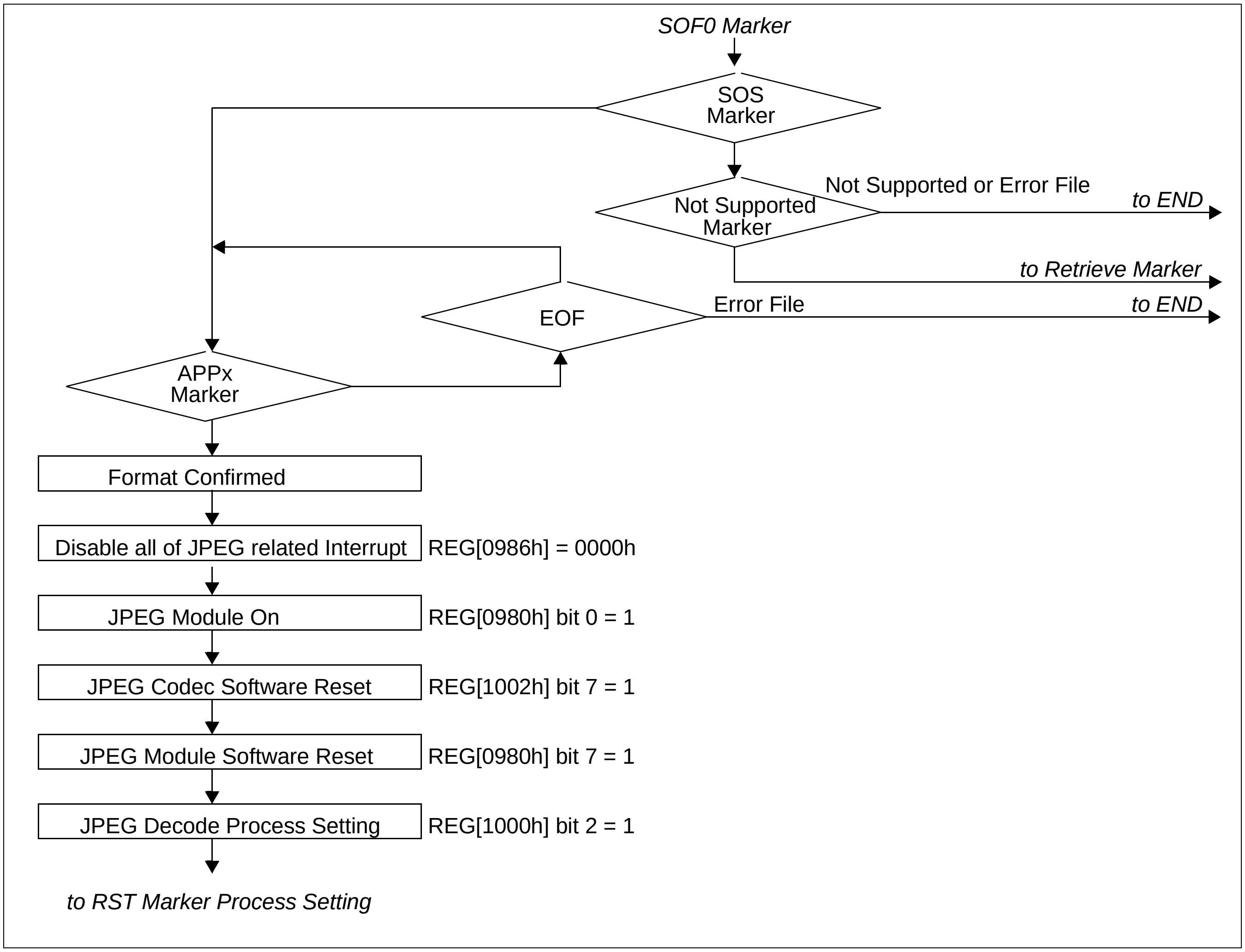


Figure 14-15: JPEG Decoding Process (2 of 6)

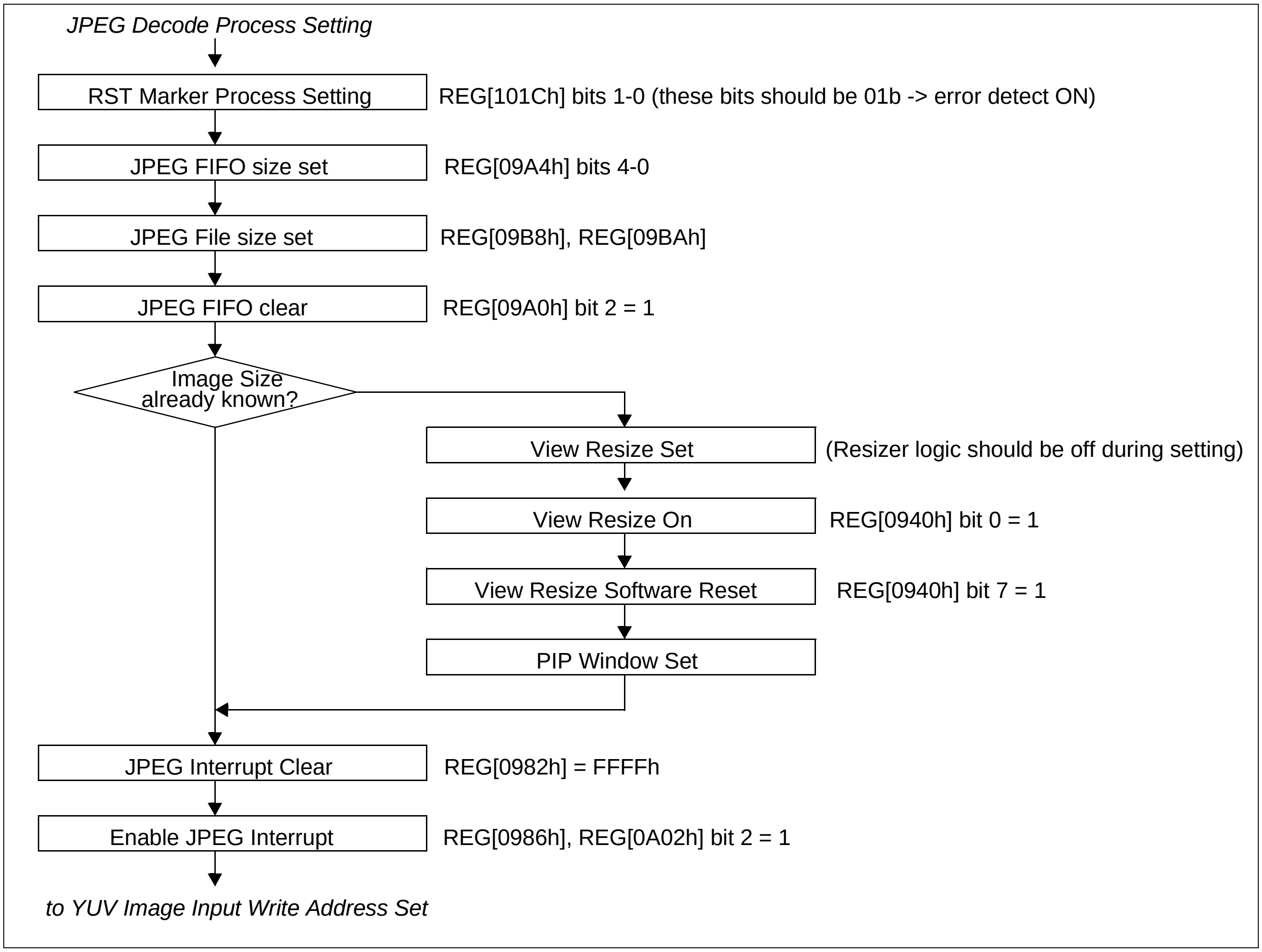


Figure 14-16: JPEG Decoding Process (3 of 6)

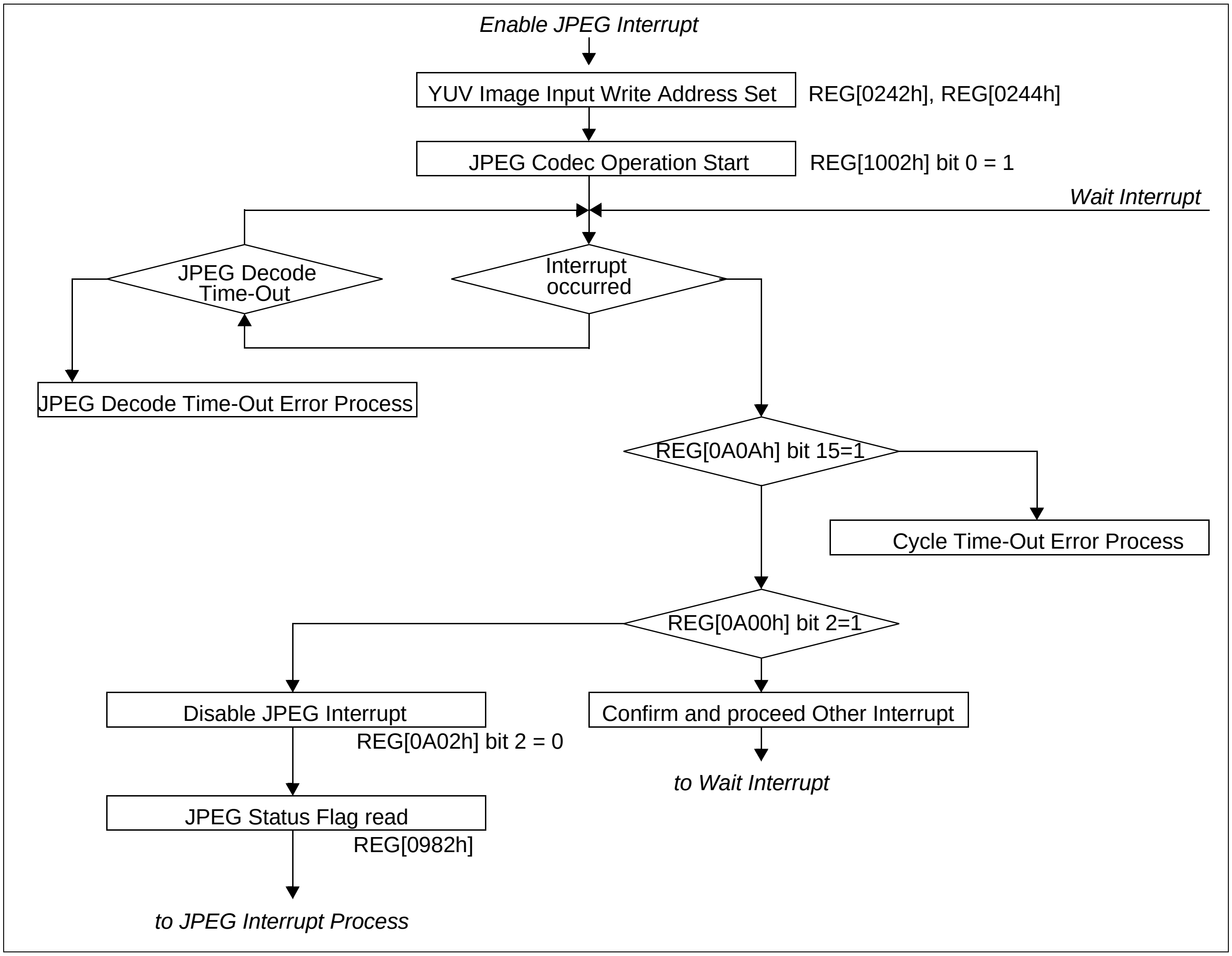


Figure 14-17: JPEG Decoding Process (4 of 6)

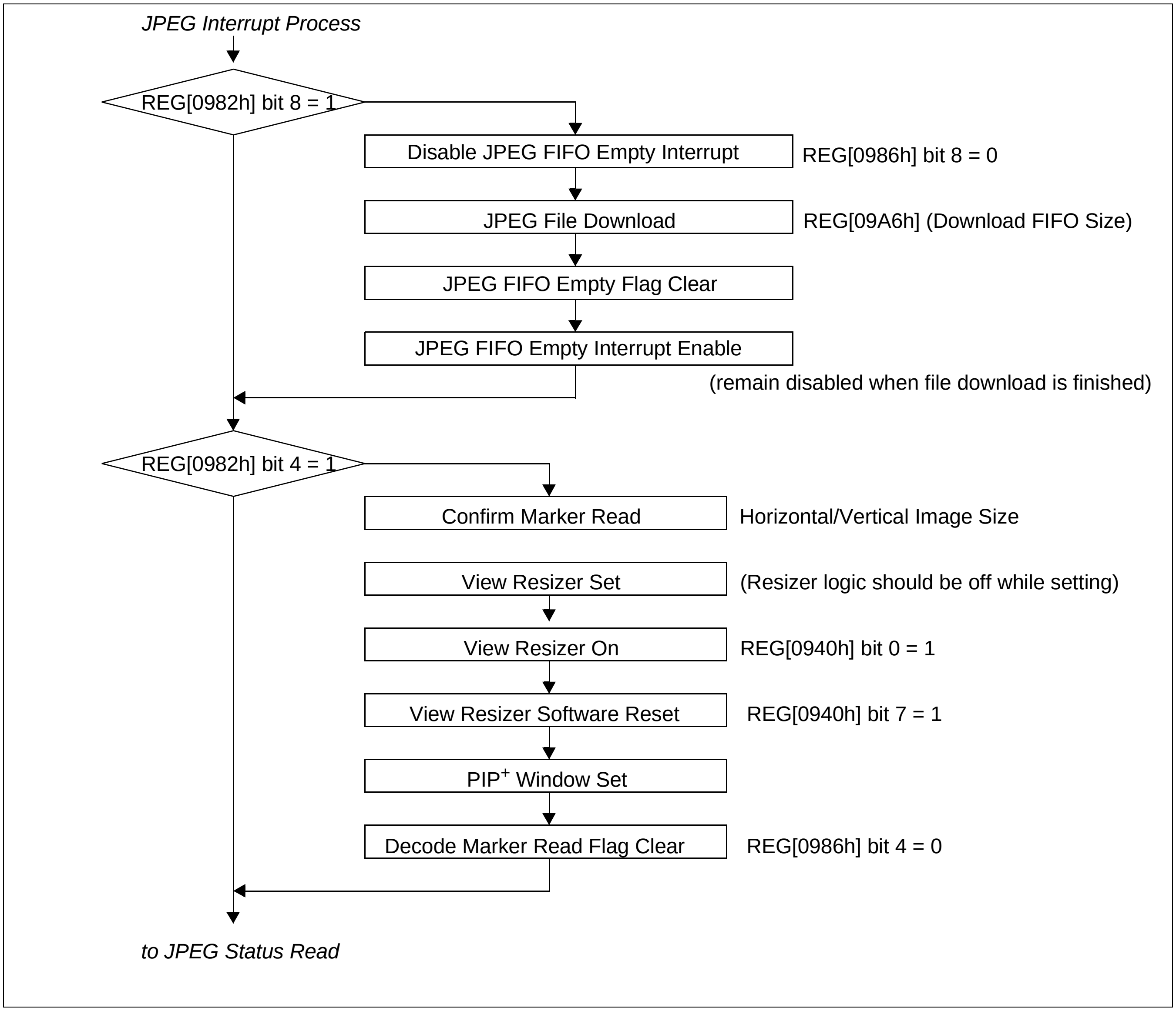


Figure 14-18: JPEG Decoding Process (5 of 6)

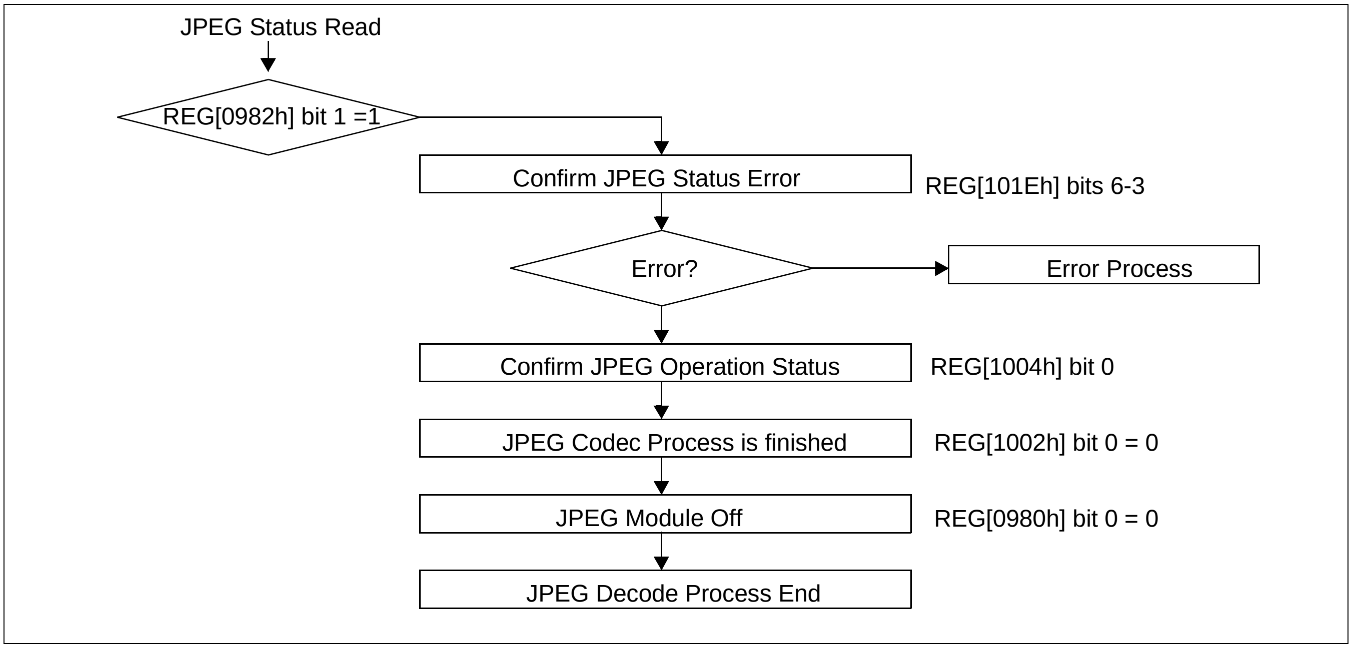


Figure 14-19: JPEG Decoding Process (6 of 6)

1. Enable the JPEG codec, set REG[0980h] bits 3-0 to 0001.
2. Initialize the JPEG Codec registers.
    a. Software reset the JPEG codec, set REG[1002h] bit 7 to 1.
    b. Select the operation mode for JPEG decoding, set REG[1000h] bit 2 = 1b.
    c. Set the RST Marker Operation Setting, set REG[101Ah].
3. Set the JPEG module registers.
    a. Enable the JPEG module and perform a JPEG software reset (REG[0980h] = 81h).
    b. Specify the JPEG FIFO size (REG[09A4h]). The FIFO size is determined using the following formula:

       JPEG FIFO size = ((REG[09A4h] bits 3-0) + 1) x 4K bytes.

       Example: for a JPEG FIFO size of 12K bytes, REG[09A4h] = 2
       (2 + 1) x 4KB = 12K bytes
    c. specify the JPEG file size, set REG[09B8h]-[09BAh].
    d. Clear the JPEG FIFO (REG[09A0h] bit 2 = 1).

4. If the image size and the YUV format are already known, set the registers for the view resizer. If they are not known, read the data after stopping the JPEG decode process using the Decode Marker Read Interrupt (REG[0986h] bit 4).
5. Start decoding process.
    a. Clear all status bits, set REG[0982h] to FFFFh
    b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0133h.
    c. Start the JPEG operation (REG[1002h] bit 0 = 1).

Host CPU Process

6. After confirming FIFO valid data size (REG[09A8h]), write data to the JPEG FIFO.
7. Wait for FIFO Empty by interrupt or polling.
   If the Decode Marker Read Interrupt is enabled, there is an interrupt between steps 6 and 7. After reading data from the registers, disable the interrupt enable and clear the interrupt. Then set the registers for the view resizer.
8. Repeat steps 6 and 7 until the end of the JPEG file is detected.
9. If the JPEG Decode Complete Interrupt is enabled, there is an interrupt when the end of file marker is written to the JPEG FIFO.
10. Verify that the JPEG decode operation is complete (REG[1004h] bit 0 = 0).

Note

When accessing the JPEG FIFO, an even number of accesses is needed for both encoding and decoding.
For the encoding process, there will be up to 3 bytes of data that is not needed. Discard this data and compare the data read to the final compressed file size in the Encode size result register (REG[09B4h]-[09B6h]).
For the decoding process, 32-bit unit data should always be written to the JPEG FIFO. Pad the end of the JPEG data stream with 00s to create 32-bits of data for the last JPEG FIFO entry.

Note

If the JPEG FIFO is accessed after the JPEG process has completed or before the JPEG process has started, any data is considered invalid and ignored.

14.2.5 YUV Data Capture

1. Set the JPEG module registers.
   a. Select the YUV data format, for YUV 4:2:2 set REG[0980h] bits 3-1 = 011b, for YUV 4:2:0 set REG[0980h] bits 3-1 = 111b.
   b. Enable the JPEG module and perform a JPEG software reset (REG[0980h] bit 7 = 1 and bit 0 = 1).
   c. Specify the JPEG FIFO size (REG[09A4h]). The FIFO size is determined using the following formula:

      JPEG FIFO size = ((REG[09A4h] bits 3-0) + 1) x 4K bytes.

      Example: for a JPEG FIFO size of 12K bytes, REG[09A4h] = 2
      (2 + 1) x 4KB = 12K bytes
   d. Clear the JPEG FIFO (REG[09A0h] bit 2 = 1).
   e. Set the JPEG FIFO Threshold Trigger (REG[09A0h] bits 5-4).
2. Set the YUV capture size.
   a. Configure the vertical pixel size (REG[100Eh]-[1010h]) and the horizontal pixel size (REG[1012h]-[1014h]). These registers are used for both the JPEG codec and YUV capture.
3. Set the Capture resizer registers (REG[0960h - 096Eh]) and reset the Capture Resizer. The vertical and horizontal dimensions must be the same as the JPEG vertical and horizontal sizes as programmed in step 2a.
4. Start capturing YUV data.
   a. Clear all status bits by writing REG[0982h] to FFFFh.
   b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0605h.
   c. To enable the JPEG FIFO for YUV Capture Mode, set REG[1002h] bit 0 as 1. The JPEG FIFO is now ready to receive YUV data.
   d. Start capturing (REG[098Ah] bit 0 = 1).

   At this stage, it is the Host CPU’s task to access the JPEG FIFO in the same way as for a JPEG Encode process. YUV data capture continues until a 0 is written to REG[098Ah] bit 0.

14.2.6 YUV Data Display

1. Set the JPEG module registers.
   a. Select the YUV data format, for YUV 4:2:2 set REG[0980h] bits 3-1 = 001b, for YUV 4:2:0 set REG[0980h] bits 3-1 = 101b.
   b. Enable the JPEG module and perform a JPEG software reset (REG[0980h] = 81h).
2. Set the YUV data display size.
   a. Configure the vertical pixel size (REG[100Eh]-[1010h]) and the horizontal pixel size (REG[1012h]-[1014h]). These registers are used for both the JPEG codec and YUV capture.
3. Set the Capture resizer registers (REG[0960h - 096Eh]) and reset the Capture Resizer. The vertical and horizontal dimensions must be the same as the JPEG vertical and horizontal sizes as programmed in step 2a.
4. Set the JPEG Line Buffer registers (If the JPEG Line Buffer empty interrupt is used).
   a. Set REG[09C6h] bit 0 =1 and set REG[0986h] bit 0 = 1.
   b. Clear the JPEG Line Buffer status bits (REG[09C0h] = FFFFh).
5. Start YUV data input.
   a. Clear all JPEG status bits (REG[0982h] = FFFFh).
   b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0001h.
   c. Write YUV data to the JPEG Line Buffer Write Port (REG[09E0h]) when the JPEG Line Buffer is empty. The following table shows the maximum data size which can be sent at one time. The minimum line unit for YUV 4:2:2 is 1, for YUV 4:2:0 it is 2. After writing the YUV data to the JPEG Line Buffer, clear the JPEG Line Buffer Empty Flag (REG[09C0h] bit 0 = 1).

Line Size	The maximum data size
> 256	Line Data Size x 16
≤ 256	Line Data Size x 32
≤ 128	Line Data Size x 64
≤ 64	Line Data Size x 128
≤ 32	Line Data Size x 256

   d. Continue writing YUV data until all the data is sent to the JPEG Line Buffer.

14.2.7 Exit Sequence

The exit sequence is the same for all cases: JPEG Decode, JPEG Encode, YUV Data Capture, and YUV Data Display.

1. Check the JPEG Operation Status bit (REG[1004h] bit 0).
2. For JPEG decode only, check the JPEG Error Status bits (REG[101Eh] bits 6-3).
3. Disable all interrupts, set REG[0986h] to 0000h.
4. Clear all status bits, set REG[0982h] to FFFFh.
5. Clear the JPEG Operation Select bit, write a 0 to REG[1000h] bit 2.
6. Perform a JPEG Software Reset, write a 1 to REG[0980h] bit 7.
7. Disable the JPEG codec, write a 0 to REG[0980h] bit 0.

15 Resizers

S1D13719 provides the function to resize the camera input data, the JPEG decode data, the display image data, and the YUV input data. There are two resizers: the View Resizer for viewing image data and the Capture Resizer for capturing image data. It is possible to use both resizers simultaneously. Resizers perform the trimming and scaling functions that can be used to “resize” image data from the camera interface and/or the JPEG decoder.

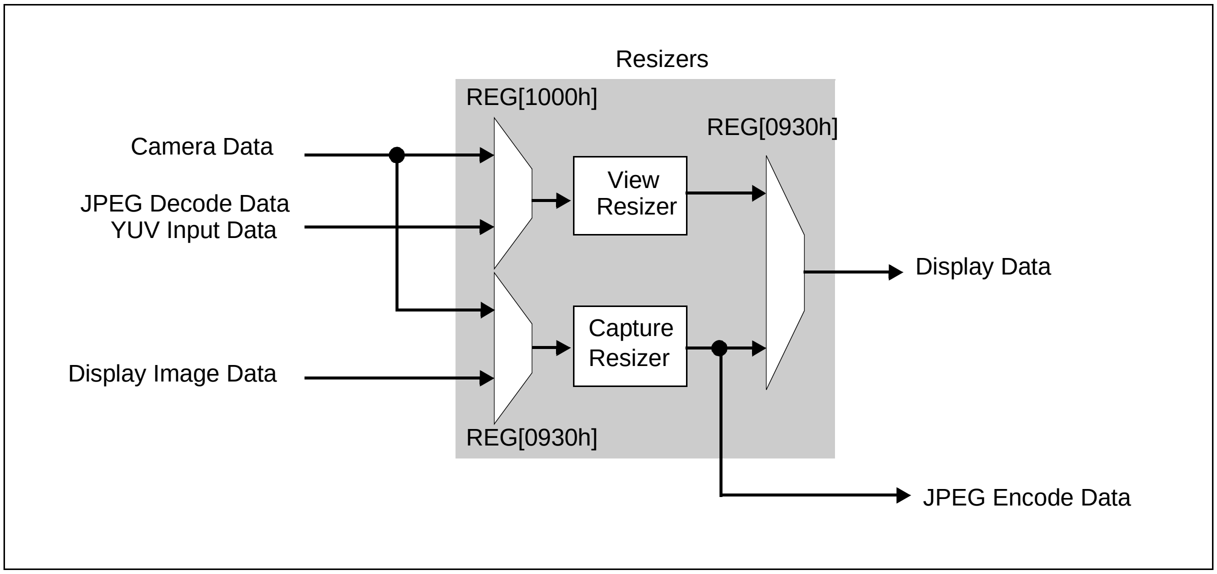


Figure 15-1: Resizer Block Diagram

15.1 View Resizer

There is View Resizer for the LCD display. YUV image data from the camera, JPEG decoded image data, and YUV data from the Host can be resized. When the encode image and the LCD display image are the same, only the capture resize can be used.

Please put YUV/RGB converter 1 into the state of reset when you encode JPEG when View Resizer is not used. (REG[0240h] bit 14 = 1)

15.2 Capture Resizer

The Capture Resizer is used for JPEG encode. Both camera image data and display image data are resized.

Table 15-1: Resizer Selection

Usage	View Resizer	Capture Resizer
Camera Image Display	available	available
JPEG Decode Image Display	available	not available
Host YUV Input Data Image Display	available	not available
JPEG Encode Image	not available	available
Host YUV Output Data Image	not available	available
Display Image JPEG Encode Image	not available	available

15.3 Trimming Function

The trimming function is similar to cropping an image and "trims" the unwanted portion of the image. The trimming is controlled using the Resizer X/Y Start/End Position registers (REG[0944h]-[094Ah] or REG[0964h]-[096Ah]). The Start and End addresses programmed in these registers are limited by the size of the actual camera image or the actual size of the decoded JPEG image and must not be set to a value greater than these actual sizes. The Start and End Position registers are set in 1 pixel increments.

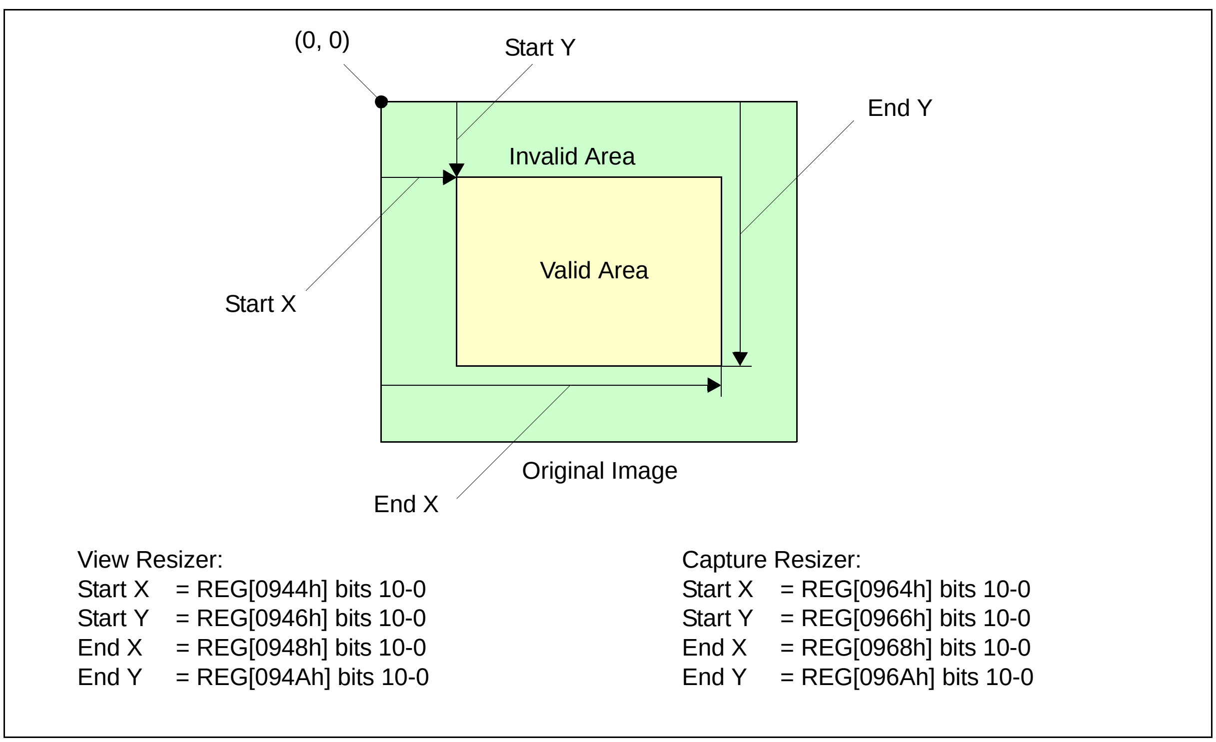


Figure 15-2: Trimming Function

15.4 Scaling Function

The scaling function takes place after the trimming stage and it specifies the desired compression ratio to be applied to the image. When image data is scaled by the capture resizer for JPEG Encoding, the JPEG Codec size registers must be set for the image size **after** scaling. The scaling function is independent in the horizontal and vertical directions and scaling rates from 128/128Å`1/128 are available. For 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 and 1/128 scaling, only the horizontal direction can be averaged.

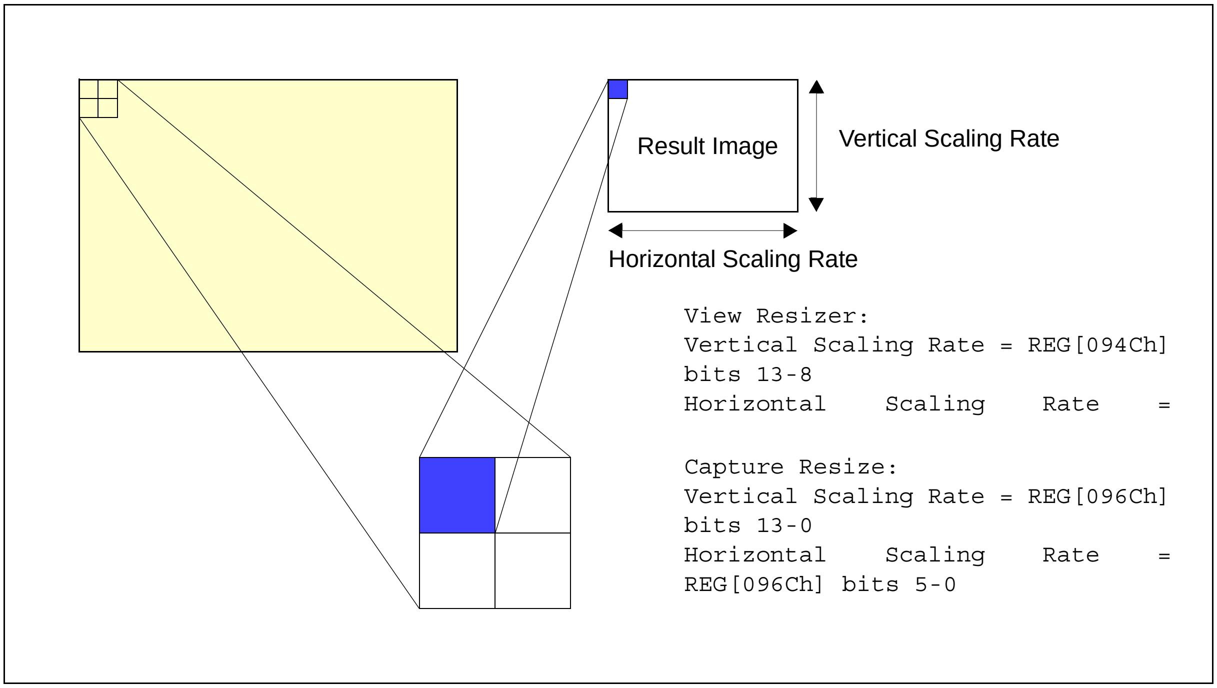


Figure 15-3: Scaling Function

15.4.1 Odd Number Scaling

For odd number scaling, one pixel is extracted from the center of the block. Both the horizontal and vertical directions use the reduction method.

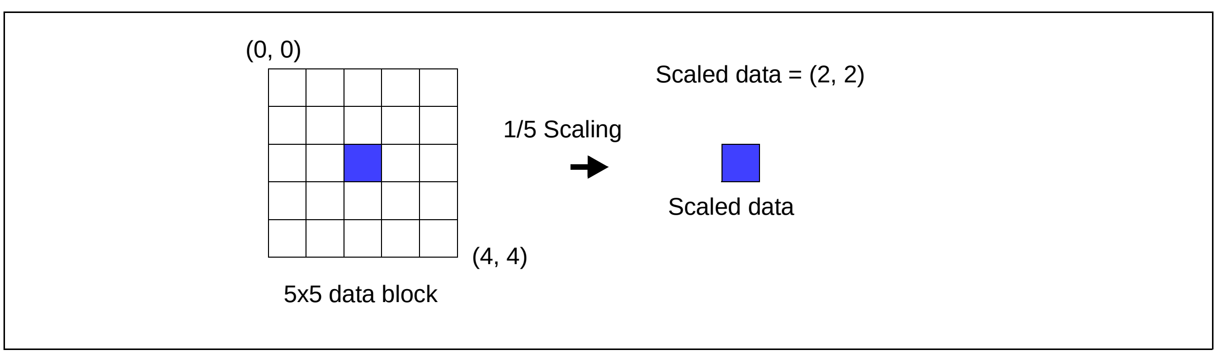


Figure 15-4: Odd number Scaling (Example: 1/5 scaling)

15.4.2 Even Number Scaling

For even number scaling, one pixel is extracted from the center of the block (as shown). Both the horizontal and vertical directions use the reduction method.

Note

For scaling ratios of 1/2, 1/4, 1/8, 1/16, 1/32 1/64 and 1/128 an horizontal average method can be used (see Section 15.4.3, “Averaging Method”).

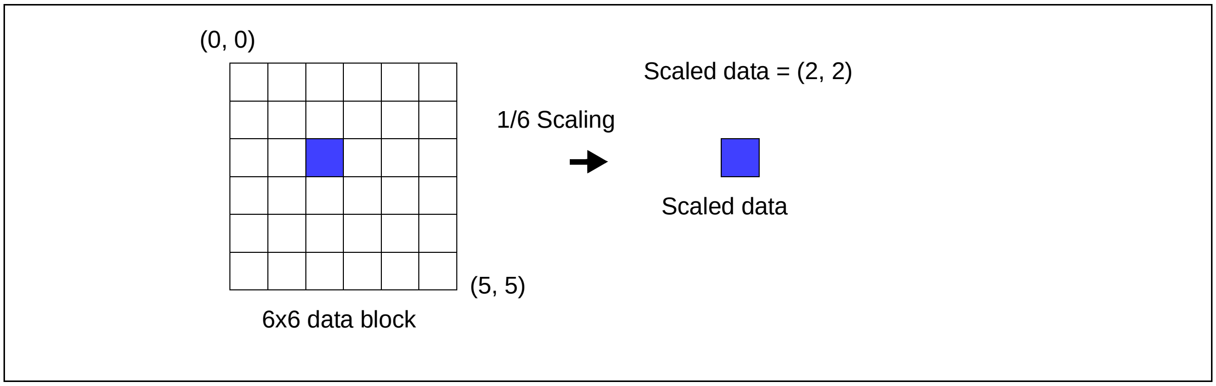


Figure 15-5: Even number Scaling (Example: 1/6 scaling)

15.4.3 Averaging Method

For scaling ratios of 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 and 1/128 one pixel is extracted from the center of the block (as shown). However, the horizontal direction is determined using an average function. The vertical direction uses the reduction method.

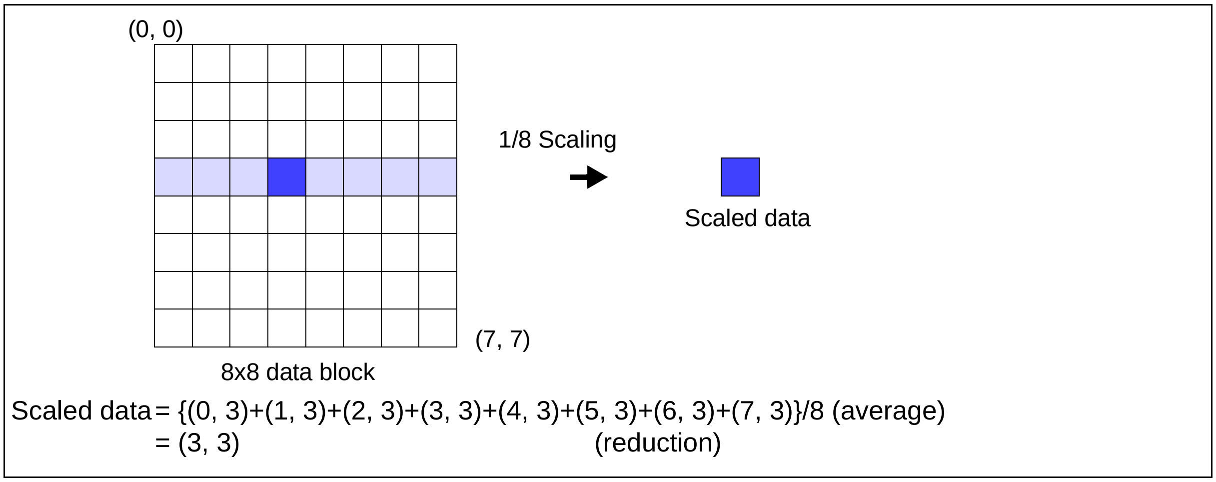


Figure 15-6: Average Method (Example: 1/8 scaling)

15.4.4 Method of calculating number of pixel after it scaled

Definition: (Unit: Pixel)

1. The size after trimming, horizontal is “A” and vertical is “B”.
2. The size after scaled, horizontal is “a” and vertical is “b”.
3. The reduction rate is horizontal “X/128” and Vertical is “Y/128”.

a = Integer value of (A x X/128).
b = Integer value of (B x Y/128).

Note

As for a and b, the calculation type is not different in the YUV format.
However, a and b that is the size after it is resized should fill the relation between the following.
YUV 4:4:4 **-** a and b of one pixel.
YUV 4:2:2 **-** In a, two pixels and b are units of one pixel.
YUV 4:2:0 **-** Unit of two pixels both a and b.
YUV 4:1:1 **-** In a, four pixels and b are units of one pixel.

16 Image Data I/O Functions

16.1 Normal JPEG Encode

The following figure shows camera image data being encoded and output to the Host as a JPEG file.

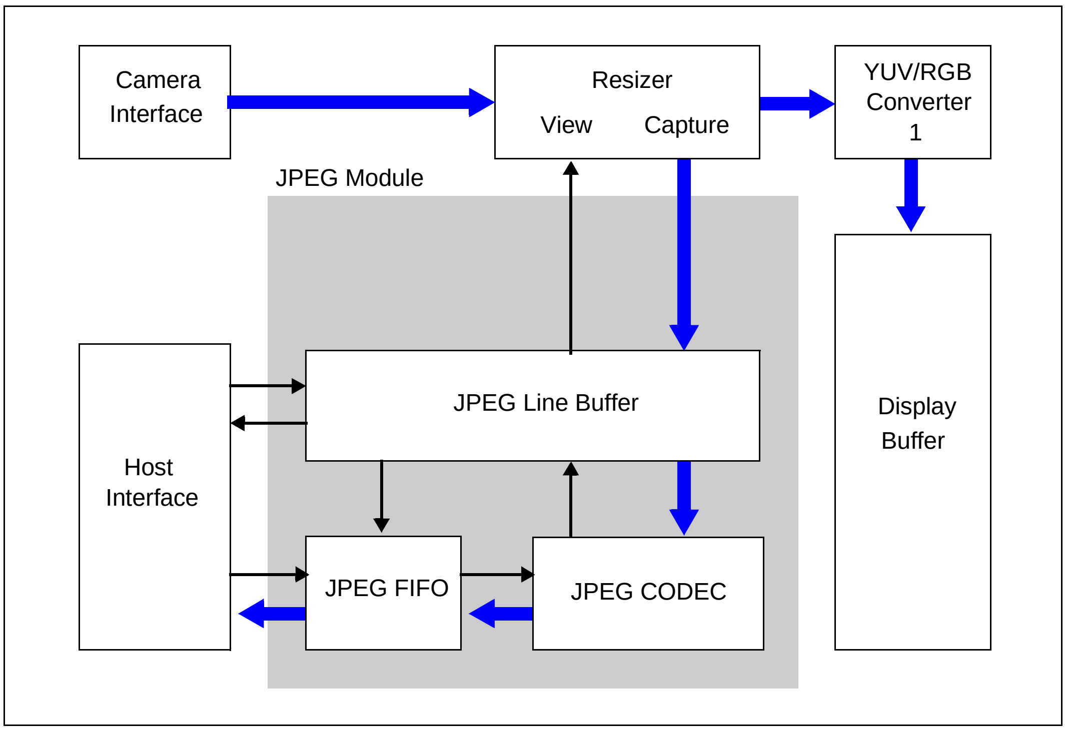


Figure 16-1: Internal JPEG Encode Data Flow

16.2 Normal JPEG Decode

The following figure shows a JPEG file from the Host being decoded and stored in the display buffer for display on the panel.

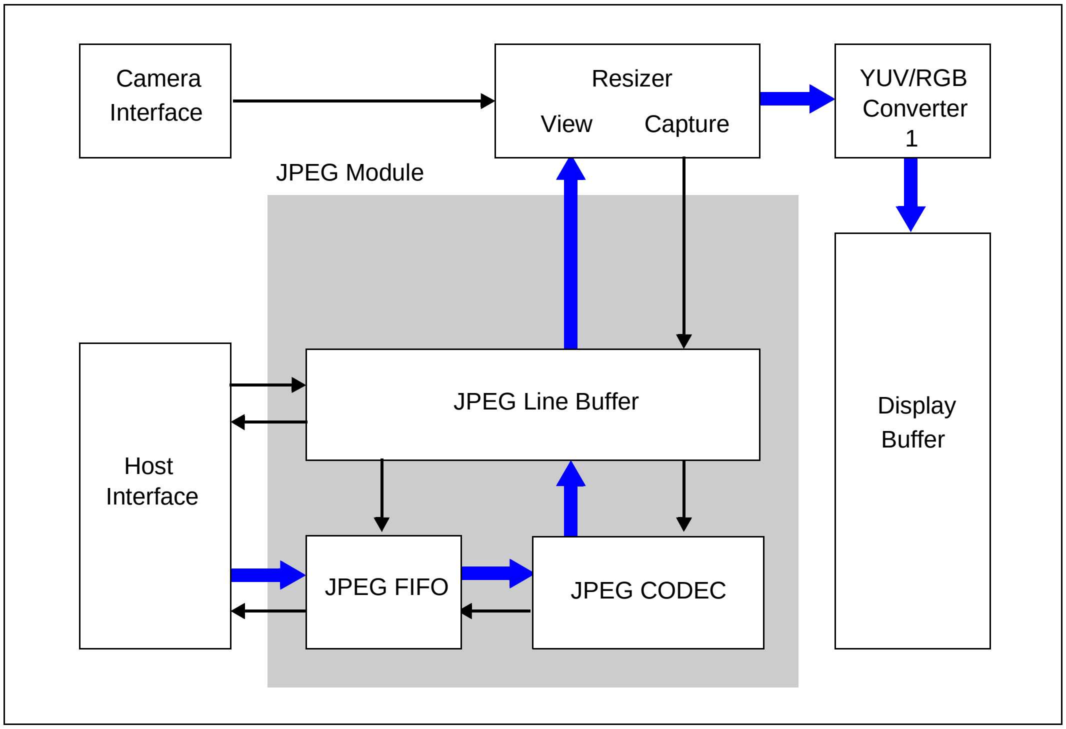


Figure 16-2: Internal JPEG Decode Data Flow

16.3 Host Input JPEG Encode

The following figure shows YUV image data from the Host being encoded into a JPEG file which is sent back to the Host.

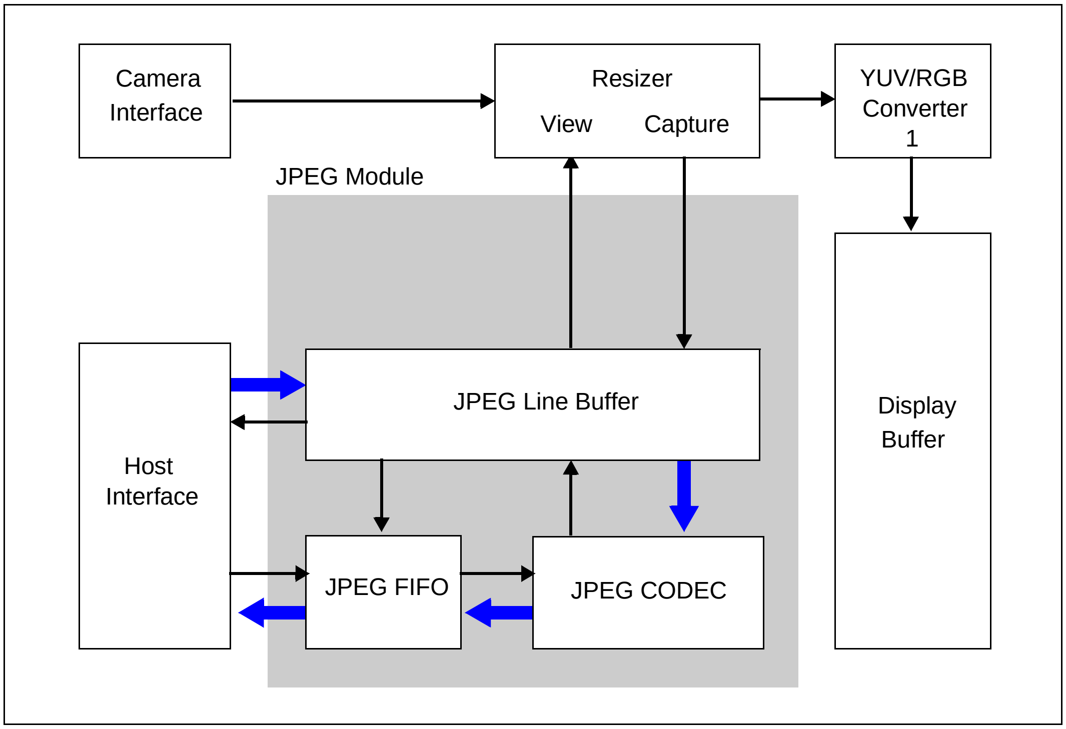


Figure 16-3: Host Input JPEG Encode Data Flow

16.4 Host Input JPEG Decode

The following figure shows a JPEG file from the Host being decoded and sent back to the Host as YUV data.

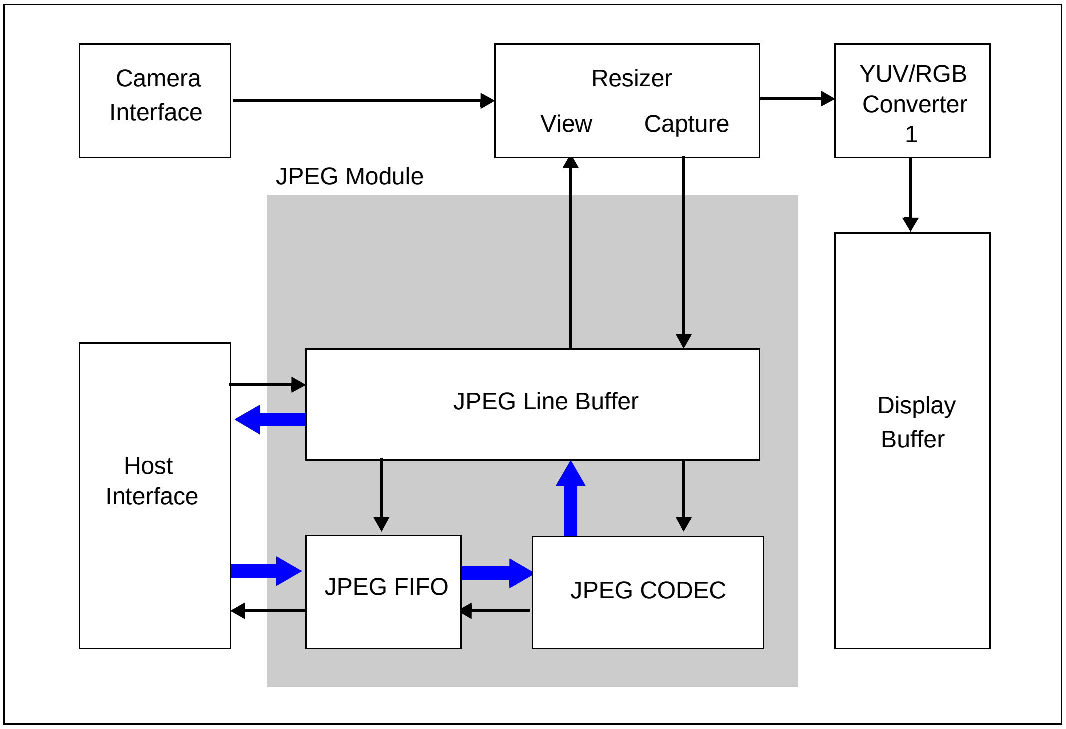


Figure 16-4: Host Input JPEG Decode Data Flow

16.5 YUV Data Output

The following figure shows YUV camera image data being stored in the display buffer and also sent to the Host.

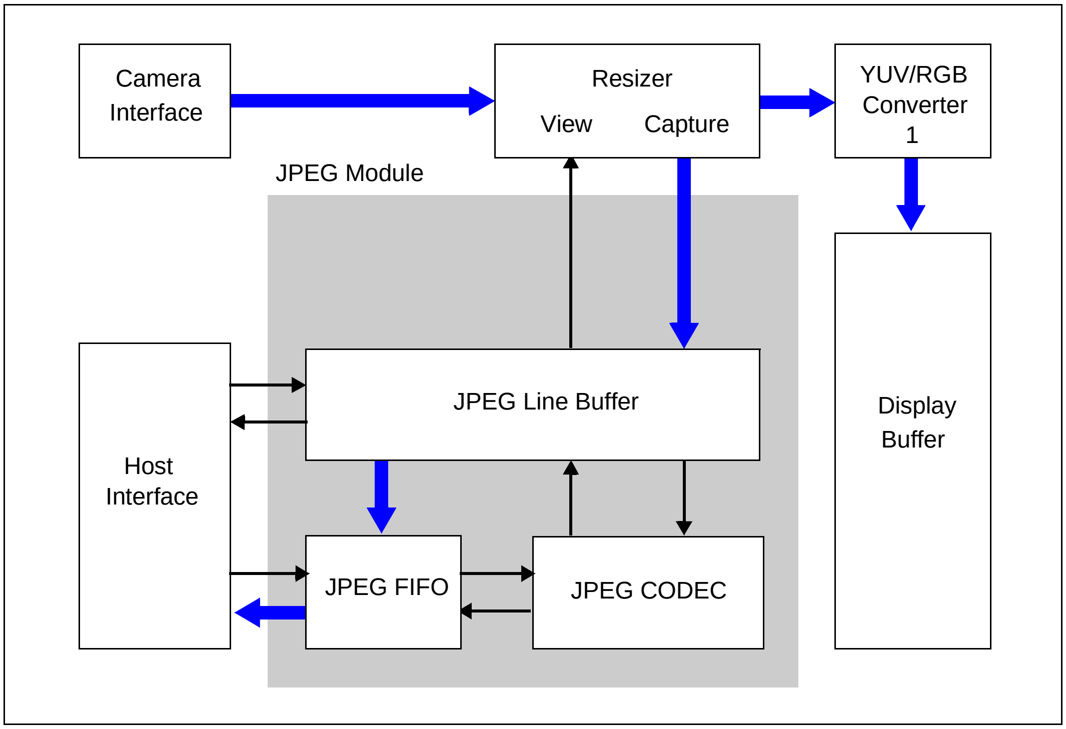


Figure 16-5: YUV Data Output Data Flow

16.6 YUV Data Input

The following figure shows YUV data from the Host being stored in the display buffer for display on the LCD panel.

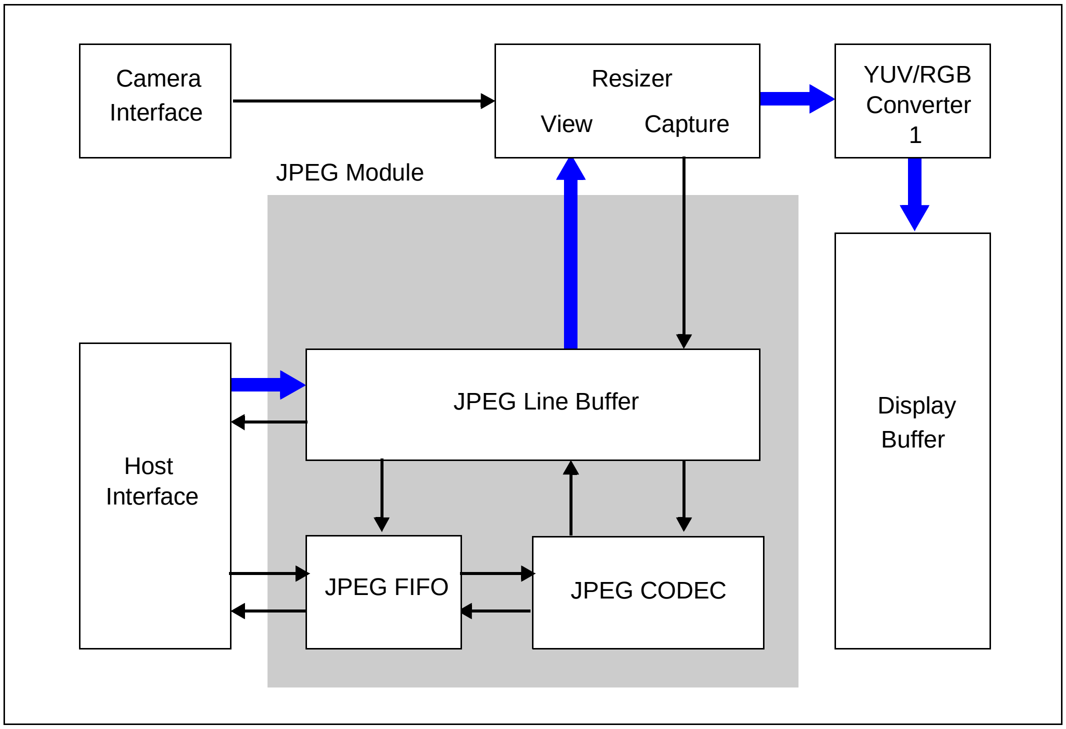


Figure 16-6: YUV Data Input Data Flow

16.7 Display Image JPEG Encode

The following figure shows display image data being encoded and output to the Host as a JPEG file.

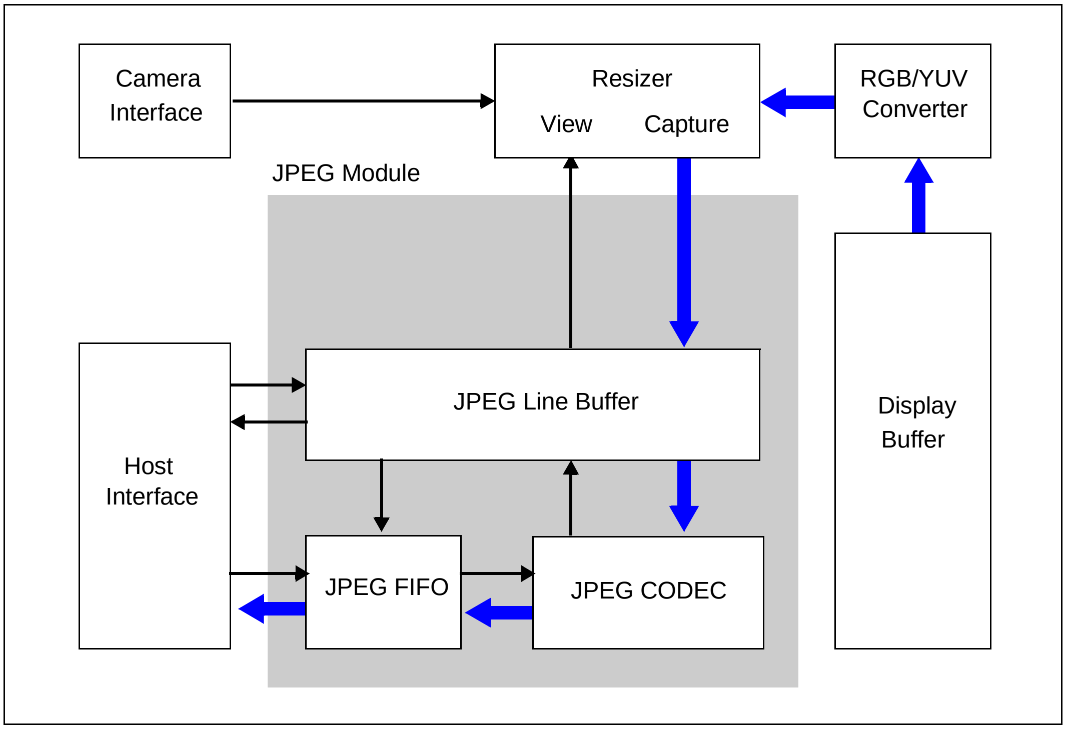


Figure 16-7: Display Image JPEG Encode Data Flow

16.8 Camera JPEG Encoded Data Output

The following figure shows Camera JPEG encoded data being stored in the display buffer and also sent to the Host.

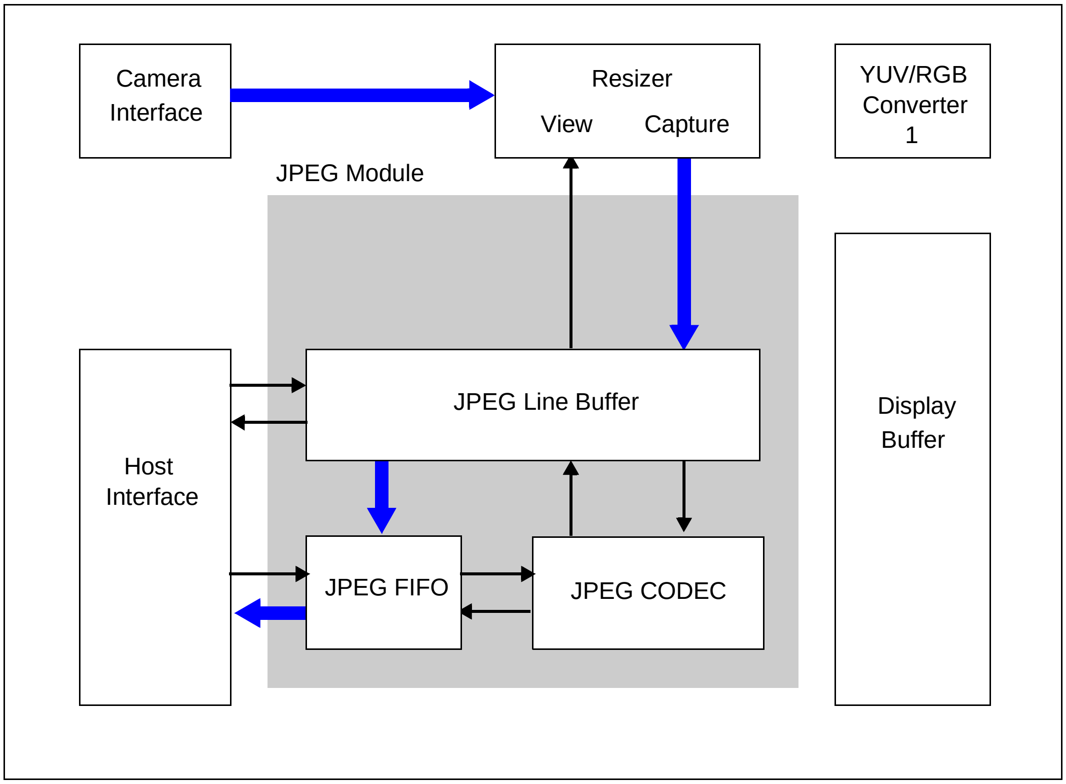


Figure 16-8: Camera JPEG encoded Data Output Data Flow

Note
This data flow corresponds to the JPEG compression function of Toshiba CMOS camera (ET8E90-AS).

16.9 YUV Data Input/Output Format

This section shows the data format for YUV data input/output when the JPEG codec is bypassed. YUV data is output from JPEG FIFO. YUV data is input from the JPEG line buffer.

16.9.1 YUV 4:2:2 Data Input/Output Format

Data output at YUV 4:2:2 (REG[0980h] bits 3-1 = 011b)

Data input at YUV 4:2:2 (REG[0980h] bits 3-1 = 001b)

Table 16-1: YUV 4:2:2 Data IO Format

Cycle Count	1	2	3	4	...	2n+1	2n+2
D15	Y_0^7	Y_1^7	Y_2^7	Y_3^7	...	Y_{2n}^7	Y_{2n+1}^7
D14	Y_0^6	Y_1^6	Y_2^6	Y_3^6	...	Y_{2n}^6	Y_{2n+1}^6
D13	Y_0^5	Y_1^5	Y_2^5	Y_3^5	...	Y_{2n}^5	Y_{2n+1}^5
D12	Y_0^4	Y_1^4	Y_2^4	Y_3^4	...	Y_{2n}^4	Y_{2n+1}^4
D11	Y_0^3	Y_1^3	Y_2^3	Y_3^3	...	Y_{2n}^3	Y_{2n+1}^3
D10	Y_0^2	Y_1^2	Y_2^2	Y_3^2	...	Y_{2n}^2	Y_{2n+1}^2
D9	Y_0^1	Y_1^1	Y_2^1	Y_3^1	...	Y_{2n}^1	Y_{2n+1}^1
D8	Y_0^0	Y_1^0	Y_2^0	Y_3^0	...	Y_{2n}^0	Y_{2n+1}^0
D7	U_0^7	V_0^7	U_2^7	V_2^7	...	U_{2n}^7	V_{2n+1}^7
D6	U_0^6	V_0^6	U_2^6	V_2^6	...	U_{2n}^6	V_{2n+1}^6
D5	U_0^5	V_0^5	U_2^5	V_2^5	...	U_{2n}^5	V_{2n+1}^5
D4	U_0^4	V_0^4	U_2^4	V_2^4	...	U_{2n}^4	V_{2n+1}^4
D3	U_0^3	V_0^3	U_2^3	V_2^3	...	U_{2n}^3	V_{2n+1}^3
D2	U_0^2	V_0^2	U_2^2	V_2^2	...	U_{2n}^2	V_{2n+1}^2
D1	U_0^1	V_0^1	U_2^1	V_2^1	...	U_{2n}^1	V_{2n+1}^1
D0	U_0^0	V_0^0	U_2^0	V_2^0	...	U_{2n}^0	V_{2n+1}^0

17 Image Data Conversion

17.1 YUV to RGB Converter 1 (YRC1)

The YRC1 converts YUV input data from the camera interface (YUV 4:2:2), or JPEG decoded image data (YUV 4:4:4, 4:2:2, 4:1:1, 4:2:0) into RGB 5:6:5 format and writes the data to the display buffer.

If the YRC1 is disabled (or bypassed), the YRC1 can write YUV 4:2:2 data directly to the display buffer.

Table 17-1: YRC1 Output Format

Format	Resolution	Main Window	PIP$^+$ Window	Register
RGB 5:6:5	16 bpp	available	available	REG[0240h] bit 15 = 0
YUV 4:2:2	24 bpp	not available	available	REG[0240h] bit 15 = 1

17.1.1 Rectangular Area Write Mode

Writes to the display buffer can be done as a rectangular area. The LCD display needs to be set with the same value as the Window Line Address Offset register (REG[0216h] / REG[021Eh]).

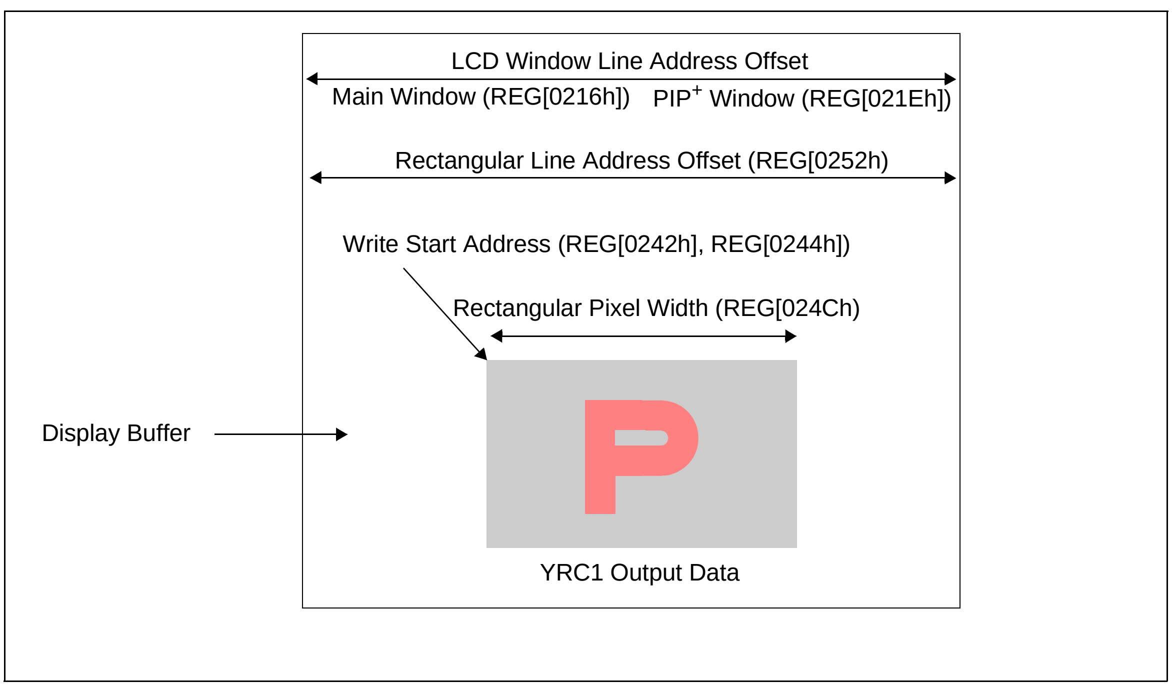


Figure 17-1: YRC1 Rectangular Area Write Mode

17.1.2 UV Data Fix

The YRC1 can fix the U or V data to the values as specified in the YRC1 UV Data Fix register (REG[024Eh]). The data is changed during writing of data to the display buffer.

Table 17-2: YRC1 UV Data Fix

U Data Fix	V Data Fix	Register
not available	not available	REG[0240h] bits 6-5= 00b
available	not available	REG[0240h] bits 6-5= 01b
not available	available	REG[0240h] bits 6-5= 10b
available	available	REG[0240h] bits 6-5= 11b

17.1.3 YUV/RGB Conversion

The YUV/RGB conversion done by the YRC1 uses the following coefficient tables and conversion types.

Conversion Coefficient Table

Table 17-3: YUV/RGB Conversion Coefficient Table

Conversion Mode	REG[0240h] bits 2-0	Color	Ey	Epb	Epr
Recommendation ITU-R BT.709	001b	E_R	1.000	0.000	1.575
		E_G	1.000	-0.187	-0.468
		E_B	1.002	1.855	0.000
Recommendation ITU-R BT.470-6 System M	100b	E_R	1.000	0.001	1.400
		E_G	1.000	-0.333	-0.712
		E_B	1.000	1.780	0.002
Recommendation ITU-R BT.470-6 System B, G	101b	E_R	1.000	0.000	1.402
		E_G	1.000	-0.344	-0.714
		E_B	1.000	1.772	0.000
SMPTE 170M	110b	E_R	1.000	0.000	1.402
		E_G	1.000	-0.344	-0.714
		E_B	1.000	1.772	0.000
SMPTE 240M(1987)	111b	E_R	1.000	0.000	1.576
		E_G	1.000	-0.226	-0.477
		E_B	1.000	1.826	0.000

Conversion Equation

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} E_R E_y & E_R E_{pb} & E_R E_{pr} \\ E_G E_y & E_G E_{pb} & E_G E_{pr} \\ E_B E_y & E_B E_{pb} & E_B E_{pr} \end{bmatrix} \cdot \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

Figure 17-2: YUV/RGB Conversion Equation

17.2 YUV to RGB Converter 2 (YRC2)

The YRC2 converts YUV format data (YUV 4:2:2) to RGB 8:8:8 format and transfers the data to LUT2.

Table 17-4: YRC2 Input Format

Format	Color Depth	YRC2	Register
YUV 4:2:2	24 bpp	USE	REG[0234h] -REG[023Fh]

17.2.1 YUV/RGB Conversion

The YUV/RGB conversion used by the YRC2 uses the following coefficient tables and conversion types.

Conversion Coefficient Table

Table 17-5: YUV/RGB Conversion Coefficient Table

Conversion Mode	REG[0240h] bits 2-0	Color	Ey	Epb	Epr
Recommendation ITU-R BT.709	001b	E_R	1.000	0.000	1.575
		E_G	1.000	-0.187	-0.468
		E_B	1.002	1.855	0.000
Recommendation ITU-R BT.470-6 System M	100b	E_R	1.000	0.001	1.400
		E_G	1.000	-0.333	-0.712
		E_B	1.000	1.780	0.002
Recommendation ITU-R BT.470-6 System B, G	101b	E_R	1.000	0.000	1.402
		E_G	1.000	-0.344	-0.714
		E_B	1.000	1.772	0.000
SMPTE 170M	110b	E_R	1.000	0.000	1.402
		E_G	1.000	-0.344	-0.714
		E_B	1.000	1.772	0.000
SMPTE 240M(1987)	111b	E_R	1.000	0.000	1.576
		E_G	1.000	-0.226	-0.477
		E_B	1.000	1.826	0.000

Conversion Equation

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} E_R E_y & E_R E_{pb} & E_R E_{pr} \\ E_G E_y & E_G E_{pb} & E_G E_{pr} \\ E_B E_y & E_B E_{pb} & E_B E_{pr} \end{bmatrix} \cdot \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

Figure 17-3: YUV/RGB Conversion Equation

17.2.2 UV Data Fix

The YRC1 can fix the U or V data to the values as specified in the YRC2 UV Data Fix register (REG[023Ch]). The data is changed during writing of data to the display buffer.

Table 17-6: YRC2 UV Data Fix

U Data Fix	V Data Fix	Register
not available	not available	REG[023Ch] bits 13-12 = 00b
available	not available	REG[023Ch] bits 13-12 = 01b
not available	available	REG[023Ch] bits 13-12 = 10b
available	available	REG[023Ch] bits 13-12 = 11b

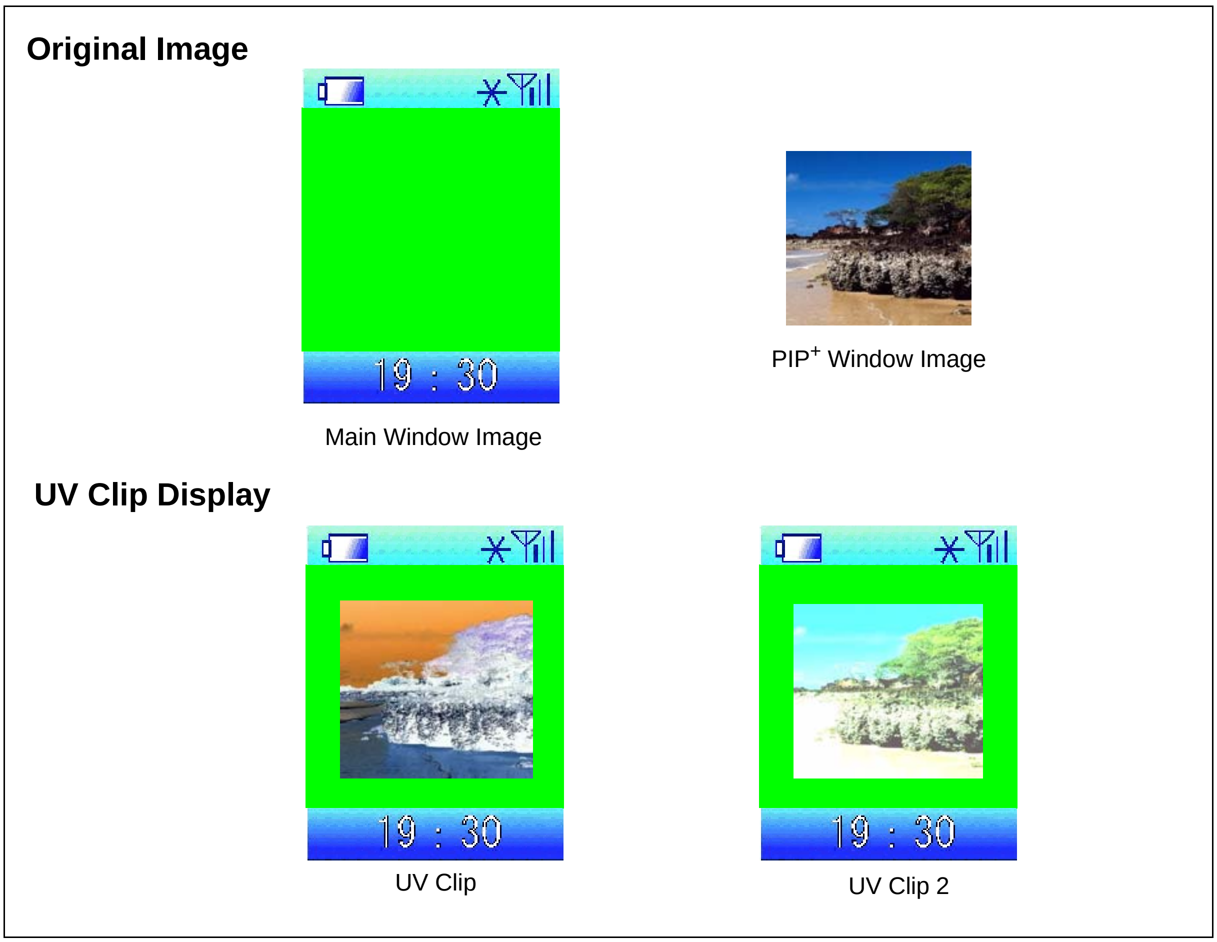


Figure 17-4: UV Clip Display

17.3 RGB to YUV Converter (RYC)

The RYC converts RGB 8:8:8 data from the display FIFO to YUV format and sends it to the capture resizer.

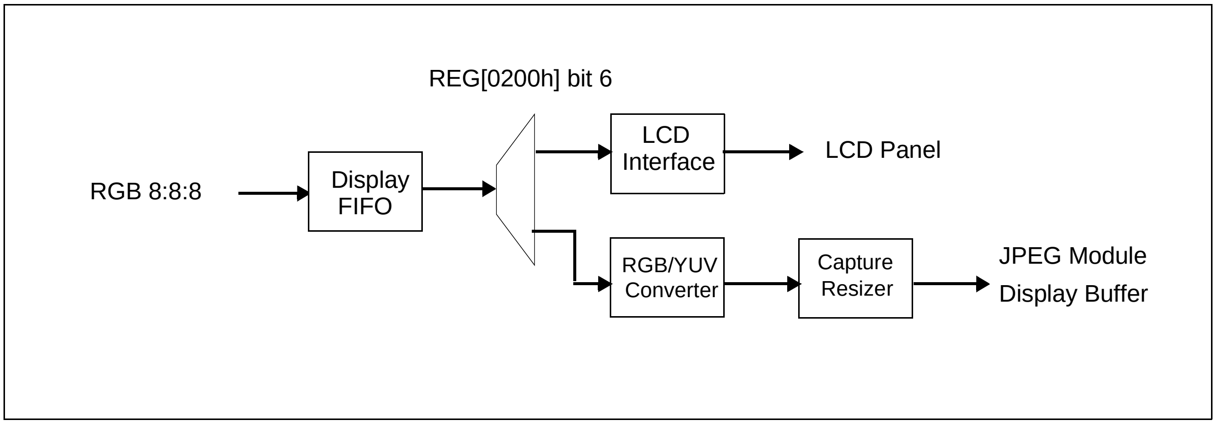


Figure 17-5: RYC Block Diagram

17.3.1 Image Size

When the RGB to YUV Converter (RYC) is enabled, the image size from the display FIFO and the resize size from the capture resizer change as follows.

Table 17-7: RYC Image Size

Memory Image JPEG Encode (REG[0200h] bit 6)	Horizontal Image Size	Vertical Image Size	RYC Output
Disabled	REG[0042h] / REG[0058h]	REG[004Ch] / REG[005Ah]	Display FIFO Data
Enabled	REG[0264h]	REG[0266h]	Stop

Table 17-8: RYC Resize Size

Memory Image JPEG Encode (REG[0200h] bit 6)	Horizontal Resize Size	Vertical Resize Size	RYC Output
Disabled	REG[0964h] / REG[0968h]	REG[0966h] / REG[096Ah]	Stop
Enabled	REG[0264h]	REG[0966h]	Display FIFO Data

17.3.2 LCD Panel Output

The output data to the LCD panel must be stopped when the RGB/YUV Converter is enabled. The LCD panel output data will become unstable and display blank (REG[0202h] bit 8) should be enabled for RGB interface type panels. Data is not output to the LCD panel for parallel/serial interface LCD panels.

17.3.3 RGB/YUV Conversion

The RGB/YUV conversion used by the RGB/YUV Converter uses the following coefficient tables and conversion types.

Conversion Coefficient Table

Table 17-9: RGB/YUV Conversion Coefficient Table

Conversion Mode	REG[0260h] bits 2-0	Color	E’g	E’b	E’r
Recommendation ITU-R BT.709	001b	Y (E’y)	0.7152	0.0722	0.2126
		U (E’pb)	-0.3860	0.5000	-0.1150
		V (E’pr)	-0.4540	-0.0460	0.5000
Recommendation ITU-R BT.470-6 System M	100b	Y (E’y)	0.5900	0.1100	0.3000
		U (E’pb)	-0.3310	0.5000	-0.1690
		V (E’pr)	-0.4210	-0.0790	0.5000
Recommendation ITU-R BT.470-6 System B, G	101b	Y (E’y)	0.5870	0.1140	0.2990
		U (E’pb)	-0.3310	0.5000	-0.1690
		V (E’pr)	-0.4190	-0.0810	0.5000
SMPTE 170M	110b	Y (E’y)	0.5870	0.1140	0.2990
		U (E’pb)	-0.3310	0.5000	-0.1690
		V (E’pr)	-0.4190	-0.0810	0.5000
SMPTE 240M(1987)	111b	Y (E’y)	0.7010	0.0870	0.2120
		U (E’pb)	-0.3840	0.5000	-0.1160
		V (E’pr)	-0.4450	-0.0550	0.5000

Conversion Equation

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} E'g & E'b & E'r \\ E'g & E'b & E'r \\ E'g & E'b & E'r \end{bmatrix} \cdot \begin{bmatrix} G \\ B \\ R \end{bmatrix} \qquad \begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} \frac{219}{255} & 0 & 0 \\ 0 & \frac{224}{255} & 0 \\ 0 & 0 & \frac{224}{255} \end{bmatrix} \cdot \begin{bmatrix} Y \\ U \\ V \end{bmatrix} + \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix}$$

Figure 17-6: RGB/YUV Conversion Equation

18 2D BitBLT Engine

18.1 Overview

The purpose of the BitBLT Engine is to off-load the work of the CPU for moving pixel data to and from the CPU and display memory and also for moving pixel data from one location to another in display memory.

There are 5 BitBLTs (Bit Block Transfer) which are used to move pixel data from one location to another.

- Read BitBLT: Move pixel data from Display Memory to CPU
- Move BitBLT: Move pixel data from one location in Display Memory to another
- **Pattern Fill BitBLT**: Move a Pixel Pattern in Display Memory and duplicate several times to produce a larger image
- **Solid Fill BitBLT**: Move a Single Color to a location in Memory

The BitBLT Engine can perform several Data Functions in combination with some of the BitBLT functions on the pixel data.

- **ROP**: Perform a Boolean function on the pixel data
- **Transparency**: Only write pixel data of which the color does not match the Transparent Color.

The BitBLT Engine supports pixel data color depths of 8 bpp and16 bpp and CPU data transfers of 16-bits or 8-bits.

The destination and source BitBLTs can be set to be either contiguous linear blocks of memory (Linear) or as a rectangular region of memory (Rectangular).

Note
The S1D13719 BitBLT engine does not support 32 bppmodes.

18.2 BitBLTs

18.2.1 Read BitBLT

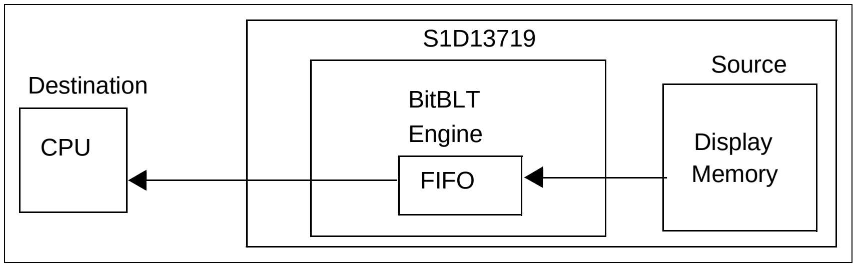


Figure 18-1: Read BitBLT Data Flow

Data can be read from memory by the Host CPU using the BitBLT Engine. The source of the data is the S1D13719 internal memory (stored as either Linear or Rectangular data format). The destination of the data to the Host CPU can also be configured to either Linear or Rectangular data format. No data functions like ROP, Transparency or Color Expansion are supported for Read BitBLTs. If these features are enabled, they are ignored. The Read Phase can also be set for the either the first data read at the start of the BitBLT for Linear or at the start of each line for Rectangular. The Read Phase allows the user to set which byte in the data read is the first byte read from memory.

18.2.2 Move BitBLT

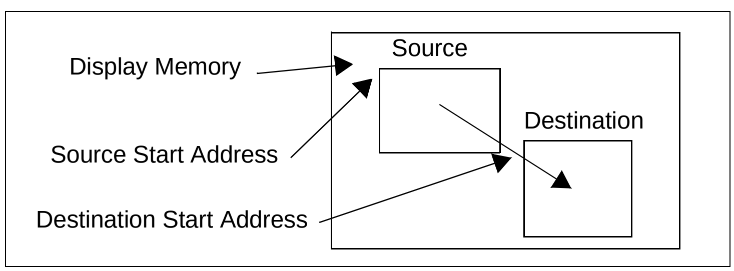


Figure 18-2: Move BitBLT data flow

The Move BitBLT copies data from the source area in memory to the destination area. The source data can also be ROP'ed with the destination data and then written back to the destination. The source data can also be Color Expanded using the Color Expansion data function and then stored to the destination. Transparency can also be applied to the source data. The source and the destination can be in either Linear or Rectangular data format. The top left hand corner of the BitBLT Window is always specified as the start address for the source and destination.

18.2.3 Pattern Fill BitBLT

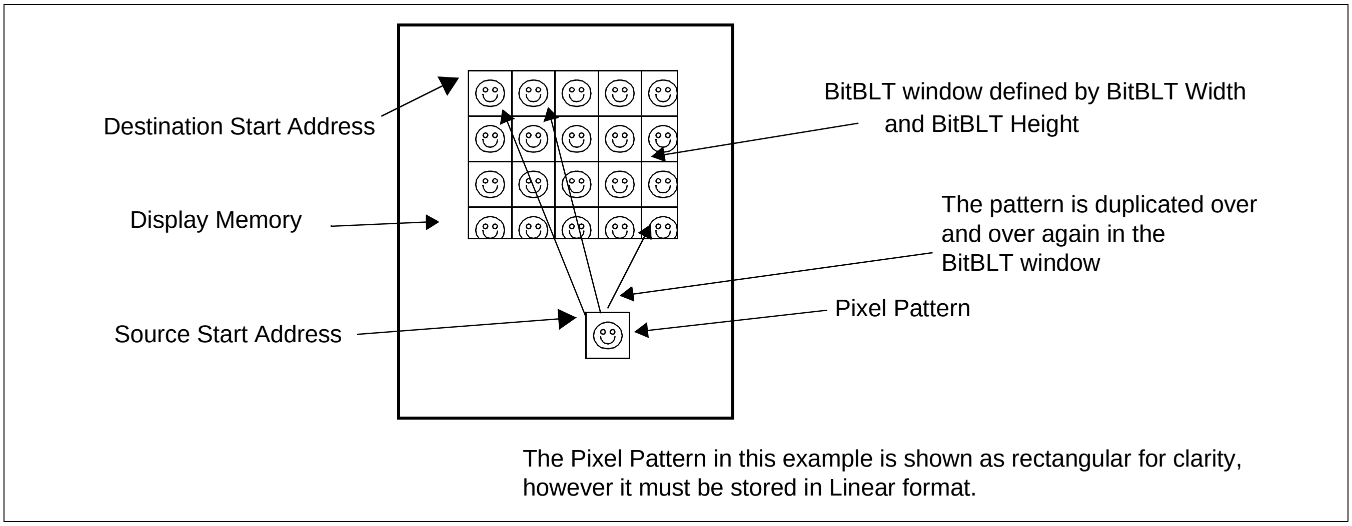


Figure 18-3: Pattern Fill Drawing

The Pattern Fill BitBLT allows an 8 x 8 pixel pattern to be duplicated multiple times to a larger area in memory as shown in the example above. The Pixel Pattern is stored at one location and it is read and drawn multiple times to the BitBLT window. For Pattern Fill BitBLTs, the Pixel Pattern, which is the source data, must be Linear and the destination, which is the BitBLT window, must be Rectangular. The source data can also be ROP'ed with the destination data and then written back to the destination.

The start of the Pixel Pattern must be aligned to a 16-bit address. The Pixel Pattern can be drawn to a BitBLT window area of 1 x 1 pixel to a max of the BitBLT Width x BitBLT Height.

18.2.4 Solid Fill BitBLT

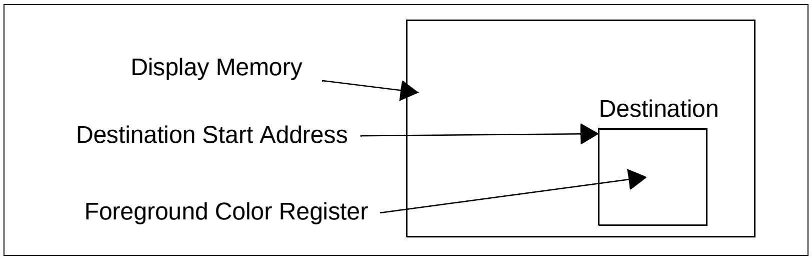


Figure 18-4: Solid Fill BitBLT Data Flow

For Solid Fill BitBLTs, the foreground color is written to the destination. The foreground color can be ROP'ed with the destination. The destination can also be Linear or Rectangular data format.

For 8 bpp, the foreground color is specified by REG[8024h] bits 7-0.
For 16 bpp, the foreground color is specified by REG[8024h] bits 15-0.

18.2.5 BitBLT Terms

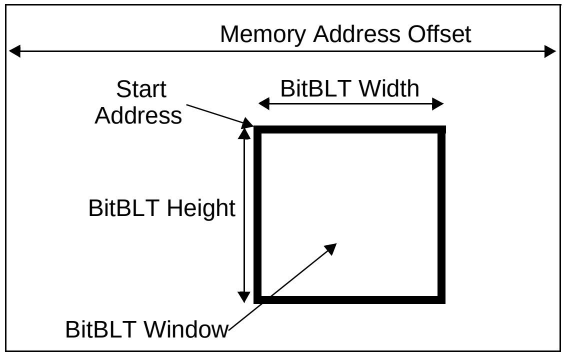


Figure 18-5: BitBLT Terms

Memory Address Offset	Width of the display (i.e. Main Window width or PIP+ Window width) in 16-bit words. The source and destination share the memory address offsets.
Start Address	Top left corner of the BitBLT window specified in bytes.
BitBLT Width	Width of the BitBLT in pixels.
BitBLT Height	Height of the BitBLT in pixels.
BitBLT Window	The area of the display memory to work with.

For each bitBLT there is a source of data and a destination for the result data. The source is the location where the data for the data function (i.e. color expansion, ROP, and transparency) is read from. The destination is where the data for the data function (i.e. ROP) is read from and also the location where the result is written to.

18.2.6 Source and Destination

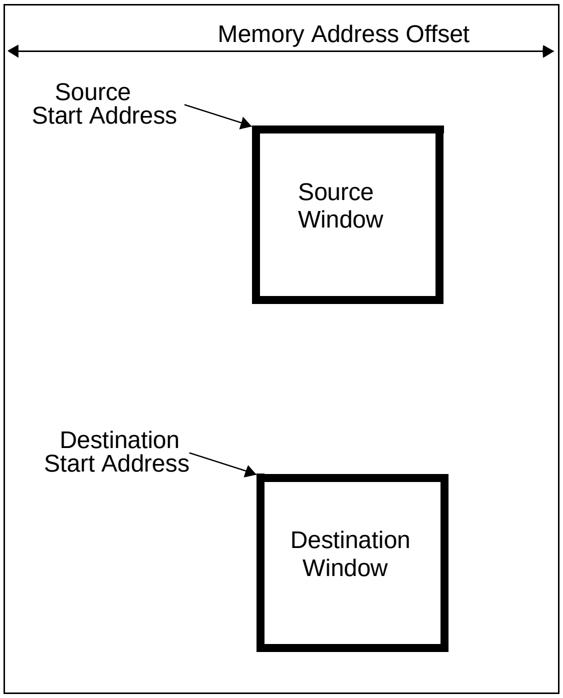


Figure 18-6: Source and Destination

18.3 Data Functions

The following data functions are supported by the BitBLT Engine. For some BitBLTs these functions can be combined together for some BitBLTs.

- Color Expansion
- ROP
- Transparency

18.3.1 ROP

ROPs allow for a boolean function to be applied to the source and destination data. The boolean function is selected using the BitBLT ROP Code bits (REG[800Ah] bits 3-0). Functions such as AND, OR, XOR, NAND, NOR, and others can be selected. The following example shows the results for 3 different ROPs with the same source and destination input.

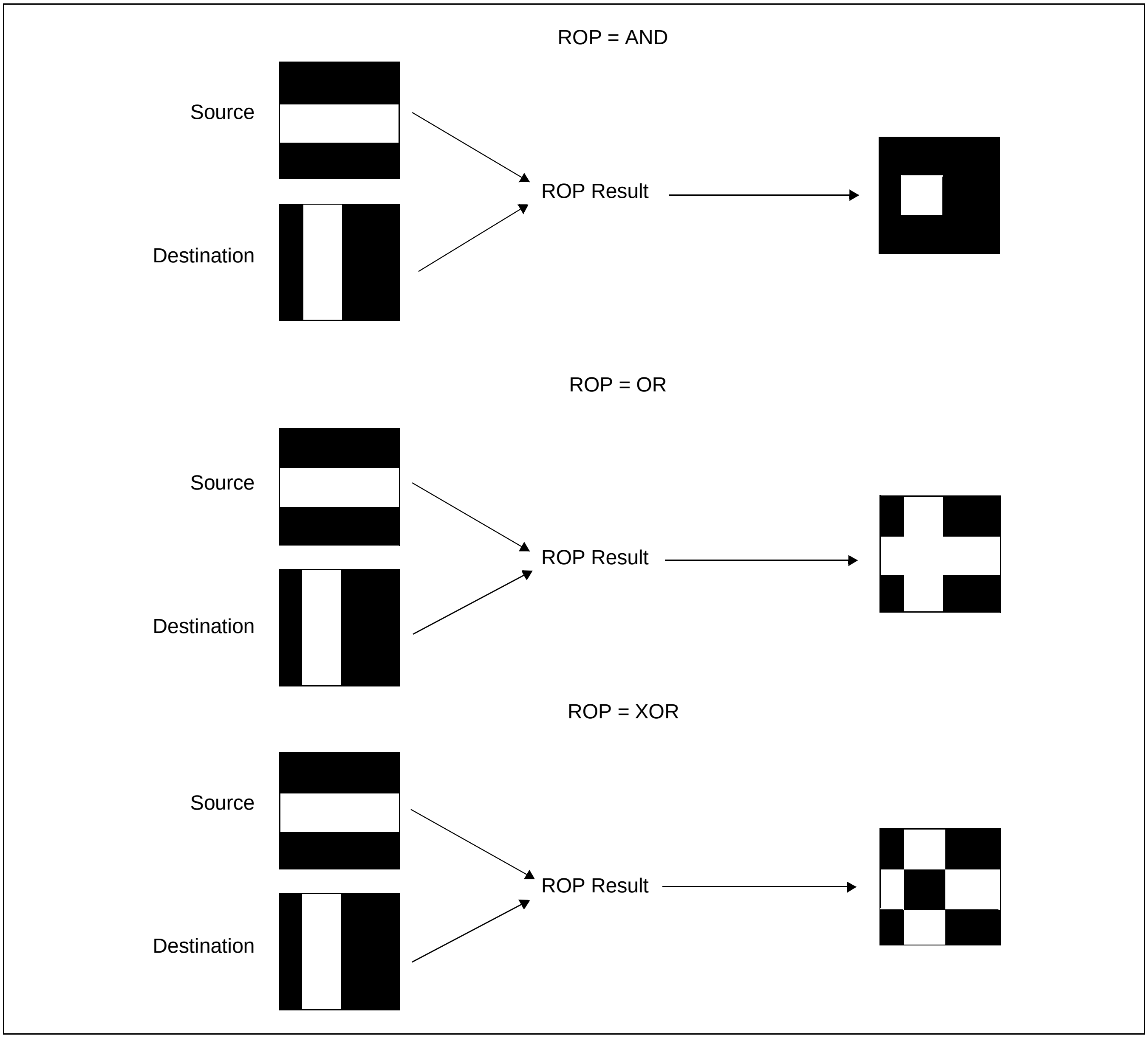


Figure 18-7: ROP Example

18.3.2 Transparency

Transparency allows for colors which do not match the background color to be written to the destination. This is useful when a non-square image contained in the BitBLT window is to be written over another image. For example, a mouse pointer is stored in memory as a block, but when the pointer is written to the display only the color of the pointer is written and the colors around it are not. The following example shows how the source image of a mouse pointer with its color set to black and color around it set to white would appear over the destination image using Transparency. The white color (which matches the background color) around the mouse pointer is not written over the destination image, yet the black mouse pointer is.

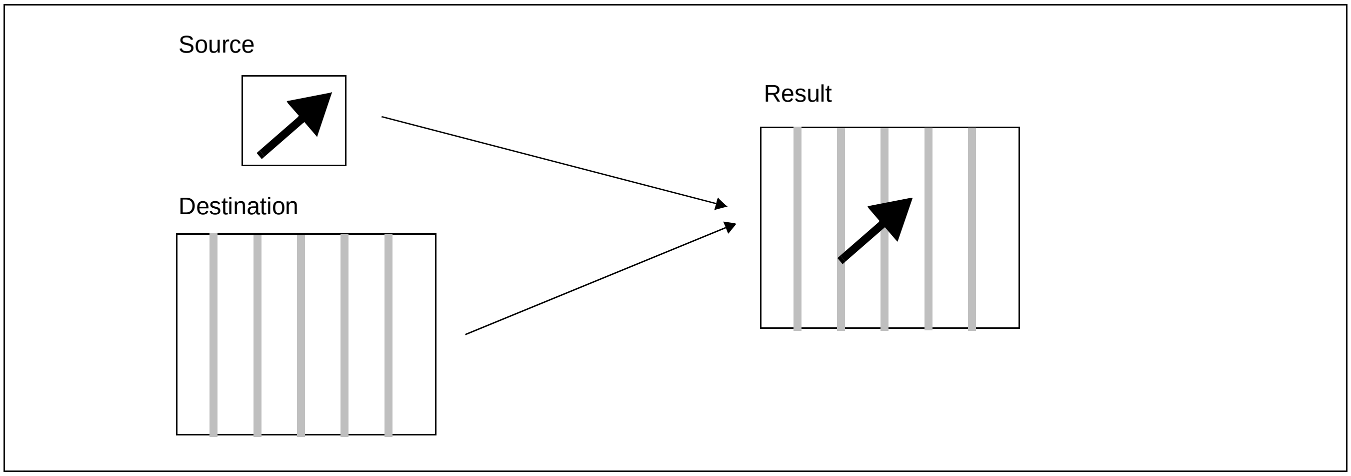


Figure 18-8: Transparency Example

18.4 Linear / Rectangular

Most BitBLTs support linear or rectangular data formats for the source and destination.

Linear means that the data in memory or to be written by the Host CPU is in a continuous format with no gaps between the EOL (End of Line) and SOL (Start of Line). The line offset is ignored for the linear data format. The following example shows how each line of linear data is stored in display memory for a BitBLT with a height of 5. Note that the SOL of Line 2 starts right after the EOL of Line 1. For 8 bpp, the next SOL starts in the byte after the previous lines EOL. For 16 bpp, it is the word after the previous line's EOL.

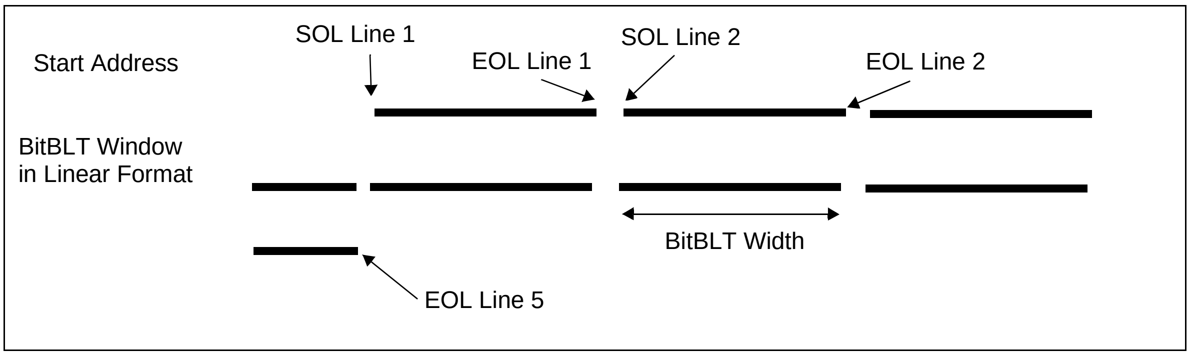


Figure 18-9: Memory Linear Example

The following example shows how linear Host CPU data is written for 16-bit writes. The SOL of the next line starts in the same 16-bit data as the EOL of the previous line.

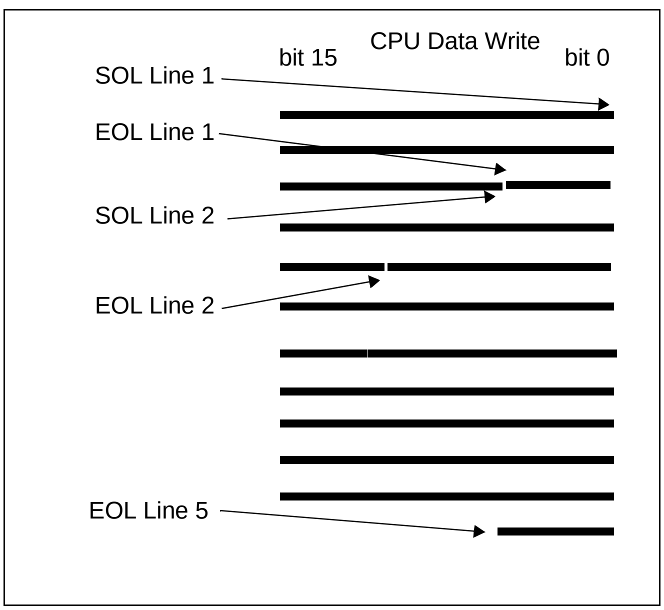


Figure 18-10: Memory Linear Example

Rectangular means that after each EOL, the SOL of the next line is the SOL of the current line plus the line offset for memory accesses. For Host CPU accesses, the SOL of the next line is always in the data written after the data with the EOL.

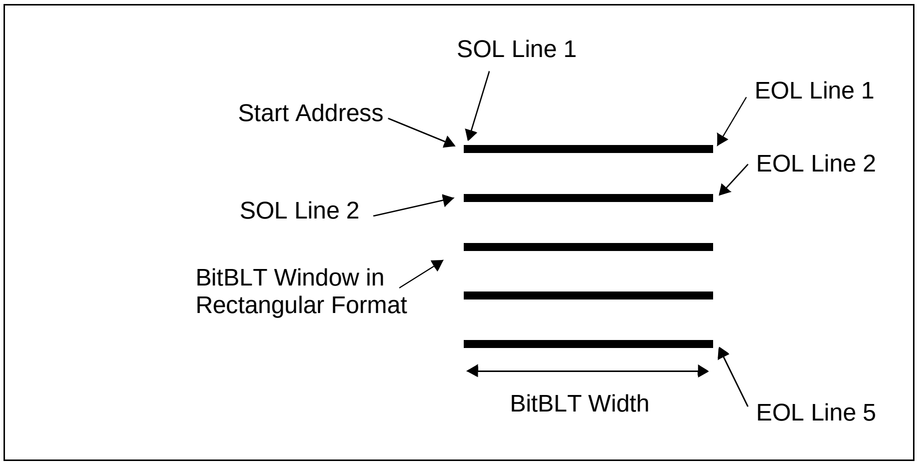


Figure 18-11: Memory Rectangular Example

The following example shows how rectangular Host CPU data is written for 16-bit writes. The SOL of the next line starts in the next 16-bit data after the EOL of the previous line.

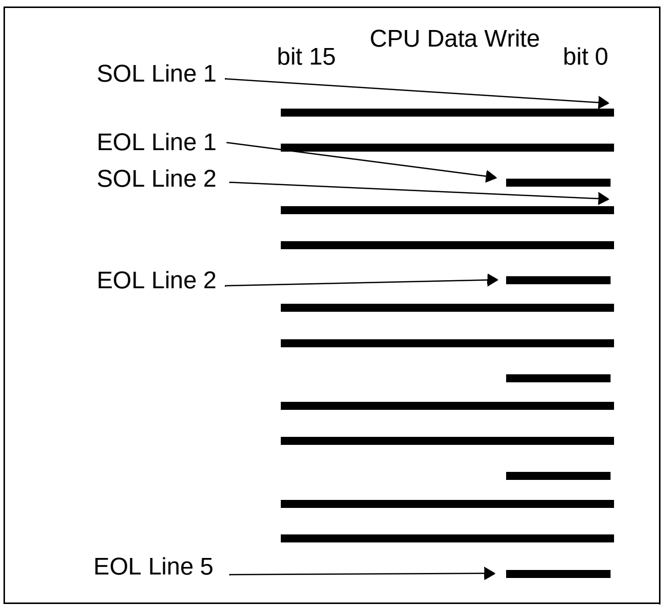


Figure 18-12: Memory Linear Example

19 Host Interface

See Section 7.3, “Host Interface Timing” for Host Interface timing information and Section 5.4, “Host Interface Pin Mapping” for pin information.

19.1 Hardware Configuration

The S1D13719 Host Interface is configured using the CNF[6:2] pins. These pins must be connected directly to VDD or VSS and select the host bus interface type, chip select mode, endian mode.

For a summary of configuration options, see Table 5-2: “Summary of Power-On/Reset Options,” on page 39.

19.1.1 CNF6 - Chip Selection

The CNF6 setting is only valid for direct and serial host bus interfaces.

When direct host bus interface is selected, CNF6 allows configuration of the chip select mode used (1 CS# mode or 2 CS# mode). In 1 CS# mode, the CS# pin is used as the S1D13719 chip select and the M/R# pin selects between the memory and register address space. Two chip select modes are available using CNF6 (1CS# and 2CS#).

For 1CS# mode, the CS# pin is used for chip select and the M/R# pin is used for the memory/register address select. For 2CS# mode, the CS# pin is used for the memory chip select and the M/R# pin is used for the register chip select.

When serial host bus interface is selected, CNF6 allows configuration of the Serial Polarity.

19.1.2 CNF5 - Endian Mode

The S1D13719 supports both big and little endian modes. The endian mode affects the direction of the data bus.

19.1.3 CNF[4:2]- Host Bus Interface Type

The S1D13719 supports Mode 80, Mode 68. Mode 80 has three variations that use different combinations of read/write signals (Type 1, Type 2, Type 3). All parallel host interfaces can use either direct or indirect addressing.

When direct addressing is selected, the address is specified with pins AB[18:1]. Indirect addressing specifies the address using an index. When the indirect or serial interface method is selected, the pull-down resistance of pins AB[18:3] is enabled and the pins can be assumed to be = 0. See Section 5.4, “Host Interface Pin Mapping” for more information.

Note
If required, the pull-down resistance on AB[18:3] can be disabled by software.

19.2 Cycle Monitoring Function

The S1D13719 internal design includes several FIFOs. Cycle monitoring is needed when FIFO read access attempts to read an empty FIFO, or attempts to write a full FIFO. There are two types of cycle monitoring functions discussed below.

19.2.1 Bus Time-Out Reset Function

The bus time-out reset function monitors the pulse width of the WAIT# pin and generates software reset if WAIT# remains active for 2-3 CLKI periods. This reset function allows the Host CPU to be notified when a bus time-out reset has occurred because of a system bus error while the WAIT# signal remains active (i.e. bus noise, etc.). This function is only for direct interfaces.

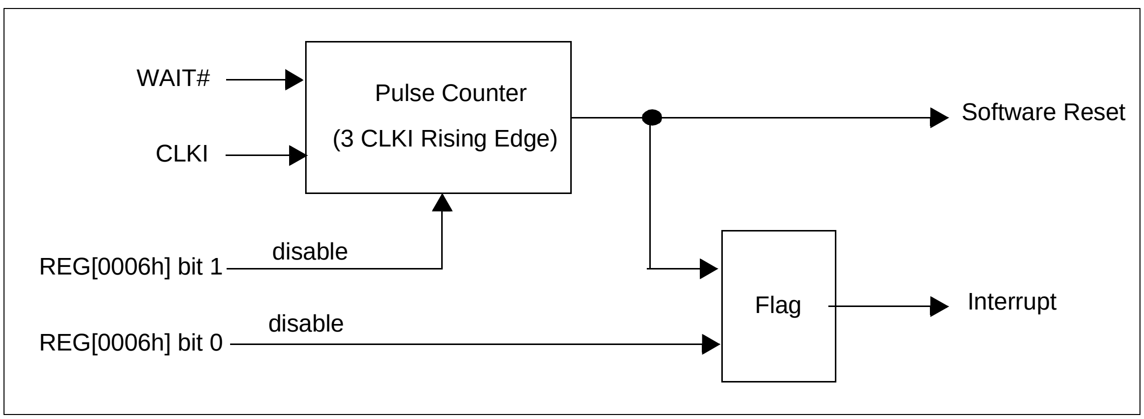


Figure 19-1: Bus Time-Out Reset Function

19.3 Indirect Interface

The S1D13719 supports three types of Host CPU interface. The indirect host interface type uses a different method of addressing the registers/memory. The following sections show example sequences for each access type.

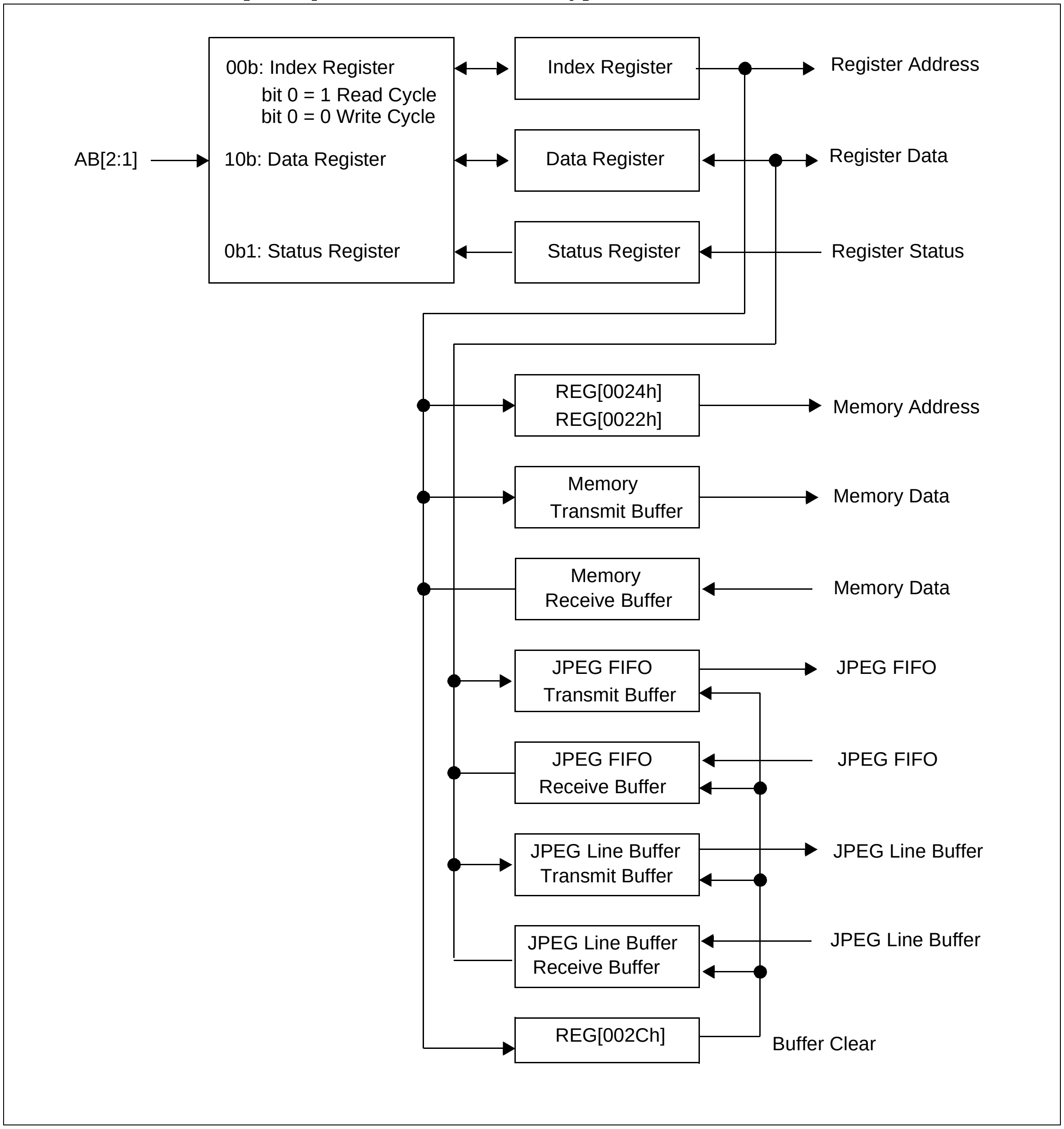


Figure 19-2: Indirect Interface Block Diagram

19.3.1 Indirect Addressing Register Ports

AB[2:1] = 00b Indirect Interface Index Register
Default = 0000h — Read/Write

Register Address bits 15-8							
15	14	13	12	11	10	9	8
Register Address bits 7-1							Read/Write Cycle Select
7	6	5	4	3	2	1	0

bits 15-1 — Register Address bits [15:1]
These bits are used for Indirect Interface modes only.
These bits set the register address for the indirect interface.

bit 0 — Read/Write Cycle Select
This bit is used for Indirect Interface modes only.
This bit selects whether a read or a write is performed.
When this bit = 0, a write is performed.
When this bit = 1, a read is performed.

AB[2:1] = 10b Indirect Interface Data Register
Default = 0000h — Read/Write

Register Data bits15-8							
15	14	13	12	11	10	9	8
Register Data bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 — Register Data bits [15:0]
These bits are used for Indirect Interface modes only. These bits are the data port for the indirect interface.

AB[2:1] = 01b Indirect Interface Status Register
Default = 0000h — Read Only

n/a					Reserved	JPEG Line Buffer Status	JPEG FIFO Status
15	14	13	12	11	10	9	8
n/a					JPEG Codec Status	n/a	Memory Status
7	6	5	4	3	2	1	0

bit 10 — Reserved
The default value for these bits is 0.

bit 9 — JPEG Line Buffer Status (Read Only)
This bit is used for Indirect Interface modes only.
This bit indicates the status of the JPEG Line Buffer. The status of this bit must be checked before accessing the JPEG Line Buffer.
When this bit returns a 0, the JPEG Line Buffer is ready (not busy).
When this bit returns a 1, the JPEG Line Buffer is busy.

bit 8	JPEG FIFO Status (Read Only) **This bit is used for Indirect Interface modes only.** This bit indicates the status of the JPEG FIFO. The status of this bit must be checked before accessing the JPEG FIFO. When this bit returns a 0, the JPEG FIFO is ready (not busy). When this bit returns a 1, the JPEG FIFO is busy.
bit 2	JPEG Codec Status (Read Only) **This bit is used for Indirect Interface modes only.** This bit indicates the status of the JPEG Codec. The status of this bit must be checked before accessing the JPEG Codec registers (REG[1000h]-REG[17A2h]). When this bit returns a 0, the JPEG Codec is ready (not busy). When this bit returns a 1, the JPEG Codec is busy.
bit 0	Memory Status (Read Only) **This bit is used for Indirect Interface modes only.** This bit indicates the status of the Memory Controller. The status of this bit must be checked before accessing the memory, however confirmation for continuous memory accesses is not necessary. When this bit returns a 0, the memory controller is ready (not busy). When this bit returns a 1, the memory controller is busy.

19.3.2 Register Access

When the indirect host interface is selected, register accesses, other than to the JPEG codec registers, should follow the procedure below.

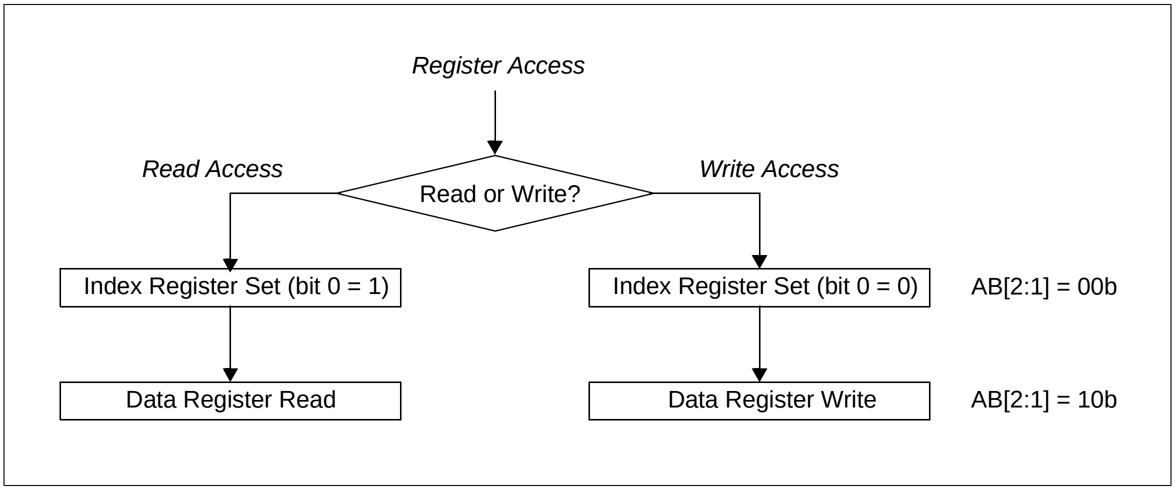


Figure 19-3: Register Access

19.3.3 JPEG Codec Register Access

When the indirect host interface is selected, JPEG codec register accesses (REG[1000h]-REG[17A2h]) should follow the procedure below.

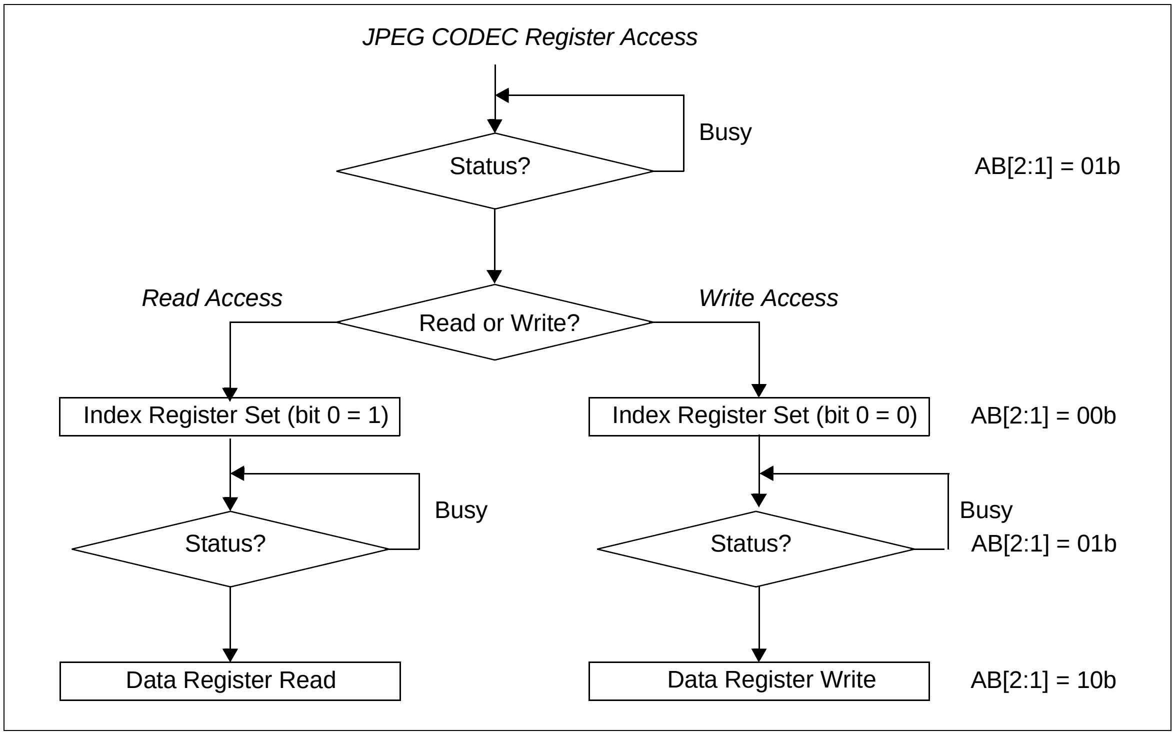


Figure 19-4: JPEG Codec Register Access

19.3.4 Memory Access

When the indirect host interface is selected, memory accesses should follow the procedure below. Please start from the address setting again when the memory read error or the write error occurs. The byte cannot be accessed.

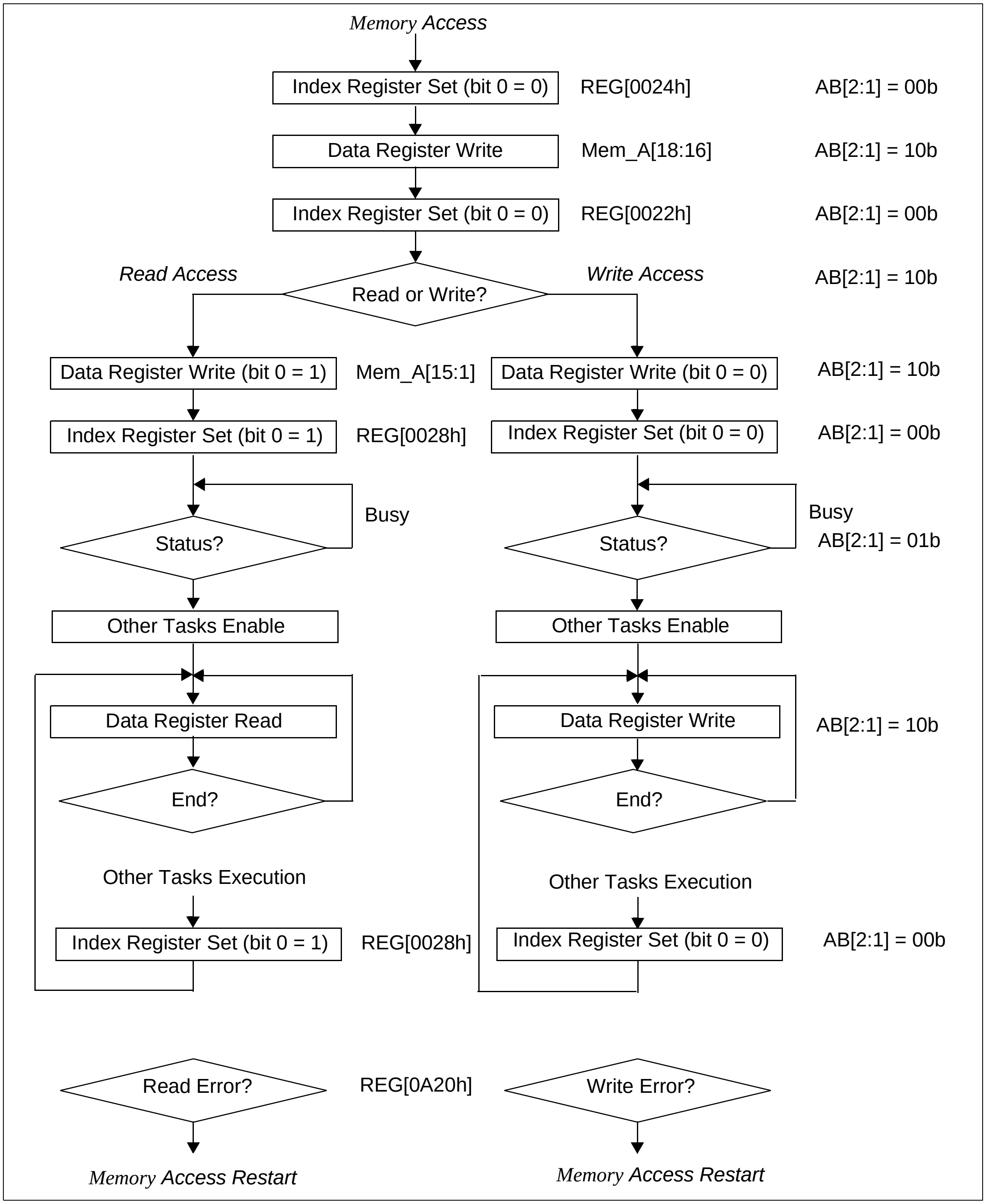


Figure 19-5: Memory Access

19.3.5 JPEG FIFO Access

When the indirect host interface is selected, JPEG FIFO accesses (REG[09A6h]) should follow the procedure below. The JPEG FIFO receive buffer and transmit buffer (see REG[002Ch]) must be cleared when a JPEG FIFO read/write error occurs and before the JPEG operation begins.

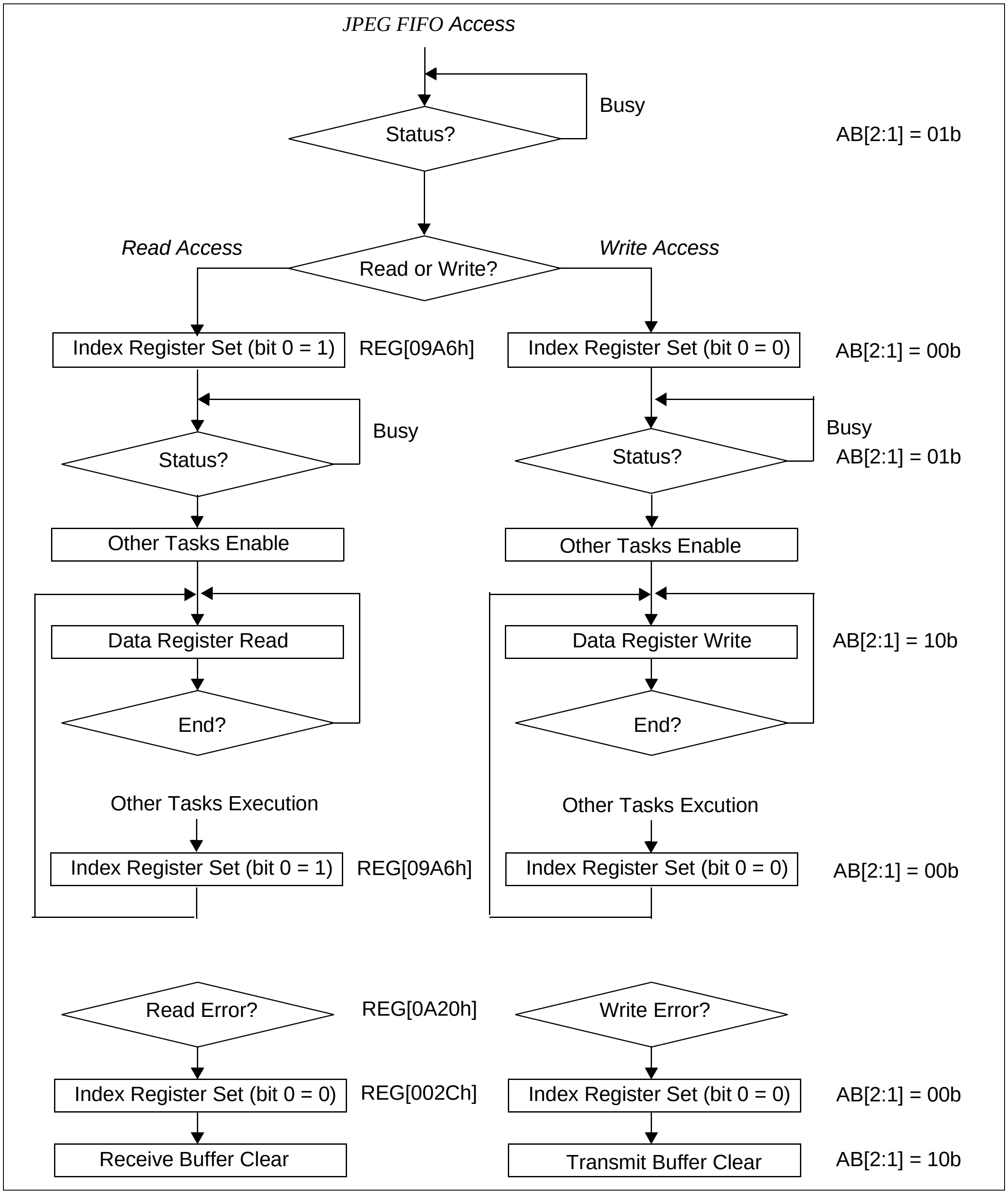


Figure 19-6: JPEG FIFO Access

19.3.6 JPEG Line Buffer Access

When the indirect host interface is selected, JPEG Line Buffer accesses (REG[09E0h]) should follow the procedure below. The JPEG Line Buffer receive buffer and transmit buffer (see REG[002Ch]) must be cleared when a JPEG Line Buffer read/write error occurs and before the JPEG operation begins.

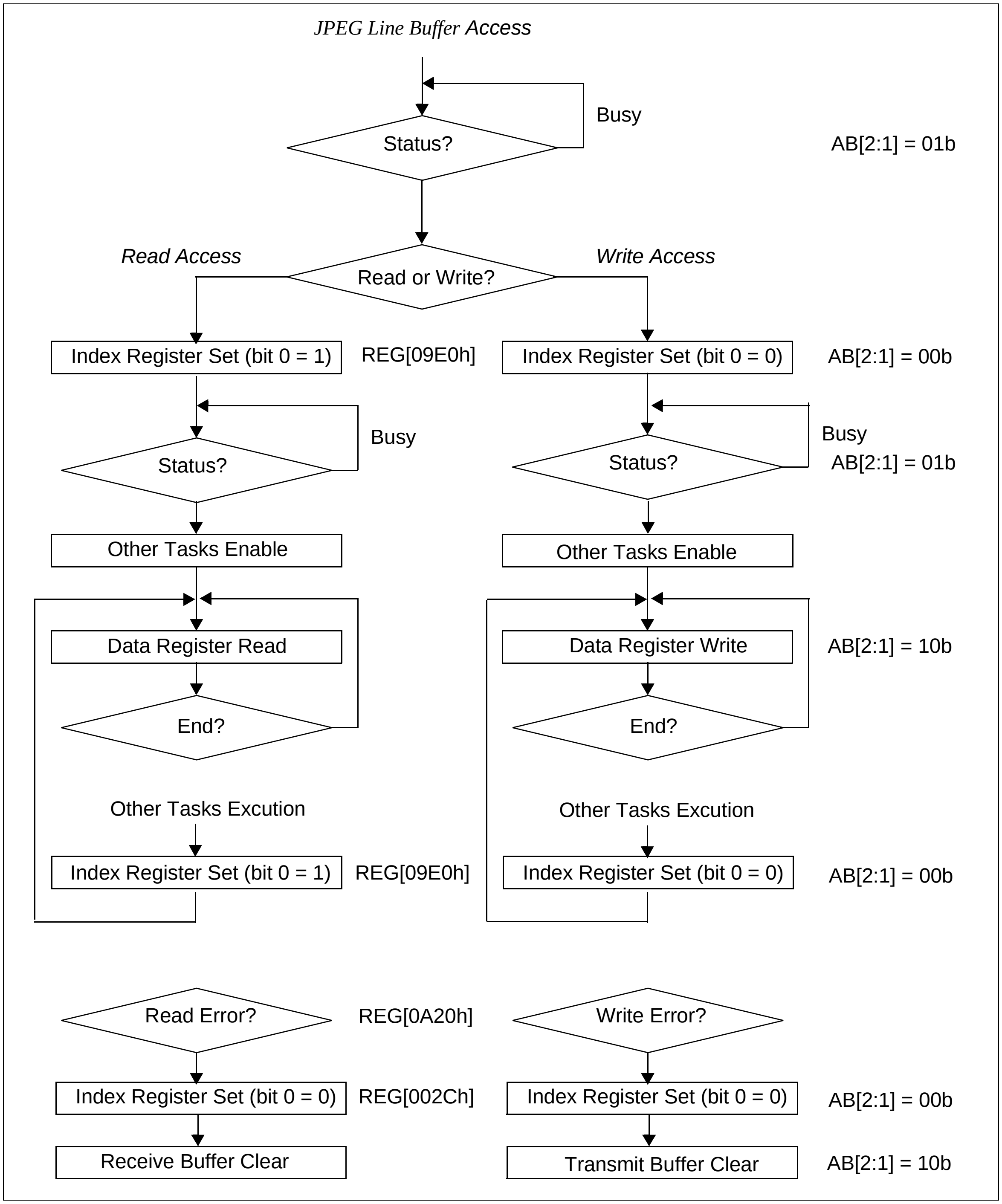


Figure 19-7: JPEG Line Buffer Access

19.4 Number of Cycles

Accessing the S1D13719 takes a different number of cycles depending on the type of access to be performed. The following diagram shows an example for the direct host interface. The number of cycles required may increase when various memory accesses compete. The cycle time-out function may be used if a maximum number of cycles is to be specified (see REG[0A0Eh]).

Note

The indirect host interface uses a fixed number of cycles for each access.

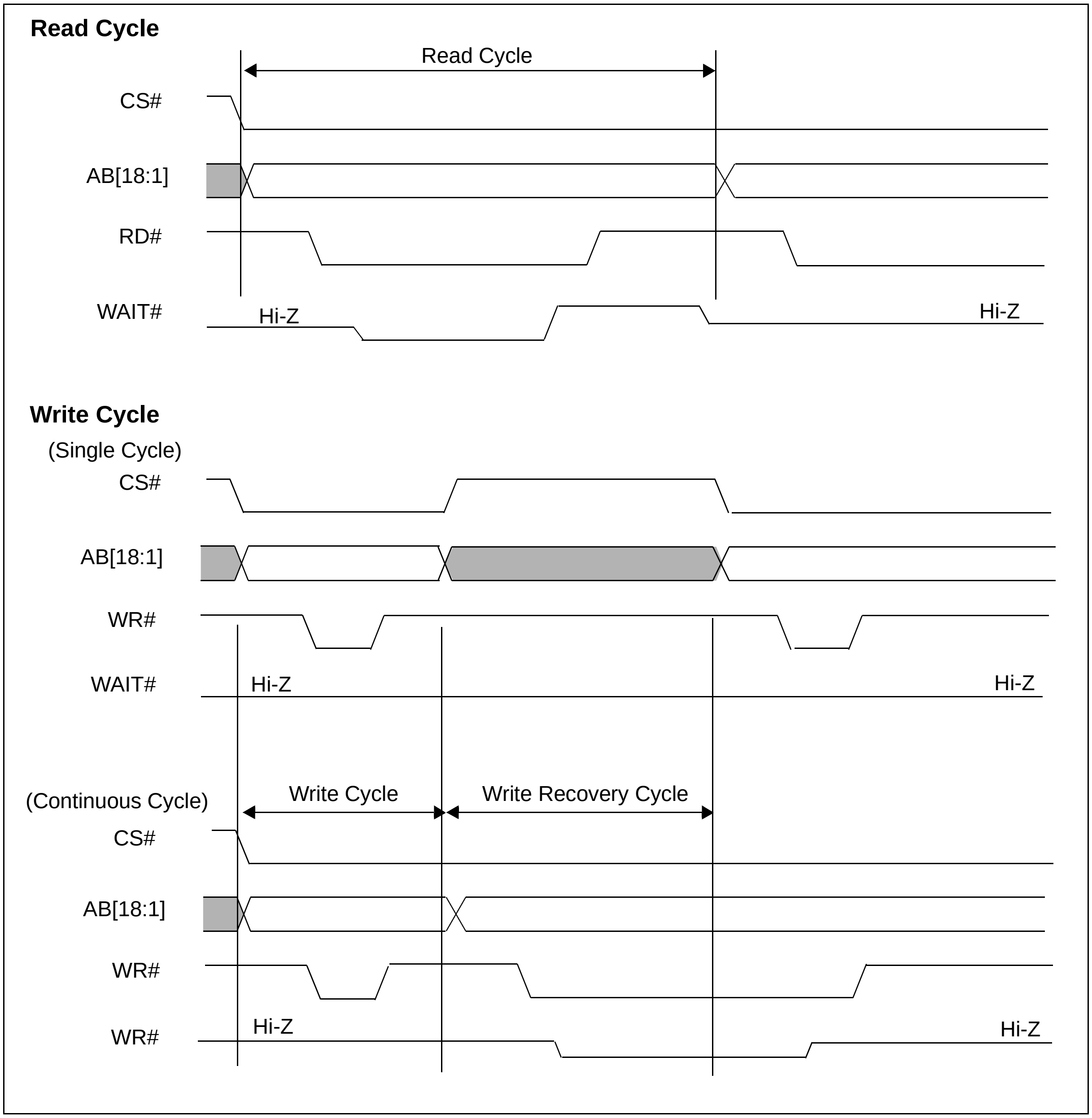


Figure 19-8: Host Interface Cycle

Table 19-1: Cycle Number

Cycle	System Clocks	WAIT# Clocks (System Clocks - 3)
Register Read Cycle	8	5
Register Write Cycle + Write Recovery Cycle	3 + 5	5
JPEG CODEC Register Read Cycle (REG[1000h]Å`REG[17A2h])	10	7
JPEG CODEC Register Write Cycle + Write Recovery Cycle (REG[1000h]Å`REG[17A2h])	3 + 7	7
JPEG FIFO Read First Cycle (REG[09A6h])	8	5
JPEG FIFO Read Cycle (REG[09A6h])	3	0
JPEG FIFO Read Last Cycle (REG[09A6h])	7	4
JPEG FIFO Write Cycle + Write Recovery Cycle (REG[09A6h])	3 + 5	5
JPEG Line Buffer Read Cycle (REG[09E0h])	8	5
JPEG Line Buffer Write Cycle + Write Recovery Cycle (REG[09E0h])	3 + 5	5
Memory Read Cycle	8	5
Memory Write Cycle + Write Recovery Cycle	3 + 4	4

20 LCD Panel Interface

The S1D13719 can connect two a maximum of two LCD panels. The image data stored in the display buffer is output to the LCD panel via the Look-up Tables (LUT1/LUT2) and the display FIFO.

The S1D13719 supports the following LCD panel interface types:

- RGB interface LCD panel
- Parallel interface LCD panel
- Serial interface LCD panel

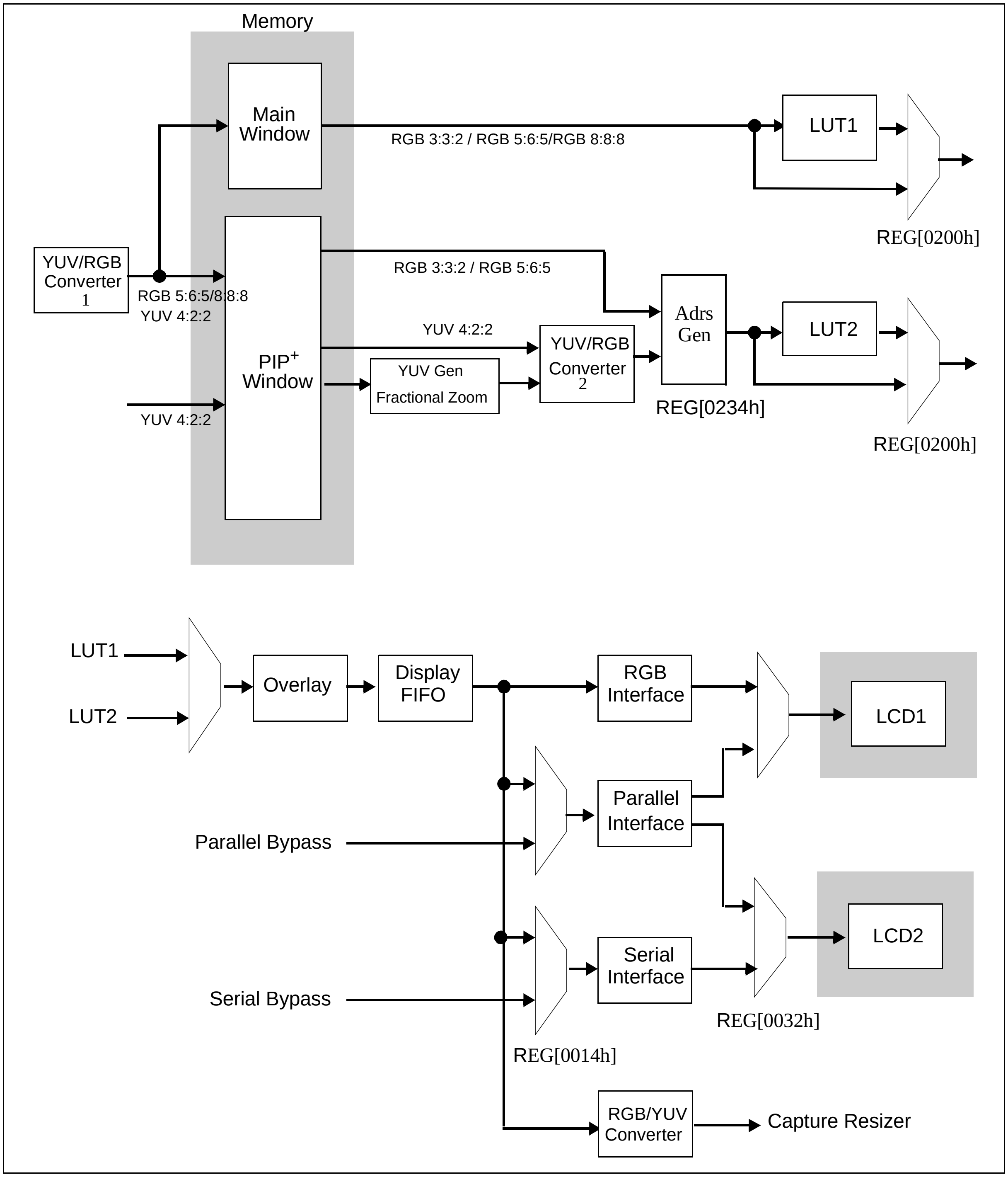


Figure 20-1: LCD Interface Block Diagram

20.1 RGB Interface LCD Panel Data Format

The following information shows the possible data output formats when LCD1 is configured for a RGB interface LCD panel.

20.1.1 9/12/16/18/24-Bit RGB Data Format

LCD1 9-bit RGB interface LCD panel RGB 3:3:3 (REG[0032h] bits 6-4= 000b)

LCD1 12-bit RGB interface LCD panel RGB 4:4:4 (REG[0032h] bits 6-4= 001b)

LCD1 16-bit RGB interface LCD panel RGB 5:6:5 (REG[0032h] bits 6-4= 010b)

LCD1 18-bit RGB interface LCD panel RGB 6:6:6 (REG[0032h] bits 6-4= 011b)

LCD1 24-bit RGB interface LCD panel RGB 8:8:8(REG[0032h] bits 6-4= 100b)

Table 20-1: 9/12/16/18/24-Bit RGB Data Format

Pin	9-Bit	12-Bit	16-Bit	18-Bit	24-Bit
FPDAT0	R^5	R^5	R^5	R^5	R^7
FPDAT1	R^4	R^4	R^4	R^4	R^6
FPDAT2	R^3	R^3	R^3	R^3	R^5
FPDAT3	G^5	G^5	G^5	G^5	G^7
FPDAT4	G^4	G^4	G^4	G^4	G^6
FPDAT5	G^3	G^3	G^3	G^3	G^5
FPDAT6	B^5	B^5	B^5	B^5	B^7
FPDAT7	B^4	B^4	B^4	B^4	B^6
FPDAT8	B^3	B^3	B^3	B^3	B^5
FPDAT9	Low	R^2	R^2	R^2	R^4
FPDAT10	Low	Low	R^1	R^1	R^3
FPDAT11	Low	Low	Low	R^0	R^2
FPDAT12	Low	G^2	G^2	G^2	G^4
FPDAT13	Low	Low	G^1	G^1	G^3
FPDAT14	Low	Low	G^0	G^0	G^2
FPDAT15	Low	B^2	B^2	B^2	B^4
FPDAT16	Low	Low	B^1	B^1	B^3
FPDAT17	Low	Low	Low	B^0	B^2
GPIO4	Low	Low	Low	Low	R^1
GPIO5	Low	Low	Low	Low	R^0
GPIO6	Low	Low	Low	Low	G^1
GPIO7	Low	Low	Low	Low	G^0
GPIO8	Low	Low	Low	Low	B^1
GPIO9	Low	Low	Low	Low	B^0

20.1.2 RGB Serial Interfaces

LCD1 ND-TFD (8-bit Serial) RGB interface LCD panel (REG[0054h] bits 7-5 = 000b)

LCD1 ND-TFD (9-bit Serial) RGB interface LCD panel (REG[0054h] bits 7-5 = 001b)

LCD1 a-Si TFT (8-bit Serial) RGB interface LCD panel (REG[0054h] bits 7-5 = 01Xb)

LCD1 uWIRE TFT (16-bit Serial) RGB interface LCD panel (REG[0054h] bits 7-5 = 10Xb)

LCD1 SPI (8 or 16-bit Serial) RGB interface LCD panel (REG[0054h] bits 7-5 = 110b)

Table 20-2: RGB Serial Interfaces

Interface Type	FPCS1#	FPSCK	FPA0	FPSO
ND-TFD 8bit	used	used	used	not used
ND TFD 9bit	used	used	used	not used
a-Si	used	used	not used	used
uWIRE	used	used	not used	used
SPI	used	used	not used	used

20.2 LCD Parallel Interface Data Format

The following information shows the possible data output formats when LCD1 or LCD2 are configured for a parallel interface LCD panel.

20.2.1 8-bit Parallel (RGB 3:3:2) Data Format

LCD1 8-bit parallel interface LCD panel RGB 3:3:2 (REG[0056h] bits 3-0 = 0000b)

LCD2 8-bit parallel interface LCD panel RGB 3:3:2 (REG[005Eh] bits 3-0 = 0000b)

Table 20-3: 8-Bit Parallel (RGB 3:3:2) Data Format

Cycle Count	1	2	3	...	n+1
D7	R_0^5	R_1^5	R_2^5	...	R_n^5
D6	R_0^4	R_1^4	R_2^4	...	R_n^4
D5	R_0^3	R_1^3	R_2^3	...	R_n^3
D4	G_0^5	G_1^5	G_2^5	...	G_n^5
D3	G_0^4	G_1^4	G_2^4	...	G_n^4
D2	G_0^3	G_1^3	G_2^3	...	G_n^3
D1	B_0^5	B_1^5	B_2^5	...	B_n^5
D0	B_0^4	B_1^4	B_2^4	...	B_n^4

20.2.2 8-Bit Parallel (RGB 4:4:4) Data Format

LCD1 8-bit parallel interface LCD panel RGB 4:4:4 (REG[0056h] bits 3-0 = 0001)

LCD2 8-bit parallel interface LCD panel RGB 4:4:4 (REG[005Eh] bits 3-0 = 0001)

Table 20-4: 8-Bit Parallel (RGB 4:4:4) Data Format

Cycle Count	1	2	3	...	3n+1	3n+2	3n+3
D7	R_0^5	B_0^5	G_1^5	...	R_n^5	B_n^5	G_{n+1}^5
D6	R_0^4	B_0^4	G_1^4	...	R_n^4	B_n^4	G_{n+1}^4
D5	R_0^3	B_0^3	G_1^3	...	R_n^3	B_n^3	G_{n+1}^3
D4	R_0^2	B_0^2	G_1^2	...	R_n^2	B_n^2	G_{n+1}^2
D3	G_0^5	R_1^5	B_1^5	...	G_n^5	R_{n+1}^5	B_{n+1}^5
D2	G_0^4	R_1^4	B_1^4	...	G_n^4	R_{n+1}^4	B_{n+1}^4
D1	G_0^3	R_1^3	B_1^3	...	G_n^3	R_{n+1}^3	B_{n+1}^3
D0	G_0^2	R_1^2	B_1^2	...	G_n^2	R_{n+1}^2	B_{n+1}^2

20.2.3 8-Bit Parallel (RGB 5:6:5) Data Format

LCD1 8-bit parallel interface LCD panel RGB 5:6:5 (REG[0056h] bits 3-0 = 1xxx)

LCD2 8-bit parallel interface LCD panel RGB 5:6:5 (REG[005Eh] bits 3-0 = 1xxx)

Table 20-5: 8-bit Parallel (RGB 5:6:5) Data Format

Cycle Count	1	2	...	n+1	n+2
D7	R_0^5	G_0^2	...	R_n^5	G_n^2
D6	R_0^4	G_0^1	...	R_n^4	G_n^1
D5	R_0^3	G_0^0	...	R_n^3	G_n^0
D4	R_0^2	B_0^5	...	R_n^2	B_n^5
D3	R_0^1	B_0^4	...	R_n^1	B_n^4
D2	G_0^5	B_0^3	...	G_n^5	B_n^3
D1	G_0^4	B_0^2	...	G_n^4	B_n^2
D0	G_0^3	B_0^1	...	G_n^3	B_n^1

20.2.4 8-Bit Parallel (RGB 6:6:6) Data Format

LCD1 8-bit parallel interface LCD panel RGB 6:6:6 (REG[0056h] bits 3-0 = 0011)

LCD2 8-bit parallel interface LCD panel RGB 6:6:6 (REG[005Eh] bits 3-0 = 0011)

Table 20-6: 8-bit Parallel (RGB 6:6:6) Data Format

Cycle Count	1	2	3	...	3n+1	3n+2	3n+3
D7	R_0^5	G_0^5	B_0^5	...	R_n^5	G_n^5	B_n^5
D6	R_0^4	G_0^4	B_0^4	...	R_n^4	G_n^4	B_n^4
D5	R_0^3	G_0^3	B_0^3	...	R_n^3	G_n^3	B_n^3
D4	R_0^2	G_0^2	B_0^2	...	R_n^2	G_n^2	B_n^2
D3	R_0^1	G_0^1	B_0^1	...	R_n^1	G_n^1	B_n^1
D2	R_0^0	G_0^0	B_0^0	...	R_n^0	G_n^0	B_n^0
D1	-	-	-	...	-	-	-
D0	-	-	-	...	-	-	-

20.2.5 8-Bit Parallel, RGB=8:8:8

When REG[0056h] bits 2-0 = 011b, the LCD1 data format is specified as this format.
When REG[005Eh] bits 2-0 = 011b, the LCD2 data format is specified as this format.

Table 20-7: 8-Bit Parallel, RGB=8:8:8 Data Format Selection

	Cycle Count						
	1	**2**	**3**	**...**	**3n+1**	**3n+2**	**3n+3**
D7	R_0^7	G_0^7	B_0^7	...	R_n^7	G_n^7	B_n^7
D6	R_0^6	G_0^6	B_0^6	...	R_n^6	G_n^6	B_n^6
D5	R_0^5	G_0^5	B_0^5	...	R_n^5	G_n^5	B_n^5
D4	R_0^4	G_0^4	B_0^4	...	R_n^4	G_n^4	B_n^4
D3	R_0^3	G_0^3	B_0^3	...	R_n^3	G_n^3	B_n^3
D2	R_0^2	G_0^2	B_0^2	...	R_n^2	G_n^2	B_n^2
D1	R_0^1	G_0^1	B_0^1	...	R_n^1	G_n^1	B_n^1
D0	R_0^0	G_0^0	B_0^0	...	R_n^0	G_n^0	B_n^0

20.2.6 16-Bit Parallel (RGB 4:4:4) Data Format

LCD1 16-bit parallel interface LCD panel RGB 4:4:4(REG[0056h] bits 3-0 = 0101b)

LCD2 16-bit parallel interface LCD panel RGB 4:4:4(REG[005Eh] bits 3-0 = 0101b)

Table 20-8: 16-bit Parallel (RGB 4:4:4) Data Format

Cycle Count	**1**	**2**	**3**	**...**	**n+1**
D15	R_0^5	R_1^5	R_2^5	...	R_n^5
D14	R_0^4	R_1^4	R_2^4	...	R_n^4
D13	R_0^3	R_1^3	R_2^3	...	R_n^3
D12	R_0^2	R_1^2	R_2^2	...	R_n^2
D11	G_0^5	G_1^5	G_2^5	...	G_n^5
D10	G_0^4	G_1^4	G_2^4	...	G_n^4
D9	G_0^3	G_1^3	G_2^3	...	G_n^3
D8	G_0^2	G_1^2	G_2^2	...	G_n^2
D7	B_0^5	B_1^5	B_2^5	...	B_n^5
D6	B_0^4	B_1^4	B_2^4	...	B_n^4
D5	B_0^3	B_1^3	B_2^3	...	B_n^3
D4	B_0^2	B_1^2	B_2^2	...	B_n^2
D3	-	-		-	-
D2	-	-		-	-
D1	-	-		-	-
D0	-	-		-	-

20.2.7 16-Bit Parallel (RGB 5:6:5) Data Format

LCD1 16-bit parallel interface LCD panel RGB 5:6:5 (REG[0056h] bits 3-0 = 0110b)

LCD2 16-bit parallel interface LCD panel RGB 5:6:5 (REG[005Eh] bits 3-0 = 0110b)

Table 20-9: 16-bit Parallel (RGB 5:6:5) Data Format

Cycle Count	1	2	3	...	n+1
D15	R_0^5	R_1^5	R_2^5	...	R_n^5
D14	R_0^4	R_1^4	R_2^4	...	R_n^4
D13	R_0^3	R_1^3	R_2^3	...	R_n^3
D12	R_0^2	R_1^2	R_2^2	...	R_n^2
D11	R_0^1	R_1^1	R_2^1	...	R_n^1
D10	G_0^5	G_1^5	G_2^5	...	G_n^5
D9	G_0^4	G_1^4	G_2^4	...	G_n^4
D8	G_0^3	G_1^3	G_2^3	...	G_n^3
D7	G_0^2	G_1^2	G_2^2	...	G_n^2
D6	G_0^1	G_1^1	G_2^1	...	G_n^1
D5	G_0^0	G_1^0	G_2^0	...	G_n^0
D4	B_0^5	B_1^5	B_2^5	...	B_n^5
D3	B_0^4	B_1^4	B_2^4	...	B_n^4
D2	B_0^3	B_1^3	B_2^3	...	B_n^3
D1	B_0^2	B_1^2	B_2^2	...	B_n^2
D0	B_0^1	B_1^1	B_2^1	...	B_n^1

20.2.8 16-Bit Parallel, RGB=8:8:8

When REG[0056h] bits 2-0 = 010b, the LCD1 data format is specified as this format.
When REG[005Eh] bits 2-0 = 010b, the LCD2 data format is specified as this format.

Table 20-10: 16-Bit Parallel, RGB=8:8:8 Data Format Selection

	Cycle Count				
	1	**2**	**3**	**...**	**n+1**
D15	R_0^7	B_0^7	G_1^7	...	R_n^7
D14	R_0^6	B_0^6	G_1^6	...	R_n^6
D13	R_0^5	B_0^5	G_1^5	...	R_n^5
D12	R_0^4	B_0^4	G_1^4	...	R_n^4
D11	R_0^3	B_0^3	G_1^3	...	R_n^3
D10	R_0^2	B_0^2	G_1^2	...	R_n^2
D9	R_0^1	B_0^1	G_1^1	...	R_n^1
D8	R_0^0	B_0^0	G_1^0	...	R_n^0
D7	G_0^7	R_1^7	B_1^7	...	G_n^7
D6	G_0^6	R_1^6	B_1^6	...	G_n^6
D5	G_0^5	R_1^5	B_1^5	...	G_n^5
D4	G_0^4	R_1^4	B_1^4	...	G_n^4
D3	G_0^3	R_1^3	B_1^3	...	G_n^3
D2	G_0^2	R_1^2	B_1^2	...	G_n^2
D1	G_0^1	R_1^1	B_1^1	...	G_n^1
D0	G_0^0	R_1^0	B_1^0	...	G_n^0

20.2.9 18-bit Parallel (RGB 6:6:6) Data Format

LCD1 18-bit parallel interface LCD panel RGB 6:6:6(REG[0056h] bits 3-0 = 0111b)
LCD2 18-bit parallel interface LCD panel RGB 6:6:6(REG[005Eh] bits 3-0 = 0111b)

Table 20-11: 18-bit Parallel (RGB 6:6:6) Data Format

Cycle Count	**1**	**2**	**3**	**...**	**n+1**
D17	R_0^5	R_1^5	R_2^5	...	R_n^5
D16	R_0^4	R_1^4	R_2^4	...	R_n^4
D15	R_0^3	R_1^3	R_2^3	...	R_n^3
D14	R_0^2	R_1^2	R_2^2	...	R_n^2
D13	R_0^1	R_1^1	R_2^1	...	R_n^1
D12	R_0^0	R_1^0	R_2^0	...	R_n^0
D11	G_0^5	G_1^5	G_2^5	...	G_n^5
D10	G_0^4	G_1^4	G_2^4	...	G_n^4
D9	G_0^3	G_1^3	G_2^3	...	G_n^3
D8	G_0^2	G_1^2	G_2^2	...	G_n^2
D7	G_0^1	G_1^1	G_2^1	...	G_n^1
D6	G_0^0	G_1^0	G_2^0	...	G_n^0
D5	B_0^5	B_1^5	B_2^5	...	B_n^5
D4	B_0^4	B_1^4	B_2^4	...	B_n^4
D3	B_0^3	B_1^3	B_2^3	...	B_n^3
D2	B_0^2	B_1^2	B_2^2	...	B_n^2
D1	B_0^1	B_1^1	B_2^1	...	B_n^1
D0	B_0^0	B_1^0	B_2^0	...	B_n^0

20.2.10 24-Bit Parallel, RGB=8:8:8

When REG[0056h] bits 2-0 = 100b, the LCD1 data format is specified as this format.
When REG[005Eh] bits 2-0 = 100b, the LCD2 data format is specified as this format.

Table 20-12: 24-Bit Parallel, RGB=8:8:8 Data Format Selection

	Cycle Count				
	1	**2**	**3**	**...**	**n+1**
D23	R_0^7	R_1^7	R_2^7		R_n^7
D22	R_0^6	R_1^6	R_2^6		R_n^6
D21	R_0^5	R_1^5	R_2^5		R_n^5
D20	R_0^4	R_1^4	R_2^4		R_n^4
D19	R_0^3	R_1^3	R_2^3		R_n^3
D18	R_0^2	R_1^2	R_2^2		R_n^2
D17	R_0^1	R_1^1	R_2^1		R_n^1
D16	R_0^0	R_1^0	R_2^0		R_n^0
D15	G_0^7	G_1^7	G_2^7	...	G_n^7
D14	G_0^6	G_1^6	G_2^6	...	G_n^6
D13	G_0^5	G_1^5	G_2^5	...	G_n^5
D12	G_0^4	G_1^4	G_2^4	...	G_n^4
D11	G_0^3	G_1^3	G_2^3	...	G_n^3
D10	G_0^2	G_1^2	G_2^2	...	G_n^2
D9	G_0^1	G_1^1	G_2^1	...	G_n^1
D8	G_0^0	G_1^0	G_2^0	...	G_n^0
D7	B_0^7	B_1^7	B_2^7	...	B_n^7
D6	B_0^6	B_1^6	B_2^6	...	B_n^6
D5	B_0^5	B_1^5	B_2^5	...	B_n^5
D4	B_0^4	B_1^4	B_2^4	...	B_n^4
D3	B_0^3	B_1^3	B_2^3	...	B_n^3
D2	B_0^2	B_1^2	B_2^2	...	B_n^2
D1	B_0^1	B_1^1	B_2^1	...	B_n^1
D0	B_0^0	B_1^0	B_2^0	...	B_n^0

20.3 LCD Parallel Interface Command/Parameter Format

The following information shows the command/parameter output format when LCD1 or LCD2 are configured for a parallel interface LCD panel.

Table 20-13: LCD1 Parallel Interface Command/Parameter Format

REG[0056h]	bits 5-4 = 00b		bits 5-4 = 01b		bits 5-4 = 10b	
D17	-	-	Command[15]	Parameter[15]	Command[15]	Parameter[15]
D16	-	-	Command[14]	Parameter[14]	Command[14]	Parameter[14]
D15	Command[15]	Parameter[15]	Command[13]	Parameter[13]	Command[13]	Parameter[13]
D14	Command[14]	Parameter[14]	Command[12]	Parameter[12]	Command[12]	Parameter[12]
D13	Command[13]	Parameter[13]	Command[11]	Parameter[11]	Command[11]	Parameter[11]
D12	Command[12]	Parameter[12]	Command[10]	Parameter[10]	-	-
D11	Command[11]	Parameter[11]	Command[9]	Parameter[9]	Command[10]	Parameter[10]
D10	Command[10]	Parameter[10]	Command[8]	Parameter[8]	Command[9]	Parameter[9]
D9	Command[9]	Parameter[9]	-	-	Command[8]	Parameter[8]
D8	Command[8]	Parameter[8]	Command[7]	Parameter[7]	Command[7]	Parameter[7]
D7	Command[7]	Parameter[7]	Command[6]	Parameter[6]	Command[6]	Parameter[6]
D6	Command[6]	Parameter[6]	Command[5]	Parameter[5]	Command[5]	Parameter[5]
D5	Command[5]	Parameter[5]	Command[4]	Parameter[4]	Command[4]	Parameter[4]
D4	Command[4]	Parameter[4]	Command[3]	Parameter[3]	Command[3]	Parameter[3]
D3	Command[3]	Parameter[3]	Command[2]	Parameter[2]	Command[2]	Parameter[2]
D2	Command[2]	Parameter[2]	Command[1]	Parameter[1]	Command[1]	Parameter[1]
D1	Command[1]	Parameter[1]	Command[0]	Parameter[0]	Command[0]	Parameter[0]
D0	Command[0]	Parameter[0]	-	-	-	-

Table 20-14: LCD2 Parallel Interface Command/Parameter Format

REG[005Eh]	bits 5-4 = 00b		bits 5-4 = 01b		bits 5-4 = 10b	
D17	-	-	Command[15]	Parameter[15]	Command[15]	Parameter[15]
D16	-	-	Command[14]	Parameter[14]	Command[14]	Parameter[14]
D15	Command[15]	Parameter[15]	Command[13]	Parameter[13]	Command[13]	Parameter[13]
D14	Command[14]	Parameter[14]	Command[12]	Parameter[12]	Command[12]	Parameter[12]
D13	Command[13]	Parameter[13]	Command[11]	Parameter[11]	Command[11]	Parameter[11]
D12	Command[12]	Parameter[12]	Command[10]	Parameter[10]	-	-
D11	Command[11]	Parameter[11]	Command[9]	Parameter[9]	Command[10]	Parameter[10]
D10	Command[10]	Parameter[10]	Command[8]	Parameter[8]	Command[9]	Parameter[9]
D9	Command[9]	Parameter[9]	-	-	Command[8]	Parameter[8]
D8	Command[8]	Parameter[8]	Command[7]	Parameter[7]	Command[7]	Parameter[7]
D7	Command[7]	Parameter[7]	Command[6]	Parameter[6]	Command[6]	Parameter[6]
D6	Command[6]	Parameter[6]	Command[5]	Parameter[5]	Command[5]	Parameter[5]
D5	Command[5]	Parameter[5]	Command[4]	Parameter[4]	Command[4]	Parameter[4]
D4	Command[4]	Parameter[4]	Command[3]	Parameter[3]	Command[3]	Parameter[3]
D3	Command[3]	Parameter[3]	Command[2]	Parameter[2]	Command[2]	Parameter[2]
D2	Command[2]	Parameter[2]	Command[1]	Parameter[1]	Command[1]	Parameter[1]
D1	Command[1]	Parameter[1]	Command[0]	Parameter[0]	Command[0]	Parameter[0]
D0	Command[0]	Parameter[0]	-	-	-	-

20.4 LCD Serial Interface Data Format

The following information shows the possible data output formats when LCD2 is configured for a serial interface LCD panel. The Serial Data Direction (MSB or LSB) is selectable using REG[005Ch] bit 4.

20.4.1 8-bit Serial (RGB 3:3:2) Data Format

LCD2 8-bit serial interface LCD panel RGB 3:3:2 (REG[005Ch] bit 7 = 0 and REG[005Ch] bits 3-2 = 00b).

Table 20-15: 8-bit Serial (RGB 3:3:2) Data Format

Cycle Count	1	2	3	...	n+1
D7	R_0^5	R_1^5	R_2^5	...	R_n^5
D6	R_0^4	R_1^4	R_2^4	...	R_n^4
D5	R_0^3	R_1^3	R_2^3	...	R_n^3
D4	G_0^5	G_1^5	G_2^5	...	G_n^5
D3	G_0^4	G_1^4	G_2^4	...	G_n^4
D2	G_0^3	G_1^3	G_2^3	...	G_n^3
D1	B_0^5	B_1^5	B_2^5	...	B_n^5
D0	B_0^4	B_1^4	B_2^4	...	B_n^4

20.4.2 8-bit Serial (RGB 4:4:4) Data Format

LCD2 8-bit serial interface LCD panel RGB 3:3:2 (REG[005Ch] bit 7 = 0 and REG[005Ch] bits 3-2 = 01b).

Table 20-16: 8-bit Serial (RGB 4:4:4) Data Format

Cycle Count	1	2	3	...	3n+1	3n+2	3n+3
D7	R_0^5	B_0^5	G_1^5	...	R_n^5	B_n^5	G_{n+1}^5
D6	R_0^4	B_0^4	G_1^4	...	R_n^4	B_n^4	G_{n+1}^4
D5	R_0^3	B_0^3	G_1^3	...	R_n^3	B_n^3	G_{n+1}^3
D4	R_0^2	B_0^2	G_1^2	...	R_n^2	B_n^2	G_{n+1}^2
D3	G_0^5	R_1^5	B_1^5	...	G_n^5	R_{n+1}^5	B_{n+1}^5
D2	G_0^4	R_1^4	B_1^4	...	G_n^4	R_{n+1}^4	B_{n+1}^4
D1	G_0^3	R_1^3	B_1^3	...	G_n^3	R_{n+1}^3	B_{n+1}^3
D0	G_0^2	R_1^2	B_1^2	...	G_n^2	R_{n+1}^2	B_{n+1}^2

20.4.3 16-Bit Serial (RGB 4:4:4 - MSB Unused) Data Format

LCD2 16-bit serial interface LCD panel RGB 4:4:4 MSB unused (REG[005Ch] bit 7 = 1 and REG[005Ch] bits 3-2 = 00b).

Table 20-17: 16-bit Serial (RGB 4:4:4 - MSB Unused) Data Format

Cycle Count	**1**	**2**	**3**	**...**	**n**
D15	R_0^3	R_1^3	R_2^3	...	R_n^3
D14	R_0^2	R_1^2	R_2^2	...	R_n^2
D13	R_0^1	R_1^1	R_2^1	...	R_n^1
D12	R_0^0	$R_1^{'}$	R_2^0	...	R_n^0
D11	G_0^3	G_1^3	G_2^3	...	G_n^3
D10	G_0^2	G_1^2	G_2^2	...	G_n^2
D9	G_0^1	G_1^1	G_2^1	...	G_n^1
D8	G_0^0	G_1^0	G_2^0	...	G_n^0
D7	B_0^3	B_1^3	B_2^3	...	B_n^3
D6	B_0^2	B_1^2	B_2^2	...	B_n^2
D5	B_0^1	B_1^1	B_2^1	...	B_n^1
D4	B_0^0	B_1^0	B_2^0	...	B_n^0
D3	-	-	-	...	-
D2	-	-	-	...	-
D1	-	-	-	...	-
D0	-	-	-	...	-

20.4.4 16-Bit Serial (RGB 4:4:4 - MSB Used) Data Format

LCD2 16-bit serial interface LCD panel RGB 4:4:4 MSB used (REG[005Ch] bit 7 = 1 and REG[005Ch] bits 3-2 = 01b).

Table 20-18: 16-bit Serial (RGB 4:4:4 - MSB Used) Data Format

Cycle Count	**1**	**2**	**3**	**...**	**n+1**
D15	R_0^5	R_1^5	R_2^5	...	R_n^5
D14	R_0^4	R_1^4	R_2^4	...	R_n^4
D13	R_0^3	R_1^3	R_2^3	...	R_n^3
D12	R_0^2	R_1^2	R_2^2	...	R_n^2
D11	G_0^5	G_1^5	G_2^5	...	G_n^5
D10	G_0^4	G_1^4	G_2^4	...	G_n^4
D9	G_0^3	G_1^3	G_2^3	...	G_n^3
D8	G_0^2	G_1^2	G_2^2	...	G_n^2
D7	B_0^5	B_1^5	B_2^5	...	B_n^5
D6	B_0^4	B_1^4	B_2^4	...	B_n^4
D5	B_0^3	B_1^3	B_2^3	...	B_n^3
D4	B_0^2	B_1^2	B_2^2	...	B_n^2
D3	-	-	-	...	-
D2	-	-	-	...	-
D1	-	-	-	...	-
D0	-	-	-	...	-

20.4.5 16-Bit Serial (RGB 5:6:5) Data Format

LCD2 16-bit serial interface LCD panel RGB 5:6:5 (REG[005Ch] bit 7 = 1 and REG[005Ch] bits 3-2 = 10).

Table 20-19: 11-7 16-bit Serial (RGB 5:6:5) Data Format

Cycle Count	1	2	3	...	n+1
D15	R_0^5	R_1^5	R_2^5	...	R_n^5
D14	R_0^4	R_1^4	R_2^4	...	R_n^4
D13	R_0^3	R_1^3	R_2^3	...	R_n^3
D12	R_0^2	R_1^2	R_2^2	...	R_n^2
D11	R_0^1	R_1^1	R_2^1	...	R_n^1
D10	G_0^5	G_1^5	G_2^5	...	G_n^5
D9	G_0^4	G_1^4	G_2^4	...	G_n^4
D8	G_0^3	G_1^3	G_2^3	...	G_n^3
D7	G_0^2	G_1^2	G_2^2	...	G_n^2
D6	G_0^1	G_1^1	G_2^1	...	G_n^1
D5	G_0^0	G_1^0	G_2^0	...	G_n^0
D4	B_0^5	B_1^5	B_2^5	...	B_n^5
D3	B_0^4	B_1^4	B_2^4	...	B_n^4
D2	B_0^3	B_1^3	B_2^3	...	B_n^3
D1	B_0^2	B_1^2	B_2^2	...	B_n^2
D0	B_0^1	B_1^1	B_2^1	...	B_n^1

20.4.6 18-bit Serial (RGB 6:6:6) Data Format

LCD2 18-bit serial interface LCD panel RGB 6:6:6 (REG[005Ch] bit 7 = 1 and REG[005Ch] bits 3-2 = 11b)

Table 20-20: 18-bit Parallel (RGB 6:6:6) Data Format

Cycle Count	**1**	**2**	**3**	**...**	**n+1**
D17	R_0^5	R_1^5	R_2^5	...	R_n^5
D16	R_0^4	R_1^4	R_2^4	...	R_n^4
D15	R_0^3	R_1^3	R_2^3	...	R_n^3
D14	R_0^2	R_1^2	R_2^2	...	R_n^2
D13	R_0^1	R_1^1	R_2^1	...	R_n^1
D12	R_0^0	R_1^0	R_2^0	...	R_n^0
D11	G_0^5	G_1^5	G_2^5	...	G_n^5
D10	G_0^4	G_1^4	G_2^4	...	G_n^4
D9	G_0^3	G_1^3	G_2^3	...	G_n^3
D8	G_0^2	G_1^2	G_2^2	...	G_n^2
D7	G_0^1	G_1^1	G_2^1	...	G_n^1
D6	G_0^0	G_1^0	G_2^0	...	G_n^0
D5	B_0^5	B_1^5	B_2^5	...	B_n^5
D4	B_0^4	B_1^4	B_2^4	...	B_n^4
D3	B_0^3	B_1^3	B_2^3	...	B_n^3
D2	B_0^2	B_1^2	B_2^2	...	B_n^2
D1	B_0^1	B_1^1	B_2^1	...	B_n^1
D0	B_0^0	B_1^0	B_2^0	...	B_n^0

20.5 LCD Bypass Function

The S1D13719 LCD Bypass function allows the Host CPU to access the LCD panel directly. When this function is enabled, the LCD controls signals from the Host CPU bypass the S1D13719 (the S1D13719 performs no timing operations). Parallel or Serial interface panels on either LCD1 or LCD2 can be used with Bypass Mode.

20.5.1 LCD Serial Bypass

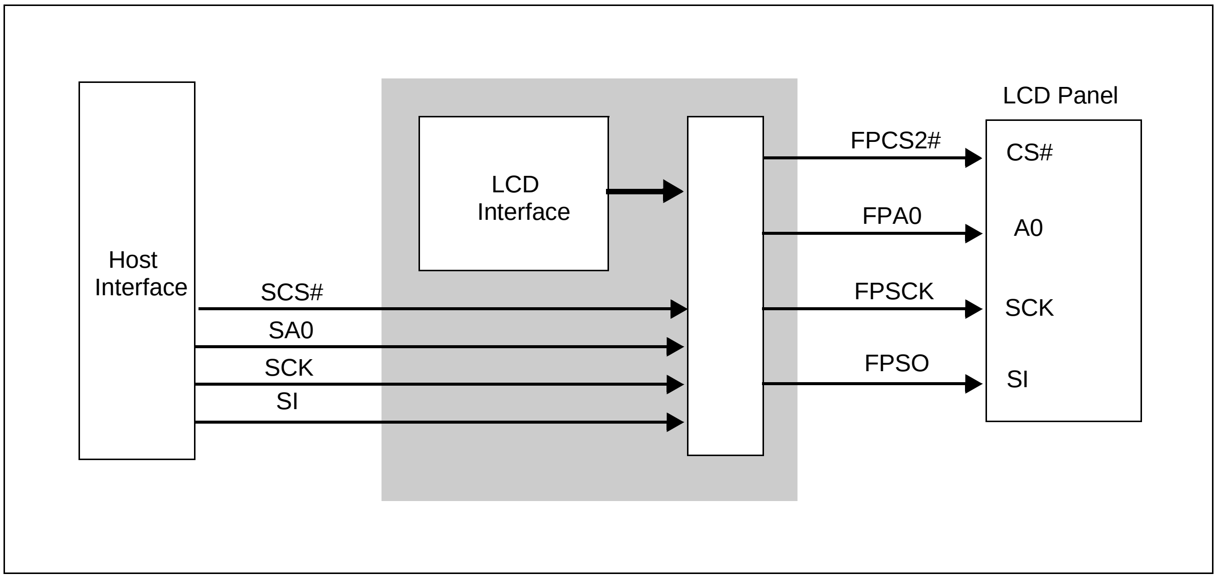


Figure 20-2: LCD Serial Bypass

LCD2 serial interface LCD panel mode A (REG[0014h] bits 12-8 = 10100)

LCD1 serial interface LCD panel mode B (REG[0014h] bits 12-8 = 10110)

Table 20-21: LCD Serial Bypass

Mode	Panel	SCS#	SCK	SA0	SI
A	LCD2	FPCS2#	FPSCK	FPA0	FPSO
B	LCD1	FPCS1#	FPSCK	FPA0	FPSO

20.5.2 LCD Parallel Bypass

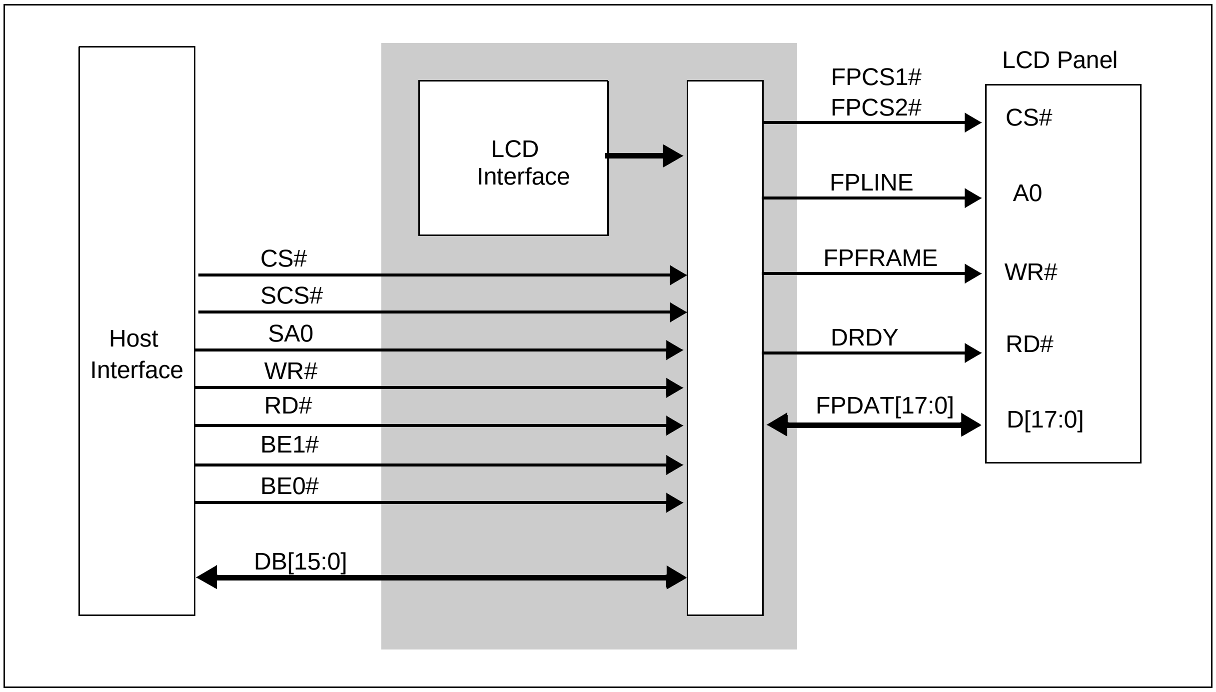


Figure 20-3: LCD Parallel Bypass

LCD1 parallel interface LCD panel mode C (REG[0014h] bits 12-8 = 10010b)

LCD1 parallel interface LCD panel mode D (REG[0014h] bits 12-8 = 10011b)

LCD1 parallel interface LCD panel mode E (REG[0014h] bits 12-8 = 11011b)

LCD2 parallel interface LCD panel mode F (REG[0014h] bits 12-8 = 10000b)

LCD2 parallel interface LCD panel mode G (REG[0014h] bits 12-8 = 10001b)

LCD2 parallel interface LCD panel mode H (REG[0014h] bits 12-8 = 11001b)

Table 20-22: LCD Parallel Bypass

Mode	Panel	SCS#	SA0	Write	Read	DB[15:0]
C	LCD1	FPCS1#	FPLINE	FPFRAME	DRDY	FPDAT[15:0]
D	LCD1	FPCS1#	FPLINE	FPFRAME	DRDY	FPDAT[17:13], FPDAT[11:1]
E	LCD1	FPCS1#	FPLINE	FPFRAME	DRDY	FPDAT[17:10], FPDAT[8:1]
F	LCD2	FPCS2#	FPLINE	FPFRAME	DRDY	FPDAT[15:0]
G	LCD2	FPCS2#	FPLINE	FPFRAME	DRDY	FPDAT[17:13], FPDAT[11:1]
H	LCD2	FPCS2#	FPLINE	FPFRAME	DRDY	FPDAT[17:10], FPDAT[8:1]

20.5.3 Direction of LCD Parallel Bypass

LCD parallel interface LCD panel write mode (REG[0014h] bit 13 = 0)

LCD parallel interface LCD panel read mode (REG[0014h] bit 13 = 1)

Table 20-23: Direction of LCD Parallel Bypass

Direction	mode	SCS#	SA0	WR#	RD#	DB[15:0]
C-H	Write	Input	Input	Input	Input	Input
C-H	Read	Input	Input	Input	Input	Output

21 Camera Interface

21.1 Camera Input Data

The S1D13719 supports camera modules up to a maximum size of 1280x1024 (SXGA). The camera interface has an 8/16-bit data bus and receives YUV 4:2:2 format image data synchronized with the camera clocks.

The S1D13719 is designed with a 2-port Came interface. However only one camera support can be used at a time.(when Camera1 is enabled, Camera2 is disabled.)

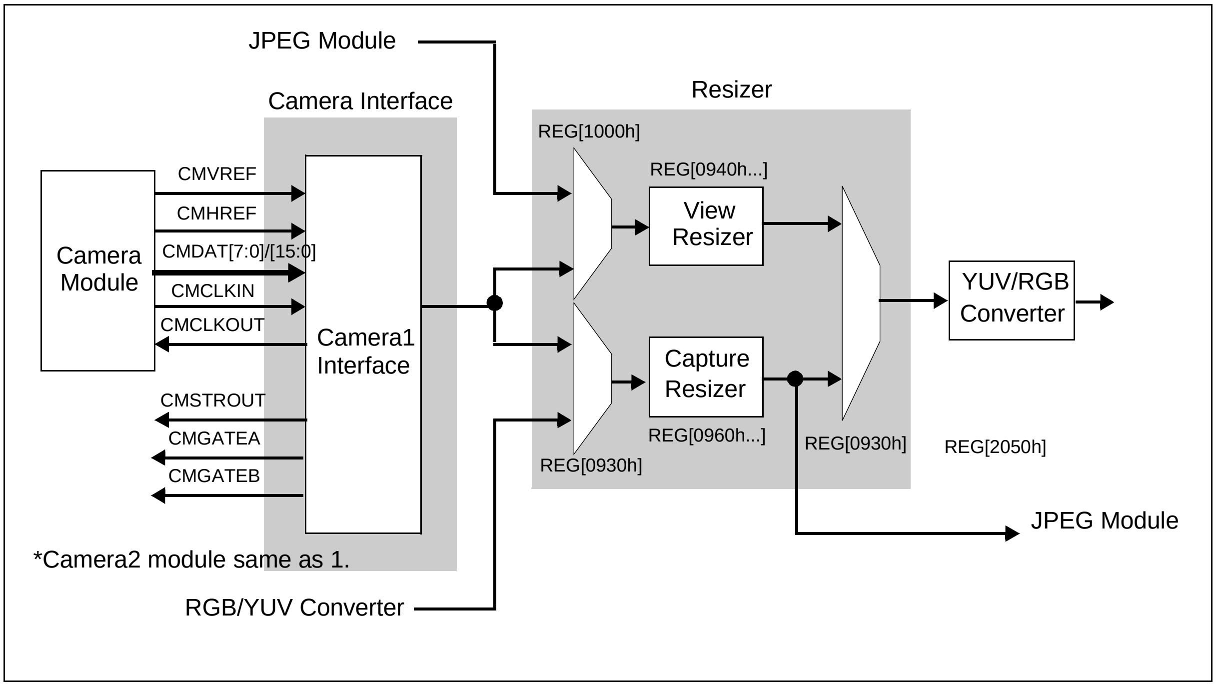


Figure 21-1: Camera Interface

To confirm whether the S1D13719 supports a specific camera implementation, see the AC timing details in Section 2.7, “Camera Interface”.

21.1.1 JPEG Camera Display

The camera image data when JPEG is used resizes with View Resizer and does the write to the buffer for the display with YUV/RGB converter 1. The camera display to the LCD panel can synchronize with the JPEG function by the register (REG[0930h] bits 1-0).

21.1.2 JPEG Encode

The JPEG encode image data resizes with Capture Resizer and does the write to the JPEG line buffer. The capture of the camera image data can be begun on the register (REG[098Ah] bit 0).

21.1.3 YUV Data Output

YUV data can be output to the Host CPU via the JPEG FIFO by resizing the camera image data using the capture resizer. The YUV data format is selected between YUV 4:2:2 an using REG[0980h] bits 3-1.

21.2 Frame Capture Interrupt

Interrupt can be generated at the capture of the camera image data. The interrupt generation timing can be synchronized with the JPEG beginning or the strobe output.

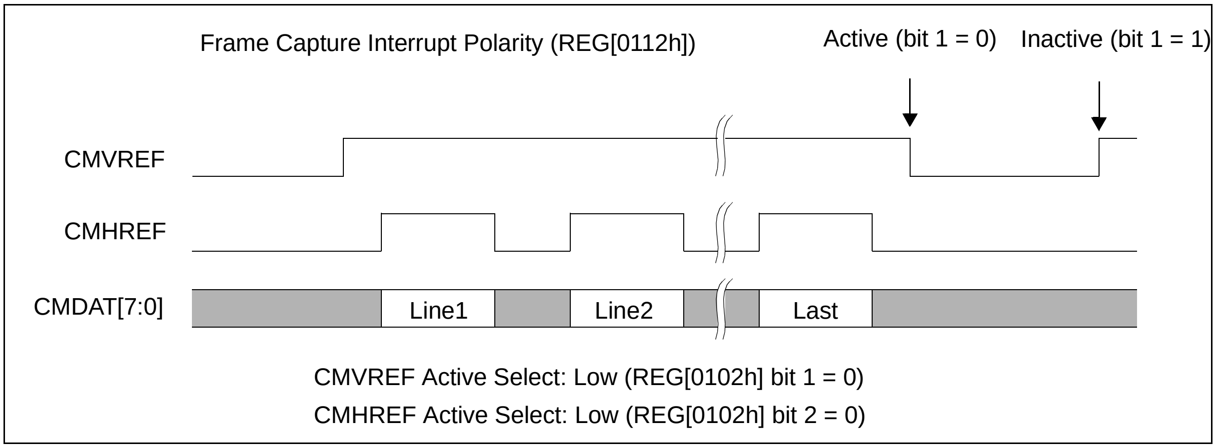


Figure 21-2: Frame Capture Interrupt

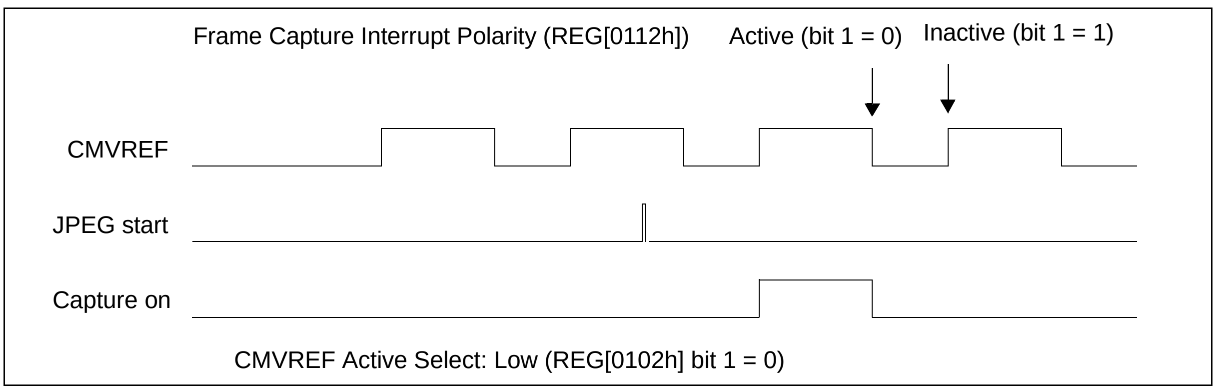


Figure 21-3: Frame Capture Interrupt (JPEG Encode)

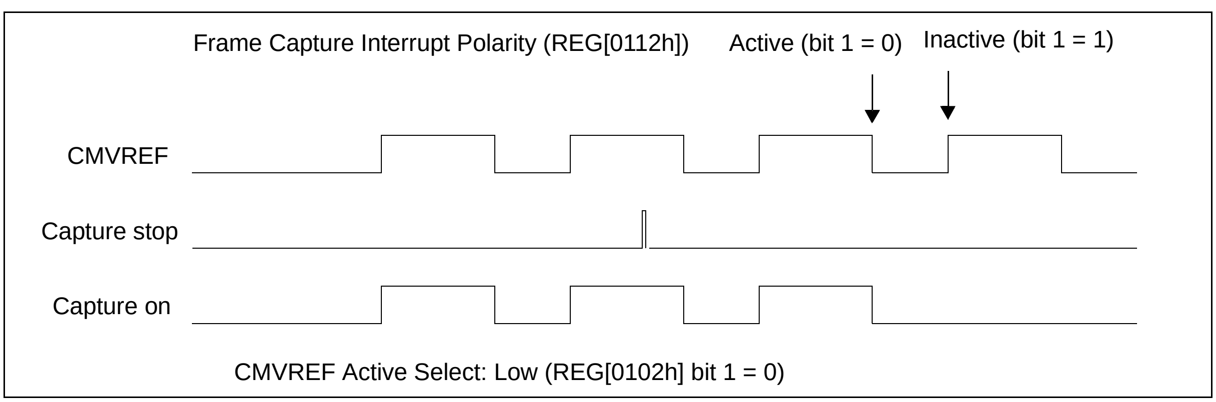


Figure 21-4: Frame Capture Interrupt (Capture Stops)

21.3 Strobe Control Signal

When the camera interface is enabled, a strobe feature is available. Typically the strobe signal controls the external camera flash or camera data and is used in conjunction with the camera interface and the JPEG Encoder to capture or display the optimal camera image after the camera flash has gone off or the camera data output is enabled.

The strobe output is controlled using REG[0120h] - REG[0124h]. The strobe control signal output pin is CMSTROUT and must be enabled using the Strobe Port Enable bit (REG[0124h] bit 3).

21.3.1 Generating a Strobe Pulse

A strobe pulse (CMSTROUT) can be generated in three ways:

JPEG Encode

1. Enable the camera interface in continuous frame capture mode (REG[0112] bit 6 = 0) and ensure that the CMVREF and CMHREF signals are present. ITU-R BT656 data format must not be enabled (REG[0110h] bit 7 = 0).
2. Enable the JPEG Module (REG[0980h] bit 0 = 1) and set the JPEG Operation Mode bits (REG[0980h] bits 3-1 to 000b (JPEG Encode). Setup the applicable JPEG Module and JPEG Codec registers.
3. Configure the Strobe Line Delay (REG[0120h]), Strobe Pulse Width (REG[0122h], Strobe Active Select (REG[0124h] bit 1), and Strobe Capture Delay (REG[0124h] bits 7-4).
4. Enable the strobe control signal output port by setting the Strobe Enable bit (REG[0124h] bit 3 = 1).
5. Enable the strobe signal (CMSTROUT) by setting the Strobe Port Select bit (REG[0124] bit 0 = 1). This bit must remain enabled for the entire duration of the delay value (REG[0124h] bits 7-4), otherwise the strobe will be disabled immediately when the Strobe Enable bit is set to 0.
6. Generate a strobe signal (CMSTROUT) by starting the JPEG Encode by setting the JPEG Start/Stop Control bit to 1 (REG[098A] bit 0 = 1). The camera frame encoded depends on the Strobe Capture Delay Control in step 3.

Before generating another strobe signal, the JPEG CODEC must be stopped, REG[098Ah] bit 0 = 0. Then generate the strobe pulse again by setting the JPEG Start/Stop Control bit to 1, REG[098Ah] bit 0 = 1.

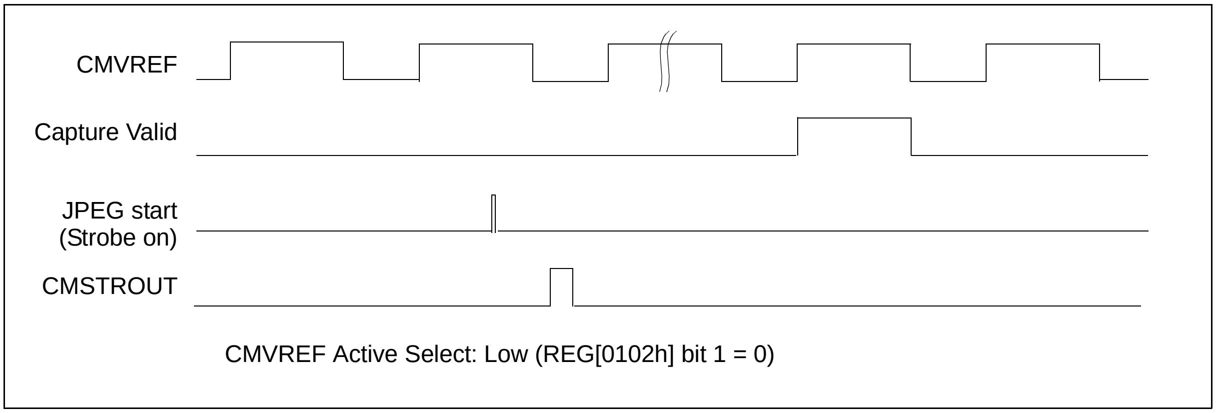


Figure 21-5: Strobe Operation (JPEG Encode Start)

Stop Capturing in Repeat Capture Mode

1. Enable the camera interface in continuous frame capture mode (REG[0112h] bit 6 = 0) and ensure that the CMVREF and CMHREF signals are present. ITU-R BT656 data format must not be enabled (REG[0110h] bit 7 = 0).
2. Configure the Strobe Line Delay Timing (REG[0120h]), Strobe Pulse Width (REG[0122h], Strobe Active Select (REG[0124h] bit 1), and Strobe Capture Delay (REG[0124h] bits 7-4).
3. Enable the strobe control signal output port by setting the Strobe Enable bit (REG[0124h] bit 3 = 1).
4. Enable the strobe signal (CMSTROUT) by stopping the camera frame capture (REG[0114h] bit 3 = 1). The last camera frame captured depends on the Strobe Capture Delay Control in step 2.

Before generating another strobe signal, the JPEG CODEC must be stopped, REG[098Ah] bit 0 = 0. Then generate the strobe pulse again by setting the JPEG Start/Stop Control bit to 1, REG[098Ah] bit 0 = 1.

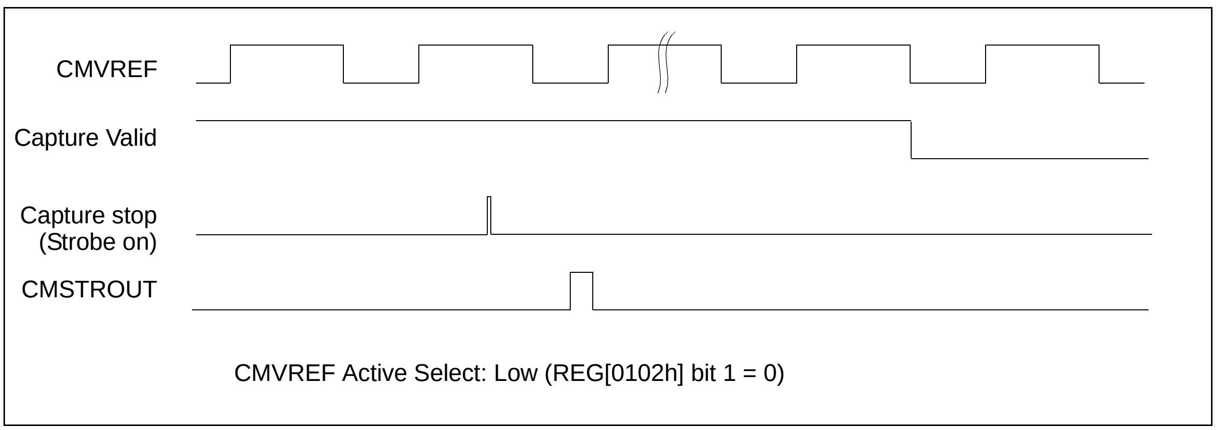


Figure 21-6: Strobe Operation (Continuous Capture Stopped)

Single Camera Frame Capture

1. Enable the camera interface in single frame capture mode (REG[0112h] bit 6 = 1) and ensure that the CMVREF and CMHREF signals are present. ITU-R BT656 data format must not be enabled (REG[0110h] bit 7 = 0).
2. Configure the Strobe Line Delay Timing (REG[0120h]), Strobe Pulse Width (REG[0122h], Strobe Active Select (REG[0124h] bit 1), and Strobe Capture Delay (REG[0124h] bits 7-4).
3. Enable the strobe control signal output port by setting the Strobe Enable bit (REG[0124h] bit 3 = 1).
4. Enable the strobe signal (CMSTROUT) by capturing a camera frame (REG[0114h] bit 2 = 1). The camera frame that is captured, is the one occurring right after the strobe signal and is not dependant on the Strobe Capture Delay in step 2.

Before generating another strobe signal, the JPEG CODEC must be stopped, REG[098Ah] bit 0 = 0. Then generate the strobe pulse again by setting the JPEG Start/Stop Control bit to 1, REG[098Ah] bit 0 = 1.

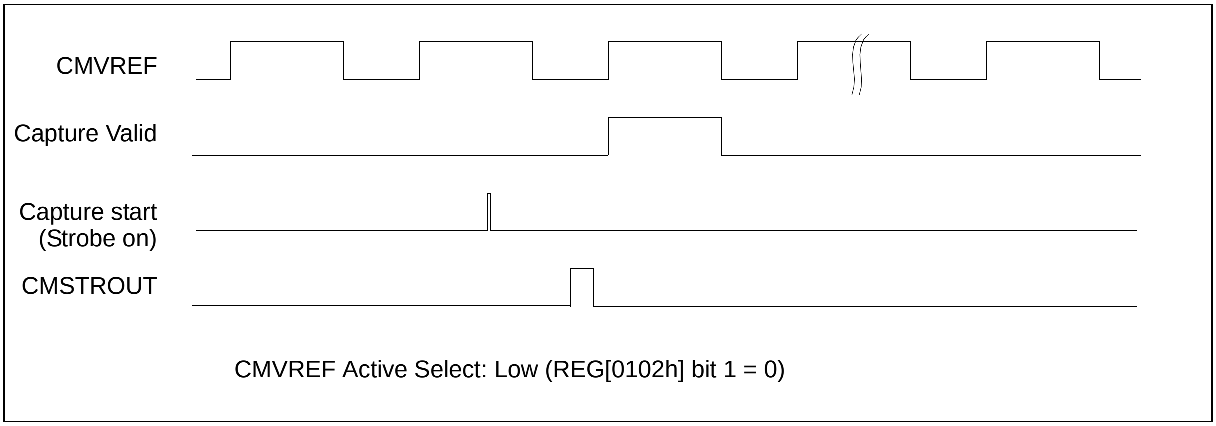


Figure 21-7: Strobe Operation (Single Frame Capture)

21.3.2 Strobe Timing

The strobe pulse (CMSTROUT) begins on the falling edge of CMHREF after CMVREF as specified by the Strobe Line Delay Timing bits (REG[0120h] bits 15-0). A zero delay (REG[0120h] bits 15-0 = 00h) starts the strobe pulse (CMSTROUT) on the first falling edge of CMHREF after CMVREF.

Note

Both the Line Delay and Pulse Width signals are specified by counting HREFs which leads to an inherent timing delay if the HREF signal stops. This inherent delay must be considered when programming the Line Delay (REG[0120h]) and Pulse Width (REG[0122h]) registers.

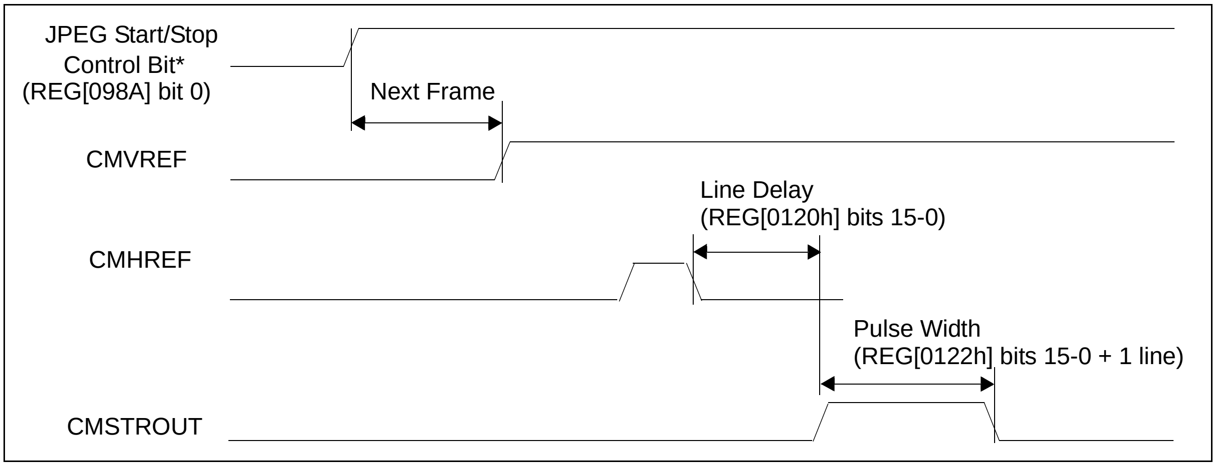


Figure 21-8: Strobe Signal Output Timing

Note

The Line Delay (REG[0120h] bits 15-0) and the Pulse Width (REG[0122h] bits 15-0) may be set greater than the period of the CMVREF signal.

22 SD Memory Card Interface

The S1D13719 SD Memory Card interface is compatible with the SD Memory Card Physical Layer Specification Version 1.0. Either a 1-bit or 4-bit interface can be selected. This implementation of the SD Memory Card interface does not support SPI mode or hardware security functions.

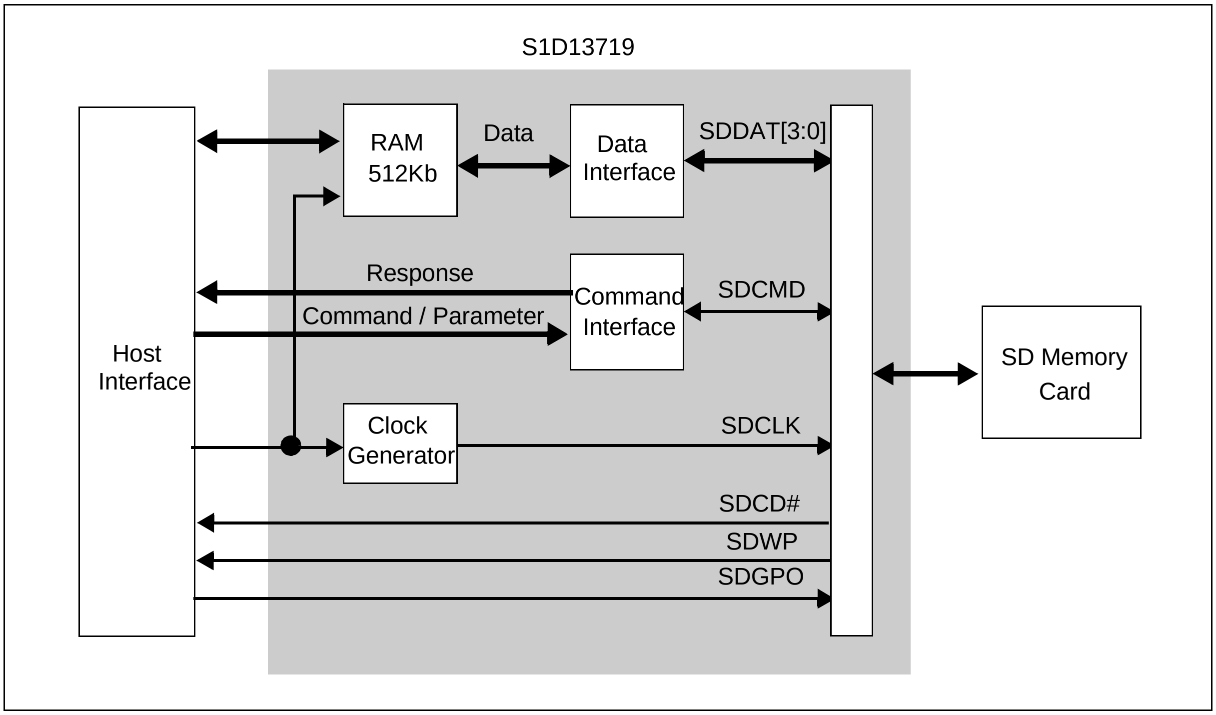


Figure 22-1: SD Memory Card Interface Block Diagram

22.1 Interface Commands

The SD memory card interface supports eight different commands.

Send Command

The send command transmits the command stream to the SDCMD pin. The command stream is composed of the contents of the command register (REG[610Ch] and the parameter registers (REG[6110h] - REG[6116h]).

Receive Response

The receive response command starts receiving the response stream from the SDCMD pin. There are two lengths of response streams (48 bits and 136 bits). The response data is written to the appropriate response registers for the length of the response stream (REG[6120h] - REG[613Eh]).

Wait Busy

This command waits for the data pins (SDDAT[3:0] to be ready.

Receive Data

The receive data command receives the data stream from the SDDAT[3:0] pins. When data is received, it is written to memory. The data length for received data can be configured between 1-512 using the SD Memory Card Data Length registers (REG[6108h] - REG[610Ah]).

Send Data

The send data command transmits the data stream from memory to the SDDAT[3:0] pins. The data length for sent data can be configured between 1-512 using the SD Memory Card Data Length registers (REG[6108h] - REG[610Ah]).

SDCLK Change

This command initiates a new clock frequency for the SDCLK pin (see REG[6104h] bit 7).

Send 8 Clock

About eight clocks are transmitted from the SDCLK pin.

Synchronous Reset

This command performs a synchronous reset of the SD memory card interface. For details on this function, see the register description for REG[6104h] bit 0.

22.2 Pin Functions

There are nine pins used by the SD memory card interface. The SD card interface pins are multiplexed with the GPIO[19:11] pins, see Section 5.8, “SD Memory Card Interface Pin Mapping” for pin mapping information.

SD Card Data IO [3:0]

These four pins, SDDAT[3:0], are the SD memory card data IO bus.

SD Card Command IO

This pin, SDCMD, is the IO pin for the serial command/response stream data.

SD Card Clock Output

This pin, SDCLK, outputs the SD memory card clock signal.

Card Detect

The SDCD# pin detects whether a SD memory card is inserted or not. The state of this pin can be determined using the SD Memory Card Interrupt.

Write Protect

The SDWP pin detects whether the SD memory card is write-protected or not.

General Output

The SDGPO pin can be used to turn on/off the external pull-ups (SDCD# or SDWP) or for an LED.

23 General Purpose IO Pins

23.1 IO Cell Structure

The GPIO pins can be configured as input pins or output pins using registers REG[0300h] and REG[0302h]. At reset all GPIO pins are configured as inputs and the pull-down resistance, controlled by REG[0308h] and REG[030Ah], is enabled.

Note
The GPIO registers (REG[0300h] - [030Fh] are asynchronous and therefore are accessible while power save mode is enabled.

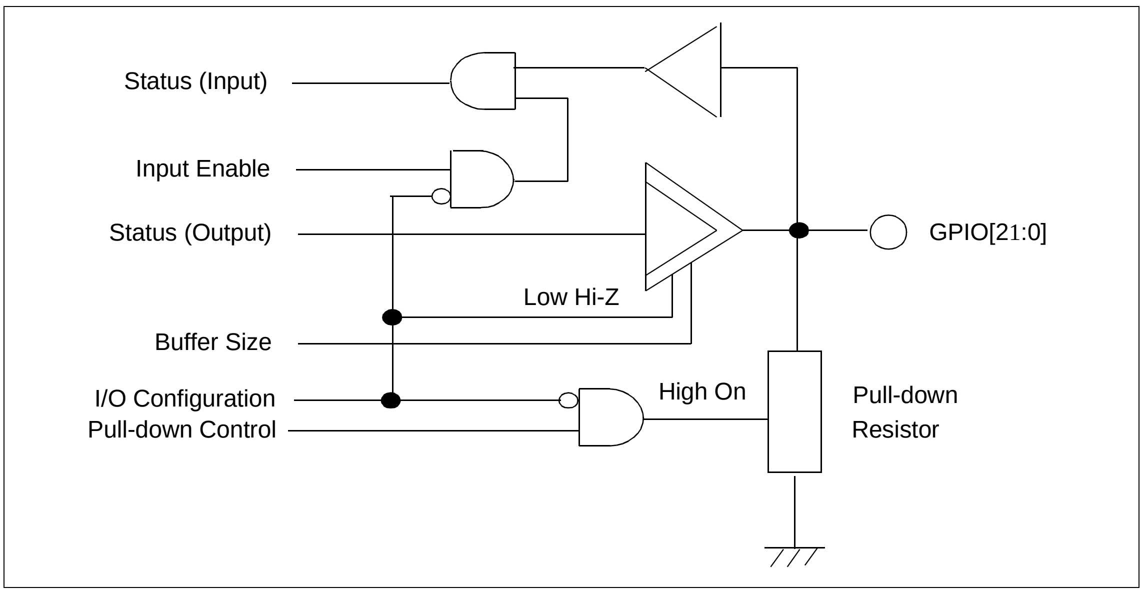


Figure 23-1: IO Cell Structure

23.2 Power Supply Considerations

The GPIO IO buffer is connected to PIOVDD.

Note
PIOVDD is used for both the panel interface and the GPIO pins.

24 Mechanical Data

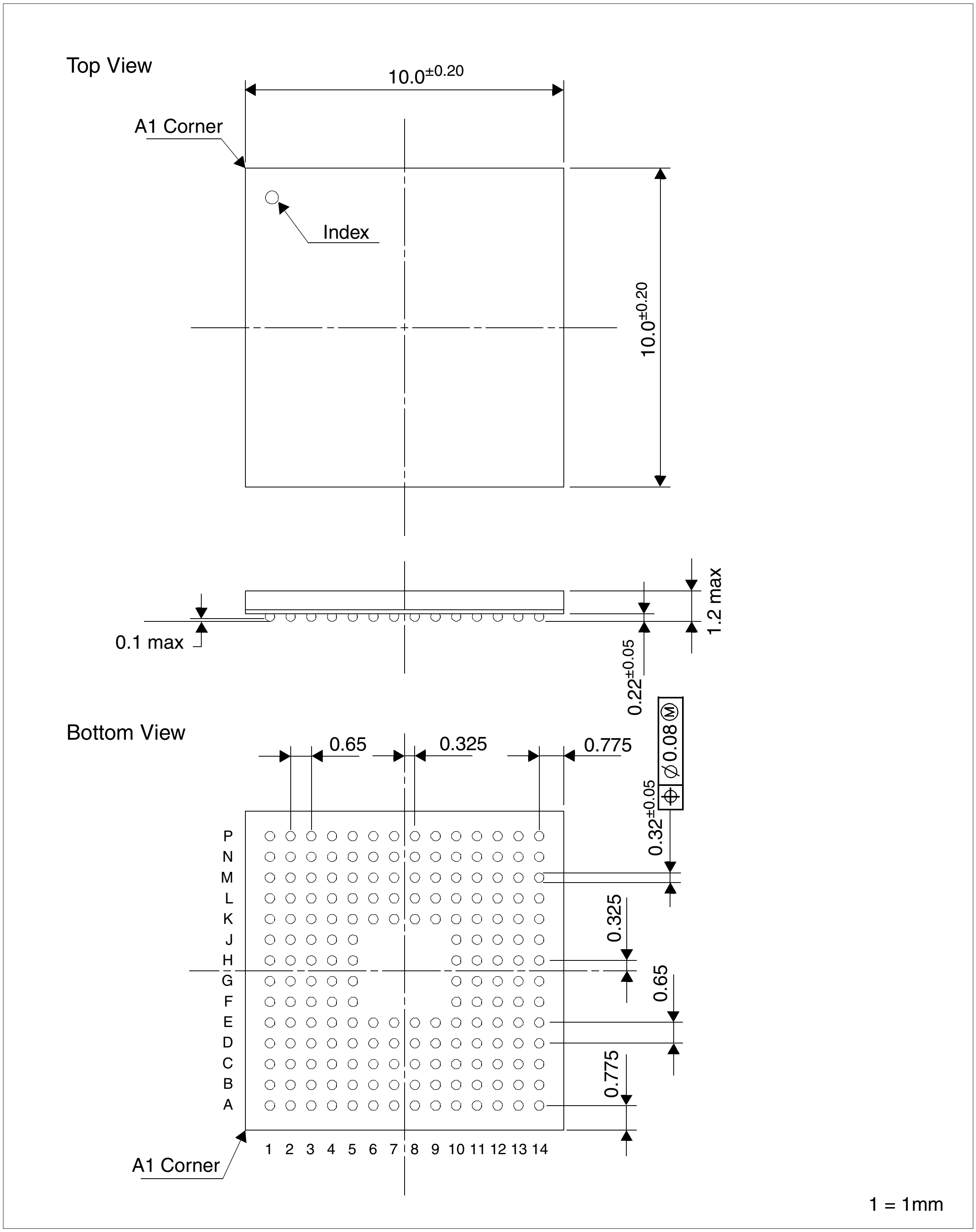


Figure 24-1: S1D13719 PFBGA 180-pin Package

25 References

The following documents contain additional information related to the S1D13719. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Research and Development Website at **www.erd.epson.com**.

- S1D13719 Product Brief (X59A-C-001-xx)

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26.1 Ordering Information

To order the S1D13719 Mobile Graphics Engine, contact the Epson sales representative in your area.

Change Record

X59A-A-001-01 Revision 1.5 - Issued: February 28, 2012

- globally remove QFP8 208-pin package
- globally remove FCBGA 240-pin package

X59A-A-001-01 Revision 1.4 - Issued: October 24, 2008

- All changes from the previous Revision are Red
- globally change “FPDRDY” to “DRDY”
- section 5.1 S1D13719 Pinout Diagram (PFBGA-180) - in table 5-1, S1D13719 PFBGA-180 Pin Mapping (Top View), change ball H11 to “CM1HREF”
- section 7.3.2 Direct 80 Type 2 - add tables 7-17 and 7-18, Direct 80 Type 2 Interface Truth Table (Big Endian / 1 CS# Mode) and Direct 80 Type 2 Interface Truth Table (Big Endian / 2 CS# Mode) respectively

X59A-A-001-01 Revision 1.3 - Issued: March 17, 2008

- Set revision to 1.3 to align with Japan revision numbering
- section 2.15, removed reference to internal oscillator
- section 2.18, added reference to QFP8 208-pin package
- section 5, globally renamed OSCVDD and OSCVSS pins to COREVDD and VSS
- section 5.3, added QFP8 pinout diagram
- section 6, removed references to OSCVDD
- section 7.2.1 Power-On Sequence - add CLKI to figure and Note 1 to table
- section 7.3.1 Direct 80 Type 1 - add 1.8 Volts timing to tables
- section 9.2.1, removed reference to internal oscillator
- section 24, added QFP8 mechanical information
- updated Epson tagline and copyright
- updated Sales and Technical Support addresses

X59A-A-001-01 Revision 1.02

- REG[023Ah] bits 6-0 - remove hex (h) designator from numbers in last two columns of table (numbers are in decimal)

X59A-A-001-01 Revision 1.01

- REG[096Ch], fixed typos, “view” resizer should read “capture” resizer
- REG[1660h] - REG[17A2h], fixed typo in table that referred to REG[17xxh] as REG[15xxh]

- REG[6100h] bits 7-4, updated divide ratio table to include 2:1 and 3:1, also updated System Clock Frequency table

X59A-A-001-01 Revision 1.0

- Released as Revision 1.0 (2004/04/20)

X59A-A-001-00 Revision 0.09

- REG[0006h] change description, 9ns -> 5ns
- REG[1000h] bit 4 DNL Marker not supported
- REG[1016h], REG[1018h] not supported
- JPEG Flow, JPEG FIFO Dummy Read x 2 -> when Host is Indirect Mode, 4 times. When Host is Direct Mode, 2 times

X59A-A-001-00 Revision 0.08

- Start showing change record
- section 5.3 Pin Descriptions, re-arrange pin numbering order in tables
- section 5.3.1 Host Interface Pins - correct typo in the description of CS#, change “bit 2” to “bit 3”
- section 5.3.2 LCD Interface Pins - change FPSCLK reset value to “1”
- section 5.5 Host Interface Pin Mapping - change table 5-6 title to “Indirect Host Interface Pin Mapping (2 CS# Mode)”
- section 7.1.1 Input Clocks - Table 7-1 Clock Input Requirements - add min/max to fosc
- section 7.1.3 PLL Clock - add description to section
- section 7.3.1 Direct 80 Type 1 - remove all references to WAIT/NO WAIT modes
- section 7.3.1 Direct 80 Type 1 - Table 7-7 Direct 80 Type 1 Interface Write Cycle Timing, change t109 to “WE# cycle time” with a min of 3
- section 7.3.1 Direct 80 Type 1 - remove notes 2 and 3 from Table 7-7 Direct 80 Type 1 Interface Write Cycle Timing
- section 7.3.2 Direct 80 Type 2 - remove all references to WAIT/NO WAIT modes
- section 7.3.2 Direct 80 Type 2 - Table 7-13 Direct 80 Type 2 Interface Write Cycle Timing, change t209 to “WEU#, WEL# cycle time” with a min of 3
- section 7.3.2 Direct 80 Type 2 - remove notes 2 and 3 from Table 7-13 Direct 80 Type 2 Interface Write Cycle Timing
- section 7.3.3 Direct 80 Type 3 - remove all references to WAIT/NO WAIT modes
- section 7.3.3 Direct 80 Type 3 - Table 7-19 Direct 80 Type 3 Interface Write Cycle Timing, change t309 to “WEU#, WEL# cycle time” with a min of 3
- section 7.3.3 Direct 80 Type 3 - remove notes 2 and 3 from Table 7-13 Direct 80 Type 3 Interface Write Cycle Timing

- section 7.3.3 Direct 80 Type 3 - Table 7-21 Direct 80 Type 3 Interface Truth Table (Little Endian / 1 CS# Mode) and Table 7-23 Direct 80 Type 3 Interface Truth Table (Little Endian / 2 CS# Mode) - change RDU# to 1 in table for 8-bit write; odd address
- section 7.3.4 Direct 68 - remove all references to WAIT/NO WAIT modes
- section 7.3.4 Direct 68 - Table 7-25 Direct 68 Interface Write Cycle Timing, change t409 to "WEU#, WEL# cycle time" with a min of 3
- section 7.3.4 Direct 68 - remove notes 2 and 3 from Table 7-25 Direct 68 Interface Write Cycle Timing
- section 7.3.4 Direct 68 - remove Table 7-27 Direct 80 Type 1 Interface Truth Table (Little Endian / 1 CS# Mode) and Table 7-28 Direct 80 Type 1 Interface Truth Table (Big Endian / 1 CS# Mode) as they do not belong
- section 7.3.5 Indirect 80 Type 1 - Table 7-31 Indirect 80 Type 1 Interface Write Cycle Timing, change t1107 to "WE# cycle time" and replace all instances of A1 with A[2:1]
- section 7.3.5 Indirect 80 Type 1 - remove Table 7-34 Indirect 80 Type 1 Interface Truth Table as it is redundant
- section 7.3.6 Indirect 80 Type 2 - Table 7-34 Indirect 80 Type 2 Interface Write Cycle Timing, change t1207 to "WEU#, WEL# cycle time", t1206 to "D[15:0] hold time from WEU#, WEL# rising edge" and replace all instances of A1 with A[2:1]
- section 7.3.7 Indirect 80 Type 3 - Table 7-37 Indirect 80 Type 3 Interface Write Cycle Timing, change t1307 to "WEU#, WEL# cycle time", t1306 to "D[15:0] hold time from WEU#, WEL# rising edge" and replace all instances of A1 with A[2:1]
- section 7.3.8 Indirect 68 - Figure 7-20 Indirect 68 Interface Write Cycle Timing, Table 7-40 Indirect 68 Interface Write Cycle Timing, Figure 7-21 Indirect 68 Interface Read Cycle Timing, and Table 7-41 Indirect 68 Interface Read Cycle Timing - replace signal names with correct ones
- section 7.4.1 Generic TFT Panel Timing- table 7-45 Generic TFT Panel Timing - change HDP Derived From to "((REG[0042h] bits 8-0) + 1) x 2"
- section 7.4.2 HR-TFT Panel Timing- table 7-59 HR-TFT Panel Horizontal Timing - change Note 12 to "t12typ = REG[009Eh] bits 4-0"
- section 7.4.2 HR-TFT Panel Timing- figure 7-32 HR-TFT Panel Vertical Timing - delete the label "Vertical Display Period"
- section 7.4.4 α-TFT Panel Timing- add section note "REG[0044h] bits 9-0 must be set to zero when using the a-TFT panel"
- section 7.4.4 α-TFT Panel Timing- table 7-52 α-TFT Panel Horizontal Timing - change Note 2 to "t1typ = REG[0080h] bits 9-0 + 1"
- section 7.4.5 TFT Type 2 Panel Timing- table 7-54 TFT Horizontal Timing - change t5 Units to Lines
- section 7.4.9 LCD1 ND-TFD, LCD2 9-Bit Serial Interface Timing - Table 7-61 LCD1 ND-TFD, LCD2 9-Bit Serial Interface Timing - update t10 Typ to 2.5

- section 7.4.12 LCD1 uWIRE Serial Interface Timing- table 7-66 uWIRE Serial Interface Timing - change t7 Typ to 1.5
- section 7.4.13 LCD1, LCD2 SPI Serial Interface Timing - add entire new section
- section 7.4.14 LCD1, LCD2 Parallel Interface (80) - Table 7-68 LCD1, LCD2 Parallel Interface Timing (80) - change t9 Typ to “Note 2”, add new t12
- section 7.4.15 LCD1, LCD2 Parallel Interface (68) - Table 7-69 LCD1, LCD2 Parallel Interface Timing (68) - change t3 Typ to 2, t9 Typ to “Note 2”, add new t12
- section 10.3 Register Restrictions - change the second bullet to “REG[0000h] through...and REG[0300h] through REG[030Eh] are not reset...”
- REG[000Eh] bits 1-0, updated V-Divider bit description to clarify its effect on PLL jitter and power consumption
- REG[0010h] bits 15-12, updated VCO Kv Set bit description to clarify its effect on PLL jitter and power consumption
- REG[0014h] bit 3 - correct typo in the table, change “bit 2” to “bit 3”
- REG[0032h] bit 9 - rename bit
- REG[0032h] bit 8 - rename bit and reverse the active settings of bit, 0 = active low, 1 = active high
- REG[0046h] bit 7 - add note to bit description “This bit does have an effect in Mode 1 LCD 2 configuration.”
- REG[0050h] bit 7 - add to bit description “This bit does have an effect in Mode 1 LCD 2 configuration.”
- REG[0068h] bits 15-8 - add formula to bit description
- REG[0068h] bits 15-8 - change reference to “REG[0056h] bit 15 = 0” to “REG[0056h] bit 15 = 1”
- REG[0068h] bits 7-0 - add formula to bit description
- REG[0068h] bits 7-0 - change reference to “REG[0056h] bit 15 = 0” to “REG[0056h] bit 15 = 1”
- REG[006Ah] bits 15-8 - add formula to bit description
- REG[006Ah] bits 15-8 - change reference to “REG[0056h] bit 15 = 0” to “REG[0056h] bit 15 = 1”
- REG[006Ah] bits 7-0 - add formula to bit description
- REG[006Ah] bits 7-0 - change reference to “REG[0056h] bit 15 = 0” to “REG[0056h] bit 15 = 1”
- REG[009Eh] - remove note
- REG[0100h] - add note “1:1 camera clock JPEG encode should be limited...”
- REG[0104h] - add note “1:1 camera clock JPEG encode should be limited...”
- REG[0110h] bit 10 - add note “For Camera clock divides of 1:1 and 2:1...”

- REG[0122h] - add equation to bit description
- REG[0124h] bit 3 - rewrite bit description
- REG[0124h] bit 1 - rewrite bit description
- REG[0124h] bit 0 - rewrite bit description
- REG[0128h] - add "in horizontal lines (CM2HREF period)" to equation
- REG[012Ah] - add "in pixels where 1 pixel is 2 CM2CLKOUTs" to equation
- REG[0200h] bits 12-11 - add note "REG[0240] bits 13-12 must be set to the same mode..." and rewrite the notes "When double buffer mode is enabled..." and "When triple buffer mode is enabled..."
- REG[0228h] - correct typos in the PIP+ field definitions
- REG[023Ah] bits 6-0 - correct typos in formulas in bit description
- REG[0254h] bits 2-1, add triple buffer to the bit description
- REG[09A8h] - add note to bit description
- added REG[09AEh]
- REG[09BCh] - correct typo and add note to bit description
- REG[0A06h] bit 1 - add mask bit to bit description
- REG[1004h] - add note "This register is read only..."
- REG[1012h - 1014h] - add note "1:1 camera clock JPEG encode should be limited..."
- REG[101Eh] - add note "This register resets to 0000h after reading"
- REG[6104h] bit 2 - correct typo in bit description, change "REG[6110h] - REG[6116]" to "REG[6118h] - REG[611E]"
- REG[8006h] - reserve this register
- REG[8020h] - correct typos in bit description, change "REG[8000h] bit 18" to "REG[8002h] bit 4"
- REG[8024h] - correct typos in bit description, change "REG[8000h] bit 18" to "REG[8002h] bit 4"
- section 11.2 Power Save Mode Function - for LCD interface outputs...for panel support, under power save mode change FPSCLK to "see note 1" and add note 1
- section 11.2 Power Save Mode Function - for camera1, camera2 clock, under power save mode change description
- section 21.3.1 Generating a Strobe Pulse- rewrite paragraphs "Before generating another strobe signal..."