AN11044

Pin FMEA for 74HC/74HCT family

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Document information

Information	Content
Keywords	FMEA, HC, HCT, CMOS
Abstract	This application note provides a Failure Modes and Effects Analysis (FMEA) for Nexperia's 74HC/74HCT family under typical failure situations

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1. Introduction

The 74HC/74HCT high-speed Si-gate CMOS logic family combines the low power advantages of the HEF4000B family with the high speed and drive capability of the Low power Schottky TTL (LSTTL).

The 74HC/74HCT family has the same pin-out as the 74 series and provides the same circuit functions. The family includes several HEF4000B family circuits that do not have TTL counterparts, and have some special circuits. The basic family of buffered devices, designated as 74HCxxxx, operates at CMOS input logic levels for high-noise immunity with negligible typical quiescent supply and input current. The family requires a power supply of 2 V to 6 V. A subset of the family, designated as 74HCTxxxx with the same features as the “HC-types” will operate with a standard TTL power supply of 5 V (±10 %) and logic input levels (0.8 V to 2.0 V) for use as pin-to-pin compatible CMOS replacements for reducing power consumption without loss of speed. These types are also suitable for TTL-to-CMOS switching converters.

2. Pin FMEA

This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of Nexperia’s HC/HCT family under typical failure situations such as a short-circuit to V_{CC} or GND or to a neighboring pin, or if a pin is left open.

A failure is classified according to its effect on the HC/HCT device and the functionality of the application; see Table 1.

Table 1. Classification of failure effects

Class	Failure effect
A	damage to device
	affects application functionality
B	no damage to device
	may affect application functionality
C	no damage to device
	no affect to application functionality

Table 2. FMEA matrix for pin short-circuit to V_{CC}

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined HIGH, no damage, no leakage, no output level change
Output	A	if output defined LOW, short-circuits and high currents can damage device, output level changes
GND	B	short-circuits and high currents can damage device, will affect functionality
Exposed pad	A	Short-circuits and high currents can damage device and will affect the functionality. It only applies in case exposed pad has GND potential by internal connection. See data sheet of product concerned.

Table 3. FMEA matrix for pin short-circuit to GND

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined LOW, no damage, no leakage, no output level change
Output	A	if output defined HIGH, short-circuits and high currents can damage device, output level changes
V_{CC}	B	if input defined LOW, no damage, affects functionality
V_{CC}	A	if input defined HIGH, short-circuits and high currents can damage device, affects functionality
Exposed pad	A	Short-circuits and high currents can damage device and will affect the functionality. It only applies in case exposed pad has V_{CC} potential by internal connection. See data sheet of product concerned.

Table 4. FMEA matrix for pin left open

Pin	Class	Remarks
Input	B	undefined operating condition, no damage, increases leakage, may affect functionality
Output	C	normal operating condition, no damage, no leakage
GND	B	undefined operating condition, no damage, increases leakage, will affect functionality
V_{CC}	B	if input defined LOW, undefined operating condition, no damage, increases leakage (only for I/O types), affects functionality
V_{CC}	B	if input defined HIGH, device is powered via input circuit, may affect functionality

Table 5. FMEA matrix for pin short-circuits between neighbor pins

Pin	Class	Remarks
Input to input	C	if inputs have same voltage levels: no damage, no leakage
	B	if inputs have different voltage levels: leakage increases, will affect functionality
Input to output	A	if input and output have different voltage levels, can cause high current and can damage device, will affect functionality
	C	if input and output have same voltage levels, no damage, no leakage
Input to GND	-	see Table 3
Input to V_{CC}	-	see Table 2
Output to output	C	if outputs have same voltage levels, no damage, no leakage
	A	if outputs have different voltage levels, can cause high current and can damage device, will affect functionality
Output to input	-	same effect as ‘input to output’ condition
Output to GND	-	see Table 3
Output to V_{CC}	-	see Table 2
GND to V_{CC}	-	not applicable, these pins are not neighbors

3. Abbreviations

Table 6. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
FMEA	Failure Modes and Effects Analysis
LSTTL	Low power Schottky TTL
TTL	Transistor-Transistor Logic

4. Revision history

Table 7. Revision history

Rev	Date	Description
v.2	20190109	AN11044, updated to latest Nexperia documentation standard
v.1	20110316	AN11044 initial version

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For sales office addresses, please send an email to: salesaddresses@nexperia.com
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