

ON Semiconductor

Is Now

The logo for onsemi, featuring the word "onsemi" in a dark teal, lowercase, sans-serif font. The letter "i" is stylized with a white dot and a teal vertical bar. A small orange triangle is positioned above the top right of the "i". A trademark symbol (TM) is located to the right of the logo.

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ON Semiconductor®

FAN7081-GF085 High Side Gate Driver

Features

- Qualified to AEC Q100
- Floating channel designed for bootstrap operation up fully operational to + 600V
- Tolerance to negative transient voltage on VS pin
- dV/dt immune.
- Gate drive supply range from 10V to 20V
- Under-voltage lockout
- CMOS Schmit-triggered inputs with pull-up
- High side output out of phase with input (Inverted input)

Typical Applications

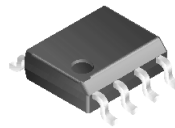
- Diesel and gasoline Injectors/Valves
- MOSFET-and IGBT high side driver applications



Description

The FAN7081-GF085 is a high-side gate drive IC designed for high voltage and high speed driving of MOSFET or IGBT, which operates up to 600V. ON Semiconductor's high-voltage process and com-mon-mode noise cancellation technique provide stable operation in the high side driver under high-dV/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to $V_S = -5V$ (typical) at $V_{BS} = 15V$. Logic input is compatible with standard CMOS outputs. The UVLO cir-cuits prevent from malfunction when VCC and VBS are lower than the specified threshold voltage. It is available with space saving SOIC-8 Package. Minimum source and sink current capability of output driver is 250mA and 500mA respectively, which is suitable for magnetic- and piezo type injectors and gen-eral MOSFET/IGBT based high side driver applications.

SOIC-8

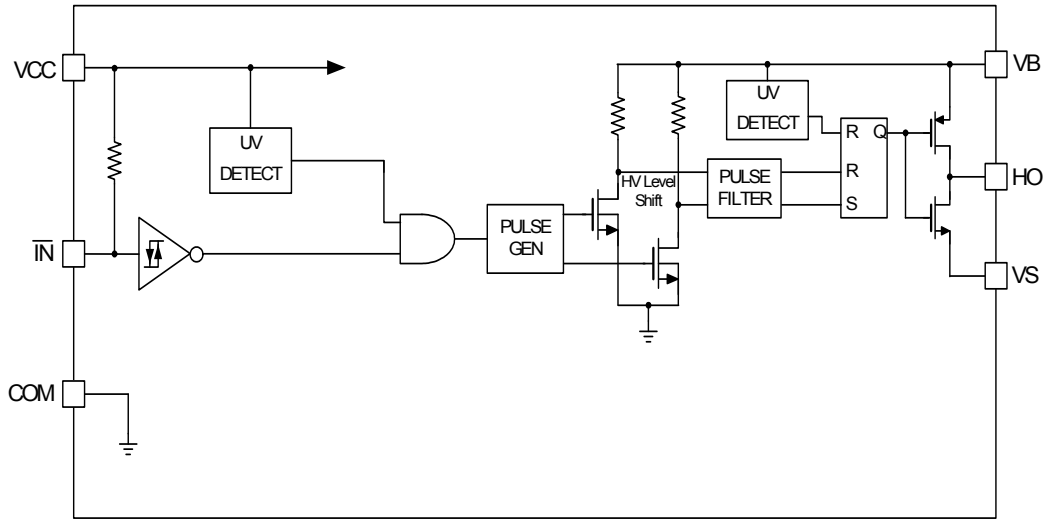


Ordering Information

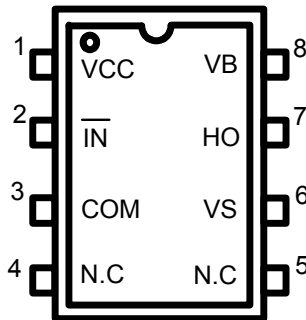
| Device | Package | Operating Temp. |
|-----------------|---------|-----------------|
| FAN7081M-GF085 | SOIC-8 | -40 °C ~ 125 °C |
| FAN7081MX-GF085 | SOIC-8 | -40 °C ~ 125 °C |

X : Tape & Reel type

Block Diagrams



Pin Assignments



Pin Definitions

| Pin Number | Pin Name | I/O | Pin Function Description |
|------------|------------------------|-----|---|
| 1 | VCC | P | Driver supply voltage |
| 2 | $\overline{\text{IN}}$ | I | Logic input for high side gate drive output, out of phase with HO |
| 3 | COM | P | Ground |
| 4 | NC | - | NC |
| 5 | NC | - | NC |
| 6 | VS | P | High side floating offset for MOSFET Source connection |
| 7 | HO | A | High side drive output for MOSFET Gate connection |
| 8 | VB | P | Driver output stage supply |

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

| Parameter | Symbol | Min. | Max. | Unit |
|---|------------------|--------|---------|------|
| High side floating supply offset voltage | VS | VB-25 | VB+0.3 | V |
| High side floating supply voltage | VB | -0.3 | 625 | V |
| High side floating output voltage | VHO | VS-0.3 | VB+0.3 | V |
| Supply voltage | VCC | -0.3 | 25 | V |
| Input voltage for $\overline{\text{IN}}$ | VIN | -0.3 | VCC+0.3 | V |
| Power Dissipation ¹⁾ | Pd | | 0.625 | W |
| Thermal resistance, junction to ambient ¹⁾ | Rthja | | 200 | °C/W |
| Electrostatic discharge voltage (Human Body Model) | V _{ESD} | 1K | | V |
| Charge device model | V _{CDM} | 500 | | V |
| Junction Temperature | T _J | | 150 | °C |
| Storage Temperature | T _S | -55 | 150 | °C |

Note: 1) The thermal resistance and power dissipation rating are measured bellow conditions;

JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions - Natural codition(StillAir)

JESD51-3: Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Package

Recommended Operating Conditions

For proper operations the device should be used within the recommended conditions. $-40^{\circ}\text{C} \leq \text{Ta} \leq 125^{\circ}\text{C}$

| Parameter | Symbol | Min. | Max. | Unit |
|---|--------------------|--|---------|------|
| High side floating supply voltage(DC) Transient:-10V@ 0.2 us | VB | VS + 10 | VS + 20 | V |
| High side floating supply offset voltage(DC) | VS | -4 (@VBS >= 10V) -5 (@VBS >= 11.5V) | 600 | V |
| High side floating supply offset voltage(Transient) | VS | -25 (~200ns) -20(200ns ~240ns) -7(240ns~400ns) | 600 | V |
| High side floating output voltage | VHO | VS | VB | V |
| Allowable offset voltage Slew Rate ¹⁾ | dv/dt | - | 50 | V/ns |
| Supply voltage | VCC | 10 | 20 | V |
| Input voltage for $\overline{\text{IN}}$ | VIN | 0 | Vcc | V |
| Switching Frequency ²⁾ | Fs | | 200 | KHz |
| Minimum Pulse Width ⁽³⁾ | T _{pulse} | 85 | - | ns |
| Ambient Temperature | Ta | -40 | 125 | °C |

Note: 1) Guaranteed by design.

2) Duty = 0.5

3) Guaranteed by design. Refer to Figure4a,4b and 4c on Page 8.

Statics Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, $V_{BS} = 15\text{V}$, $V_S = 0\text{V}$, $R_L = 50\Omega$, $C_L = 2.5\text{nF}$.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|------------------|--|--------------|------|-------------|---------------|
| Vcc and VBS supply Characteristics | | | | | | |
| VCC and VBS supply under voltage positive going threshold | VCCUV+ VBSUV+ | | - | 8.7 | 9.8 | V |
| VCC and VBS supply under voltage negative going threshold | VCCUV- VBSUV- | | 7.4 | 8.2 | - | V |
| VCC and VBS supply under voltage hysteresis | VCCUVH VBSUVH | - | 0.2 | 0.5 | - | V |
| Under voltage lockout response time | tduvcc tduvbs | VCC: 10V-->7.3V or 7.3V-->10V VBS: 10V-->7.3V or 7.3V-->10V | 0.5 0.5 | | 20 20 | us us |
| Offset supply leakage current | ILK | $V_B = V_S = 600\text{V}$ | - | - | 50 | μA |
| Quiescent VBS supply current | IQBS | $V_{IN} = 0$ | - | 23 | 250 | μA |
| Quiescent Vcc supply current | IQCC1 | $V_{IN} = 0\text{V}$ | - | 42 | 120 | μA |
| Quiescent Vcc supply current | IQCC2 | $V_{IN} = 15\text{V}$ | - | 25 | 100 | μA |
| Input Characteristics | | | | | | |
| High logic level input voltage | V_{IH} | | $0.63V_{CC}$ | - | - | V |
| Low logic level input voltage | V_{IL} | | - | - | $0.4V_{CC}$ | V |
| Low logic level input bias current for IN | I_{IN+} | $V_{IN} = 0$ | - | 15 | 50 | μA |
| High logic level input bias current for IN | I_{IN-} | $V_{IN} = 15\text{V}$ | - | 0 | 1 | μA |
| Output characteristics | | | | | | |
| High level output voltage, $V_{BIAS-VO}$ | V_{OH} | $I_O = 0$ | - | - | 0.1 | V |
| Low level output voltage, V_O | V_{OL} | $I_O = 0$ | - | - | 0.1 | V |
| Peak output source current | I_{O1+} | | 250 | - | - | mA |
| Peak output sink current | I_{O1-} | | 500 | - | - | mA |
| Equivalent output resistance | ROP | | | 40 | 60 | Ω |
| | RON | | | 20 | 30 | Ω |

Note: The input parameter are referenced to COM. The VO and IO parameters are referenced to COM.

Dynamic Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, $V_{BS} = 15\text{V}$, $V_S = 0\text{V}$, $R_L = 50\Omega$, $C_L = 2.5\text{nF}$.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--|------------------|---|------|------|------|------|
| Input-to-output turn-on propagation delay | t _{plh} | 50% input level to 10% output level, V _S = 0V | | 130 | 300 | ns |
| Input-to-output turn-off propagation delay | t _{phl} | 50% input level to 90% output level V _S = 0V | - | 140 | 300 | ns |
| Output rising time | t _{r1} | 10% to 90%, T _j =25°C, V _{BS} =15V | - | 15 | 400 | ns |
| | t _{r2} | 10% to 90% | | - | 500 | ns |
| Output falling time | t _{f1} | 90% to 10%, T _j =25°C, V _{BS} =15V | - | 10 | 150 | ns |
| | t _{f2} | 90% to 10% | | - | 500 | ns |

Application Information

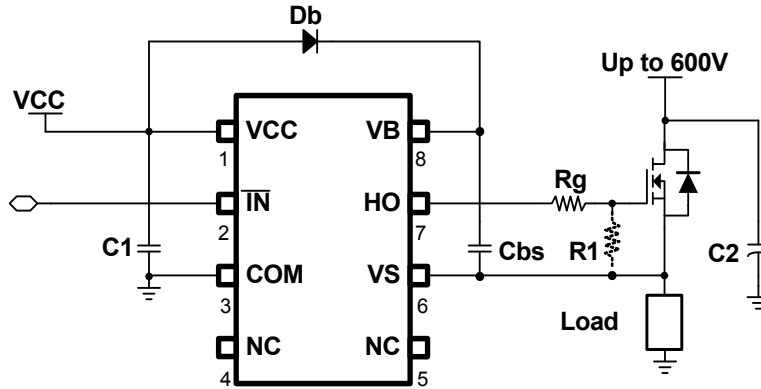
1. Relationship in input/output and supplies

| Table.1 Truth table for Vcc, VBS, VIN, and VHO | | | |
|--|------------|------|-----|
| VCC | VBS | IN | HO |
| < VCCUVLO- | X | X | OFF |
| X | < VBSUVLO- | X | OFF |
| X | X | HIGH | OFF |
| > VCCUVLO+ | > VBSUVLO+ | LOW | ON |

Notes:

X means independent from signal

Typical Application Circuit



Typical Waveforms

1. Input/Output Timing

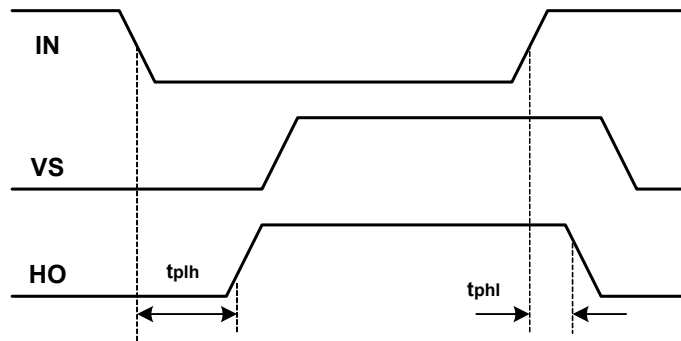


Figure 1. Input /output Timing Diagram

2. Output(HO) Switching Timing

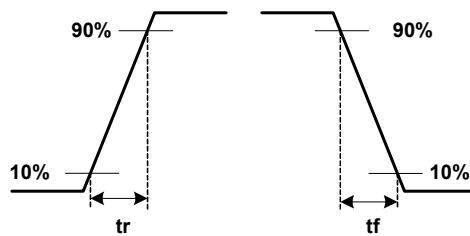


Figure 2. Switching Time Waveform Definitions

3.VB Drop Voltage Diagram

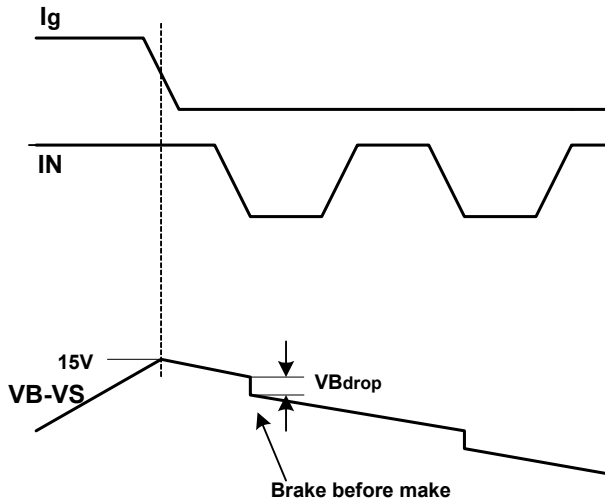


Figure 3a. VB Drop Voltage Diagram

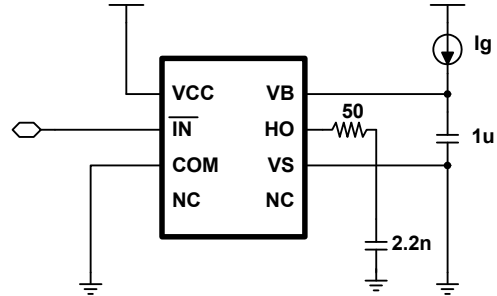


Figure3b. VB Drop Voltage Test Circuit

4.Recommendation Min. Short Pulse Width

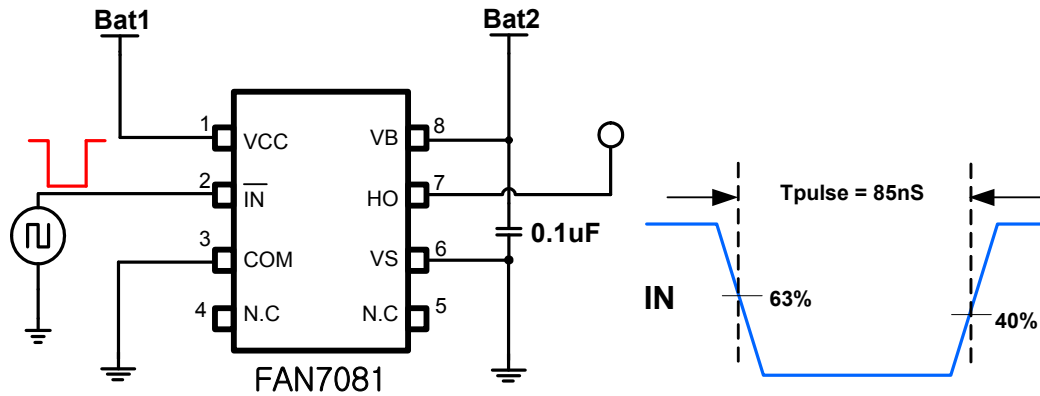


Figure 4a.Short Pulse Width Test Circuit and Pulse Width Waveform

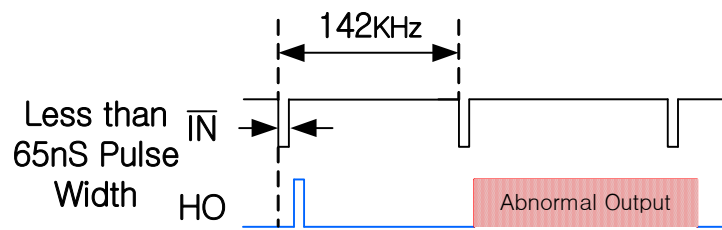


Figure 4b. Abnormal Output Waveform with short pulse width

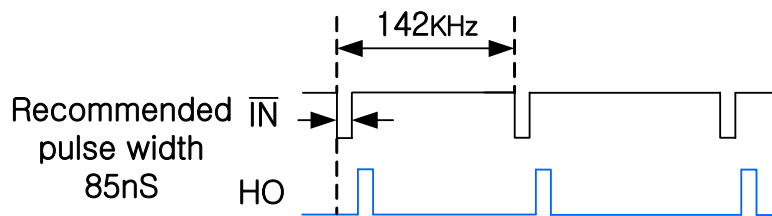


Figure 4c. Recommendation of pulse width Output Waveform

Performance Graphs

This performance graphs based on ambient temperature -40°C ~125°C

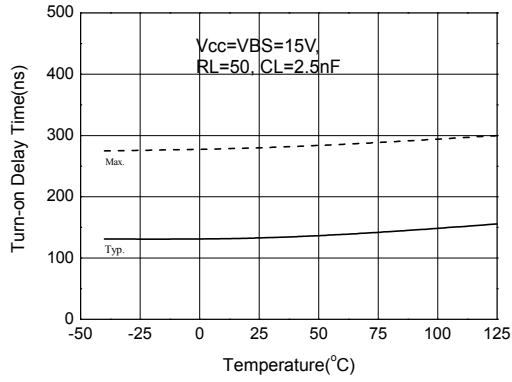


Figure 5a. Turn-On Delay Time vs Temperature

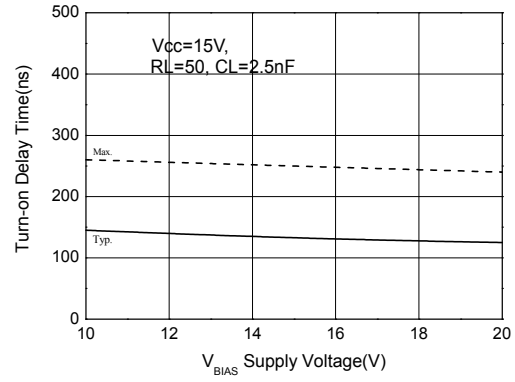


Figure 5b. Turn-On Delay Time vs VBS Supply Voltage

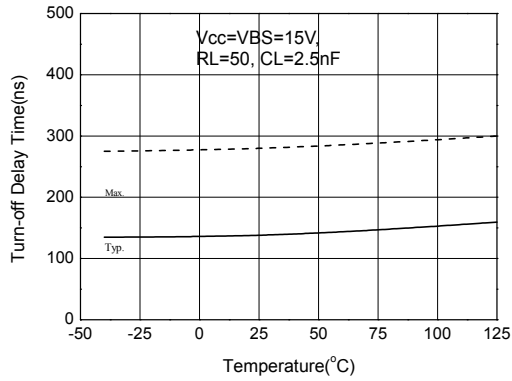


Figure 6a. Turn-Off Delay Time vs Temperature

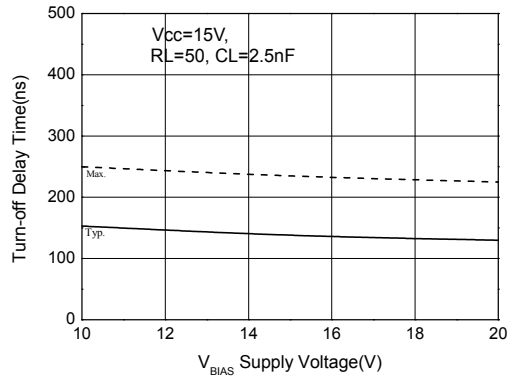


Figure 6b. Turn-Off Delay Time vs VBS Supply Voltage

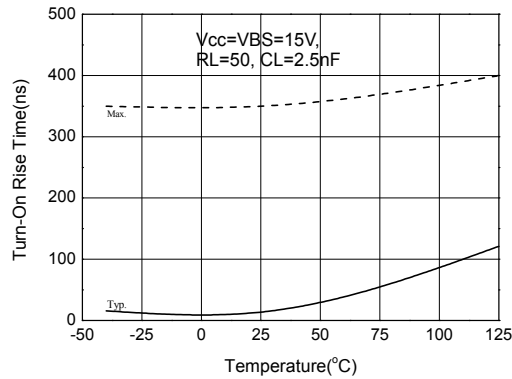


Figure 7a. Turn-On Rising Time vs Temperature

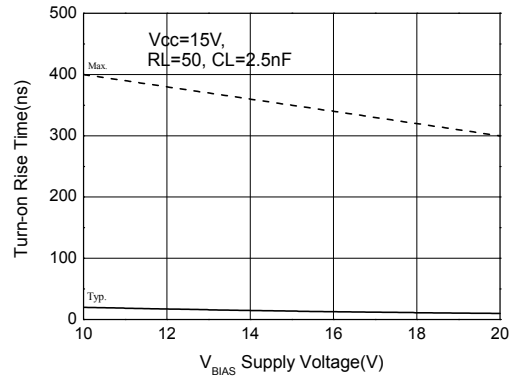


Figure 7b. Turn-ON Rising Time vs VBS Supply Voltage

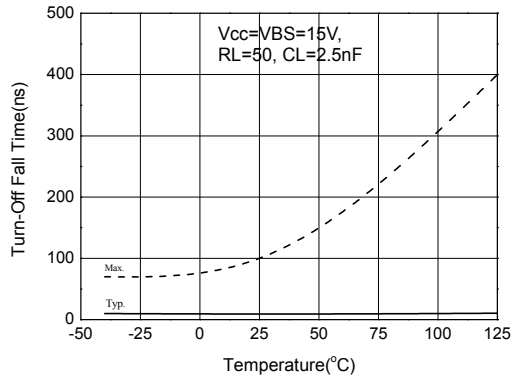


Figure 8a. Turn-Off Falling Time vs Temperature

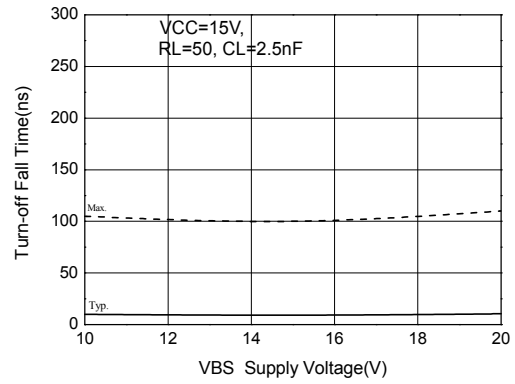


Figure 8b. Turn-Off Falling Time vs VBS Supply Voltage

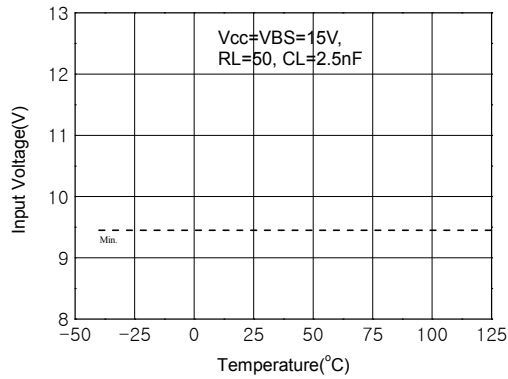


Figure 9a. Logic "1" IN Voltage vs Temperature

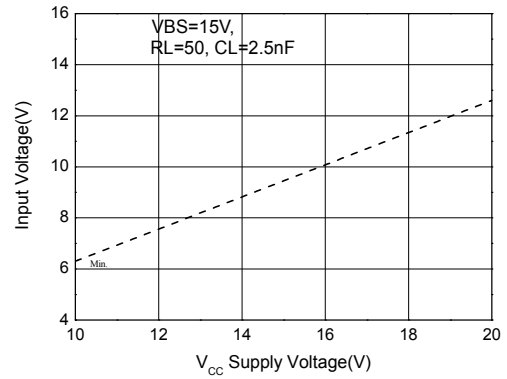


Figure 9b. Logic "1" IN Voltage vs VCC Supply Voltage

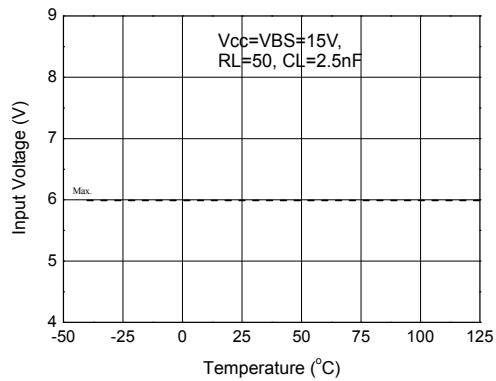


Figure 10a. Logic "0" IN Voltage vs Temperature

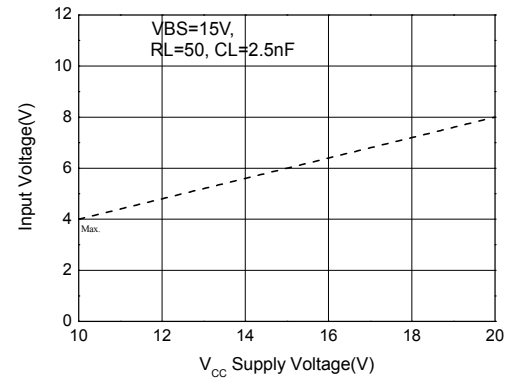


Figure 10b. Logic "0" IN Voltage vs VCC Supply Voltage

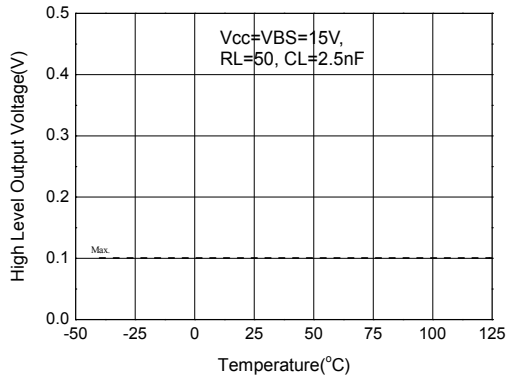


Figure 11a. High Level Output vs Temperature

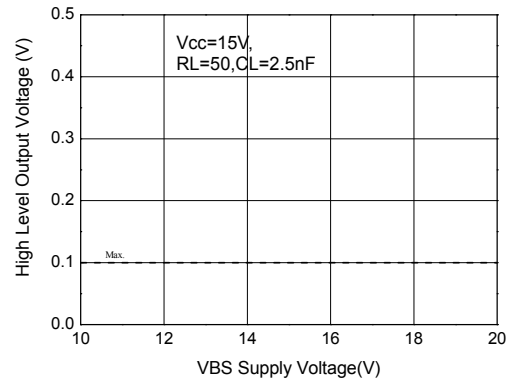


Figure 11b. High Level Output vs VBS Supply Voltage

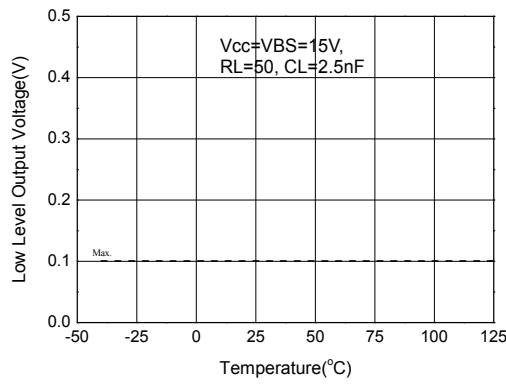


Figure 12a. Low Level Output vs Temperature

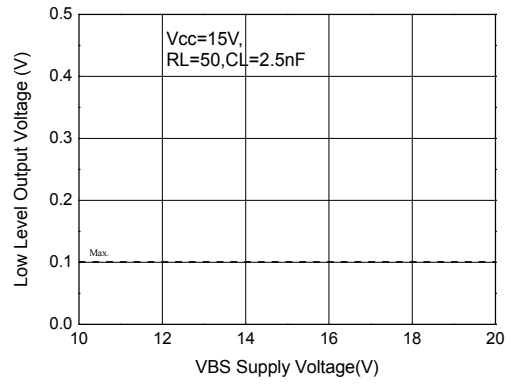


Figure 12b. Low Level Output vs VBS Supply Voltage

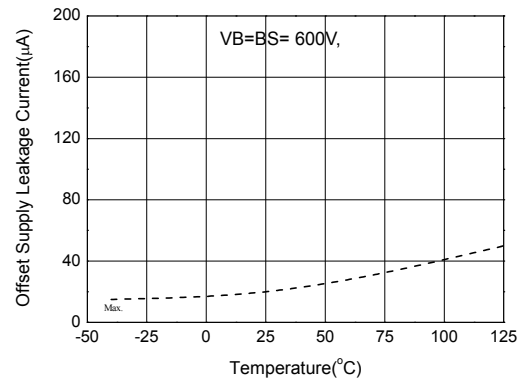


Figure 13a. Offset Supply Leakage Current vs Temperature

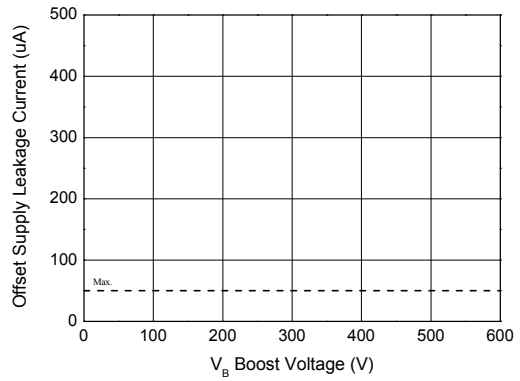


Figure 13b. Offset Supply Leakage Current vs VB Boost Voltage

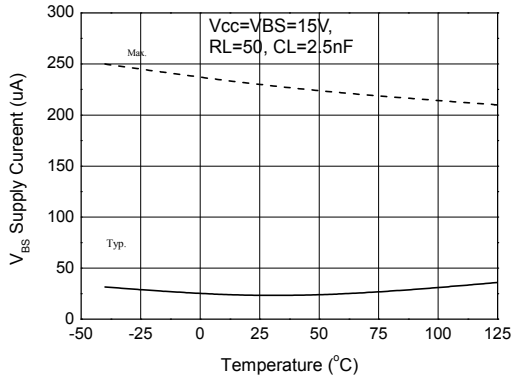


Figure 14a. VBS Supply Current vs Temperature

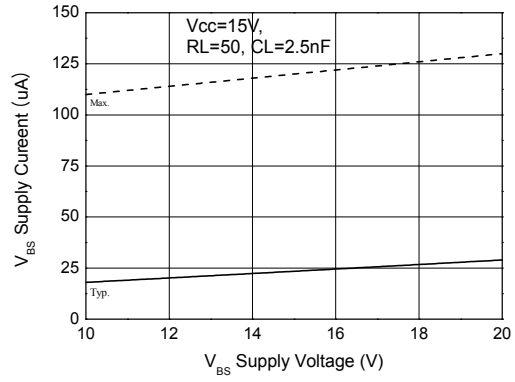


Figure 14b. VBS Supply Current vs VBS Supply Voltage

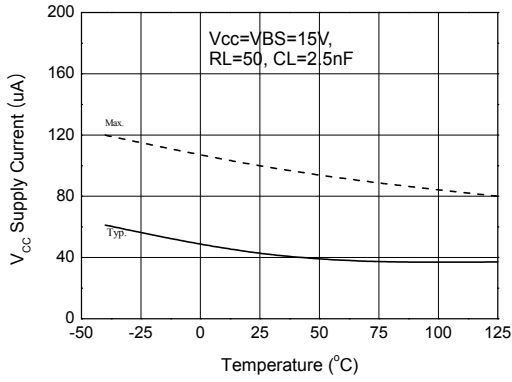


Figure 15a. VCC Supply Current vs Temperature

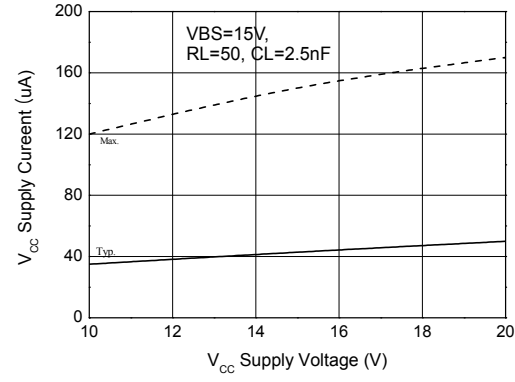


Figure 15b. VCC Supply Current vs VCC Supply Voltage

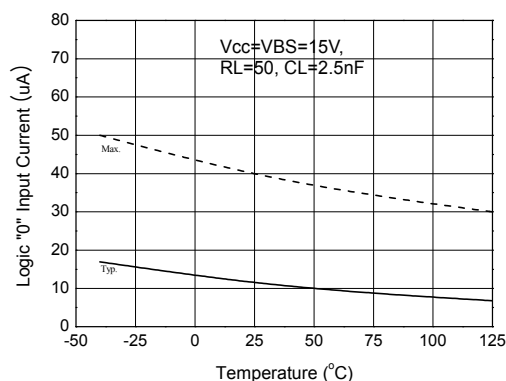


Figure 16a. Logic "0" IN Current vs Temperature

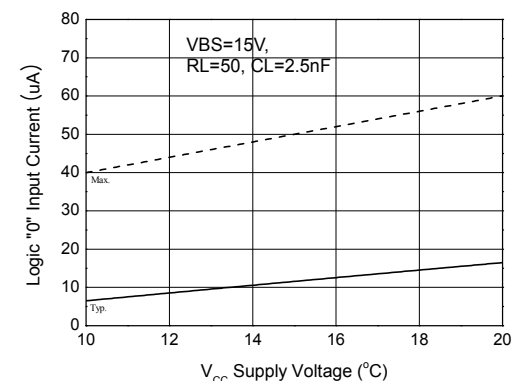


Figure 16b. Logic "0" IN Current vs VCC Supply Voltage

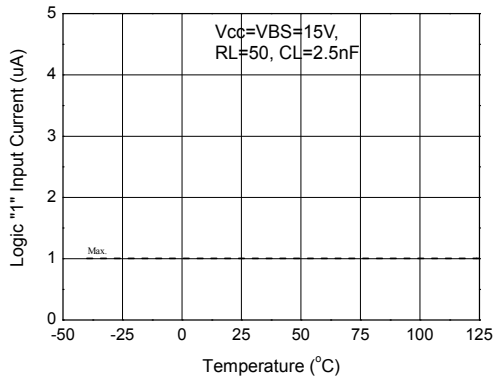


Figure 17a. Logic "1" IN Current vs Temperature

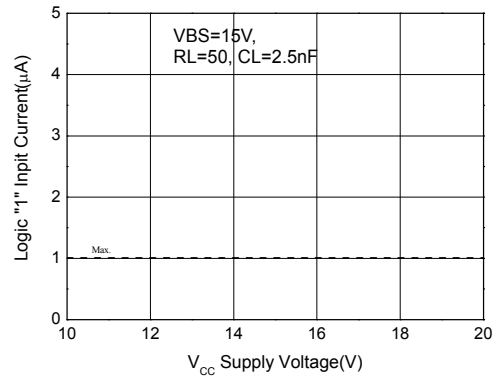


Figure 17b. Logic "1" IN Current vs VCC Supply Voltage

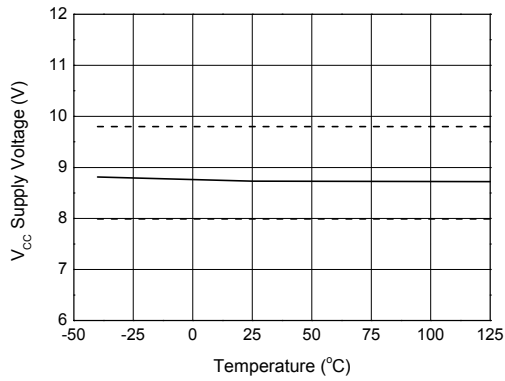


Figure 18a. VCC Under voltage Threshold(+) vs Temperature

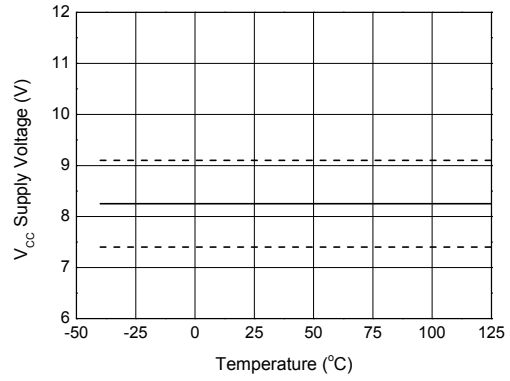


Figure 18b. VCC Under voltage Threshold(-) vs Temperature

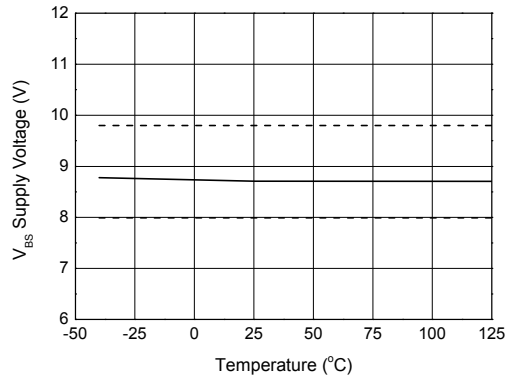


Figure 19a. VBS Under voltage Threshold(+) vs Temperature

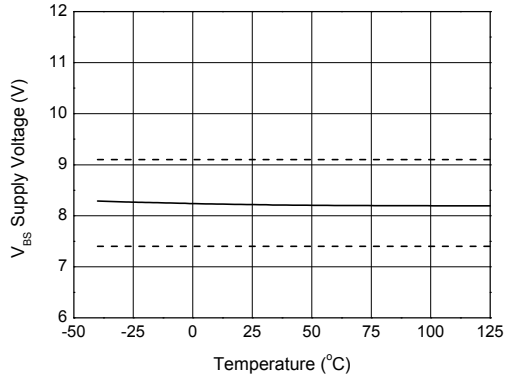


Figure 19b. VBS Under voltage Threshold(-) vs Temperature

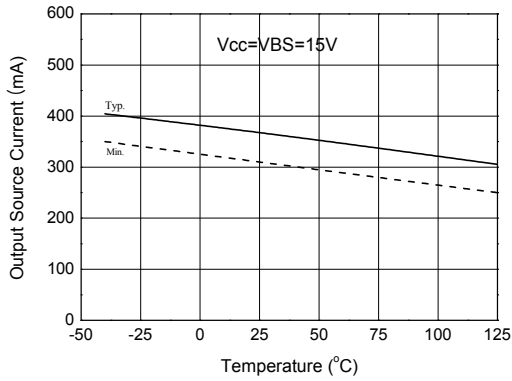


Figure 20a. Output Source Current vs Temperature

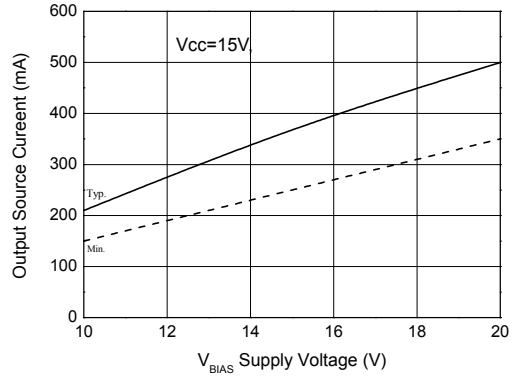


Figure 20b. Output Source Current vs VBS Supply Voltage

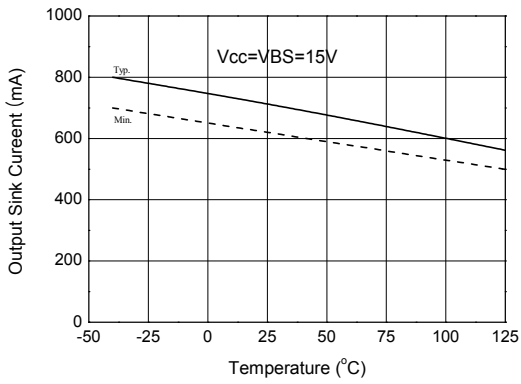


Figure 21a. Output Sink Current vs Temperature

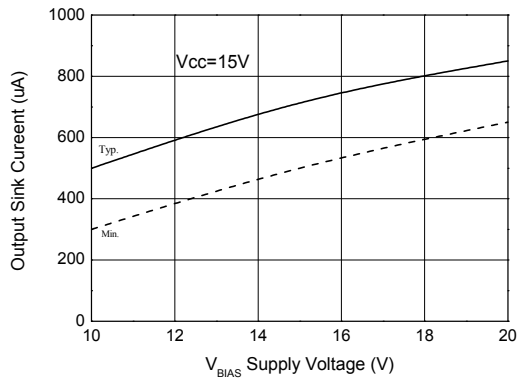


Figure 21b. Output Sink Current vs VBS Supply Voltage

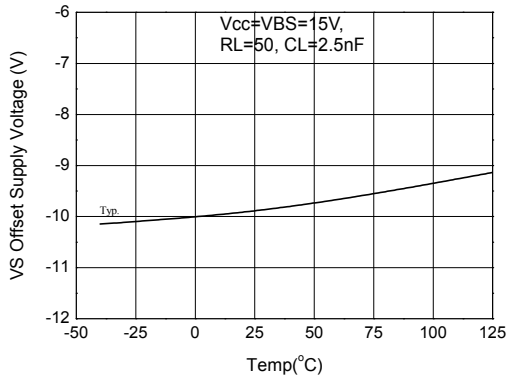


Figure 22a. Maximum VS Negative Voltage vs Temperature

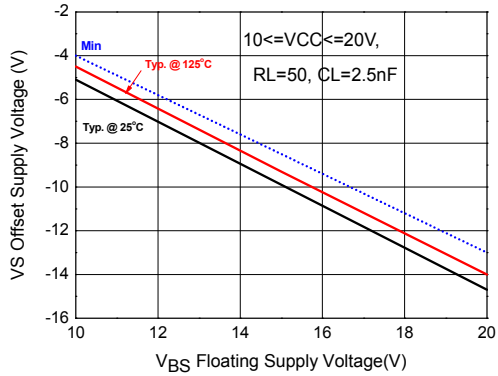


Figure 22b. Maximum VS Negative Voltage vs VBS Supply Voltage

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