

# 74ALVC164245

16-bit dual supply translating transceiver; 3-state

Rev. 11 — 27 July 2021

Product data sheet

## 1. General description

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The 74ALVC164245 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC164245 is a 16-bit (dual octal) dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The direction control inputs (1DIR and 2DIR) determine the direction of the data flow. nDIR (active HIGH) enables data from nAn ports to nBn ports. nDIR (active LOW) enables data from nBn ports to nAn ports. The output enable inputs ( $1\overline{OE}$  and  $2\overline{OE}$ ), when HIGH, disable both nAn and nBn ports by placing them in a high-impedance OFF-state. Pins nAn,  $n\overline{OE}$  and nDIR are referenced to  $V_{CC(A)}$  and pins nBn are referenced to  $V_{CC(B)}$ .

In suspend mode, when one of the supply voltages is zero, there will be no current flow from the non-zero supply towards the zero supply. The nAn-outputs must be set 3-state and the voltage on the A-bus must be smaller than  $V_{diode}$  (typical 0.7 V).  $V_{CC(B)} \geq V_{CC(A)}$  (except in suspend mode).

## 2. Features and benefits

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- Wide supply voltage range:
  - 3 V port ( $V_{CC(A)}$ ): 1.5 V to 3.6 V
  - 5 V port ( $V_{CC(B)}$ ): 1.5 V to 5.5 V
- CMOS low power consumption
- Overvoltage tolerant inputs to 5.5 V
- Direct interface with TTL levels
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Control inputs voltage range from 2.7 V to 5.5 V
- High-impedance outputs when  $V_{CC(A)}$  or  $V_{CC(B)} = 0$  V
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

| Type number     | Package           |         |  | Version  |
|-----------------|-------------------|---------|--|----------|
|                 | Temperature range | Name    | Description  |          |
| 74ALVC164245DGG | -40 °C to +125 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |

### 4. Functional diagram

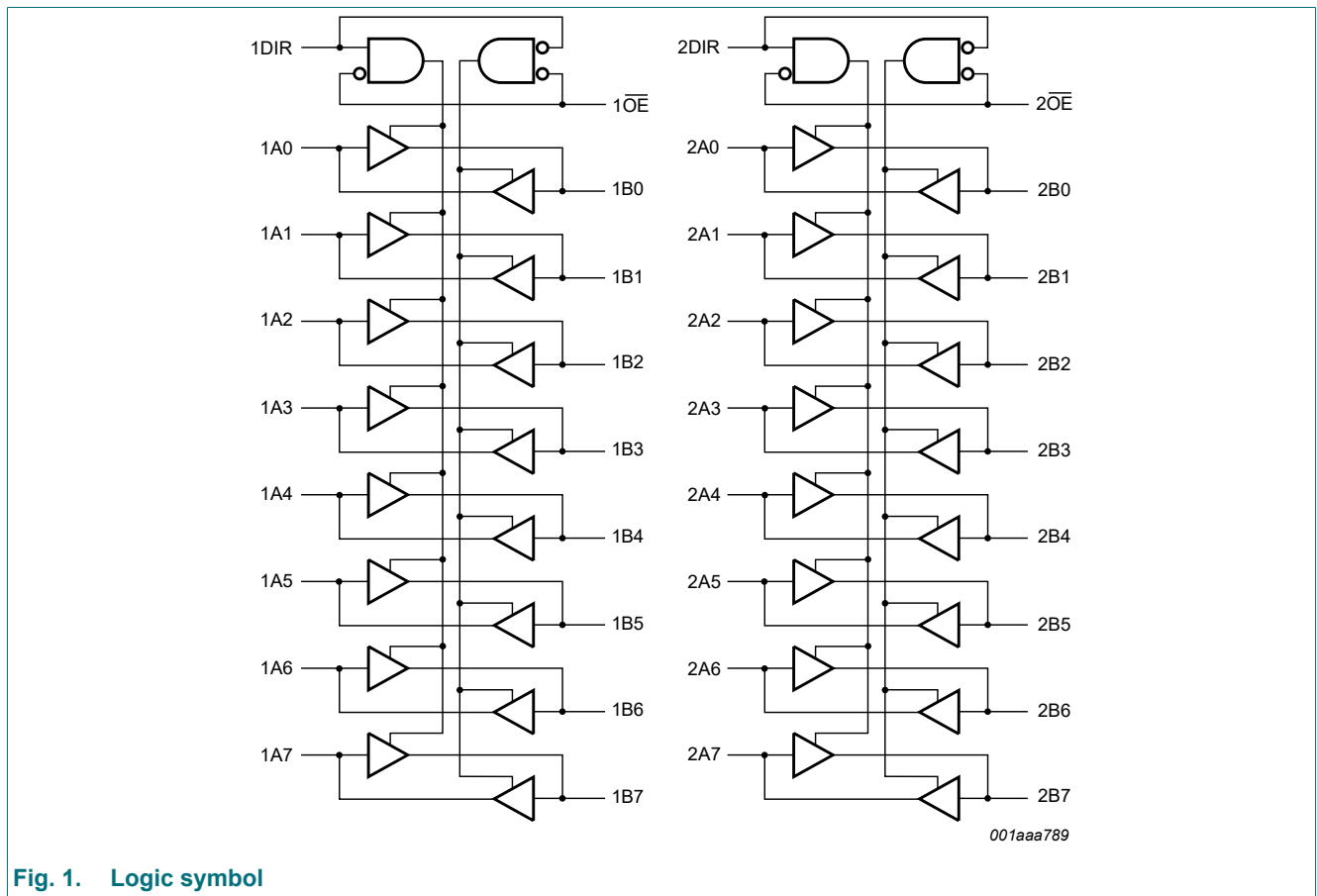


Fig. 1. Logic symbol

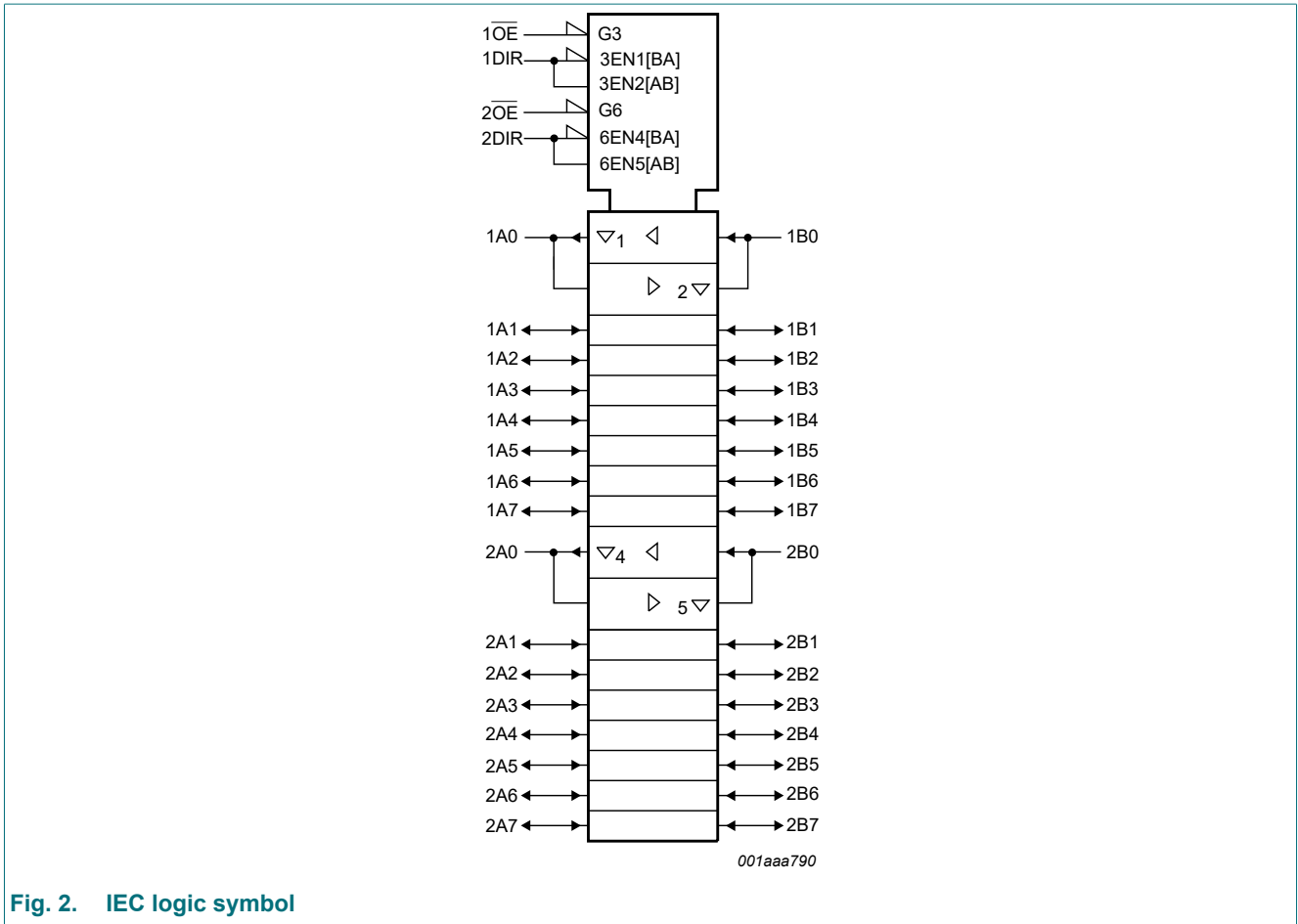


Fig. 2. IEC logic symbol

## 5. Pinning information

### 5.1. Pinning

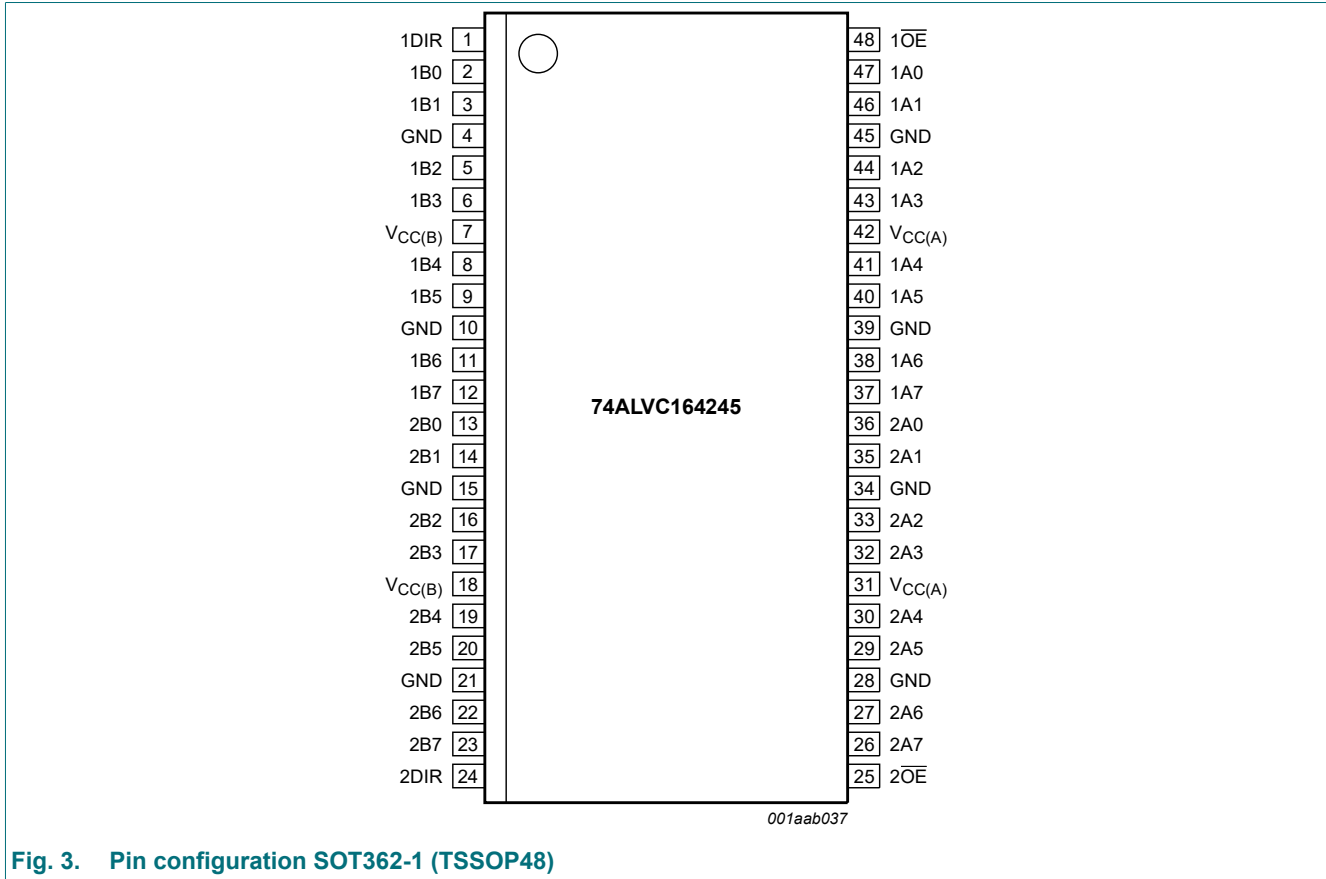


Fig. 3. Pin configuration SOT362-1 (TSSOP48)

### 5.2. Pin description

Table 2. Pin description

| Symbol                                 | Pin                            | Description                      |
|--|--------------------------------|----------------------------------|
| 1DIR, 2DIR                             | 1, 24                          | direction control input          |
| 1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7 | 2, 3, 5, 6, 8, 9, 11, 12       | data input/output                |
| 2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7 | 13, 14, 16, 17, 19, 20, 22, 23 | data input/output                |
| GND                                    | 4, 10, 15, 21, 28, 34, 39, 45  | ground (0 V)                     |
| V <sub>CC(B)</sub>                     | 7, 18                          | supply voltage B (5 V bus)       |
| 1OE, 2OE                               | 48, 25                         | output enable input (active LOW) |
| 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7 | 47, 46, 44, 43, 41, 40, 38, 37 | data input/output                |
| 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7 | 36, 35, 33, 32, 30, 29, 27, 26 | data input/output                |
| V <sub>CC(A)</sub>                     | 31, 42                         | supply voltage A (3 V bus)       |

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

| Inputs |      | Outputs   |           |
|--------|------|-----------|-----------|
| nOE    | nDIR | nAn       | nBn       |
| L      | L    | nAn = nBn | inputs    |
| L      | H    | inputs    | nBn = nAn |
| H      | X    | Z         | Z         |

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol               | Parameter                     | Conditions                        | Min  | Max            | Unit |
|----------------------|-------------------------------|-----------------------------------|------|----------------|------|
| $V_{CC(B)}$          | supply voltage B              | $V_{CC(B)} \geq V_{CC(A)}$        | -0.5 | +6.0           | V    |
| $V_{CC(A)}$          | supply voltage A              | $V_{CC(B)} \geq V_{CC(A)}$        | -0.5 | +4.6           | V    |
| $I_{IK}$             | input clamping current        | $V_I < 0$ V                       | -50  | -              | mA   |
| $V_I$                | input voltage                 | [1]                               | -0.5 | +6.0           | V    |
| $V_{I/O}$            | input/output voltage          |                                   | -0.5 | $V_{CC} + 0.5$ | V    |
| $I_{OK}$             | output clamping current       | $V_O > V_{CC}$ or $V_O < 0$ V     | -    | $\pm 50$       | mA   |
| $V_O$                | output voltage                | output HIGH or LOW [1]            | -0.5 | $V_{CC} + 0.5$ | V    |
|                      |                               | output 3-state [1]                | -0.5 | +6.0           | V    |
| $I_{O(sink/source)}$ | output sink or source current | $V_O = 0$ V to $V_{CC}$           | -    | $\pm 50$       | mA   |
| $I_{CC}$             | supply current                |                                   | -    | 100            | mA   |
| $I_{GND}$            | ground current                |                                   | -100 | -              | mA   |
| $T_{stg}$            | storage temperature           |                                   | -65  | +150           | °C   |
| $T_j$                | junction temperature          | [2]                               | -    | +150           | °C   |
| $P_{tot}$            | total power dissipation       | $T_{amb} = -40$ °C to +125 °C [3] | -    | 500            | mW   |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SOT362-1 (TSSOP48) packages:  $P_{tot}$  derates linearly with 12.2 mW/K above 109 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol              | Parameter                           | Conditions                                    | Min | Typ | Max         | Unit |
|---------------------|-------------------------------------|---|-----|-----|-------------|------|
| $V_{CC(B)}$         | supply voltage B                    | $V_{CC(B)} \geq V_{CC(A)}$                    |     |     |             |      |
|                     |                                     | maximum speed performance                     | 2.7 | -   | 5.5         | V    |
|                     |                                     | low-voltage applications                      | 1.5 | -   | 5.5         | V    |
| $V_{CC(A)}$         | supply voltage A                    | $V_{CC(B)} \geq V_{CC(A)}$                    |     |     |             |      |
|                     |                                     | maximum speed performance                     | 2.7 | -   | 3.6         | V    |
|                     |                                     | low-voltage applications                      | 1.5 | -   | 3.6         | V    |
| $V_I$               | input voltage                       | control inputs: $\overline{nOE}$ and nDIR     | 0   | -   | 5.5         | V    |
| $V_{I/O}$           | input/output voltage                | nAn port                                      | 0   | -   | $V_{CC(A)}$ | V    |
|                     |                                     | nBn port                                      | 0   | -   | $V_{CC(B)}$ | V    |
| $V_O$               | output voltage                      | nAn port                                      | 0   | -   | $V_{CC(A)}$ | V    |
|                     |                                     | nBn port                                      | 0   | -   | $V_{CC(B)}$ | V    |
| $T_{amb}$           | ambient temperature                 |   | -40 | -   | +125        | °C   |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC(A)} = 2.7 \text{ V to } 3.0 \text{ V}$ | 0   | -   | 20          | ns/V |
|                     |                                     | $V_{CC(A)} = 3.0 \text{ V to } 3.6 \text{ V}$ | 0   | -   | 10          | ns/V |
|                     |                                     | $V_{CC(B)} = 3.0 \text{ V to } 4.5 \text{ V}$ | 0   | -   | 20          | ns/V |
|                     |                                     | $V_{CC(B)} = 4.5 \text{ V to } 5.5 \text{ V}$ | 0   | -   | 10          | ns/V |

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol   | Parameter                | Conditions  | -40 °C to +85 °C |        |     | -40 °C to +125 °C |     | Unit |
|----------|--------------------------|---|------------------|--------|-----|-------------------|-----|------|
|          |                          |   | Min              | Typ[1] | Max | Min               | Max |      |
| $V_{IH}$ | HIGH-level input voltage | nBn port  |                  |        |     |                   |     |      |
|          |                          | $V_{CC(B)} = 3.0 \text{ V to } 5.5 \text{ V}$ [2] | 2.0              | -      | -   | 2.0               | -   | V    |
|          |                          | nAn port, $\overline{nOE}$ and nDIR               |                  |        |     |                   |     |      |
|          |                          | $V_{CC(A)} = 3.0 \text{ V to } 3.6 \text{ V}$     | 2.0              | -      | -   | 2.0               | -   | V    |
|          |                          | $V_{CC(A)} = 2.3 \text{ V to } 2.7 \text{ V}$ [2] | 1.7              | -      | -   | 1.7               | -   | V    |
| $V_{IL}$ | LOW-level input voltage  | nBn port  |                  |        |     |                   |     |      |
|          |                          | $V_{CC(B)} = 4.5 \text{ V to } 5.5 \text{ V}$ [2] | -                | -      | 0.8 | -                 | 0.8 | V    |
|          |                          | $V_{CC(B)} = 3.0 \text{ V to } 3.6 \text{ V}$ [2] | -                | -      | 0.7 | -                 | 0.7 | V    |
|          |                          | nAn port, $\overline{nOE}$ and nDIR               |                  |        |     |                   |     |      |
|          |                          | $V_{CC(A)} = 3.0 \text{ V to } 3.6 \text{ V}$     | -                | -      | 0.8 | -                 | 0.8 | V    |
|          |                          | $V_{CC(A)} = 2.3 \text{ V to } 2.7 \text{ V}$ [2] | -                | -      | 0.7 | -                 | 0.7 | V    |

## 16-bit dual supply translating transceiver; 3-state

| Symbol   | Parameter                 | Conditions  | -40 °C to +85 °C         |                          |      | -40 °C to +125 °C        |      | Unit |
|--|---------------------------|---|--------------------------|--------------------------|------|--------------------------|------|------|
|  |                           |   | Min                      | Typ[1]                   | Max  | Min                      | Max  |      |
| V <sub>OH</sub>                                      | HIGH-level output voltage | nBn port; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                     |                          |                          |      |                          |      |      |
|  |                           | I <sub>O</sub> = -24 mA; V <sub>CC(B)</sub> = 4.5 V   | V <sub>CC(B)</sub> - 0.8 | -                        | -    | V <sub>CC(B)</sub> - 1.2 | -    | V    |
|  |                           | I <sub>O</sub> = -12 mA; V <sub>CC(B)</sub> = 4.5 V   | V <sub>CC(B)</sub> - 0.5 | -                        | -    | V <sub>CC(B)</sub> - 0.8 | -    | V    |
|  |                           | I <sub>O</sub> = -18 mA; V <sub>CC(B)</sub> = 3.0 V   | V <sub>CC(B)</sub> - 0.8 | -                        | -    | V <sub>CC(B)</sub> - 1.0 | -    | V    |
|  |                           | I <sub>O</sub> = -100 μA; V <sub>CC(B)</sub> = 3.0 V  | V <sub>CC(B)</sub> - 0.2 | V <sub>CC(B)</sub>       | -    | V <sub>CC(B)</sub> - 0.3 | -    | V    |
|  |                           | nAn port; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                     |                          |                          |      |                          |      |      |
|  |                           | I <sub>O</sub> = -24 mA; V <sub>CC(A)</sub> = 3.0 V   | V <sub>CC(A)</sub> - 0.7 | -                        | -    | V <sub>CC(A)</sub> - 1.0 | -    | V    |
|  |                           | I <sub>O</sub> = -100 μA; V <sub>CC(A)</sub> = 3.0 V  | V <sub>CC(A)</sub> - 0.2 | -                        | -    | V <sub>CC(A)</sub> - 0.3 | -    | V    |
|  |                           | I <sub>O</sub> = -12 mA; V <sub>CC(A)</sub> = 2.7 V   | V <sub>CC(A)</sub> - 0.5 | -                        | -    | V <sub>CC(A)</sub> - 0.8 | -    | V    |
|  |                           | I <sub>O</sub> = -8 mA; V <sub>CC(A)</sub> = 2.3 V  | V <sub>CC(A)</sub> - 0.6 | -                        | -    | V <sub>CC(A)</sub> - 0.6 | -    | V    |
| I <sub>O</sub> = -100 μA; V <sub>CC(A)</sub> = 2.3 V | V <sub>CC(A)</sub> - 0.2  | V <sub>CC(A)</sub>  | -                        | V <sub>CC(A)</sub> - 0.3 | -    | V                        |      |      |
| V <sub>OL</sub>                                      | LOW-level output voltage  | nBn port; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                     |                          |                          |      |                          |      |      |
|  |                           | I <sub>O</sub> = 24 mA; V <sub>CC(B)</sub> = 4.5 V  | -                        | -                        | 0.55 | -                        | 0.80 | V    |
|  |                           | I <sub>O</sub> = 12 mA; V <sub>CC(B)</sub> = 4.5 V  | -                        | -                        | 0.40 | -                        | 0.60 | V    |
|  |                           | I <sub>O</sub> = 100 μA; V <sub>CC(B)</sub> = 4.5 V   | -                        | -                        | 0.20 | -                        | 0.30 | V    |
|  |                           | I <sub>O</sub> = 18 mA; V <sub>CC(B)</sub> = 3.0 V  | -                        | -                        | 0.55 | -                        | 0.80 | V    |
|  |                           | I <sub>O</sub> = 100 μA; V <sub>CC(B)</sub> = 3.0 V   | -                        | -                        | 0.20 | -                        | 0.30 | V    |
|  |                           | nAn port; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                     |                          |                          |      |                          |      |      |
|  |                           | I <sub>O</sub> = 24 mA; V <sub>CC(A)</sub> = 3.0 V  | -                        | -                        | 0.55 | -                        | 0.80 | V    |
|  |                           | I <sub>O</sub> = 100 μA; V <sub>CC(A)</sub> = 3.0 V   | -                        | -                        | 0.20 | -                        | 0.30 | V    |
|  |                           | I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = 2.7 V  | -                        | -                        | 0.40 | -                        | 0.60 | V    |
| I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = 2.3 V   | -                         | -   | 0.60                     | -                        | 0.60 | V                        |      |      |
| I <sub>O</sub> = 100 μA; V <sub>CC(A)</sub> = 2.3 V  | -                         | -   | 0.20                     | -                        | 0.20 | V                        |      |      |
| I <sub>I</sub>                                       | input leakage current     | V <sub>I</sub> = 5.5 V or GND   | -                        | ±0.1                     | ±5   | -                        | ±10  | μA   |
| I <sub>OZ</sub>                                      | OFF-state output current  | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND [3] | -                        | ±0.1                     | ±10  | -                        | ±20  | μA   |
| I <sub>CC</sub>                                      | supply current            | V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A                                     | -                        | 0.1                      | 40   | -                        | 80   | μA   |
| ΔI <sub>CC</sub>                                     | additional supply current | per control pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A [4]               | -                        | 5                        | 500  | -                        | 5000 | μA   |
| C <sub>I</sub>                                       | input capacitance         |   | -                        | 4.0                      | -    | -                        | -    | pF   |
| C <sub>I/O</sub>                                     | input/output capacitance  | nAn and nBn port  | -                        | 5.0                      | -    | -                        | -    | pF   |

[1] All typical values are measured at V<sub>CC(B)</sub> = 5.0 V, V<sub>CC(A)</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

[2] If V<sub>CC(A)</sub> < 2.7 V, the switching levels at all inputs are not TTL compatible.

[3] For transceivers, the parameter I<sub>OZ</sub> includes the input leakage current.

[4] V<sub>CC(A)</sub> = 2.7 V to 3.6 V: other inputs at V<sub>CC(A)</sub> or GND; V<sub>CC(B)</sub> = 4.5 V to 5.5 V: other inputs at V<sub>CC(B)</sub> or GND.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ ;  $C_L = 50\text{ pF}$ ; for test circuit see Fig. 6.

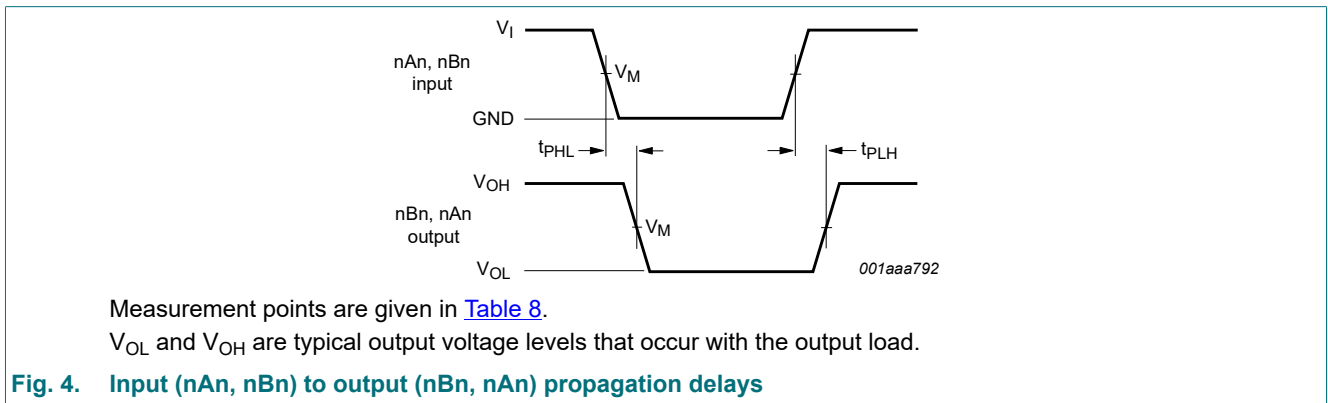
| Symbol    | Parameter         | Conditions   | -40 °C to +85 °C |        |      | -40 °C to +125 °C |      | Unit |
|-----------|-------------------|--|------------------|--------|------|-------------------|------|------|
|           |                   |  | Min              | Typ[1] | Max  | Min               | Max  |      |
| $t_{pd}$  | propagation delay | nAn to nBn; see Fig. 4 [2]   |                  |        |      |                   |      |      |
|           |                   | $V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$ ;<br>$V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$ | 1.5              | 3.3    | 7.6  | 1.5               | 9.5  | ns   |
|           |                   | $V_{CC(A)} = 2.7\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$                 | 1.0              | 3.0    | 5.9  | 1.0               | 7.5  | ns   |
|           |                   | $V_{CC(A)} = 3.0\text{ V to }3.6\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$ | 1.0              | 2.9    | 5.8  | 1.0               | 7.5  | ns   |
|           |                   | nBn to nAn; see Fig. 4 [2]   |                  |        |      |                   |      |      |
|           |                   | $V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$ ;<br>$V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$ | 1.0              | 3.0    | 7.6  | 1.0               | 9.5  | ns   |
|           |                   | $V_{CC(A)} = 2.7\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$                 | 1.0              | 4.3    | 6.7  | 1.0               | 8.5  | ns   |
|           |                   | $V_{CC(A)} = 3.0\text{ V to }3.6\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$ | 1.2              | 2.5    | 5.8  | 1.2               | 7.5  | ns   |
| $t_{en}$  | enable time       | nOE to nBn; see Fig. 5 [3]   |                  |        |      |                   |      |      |
|           |                   | $V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$ ;<br>$V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$ | 1.5              | 4.1    | 11.5 | 1.5               | 14.5 | ns   |
|           |                   | $V_{CC(A)} = 2.7\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$                 | 1.5              | 3.6    | 9.2  | 1.5               | 11.5 | ns   |
|           |                   | $V_{CC(A)} = 3.0\text{ V to }3.6\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$ | 1.0              | 3.2    | 8.9  | 1.0               | 12.0 | ns   |
|           |                   | nOE to nAn; see Fig. 5 [3]   |                  |        |      |                   |      |      |
|           |                   | $V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$ ;<br>$V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$ | 1.5              | 4.6    | 12.3 | 1.5               | 15.5 | ns   |
|           |                   | $V_{CC(A)} = 2.7\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$                 | 1.5              | 4.3    | 9.3  | 1.5               | 12.0 | ns   |
|           |                   | $V_{CC(A)} = 3.0\text{ V to }3.6\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$ | 1.0              | 3.2    | 8.9  | 1.0               | 11.5 | ns   |
| $t_{dis}$ | disable time      | nOE to nBn; see Fig. 5 [4]   |                  |        |      |                   |      |      |
|           |                   | $V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$ ;<br>$V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$ | 2.0              | 2.7    | 10.5 | 2.0               | 13.5 | ns   |
|           |                   | $V_{CC(A)} = 2.7\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$                 | 2.5              | 4.6    | 9.0  | 2.5               | 11.5 | ns   |
|           |                   | $V_{CC(A)} = 3.0\text{ V to }3.6\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$ | 2.1              | 4.9    | 8.6  | 2.1               | 11.0 | ns   |
|           |                   | nOE to nAn; see Fig. 5 [4]   |                  |        |      |                   |      |      |
|           |                   | $V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$ ;<br>$V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$ | 1.0              | 2.7    | 9.3  | 1.0               | 12.0 | ns   |
|           |                   | $V_{CC(A)} = 2.7\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$                 | 1.5              | 3.5    | 9.0  | 1.5               | 11.5 | ns   |
|           |                   | $V_{CC(A)} = 3.0\text{ V to }3.6\text{ V}$ ;<br>$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$ | 2.0              | 3.2    | 8.6  | 2.0               | 11.0 | ns   |

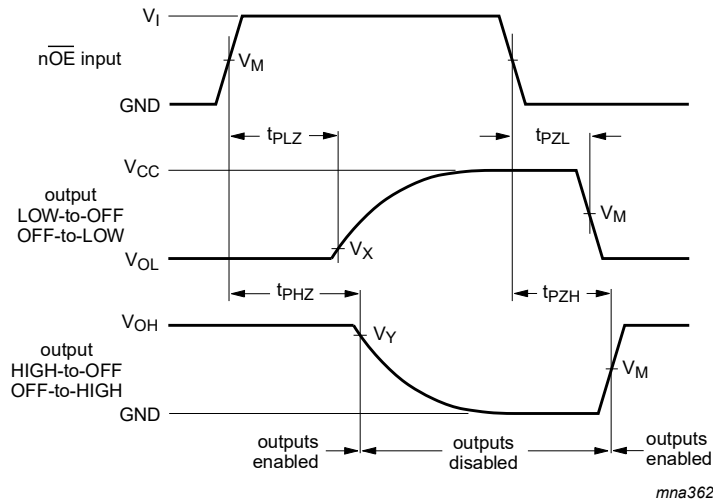


| Symbol          | Parameter                     | Conditions   | -40 °C to +85 °C |        |     | -40 °C to +125 °C |     | Unit |    |
|-----------------|-------------------------------|--|------------------|--------|-----|-------------------|-----|------|----|
|                 |                               |  | Min              | Typ[1] | Max | Min               | Max |      |    |
| C <sub>PD</sub> | power dissipation capacitance | 5 V port: nAn to nBn;<br>V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC(B)</sub> = 5 V;<br>V <sub>CC(A)</sub> = 3.3 V | [5]              |        |     |                   |     |      |    |
|                 |                               |  | outputs enabled  | -      | 30  | -                 | -   | -    | pF |
|                 |                               | outputs disabled   | -                | 15     | -   | -                 | -   | pF   |    |
|                 |                               | 3 V port: nBn to nAn;<br>V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC(B)</sub> = 5 V;<br>V <sub>CC(A)</sub> = 3.3 V | [5]              |        |     |                   |     |      |    |
|                 |                               |  | outputs enabled  | -      | 40  | -                 | -   | -    | pF |
|                 |                               |  | outputs disabled | -      | 5   | -                 | -   | -    | pF |

- [1] All typical values are measured at nominal voltage for V<sub>CC(B)</sub> and V<sub>CC(A)</sub> and at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.
- [4] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

### 10.1. Waveforms and test circuit



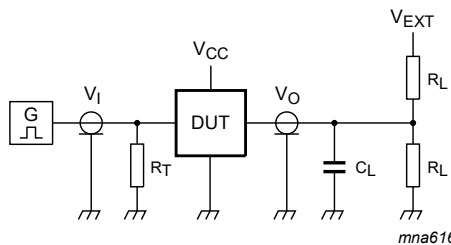


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with output load.

**Fig. 5. 3-state enable and disable times**

**Table 8. Measurement points**

| Direction            | Supply voltage |                | Input       |                        | Output                 |                        |                        |
|----------------------|----------------|----------------|-------------|------------------------|------------------------|------------------------|------------------------|
|                      | $V_{CC(A)}$    | $V_{CC(B)}$    | $V_I$       | $V_M$                  | $V_M$                  | $V_X$                  | $V_Y$                  |
| nAn port to nBn port | 2.3 V to 2.7 V | 2.7 V to 3.6 V | $V_{CC(A)}$ | $0.5 \times V_{CC(A)}$ | 1.5 V                  | $V_{OL(B)} + 0.3 V$    | $V_{OH(B)} - 0.3 V$    |
| nBn port to nAn port | 2.3 V to 2.7 V | 2.7 V to 3.6 V | 2.7 V       | 1.5 V                  | $0.5 \times V_{CC(A)}$ | $V_{OL(A)} + 0.15 V$   | $V_{OH(A)} - 0.15 V$   |
| nAn port to nBn port | 2.7 V to 3.6 V | 4.5 V to 5.5 V | 2.7 V       | 1.5 V                  | $0.5 \times V_{CC(B)}$ | $0.2 \times V_{CC(B)}$ | $0.8 \times V_{CC(B)}$ |
| nBn port to nAn port | 2.7 V to 3.6 V | 4.5 V to 5.5 V | 3.0 V       | 1.5 V                  | 1.5 V                  | $V_{OL(A)} + 0.3 V$    | $V_{OH(A)} - 0.3 V$    |



Test data is given in [Table 9](#).  
 Definitions for test circuit:  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_L$  = Load resistance.  
 $V_{EXT}$  = External voltage for measuring switching times.

**Fig. 6. Test circuit for measuring switching times**

**Table 9. Test data**

| Direction            | Supply voltage |                | Load  |              | $V_{EXT}$          |                    |                    |
|----------------------|----------------|----------------|-------|--------------|--------------------|--------------------|--------------------|
|                      | $V_{CC(A)}$    | $V_{CC(B)}$    | $C_L$ | $R_L$        | $t_{PLH}, t_{PHL}$ | $t_{PZH}, t_{PHZ}$ | $t_{PZL}, t_{PLZ}$ |
| nAn port to nBn port | 2.3 V to 2.7 V | 2.7 V to 3.6 V | 50 pF | 500 $\Omega$ | open               | GND                | $2 \times V_{CC}$  |
| nBn port to nAn port | 2.3 V to 2.7 V | 2.7 V to 3.6 V | 50 pF | 500 $\Omega$ | open               | GND                | 6.0 V              |
| nAn port to nBn port | 2.7 V to 3.6 V | 4.5 V to 5.5 V | 50 pF | 500 $\Omega$ | open               | GND                | $2 \times V_{CC}$  |
| nBn port to nAn port | 2.7 V to 3.6 V | 4.5 V to 5.5 V | 50 pF | 500 $\Omega$ | open               | GND                | 6.0 V              |

### 11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

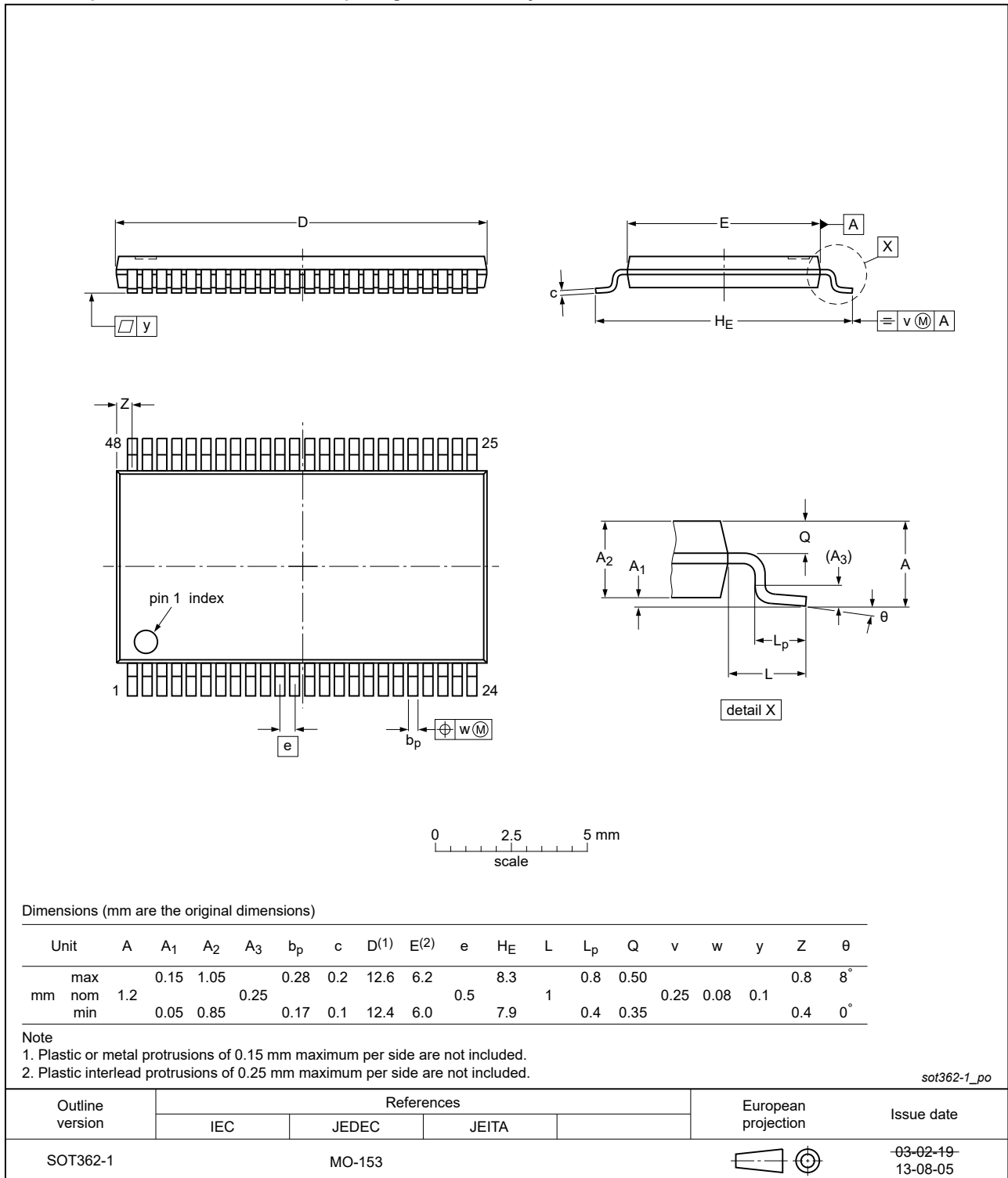


Fig. 7. Package outline SOT362-1 (TSSOP48)

## 12. Abbreviations

Table 10. Abbreviations

| Acronym | Description                             |
|---------|---|
| CMOS    | Complementary Metal-Oxide Semiconductor |
| DUT     | Device Under Test                       |
| ESD     | ElectroStatic Discharge                 |
| HBM     | Human Body Model                        |
| MM      | Machine Model                           |
| TTL     | Transistor-Transistor Logic             |

## 13. Revision history

Table 11. Revision history

| Document ID       | Release date  | Data sheet status     | Change notice | Supersedes        |
|-------------------|---|-----------------------|---------------|-------------------|
| 74ALVC164245 v.11 | 20210727  | Product data sheet    | -             | 74ALVC164245 v.10 |
| Modifications:    | <ul style="list-style-type: none"> <li>Type number 74ALVC164245DL (SOT370-1/SSOP48) removed.</li> <li><a href="#">Section 2</a> updated.</li> <li><a href="#">Section 7</a>: derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>   |                       |               |                   |
| 74ALVC164245 v.10 | 20190409  | Product data sheet    | -             | 74ALVC164245 v.9  |
| Modifications:    | <ul style="list-style-type: none"> <li><a href="#">Table 6</a>: Typo corrected for <math>V_{OL(max)}</math> at <math>V_{CC(B)} = 4.5 V</math>.</li> </ul>   |                       |               |                   |
| 74ALVC164245 v.9  | 20181112  | Product data sheet    | -             | 74ALVC164245 v.8  |
| Modifications:    | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74ALVC164245BX (SOT1134-2) removed.</li> <li>Package outline drawing <a href="#">Fig. 7</a> updated.</li> </ul> |                       |               |                   |
| 74ALVC164245 v.8  | 20120315  | Product data sheet    | -             | 74ALVC164245 v.7  |
| Modifications:    | <ul style="list-style-type: none"> <li>For type number 74ALVC164245BX the sot code has changed to SOT1134-2.</li> </ul>   |                       |               |                   |
| 74ALVC164245 v.7  | 20111117  | Product data sheet    | -             | 74ALVC164245 v.6  |
| Modifications:    | <ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>  |                       |               |                   |
| 74ALVC164245 v.6  | 20110616  | Product data sheet    | -             | 74ALVC164245 v.5  |
| 74ALVC164245 v.5  | 20100413  | Product data sheet    | -             | 74ALVC164245 v.4  |
| 74ALVC164245 v.4  | 20081111  | Product data sheet    | -             | 74ALVC164245 v.3  |
| 74ALVC164245 v.3  | 20040914  | Product data sheet    | -             | 74ALVC164245 v.2  |
| 74ALVC164245 v.2  | 20040601  | Product data sheet    | -             | 74ALVC164245 v.1  |
| 74ALVC164245 v.1  | 19980826  | Product specification | -             | -                 |

## 14. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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