# PIC32MK GPG/MCJ Family

## PIC32MK General Purpose and Motor Control GPG/MCJ with CAN FD Family Silicon Errata and Data Sheet Clarifications

## PIC32MK (GPG/MCJ) Family Errata

The PIC32MK family of devices that you have received conform functionally to the device data sheet, PIC32MK General Purpose and Motor Control (GPG/MCJ) with CAN FD Family Data Sheet (DS60001570**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table. The silicon issues are summarized in the Table of Contents following this section.

The errata described in this document will be addressed in future revisions of the PIC32MK family silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

**Table 1. PIC32MK Family Silicon Device Identification**

| Part Number | Device Identification (DEVID[27:0]) | Revision ID (DEVID[31:28]) |
| --- | --- | --- |
| | | A1 |
| PIC32MK0512MCJ064 | 0x6300053 | 0x1 |
| PIC32MK0512MCJ048 | 0x6301053 | |
| PIC32MK0256MCJ064 | 0x6304053 | |
| PIC32MK0256MCJ048 | 0x6305053 | |
| PIC32MK0512GPG064 | 0x6318053 | |
| PIC32MK0512GPG048 | 0x6319053 | |
| PIC32MK0256GPG064 | 0x631C053 | |
| PIC32MK0256GPG048 | 0x631D053 | |

Data Sheet clarifications and corrections (if applicable) are located in the section "Data Sheet Clarifications", following the discussion of silicon issues.

## Table of Contents

# 1. Silicon Errata Issues Summary

The following errata issues are to be noted for the current device data sheet, PIC32MK General Purpose and Motor Control (GPG/MCJ) with CAN FD Family (DS60001570**C**).

**Table 1-1. Silicon Errata Summary**

| Module | Feature | Item # | Issue Summary | Affected Revisions |
|---|---|---|---|---|
| | | | | A1 |
| Oscillator | Hardware Clock Source Selection | 2.1.1 | Clock source selection in hardware, that is, using the Fuse Configuration register FNOSC <2:0> bits (DEVCFG1 <2:0>) does not work. | X |
| ADC | Scan mode | 2.2.1 | Shared ADC7 on high Offset and Gain Error in Scan mode. | X |
| I2C | Speed | 2.3.1 | $I^2C$ master module does not meet low period of the SCL Clock ($t_{LOW}$) parameter from $I^2C$ specification for clock frequency >= 400 kHz. | X |
| I2C | Slave | 2.3.2 | The 7-bit address that matches the 10-bit upper address value (111_10xx) is not accepted regardless of the STRICT bit setting. | X |

## 2. Silicon Errata Issues

The following issues apply to the PIC32MK GPG/MCJ family of devices.

**Notes:**

- An 'X' indicates the issue is present in this revision of silicon.
- Cells with a dash ('-') indicate that this silicon revision does not exist for this issue.
- Blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

### 2.1 Oscillator

#### 2.1.1 Hardware Clock Source Selection

After a Brown-out Reset, the system clock source may default to FRC instead of the clock source defined using the Fuse Configuration register FNOSC<2:0> bits (DEVCFG1<2:0>).

**Workaround:**

Upon any reset, verify if the Current Clock Source Selection register COSC<2:0> bits (OSCCON<14:12>) match the clock source selected using the Fuse Configuration register FNOSC<2:0> bits (DEVCFG1<2:0>). If the clock sources do not match, perform a software clock switch to the desired clock source. Refer to Section 42. *Oscillators with Enhanced PLL (DS60001250), subsection 42.3.7.2 Oscillator Switching Sequence* in the *PIC32 Family Reference Manual* for details on software clock switching.

**Affected Revisions:**

| A1 | | | | | | | |
|----|----|----|----|----|----|----|----|
| X | | | | | | | |

### 2.2 ADC

#### 2.2.1 Scan Mode

Shred ADC 7 has high offset and gain error up to 38 Lsb in ADC7 Scan mode, as defined in the ADCCSS1/ADCCSS2 registers.

**Workaround:**

Increase the user-defined SMAC<9:0> bits (ADCCON2<25:16> sample time register valaue by 4 $T_{AD}$. This will reduce the ADC7 throughput that the user must consider, but it will reduce the gain and offset to less that 4 Lsb in 12-bit mode.

**Affected Revisions:**

| A1 | | | | | | | |
|----|----|----|----|----|----|----|----|
| X | | | | | | | |

### 2.3 I²C

#### 2.3.1 Speed

The I²C master module does not meet low period of the SCL clock ($t_{LOW}$) parameter from I² C specification for clock frequency >= 400 kHz.

**Workaround:**

None.

**Affected Revisions:**

| A1 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 2.3.2 Slave

The 7-bit address that matches the 10-bit upper address value (111_10xx) is not accepted regardless of the STRICT bit setting.

**Workaround:**

None

**Affected Revisions:**

| A1 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 3.    Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the current device data sheet, PIC32MK General Purpose and Motor Control (GPG/MCJ) with CAN FD Family (DS60001570**C**), and are showed in **BOLD** type.

Currently there are no known issues to report.

## 4.    Revision History

**Revision B - June 2020**

Addition of A1 silicon revision.

The following silicon errata issues were added:

- Oscillator: 2.1.1 Hardware Clock Source Selection
- ADC 2.2.1  Scan Mode
- I$^2$C Speed 2.3.1  Speed and I$^2$C Slave 2.3.2  Slave

**Revision A - May 2019**

This is the initial released version of this document.

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