High Isolation SP4T SWITCH

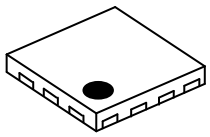
■ GENERAL DESCRIPTION

The NJG1699MD7 is a GaAs high isolation SP4T switch MMIC. It features low insertion loss and very high isolation. It has integrated DC blocking capacitor at PC port.

The ESD protection circuits are integrated in the IC to achieve high ESD tolerance.

The ultra-small and ultra-thin EQFN14-D7 package is adopted.

■ PACKAGE OUTLINE



NJG1699MD7

■ APPLICATIONS

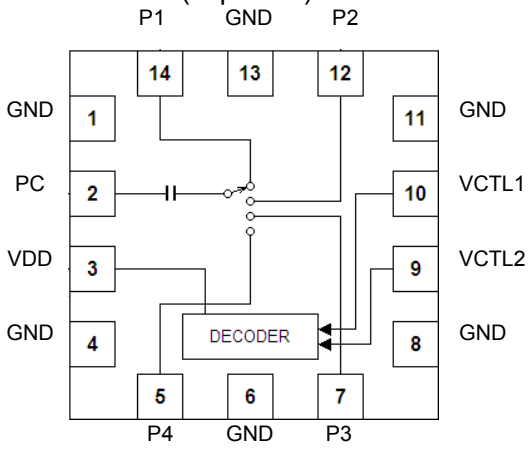
Suitable for multi-mode 2G/3G and LTE application receive system Rx signal switching

■ FEATURES

- Low operation voltage V_{DD}=+2.7V typ.
- Low control voltage $V_{CTL(H)}$=+1.8V typ.
- High isolation 50dB typ. @f=1.0GHz, P_{IN}=0dBm
  48dB typ. @f=2.0GHz, P_{IN}=0dBm
  43dB typ. @f=2.7GHz, P_{IN}=0dBm
- Low insertion loss 0.55dB typ. @f=1.0GHz, P_{IN}=0dBm
  0.55dB typ. @f=2.0GHz, P_{IN}=0dBm
  0.65dB typ. @f=2.7GHz, P_{IN}=0dBm
- Small package EQFN14-D7 (Package size: 1.6x1.6x0.397mm typ.)
- RoHS compliant and Halogen Free
- MSL 1

■ PIN CONFIGURATION

(Top View)



Pin connection

1. GND	8. GND
2. PC	9. VCTL2
3. VDD	10. VCTL1
4. GND	11. GND
5. P4	12. P2
6. GND	13. GND
7. P3	14. P1

Exposed PAD: GND

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

ON PATH	VCTL1	VCTL2
PC-P1	H	L
PC-P2	L	L
PC-P3	L	H
PC-P4	H	H

NOTE: Please note that any information on this catalog will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C, Z_s=Z_l=50Ω)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	V_{DD} =2.7V	28	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	VCTL1, VCTL2 terminal	5.0	V
Power Dissipation	P_D	Four-layer FR4 PCB with through-hole (76.2x114.3mm), T_j=150°C	1300	mW
Operating Temp.	T_{opr}		-40~+90	°C
Storage Temp.	T_{stg}		-55~+150	°C

■ELECTRICAL CHARACTERISTICS

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω, V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, with application circuit)

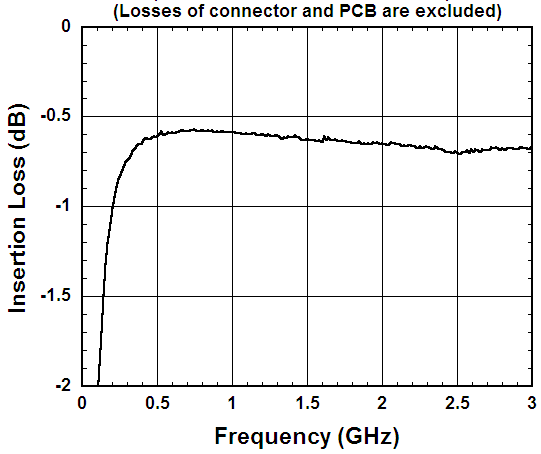
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	VDD terminal	1.5	2.7	4.5	V
Operating Current	I_{DD}		-	20	40	μA
Control Voltage (LOW)	$V_{CTL(L)}$	VCTL1, VCTL2 terminal	0	0	0.45	V
Control Voltage (HIGH)	$V_{CTL(H)}$	VCTL1, VCTL2 terminal	1.35	1.8	4.5	V
Control Current	I_{CTL}	$V_{CTL(H)}$ =1.8V	-	5	10	μA
Insertion Loss 1	LOSS1	f=1.0GHz, P_{IN}=0dBm	-	0.55	0.75	dB
Insertion Loss 2	LOSS2	f=2.0GHz, P_{IN}=0dBm	-	0.55	0.75	dB
Insertion Loss 3	LOSS3	f=2.7GHz, P_{IN}=0dBm	-	0.60	0.80	dB
Isolation 1	ISL1	PC-P1, P2, P3, P4 f=1.0GHz, P_{IN}=0dBm	45	50	-	dB
Isolation 2	ISL2	PC-P1, P2, P3, P4 f=2.0GHz, P_{IN}=0dBm	45	48	-	dB
Isolation 3	ISL3	PC-P1, P2, P3, P4 f=2.7GHz, P_{IN}=0dBm	40	43	-	dB
Input power at 0.2dB Compression Point	$P_{-0.2dB}$	f=2.0GHz	18	22	-	dBm
VSWR	VSWR	f=2.0GHz, On port	-	1.3	1.5	-
Switching time	T_{SW}	50% V_{CTL} to 10/90% RF	-	2	5	μs

■ TERMINAL INFORMATION

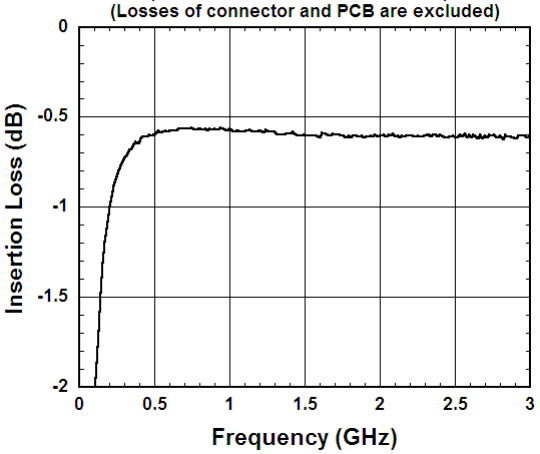
No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
2	PC	RF input/output port. No DC blocking capacitor is required for this port because of internal capacitor.
3	VDD	Positive voltage supply terminal. The positive voltage (+1.5~+4.5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
4	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
5	P4	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
6	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
7	P3	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
8	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
9	VCTL2	Control signal input terminal. This terminal is set to High-Level (+1.35~+4.5V) or Low-Level (0~+0.45V).
10	VCTL1	Control signal input terminal. This terminal is set to High-Level (+1.35~+4.5V) or Low-Level (0~+0.45V).
11	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
12	P2	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
13	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
14	P1	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
Exposed Pad	GND	Ground terminal.

■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

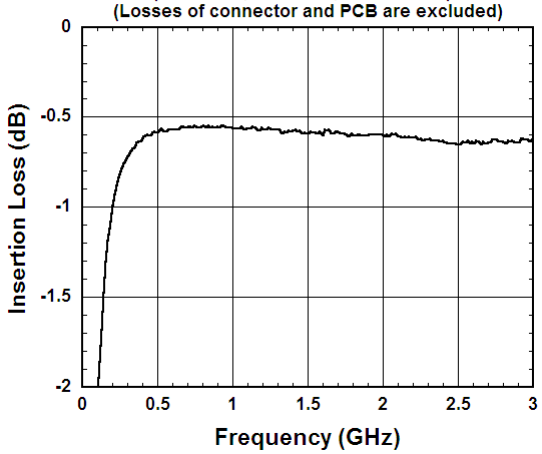
Insertion Loss vs. Frequency
(PC-P1 ON, V_{DD}=2.7V, V_{CTL}=0/1.8V)
(Losses of connector and PCB are excluded)



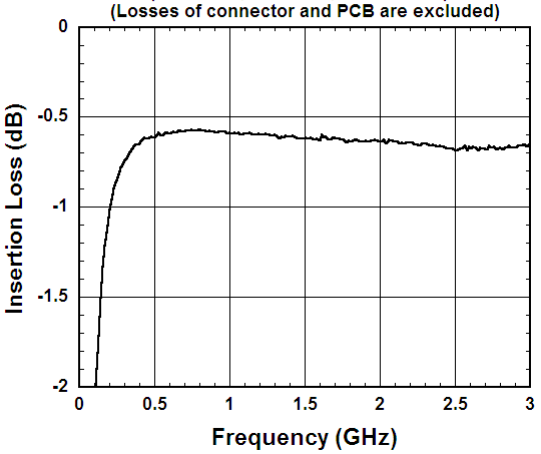
Insertion Loss vs. Frequency
(PC-P2 ON, V_{DD}=2.7V, V_{CTL}=0/1.8V)
(Losses of connector and PCB are excluded)



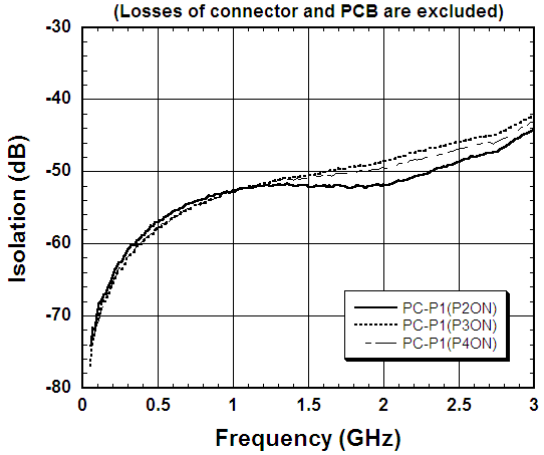
Insertion Loss vs. Frequency
(PC-P3 ON, V_{DD}=2.7V, V_{CTL}=0/1.8V)
(Losses of connector and PCB are excluded)



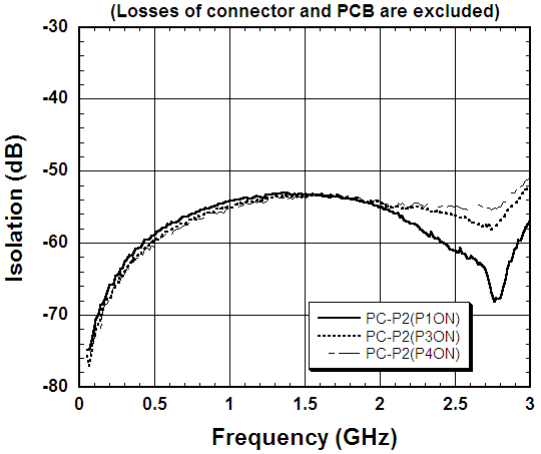
Insertion Loss vs. Frequency
(PC-P4 ON, V_{DD}=2.7V, V_{CTL}=0/1.8V)
(Losses of connector and PCB are excluded)



PC-P1 Isolation vs. Frequency
(V_{DD}=2.7V, V_{CTL}=0/1.8V)
(Losses of connector and PCB are excluded)

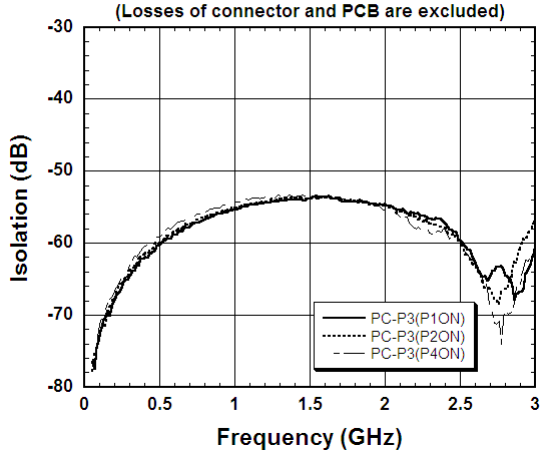


PC-P2 Isolation vs. Frequency
(V_{DD}=2.7V, V_{CTL}=0/1.8V)
(Losses of connector and PCB are excluded)

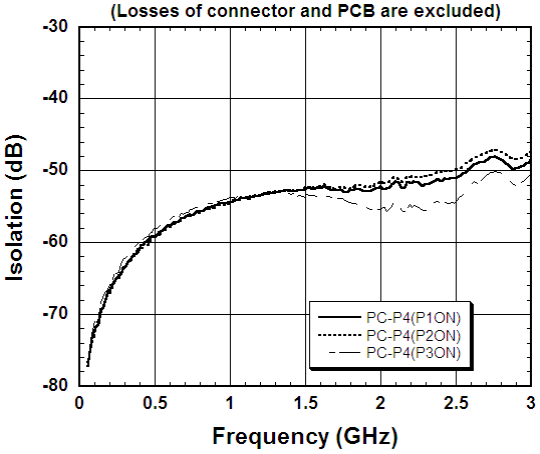


■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

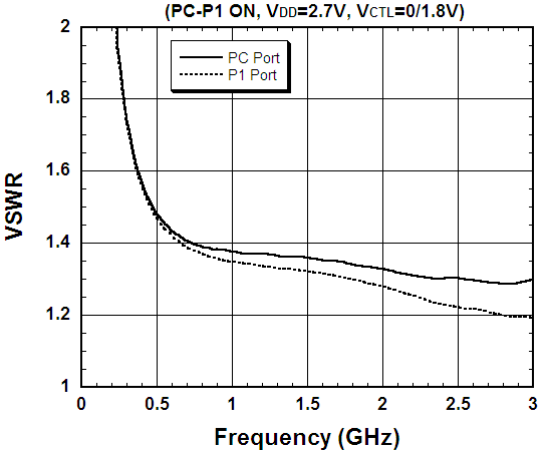
PC-P3 Isolation vs. Frequency
(VDD=2.7V, VCTL=0/1.8V)
(Losses of connector and PCB are excluded)



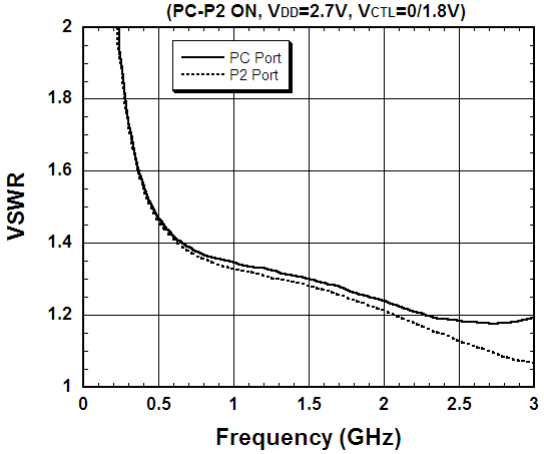
PC-P4 Isolation vs. Frequency
(VDD=2.7V, VCTL=0/1.8V)
(Losses of connector and PCB are excluded)



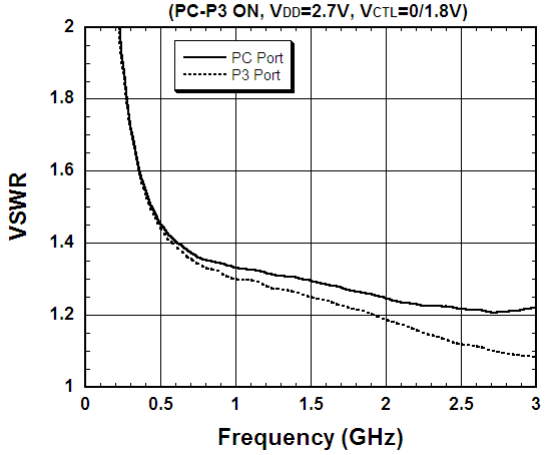
VSWR vs. Frequency
(PC-P1 ON, VDD=2.7V, VCTL=0/1.8V)



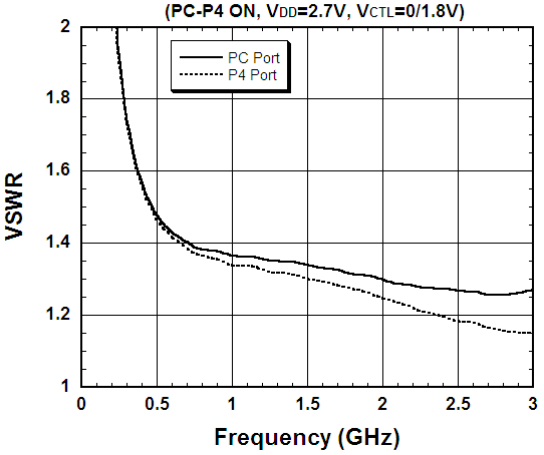
VSWR vs. Frequency
(PC-P2 ON, VDD=2.7V, VCTL=0/1.8V)



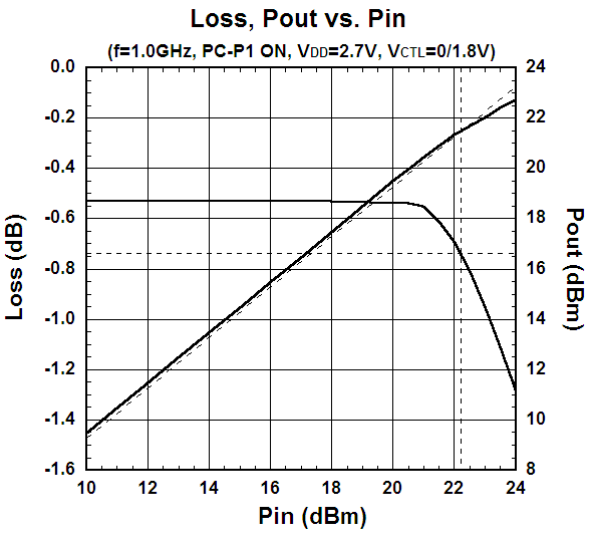
VSWR vs. Frequency
(PC-P3 ON, VDD=2.7V, VCTL=0/1.8V)

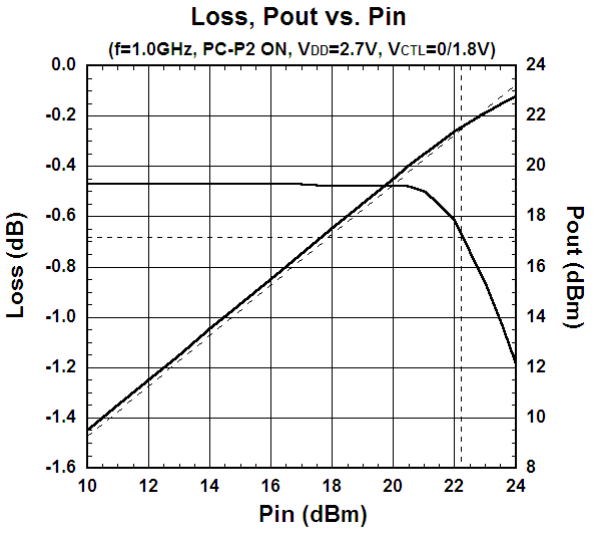


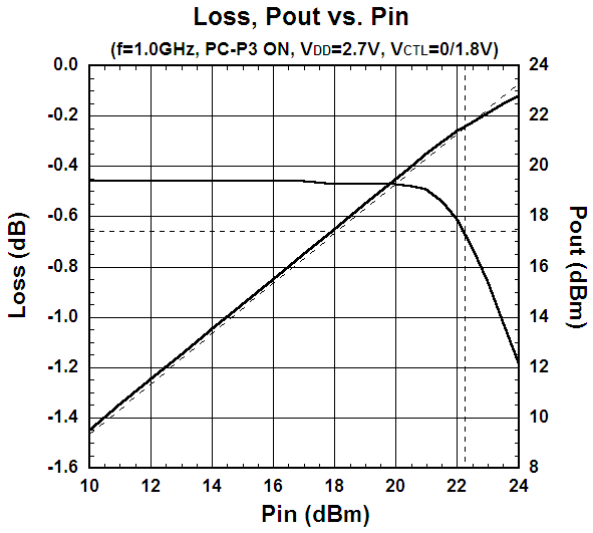
VSWR vs. Frequency
(PC-P4 ON, VDD=2.7V, VCTL=0/1.8V)

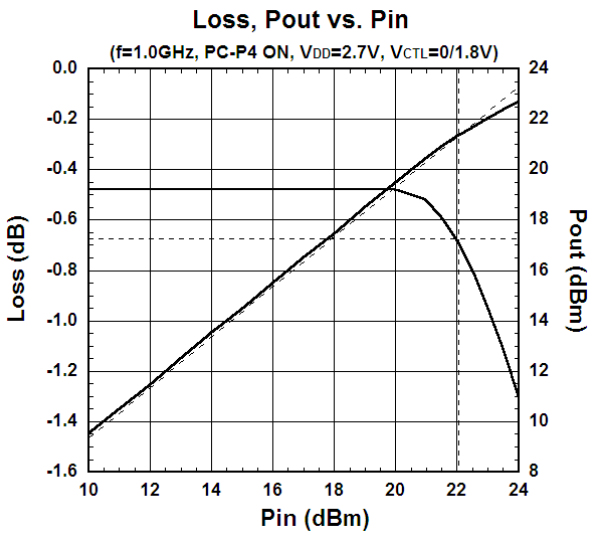


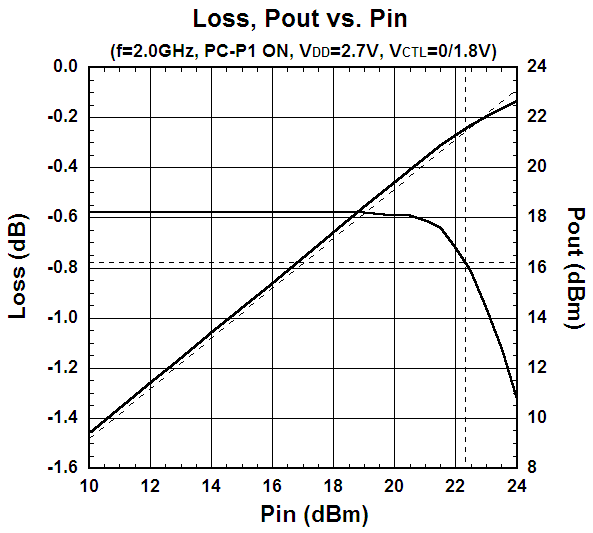
■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

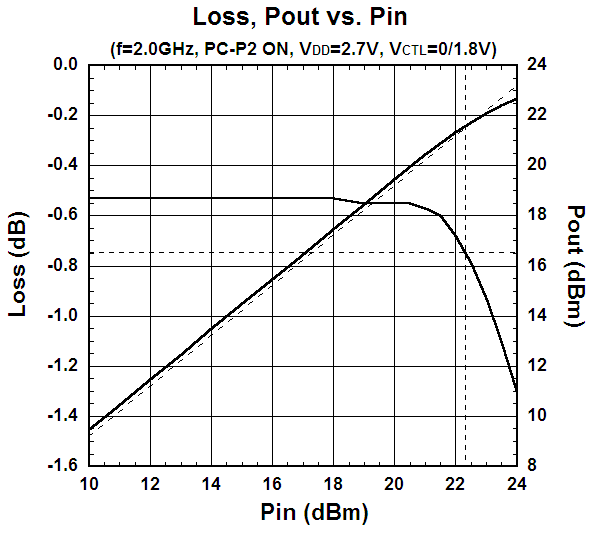












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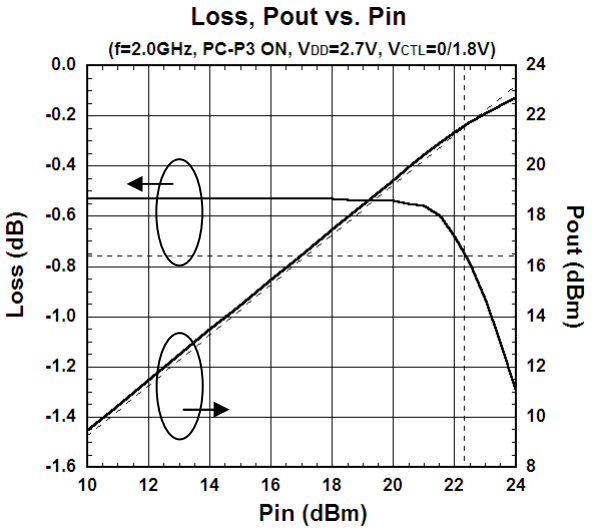
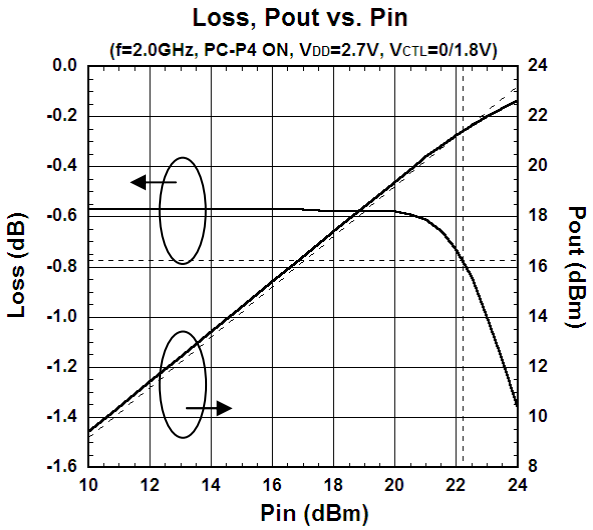
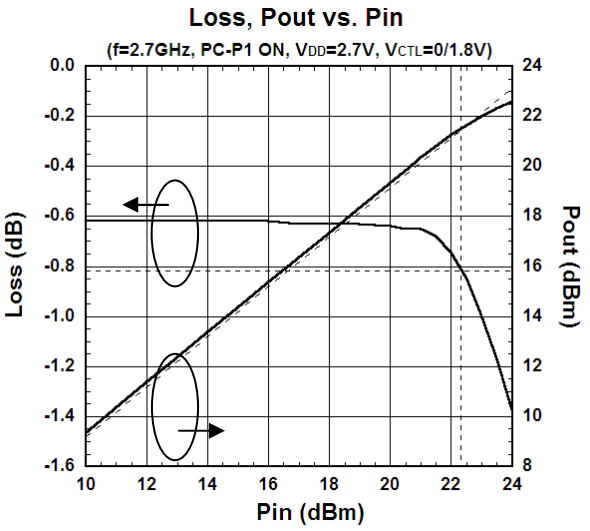
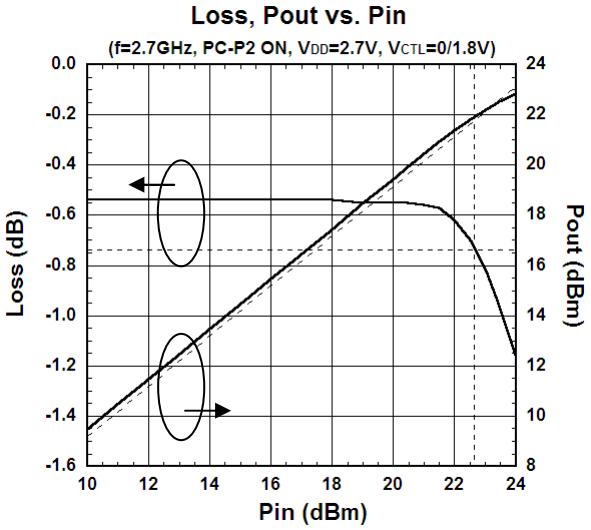
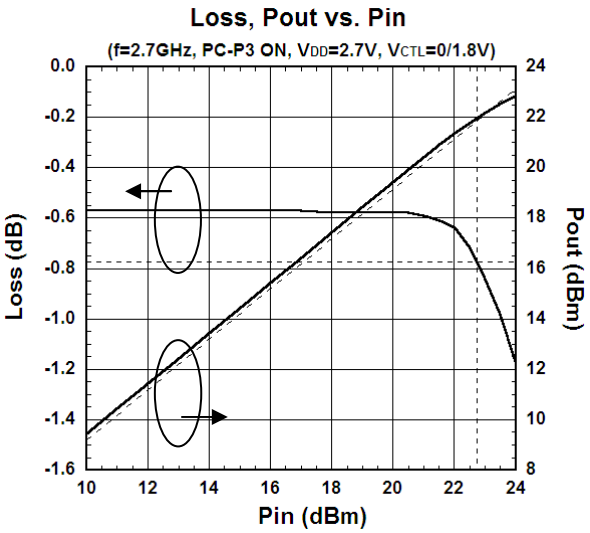
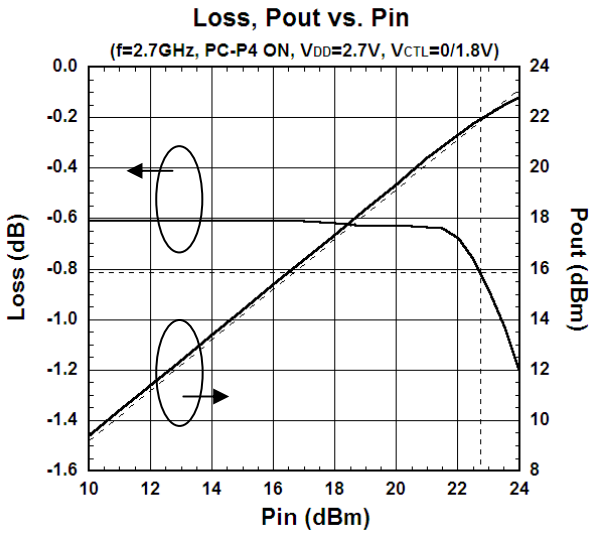






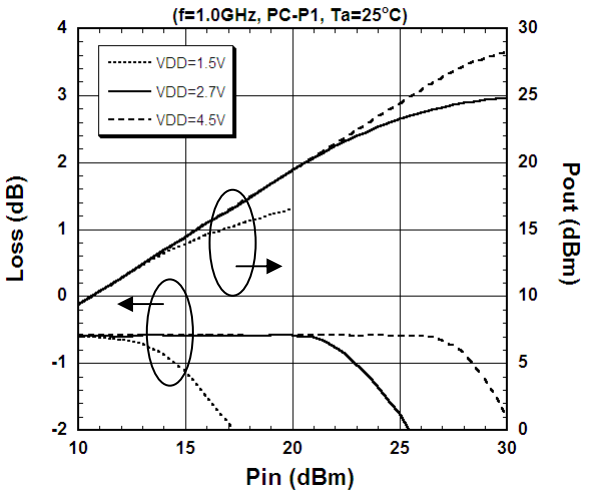




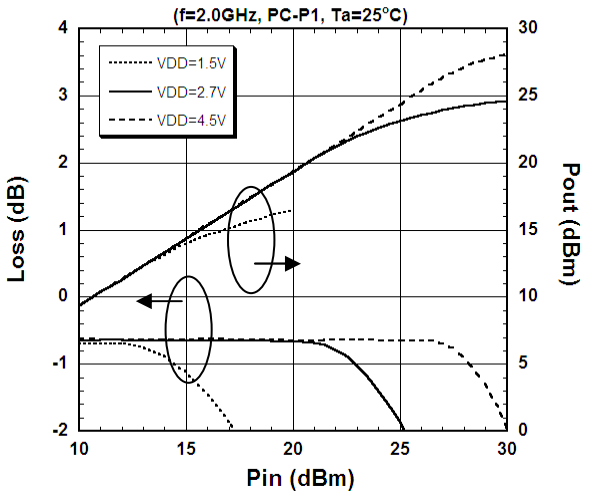


■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

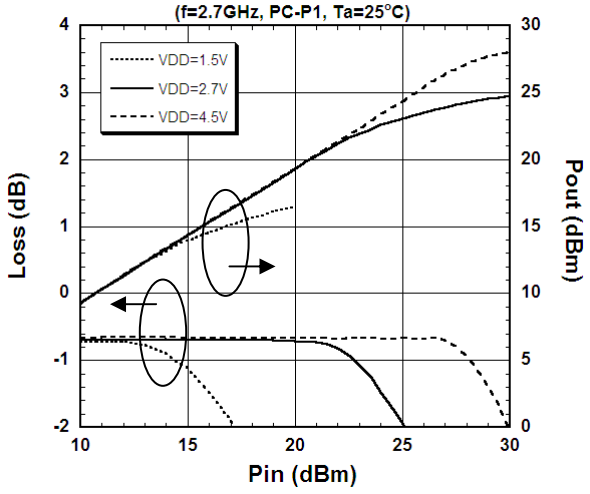
Loss, Pout vs. Pin
(f=1.0GHz, PC-P1, Ta=25°C)



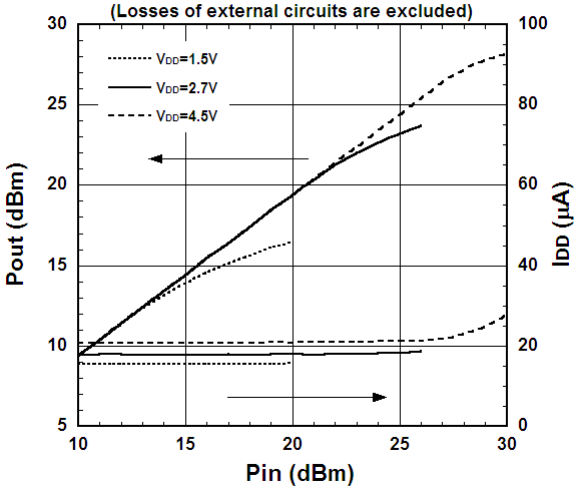
Loss, Pout vs. Pin
(f=2.0GHz, PC-P1, Ta=25°C)



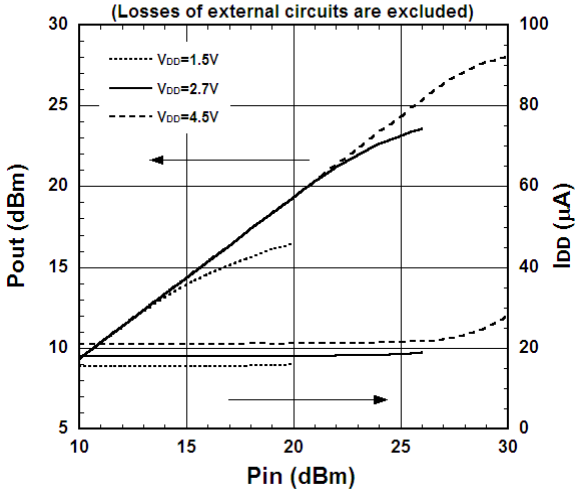
Loss, Pout vs. Pin
(f=2.7GHz, PC-P1, Ta=25°C)



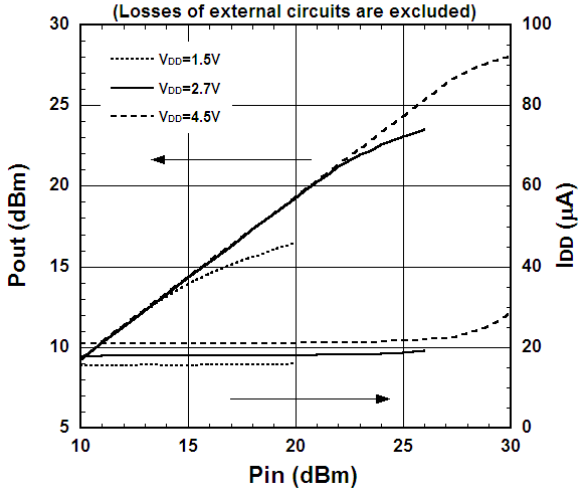
Pout, IDD vs. Pin
(f=1.0GHz, PC-P1 ON, VCTL=1.8V)
(Losses of external circuits are excluded)



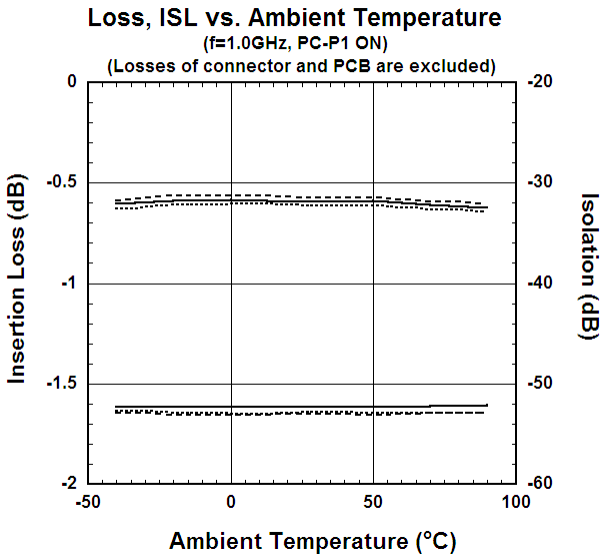
Pout, IDD vs. Pin
(f=2.0GHz, PC-P1 ON, VCTL=1.8V)
(Losses of external circuits are excluded)

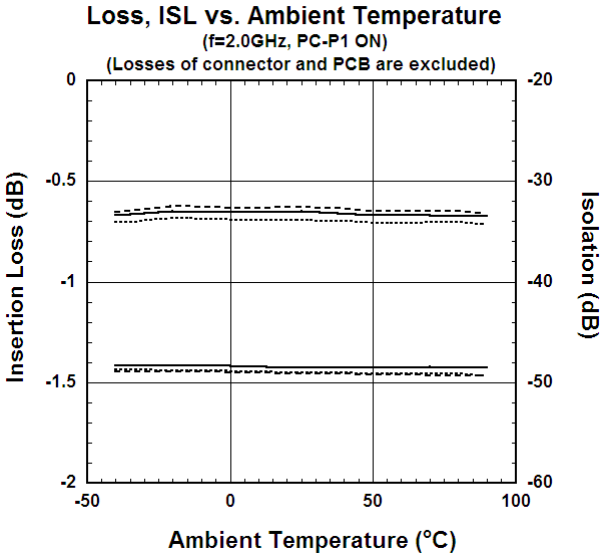


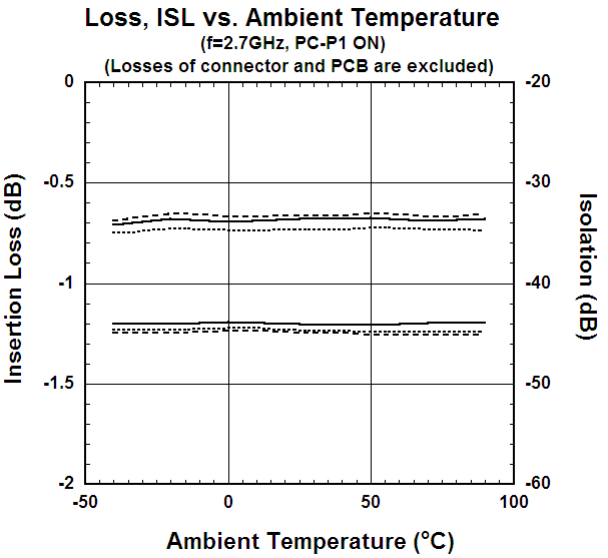
Pout, IDD vs. Pin
(f=2.7GHz, PC-P1 ON, VCTL=1.8V)
(Losses of external circuits are excluded)

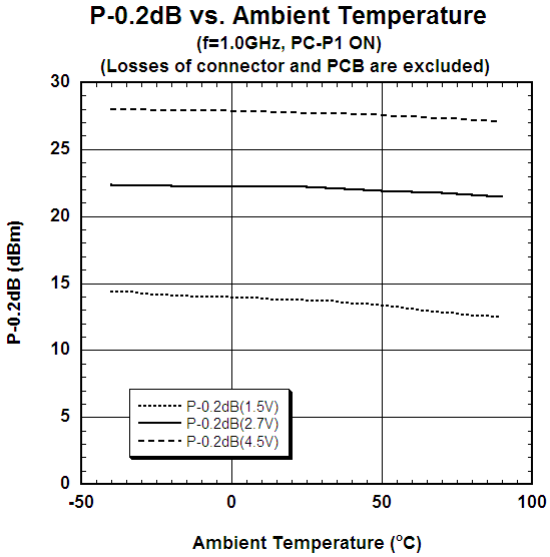


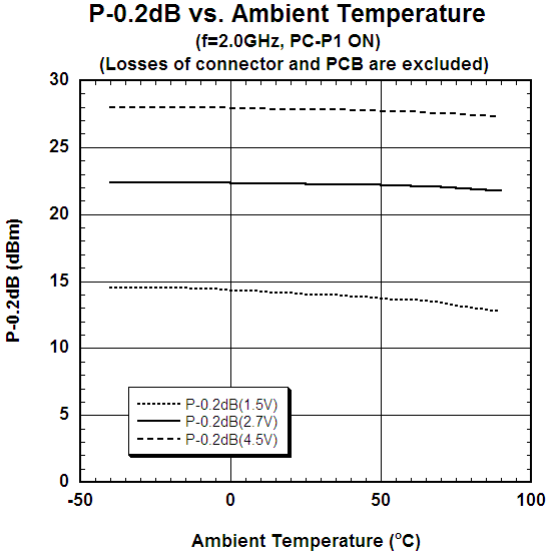
■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

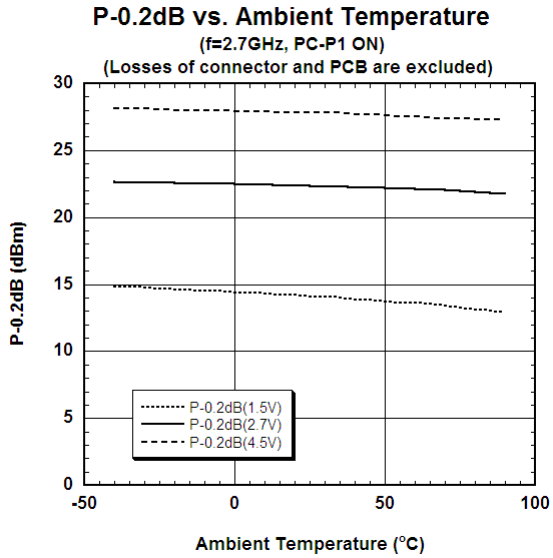




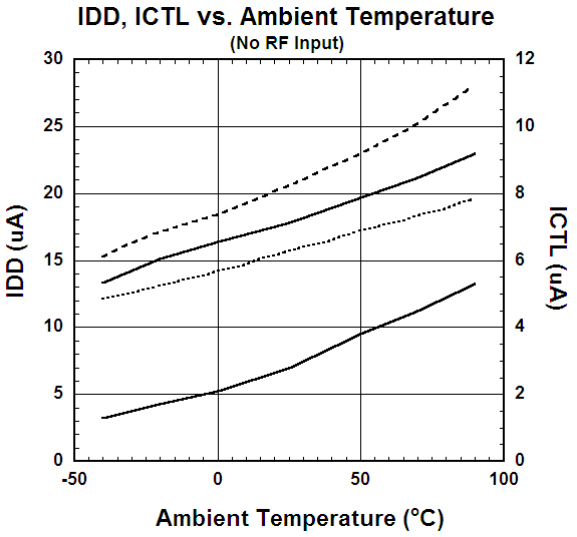


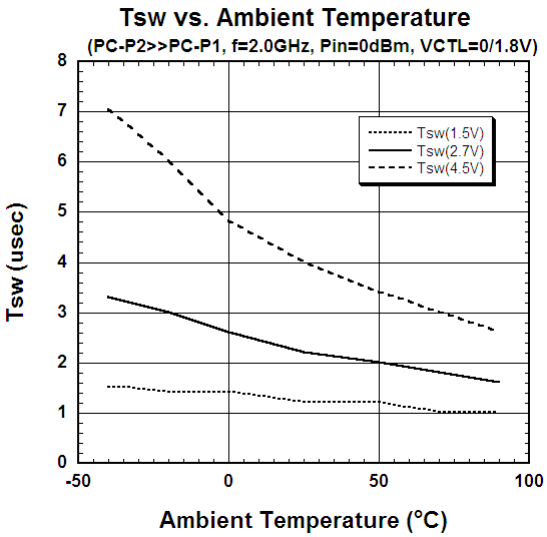




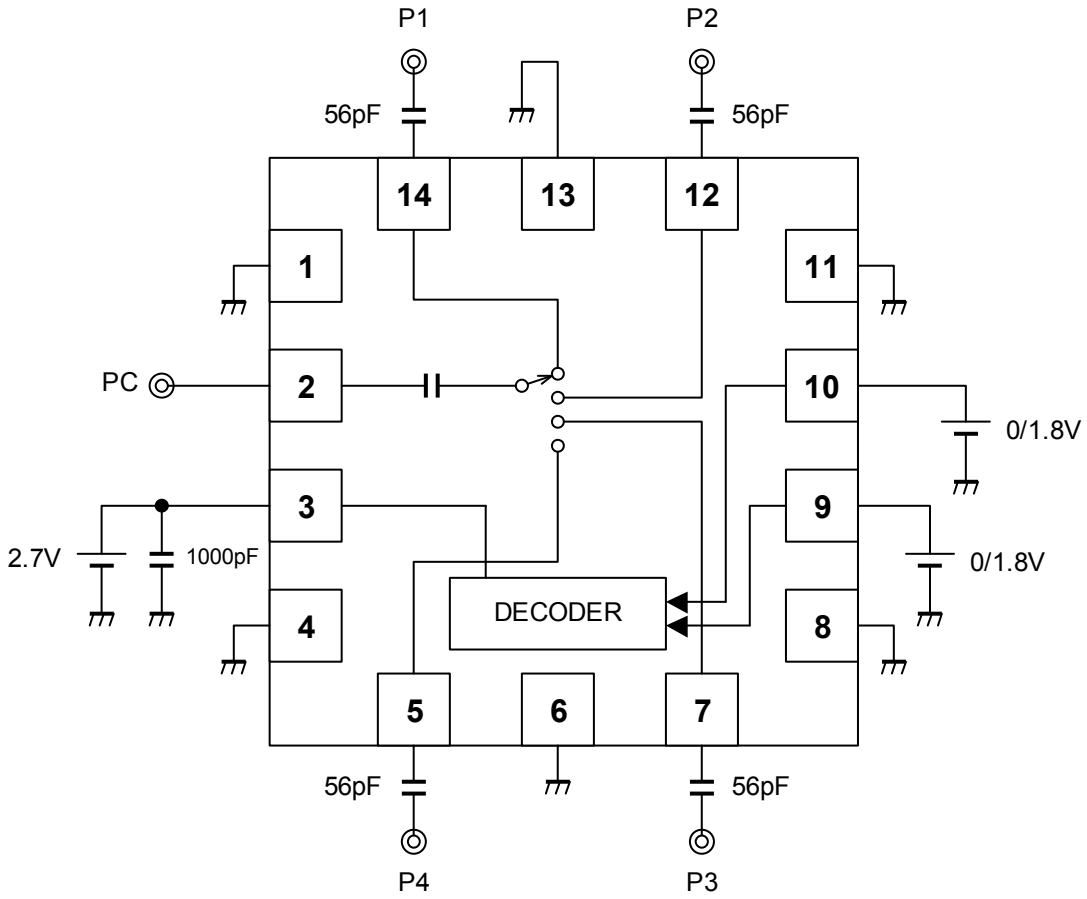


■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)





■APPLICATION CIRCUIT



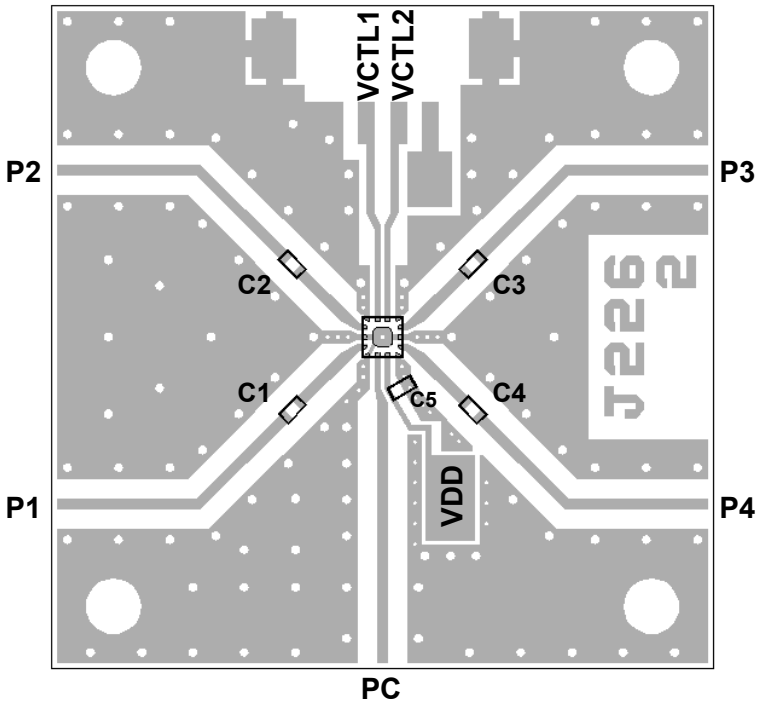
No external DC blocking capacitor at PC terminal is required because of the internal capacitor in IC.

■ PARTS LIST

Part ID	Value	Notes
C1~C4	56pF	MURATA (GRM15)
C5	1000pF	MURATA (GRM15)

■APPLIED CIRCUIT BOARD EXAMPLES

(TOP VIEW)

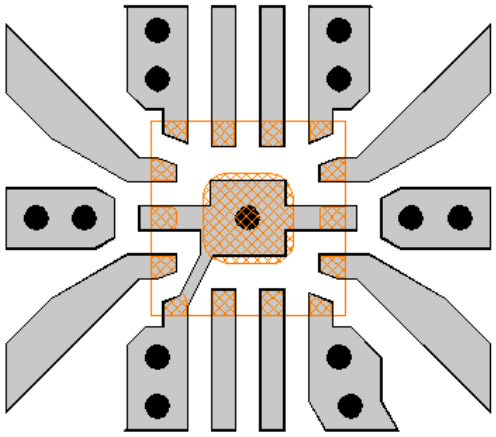


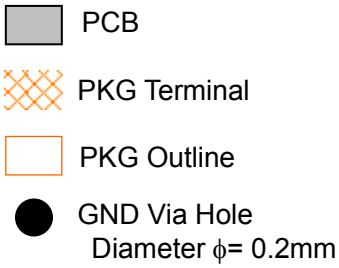
PCB: FR-4, t=0.2mm
Capacitor Size: 1005 (1.0 x 0.5 mm)
Strip Line Width: 0.4mm
PCB Size: 25.8 x 25.8mm
Through Hole Diameter: 0.2mm

Losses of PCB, capacitors and connectors

Paths	Frequency (GHz)	Loss (dB)
PC-P1 PC-P2 PC-P3 PC-P4	1.0	0.31
	2.0	0.44
	2.7	0.55

<PCB LAYOUT GUIDELINE>





PRECAUTIONS

[1] The DC current at RF ports must be equal to zero, which can be achieved with DC blocking capacitors (C1~C4).

(However, in case there is no possibility that DC current flows, the DC blocking capacitors are unnecessary, i.e. the RF signals are fed by SAW filters that block DC current by nature, etc.)

[2] To reduce stripline influence on RF characteristics, please locate the bypass capacitor (C5) close to VDD terminal.

[3] For good isolation, the GND terminals must be connected to the PCB ground plane of substrate, and the through-holes connecting the backside ground plane should be placed near by the pin connection.

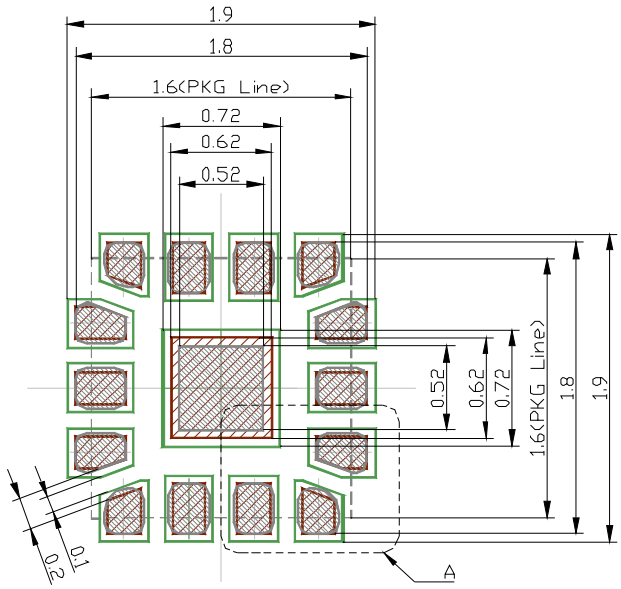
■ RECOMMENDED FOOTPRINT PATTERN (EQFN14-D7 PACKAGE Reference)

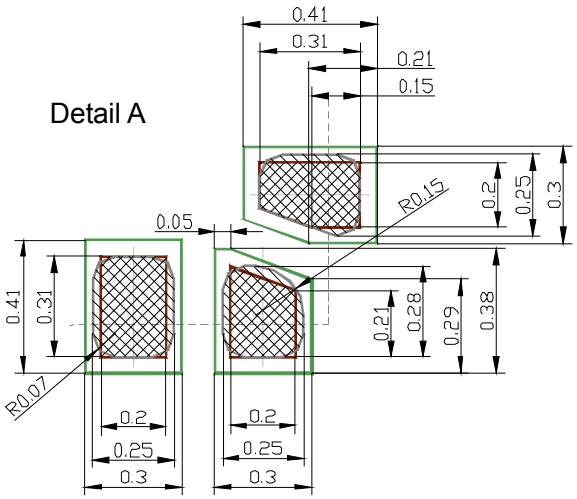
:Land

:Mask (Open area) *Metal mask thickness : 100um

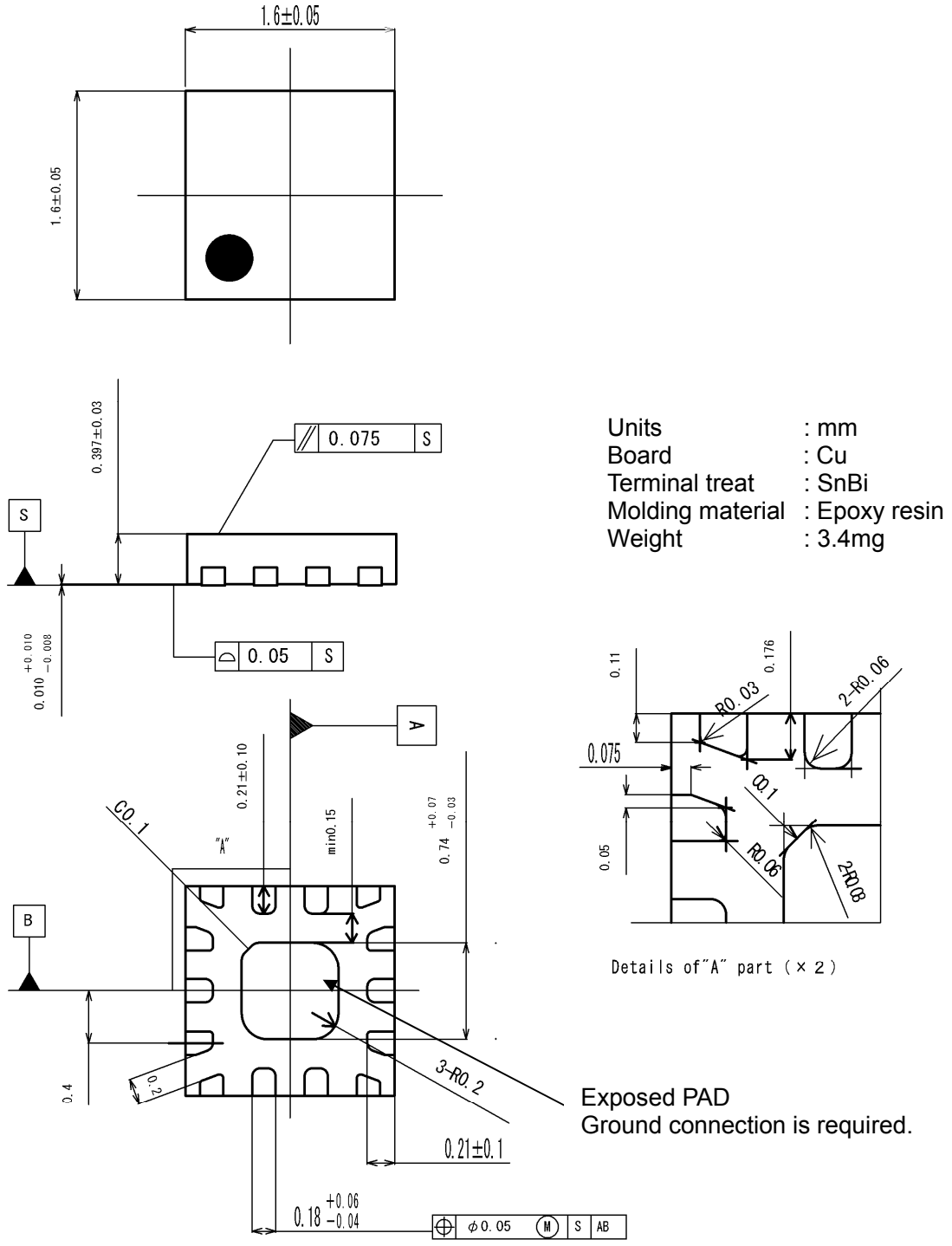
:Resist(Open area)

PKG: 1.6mm x 1.6mm
Pin pitch: 0.4mm





■ PACKAGE OUTLINE (EQFN14-D7)



Units : mm
Board : Cu
Terminal treat : SnBi
Molding material : Epoxy resin
Weight : 3.4mg

Details of"A" part (×2)

Exposed PAD
Ground connection is required.

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.