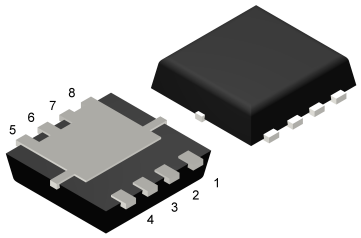
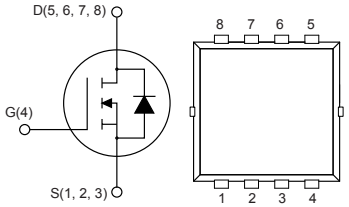
Datasheet

N-channel 100 V, 62 mΩ typ., 4.5 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 3.3x3.3 package



PowerFLAT™ 3.3x3.3



AM15810v1

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL4N10F7	100 V	70 mΩ	4.5 A

- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ration for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Maturity status link	
STL4N10F7	
Device summary	
Order code	STL4N10F7
Marking	4N1F7
Package	PowerFLAT™ 3.3x3.3
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_{pcb} = 25 °C	4.5	A
	Drain current (continuous) at T_{pcb} = 100 °C	3.2	A
I_{DM}(1)(2)	Drain current (pulsed)	18	A
P_{TOT}(1)	Total dissipation at T_{pcb} = 25 °C	2.9	W
I_D(3)	Drain current (continuous) at T_c = 25 °C	17	A
	Drain current (continuous) at T_c = 100 °C	11	A
I_{DM} (2)(3)	Drain current (pulsed)	68	A
P_{TOT}(3)	Total dissipation at T_c = 25 °C	35.7	W
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		°C

1. *This value is rated according to $R_{thj\text{-}pcb}$.*
2. *Pulse width is limited by safe operating area.*
3. *This value is rated according to $R_{thj\text{-}case}$.*

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	3.5	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	42.8	°C/W

1. *When mounted on an 1-inch^2 FR-4 board, 2oz Cu, t < 10 s*

2 Electrical characteristics

(T_C= 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 100 V			1	µA
		V_{GS} = 0 V, V_{DS} = 100 V, T_C= 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.25 A		62	70	mΩ

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	408	-	pF
C_{oss}	Output capacitance		-	112	-	pF
C_{rss}	Reverse transfer capacitance		-	10	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 4.5 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	7.8	-	nC
Q_{gs}	Gate-source charge		-	3	-	nC
Q_{gd}	Gate-drain charge		-	1.7	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 2.25 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	6.3	-	ns
t_r	Rise time		-	3	-	ns
$t_{d(off)}$	Turn-off delay time		-	11	-	ns
t_f	Fall time		-	4	-	ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 2.25 A, V_{GS} = 0 V	-		1.1	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	I_{SD} = 2.25 A, di/dt = 100 A/µs,	-	30		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 80 V,T_j = 150 °C	-	24		nC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	1.6		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 3. Safe operating area

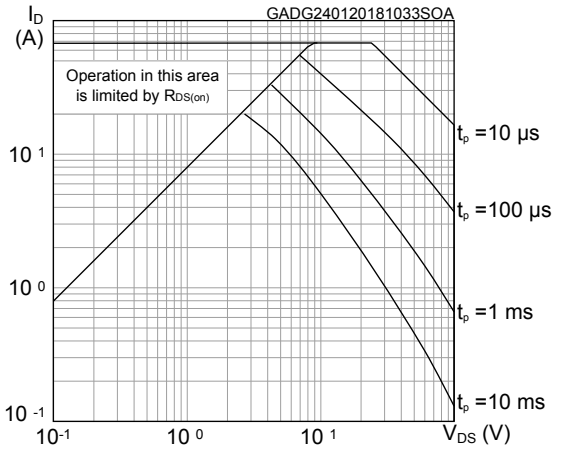


Figure 4. Thermal impedance

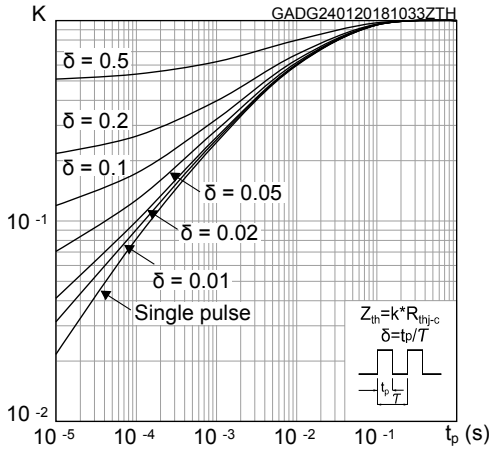


Figure 5. Output characteristics

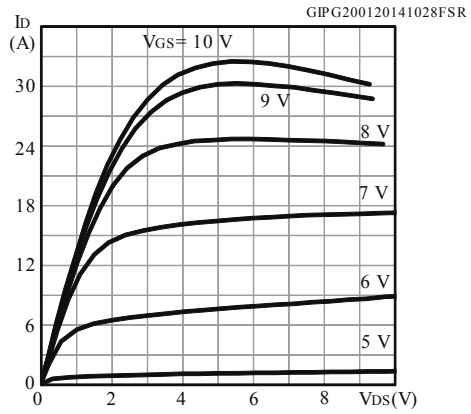


Figure 6. Transfer characteristics

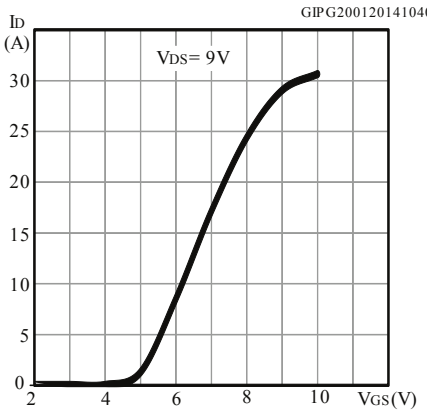


Figure 7. Gate charge vs gate-source voltage

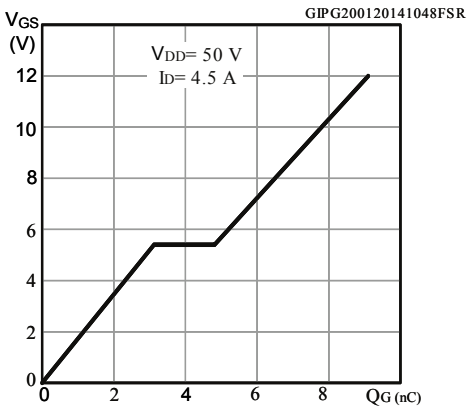


Figure 8. Static drain-source on-resistance

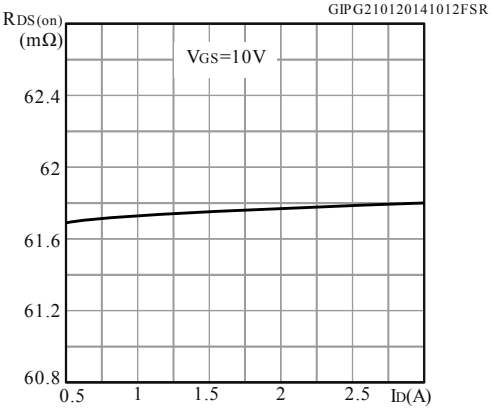


Figure 9. Capacitance variations

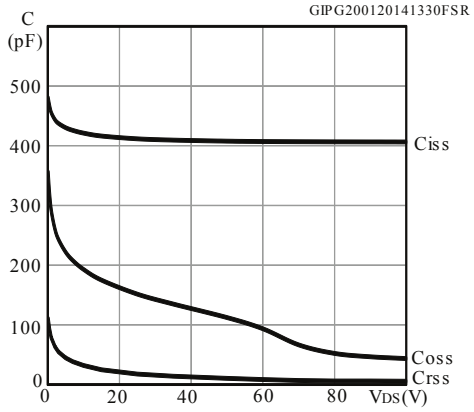


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

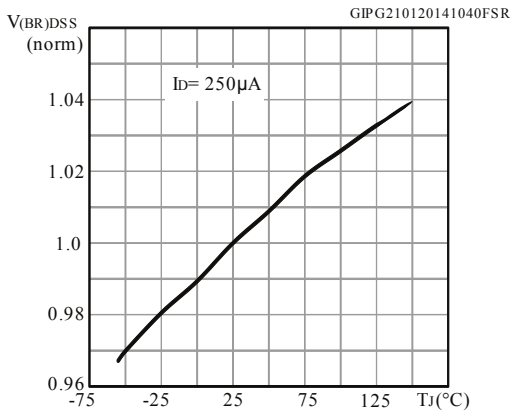


Figure 11. Normalized gate threshold voltage vs temperature

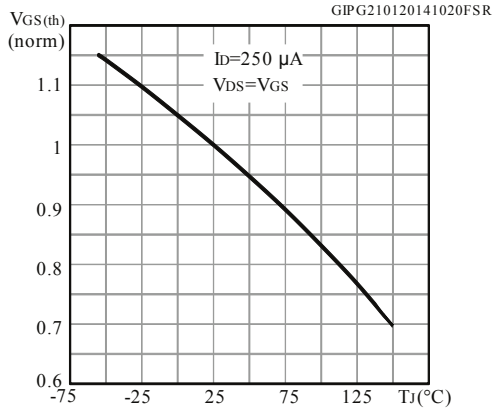


Figure 12. Normalized on-resistance vs temperature

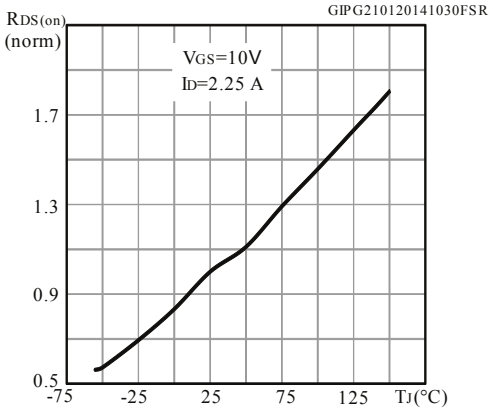
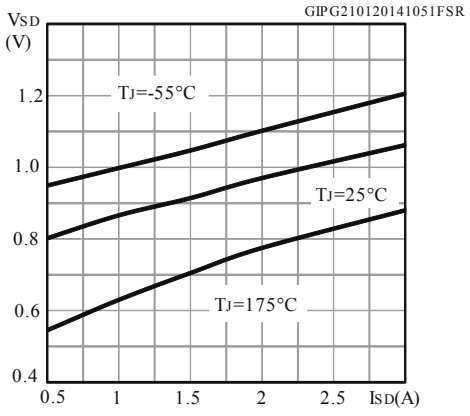


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Test circuit for resistive load switching times

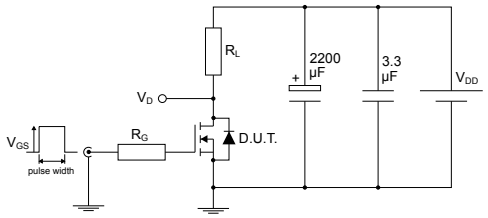


Figure 15. Test circuit for gate charge behavior

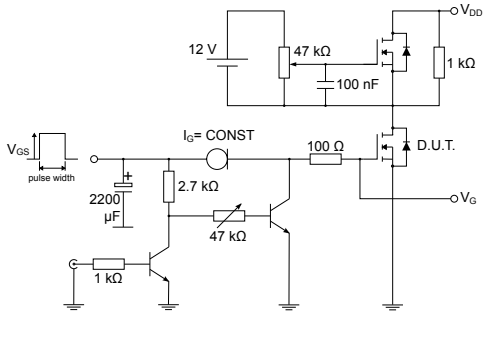


Figure 16. Test circuit for inductive load switching and diode recovery times

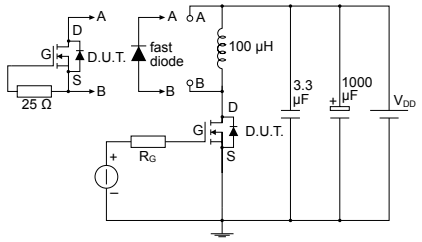


Figure 17. Unclamped inductive load test circuit

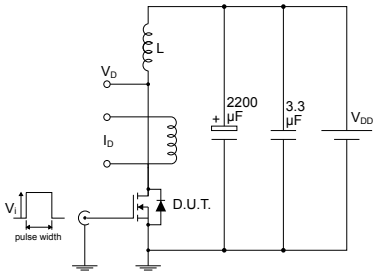


Figure 18. Unclamped inductive waveform

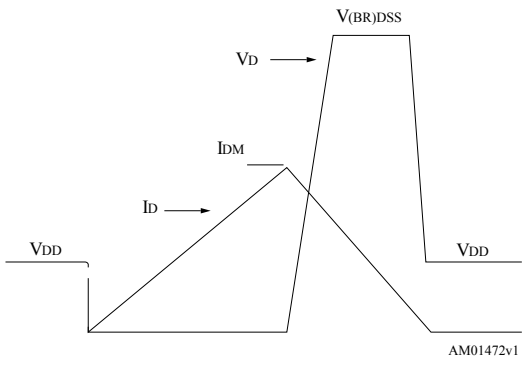
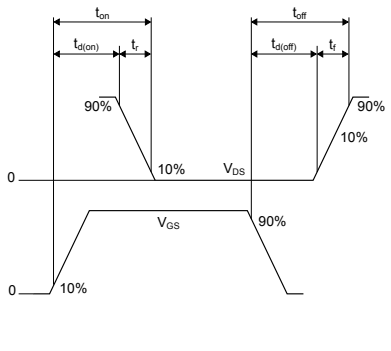


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 3.3x3.3 package information

Figure 20. **PowerFLAT™ 3.3x3.3 package outline**

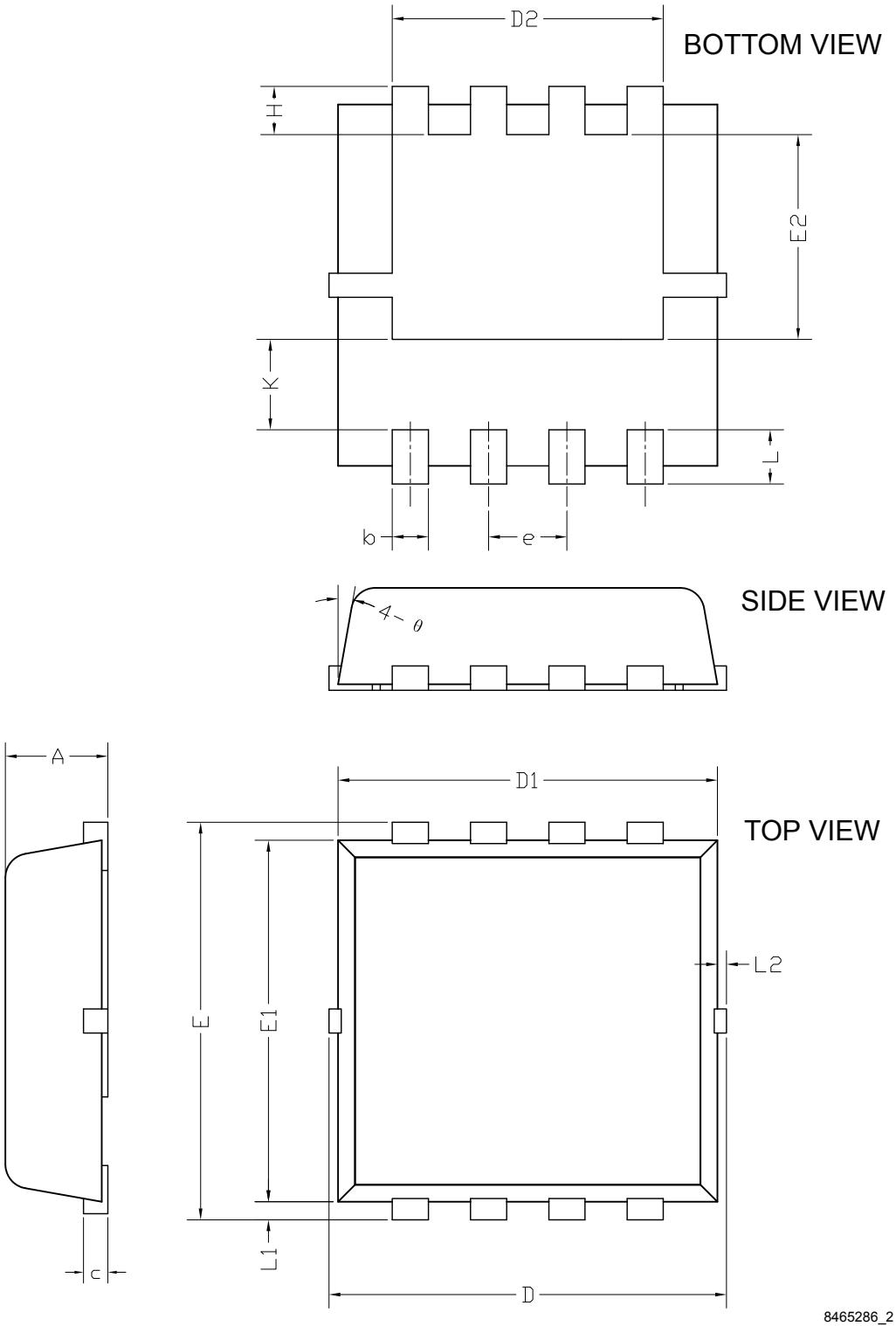
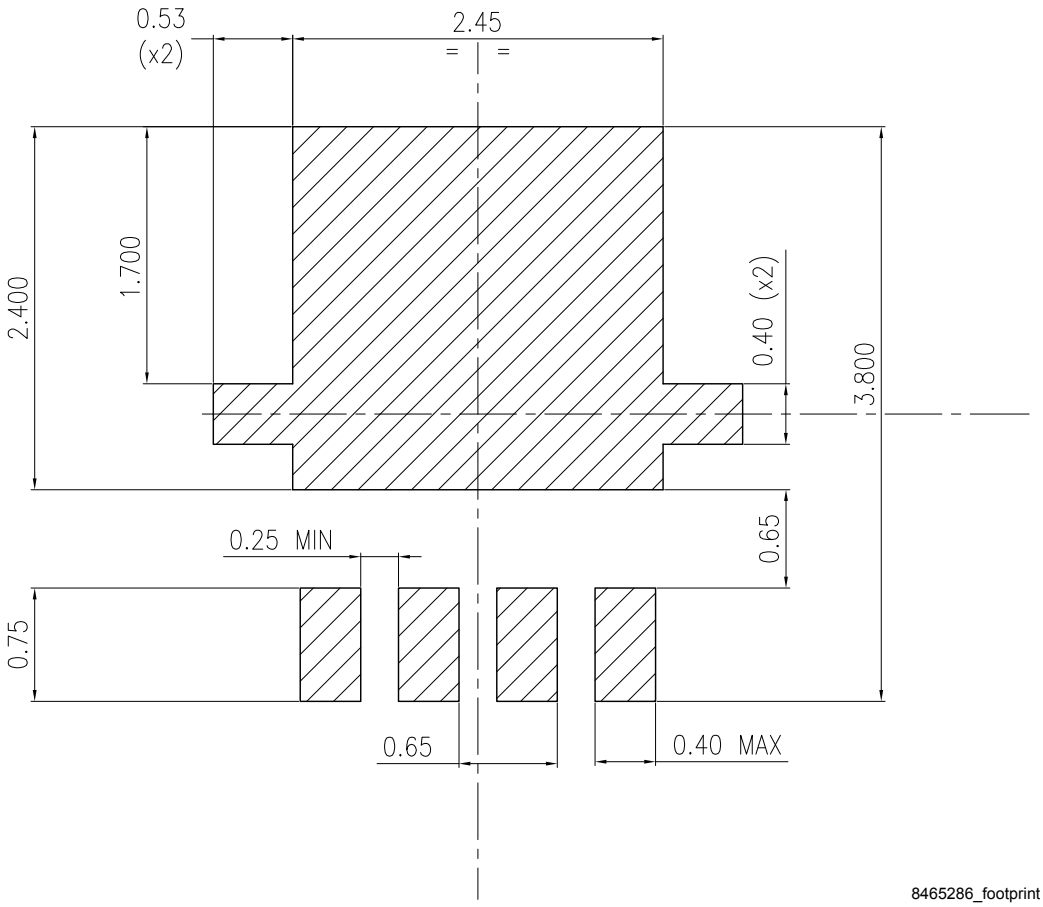


Table 7. **PowerFLAT™ 3.3x3.3 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
θ	8°	10°	12°

Figure 21. **PowerFLAT™ 3.3x3.3 recommended footprint (dimensions in mm)**



Revision history

Table 8. **Document revision history**

Date	Revision	Changes
10-Jul-2013	1	First release.
21-Jan-2014	2	Inserted *Section 2.1: Electrical characteristics (curves)*. Document status promoted form preliminary to production data.
19-Feb-2014	3	Added: I_D (at T_C = 25 °C and 125 °C), I_{DM} and P_{TOT} in *Table 2* Modified: *Figure 2* and *3* Minor text changes
10-Mar-2014	4	Modified: marking in *Table 1* Minor text changes
01-Feb-2018	5	Updated title, features and description on cover page. Removed maturity status indication from cover page. Updated Section 1 Electrical ratings. Updated Table 6. Source drain diode. Updated Section 2.1 Electrical characteristics (curves). Minor text changes

Contents

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